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Overview of HPM Effects in Electronics

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Abstract:

The following presentation contains an overview of HPM effects in modern electronics. HPM effects can be categorized into two basic level of effects, which are damaging and non-damaging. Damaging effects include junction breakdowns, dielectric breakdowns, and latch-up. These types of effects render a system inoperable until repaired. With non-damaging effects, HPM signals couple to into system components generating circuit responses that can overwhelm normal operation. Non-damaging effects can temporarily render a system inoperable or cause a system to lock and require a restart. Since modern systems are so complex, fundamental mechanisms of upset in circuit primitives are studied. All topics covered and all figured contained within are found in open literature. All data plots presented were obtained from experimental measurements conducted at the University of Maryland College Park and are also found in the open literature. [1-11].

Two Categories of HPM Effects

Damage:

- Large amounts of HPM energy couples to a system causing permanent damage to component electronics rendering the system inoperable.
- These effects are largely the result of thermal effects caused by large transient currents.
- Damaged components must be replaced to restore the system
- We will discuss 3 primary mechanism of damage:
    - Junction breakdown
    - Dielectric breakdown
    - Latch-up

Non-destructive effects:

- HPM couples to a system generating undesirable circuit responses which cascade through a system causing disruption to normal operation. No permanent damage occurs.
- Requires less energy to stimulate these effects compared to damage effects
- Effect can be momentary or persistent, which would require a system reset in order to restore normal operation
- We will be discussing some of the fundamental mechanism which cause these effects to occur

Coupling

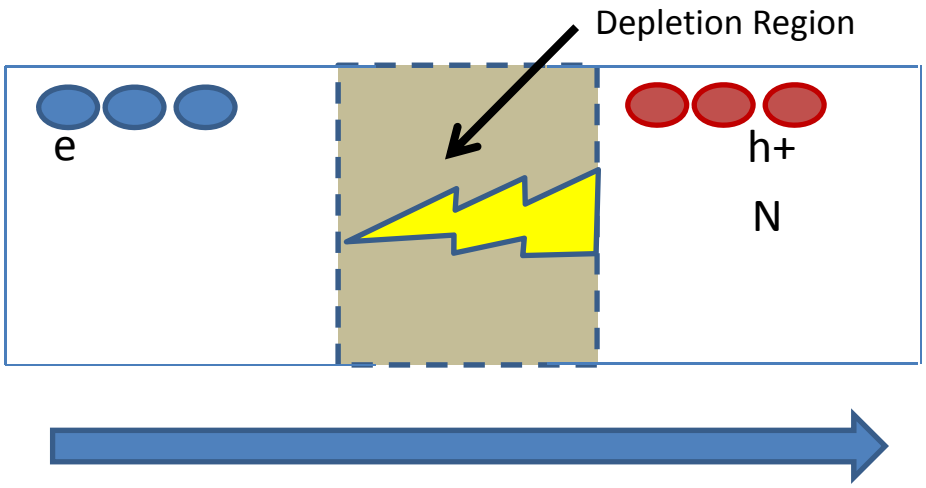
Front Door Coupling

- Coupling to elements of a system intended to communicate with the external environment
    - Blue tooth
    - Wireless antenna
    - Radio/TV transmitting towers
- Difficult to shield against without degrading system performance
    - HPM signals capable of coupling to the system will be within the operational band width.
    - Most receives have low noise amplifies that can unintentionally amplify unwanted HPM signals
- Usually has good immunity against out of band signals because of filtering.

Backdoor Coupling

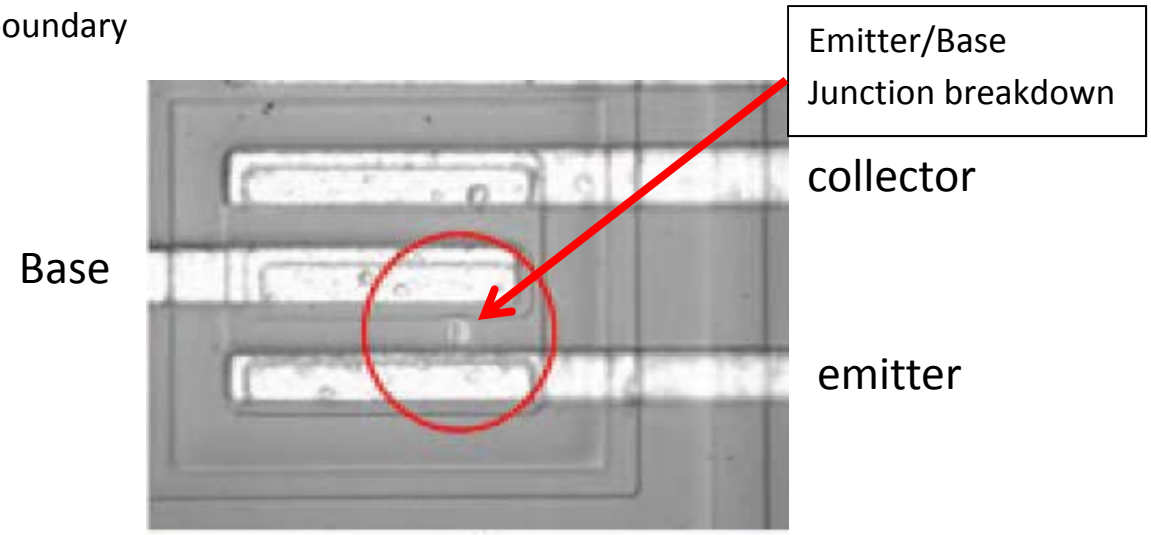
- HPM penetrates enclosures and excites EM modes within the enclosures through apertures
    - Ventilation holes
    - Cable Feed-throughs
    - Seems
- Complex field patterns can occur within enclosures
    - Many enclosures have dimensions substantially larger than the wavelength of the HPM radiation.
    - EM boundaries are very complex and rarely static
- Voltage signals then couple directly to circuit board traces, power lines, and cables.
- Wire traces and other passive circuit elements set up resonances which can lower HPM effects thresholds.

Junction Breakdown



- High reverse bias fields across a PN junction accelerate electrons to high velocities.
- At high enough energy these electrons cause impact ionizations freeing more electrons eventually leading to very high transient currents (Avalanche breakdown). Alternatively, the fields themselves break the covalent bonds creating a sudden current spike. (second or Zener breakdown).

- Localized heating due to breakdown currents can deform junction boundary



Predicting junction damage threshold: Wunsch-Bell

- Junction failures are linked primarily to junction temperature
- Assumed that voltage drop is entirely across the junction and hence all power is dissipated in the junction.
- 1 D linear diffusion equation used to derive approximate failure threshold in for a given pulse width

$$\frac{\partial}{\partial x}\left(\kappa \frac{\partial T}{\partial x}\right) - \rho C_p \frac{\partial T}{\partial t} = 0 \longrightarrow \frac{P}{A} = \sqrt{\pi \kappa \rho C_p}\,(T_m - T_i)\,t^{-\frac{1}{2}}$$

C_p = specific heat of silicon

P=density

T_m= failure temp

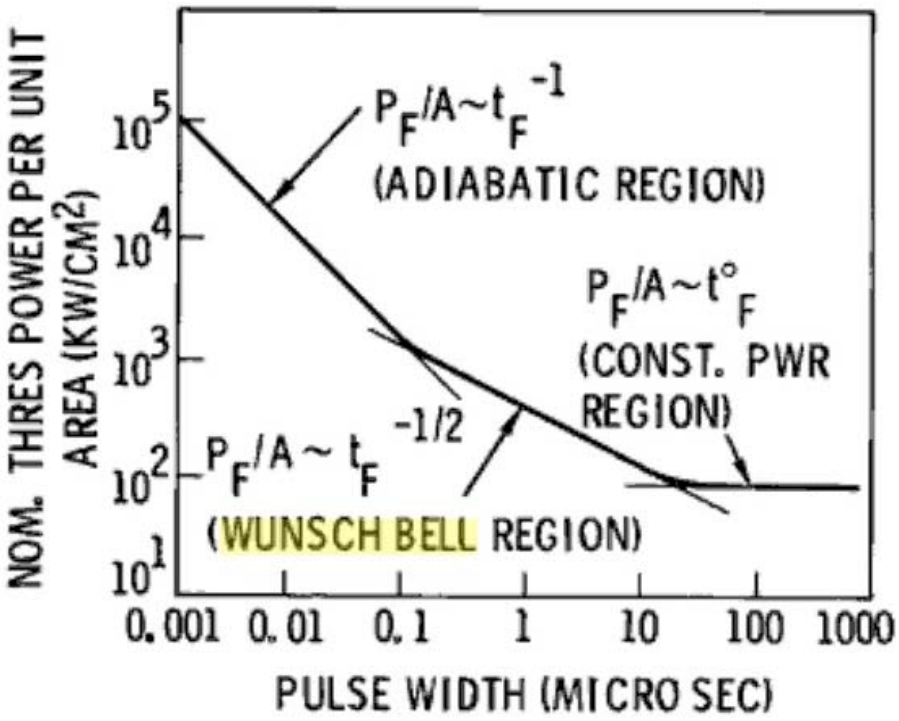
P = input power

κ = thermal conductivity

T_i= initial temperature

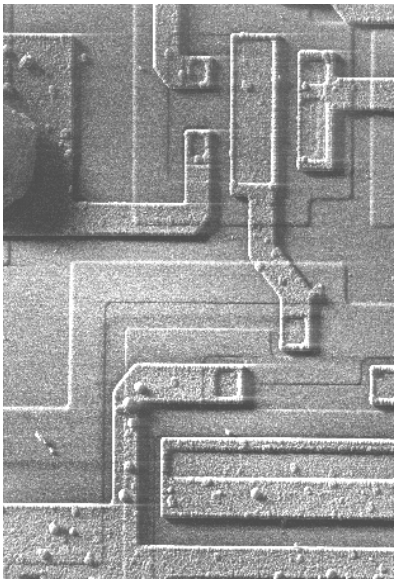
t = pulse width

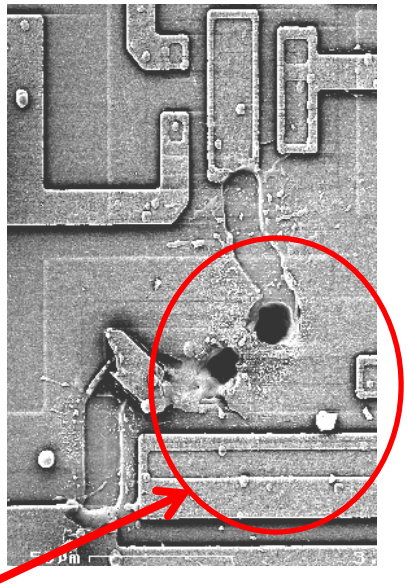
A = Junction cross section area



Dielectric breakdown

- HPM induced voltages strain insulating material beyond its breakdown threshold.
- Large currents from surface flashovers can melt metal interconnects on IC's as well as ball bond wires.
- CMOS gate oxide breakdown can cause a conduction path to form between the metal gate and the semiconductor surface
- Silicon dioxide and silicon nitride dielectric strength ~> 1e7 V/cm





Sever damage to metal layer due to a flashover event caused by an HPM pulse.

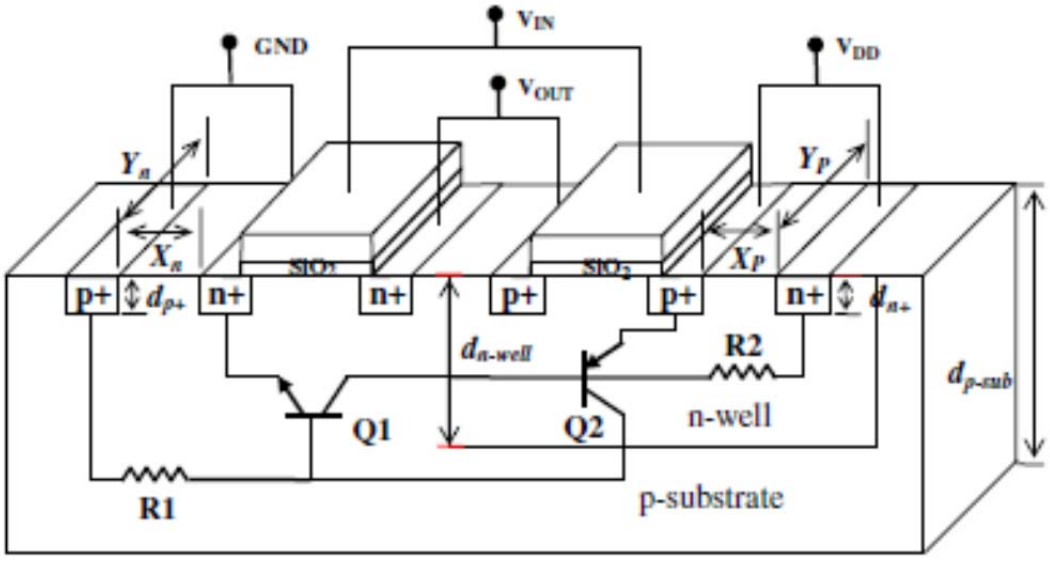
CMOS gate thickness as technology advances

Foundry	Feature Size	Oxide Thickness	Year Introduced
TSMC	0.35 µm	7.9 nm	1995
TSMC	0.25 µm	5.7 nm	1998
IBM	0.13 µm	3.2 nm	2000
IBM	65 nm	1.25 nm	2006
Intel	*45 nm	1 nm	2008
Intel	*22 nm	0.5 nm	2011

Latch-up

- Latch-up only occurs in CMOS devices
- Extreme Input Voltages that exceed Vdd (or drop below ground) can trigger parasitic SCR.
    - Excess voltage can forward bias PN junction at VDD or Ground terminal increasing current in the n-well of the substrate.
    - Substrate current will turn on one parasitic BJT which will cause current to flow into the substrate (or n-well) turning on the second BJT
    - Current from the second BJT cause increases current in the n-well (or substrate if initiated from the ground side) creating a positive feedback loop maintaining the conduction path from VDD to ground after the initial triggering pulse has expired
- This effect creates a short-circuit which will most likely burn out the device.

Schematic of a CMOS device and its associated parasitic BJT's



How do we study Non-Destructive HPM effects?

- Modern electronics are extremely complex!
- For example, Intel's new Ivy Bridge processor has transistor count of 1.4 billion! And this is just one of hundreds of components that make up modern PC's
- Deterministic vulnerability evaluation of entire systems is impossible, and effects are highly probabilistic.

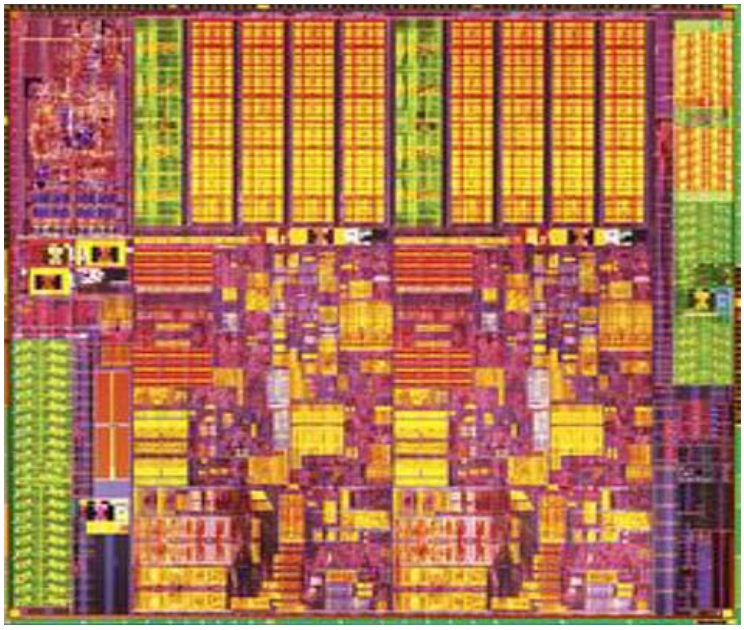


Image of Intel's Ivy Bridge chip obtained from www.intel.com

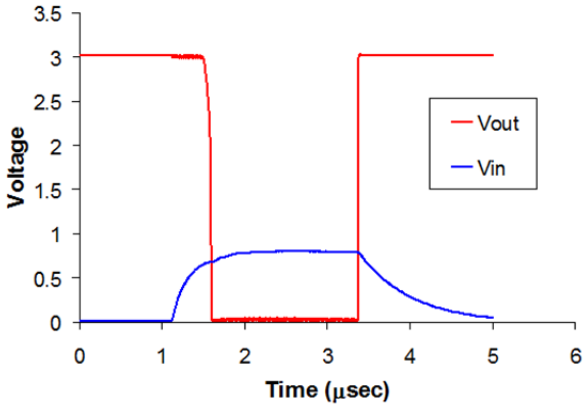
- Most studies on systems are done empirically and results are classified material.
- We will look at the response elementary circuit components to HPM signals which are in the open literature and not classified, and are the catalyst for system failures.

A European fighter jet undergoing HPM testing at the Swedish Microwave Test Facility.

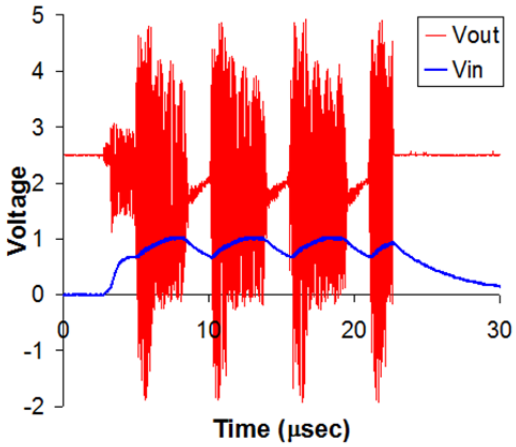
Fundamental upset mechanisms in primitive circuit elements

- Studies in the open literature focus on the characteristic responses of simple common circuit elements such as the CMOS inverter to the stresses caused by HPM signals.
- These signals can cause many upset mechanisms such as bit errors and clock timing errors
- We will focus on CMOS since this technology is almost universal in all contemporary digital systems.
- Below are examples of some of the common responses of CMOS devices.

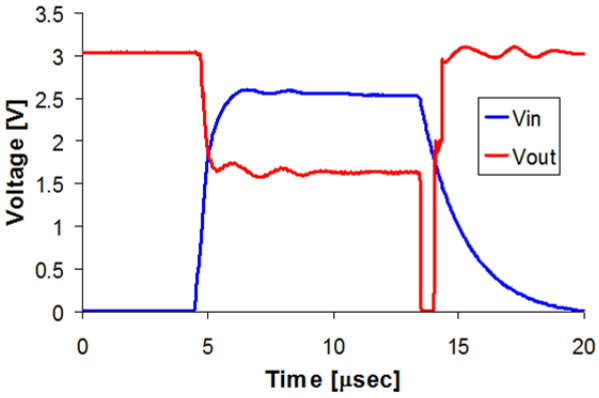
Prompt State Change



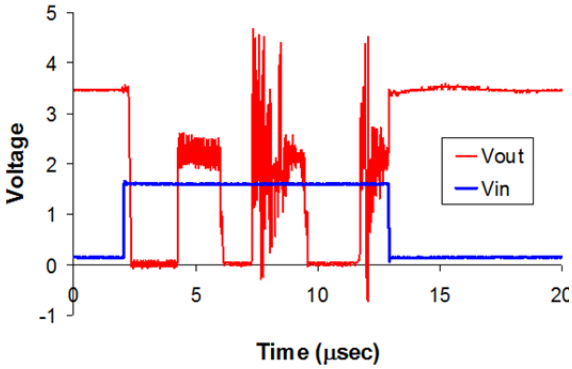
Oscillations



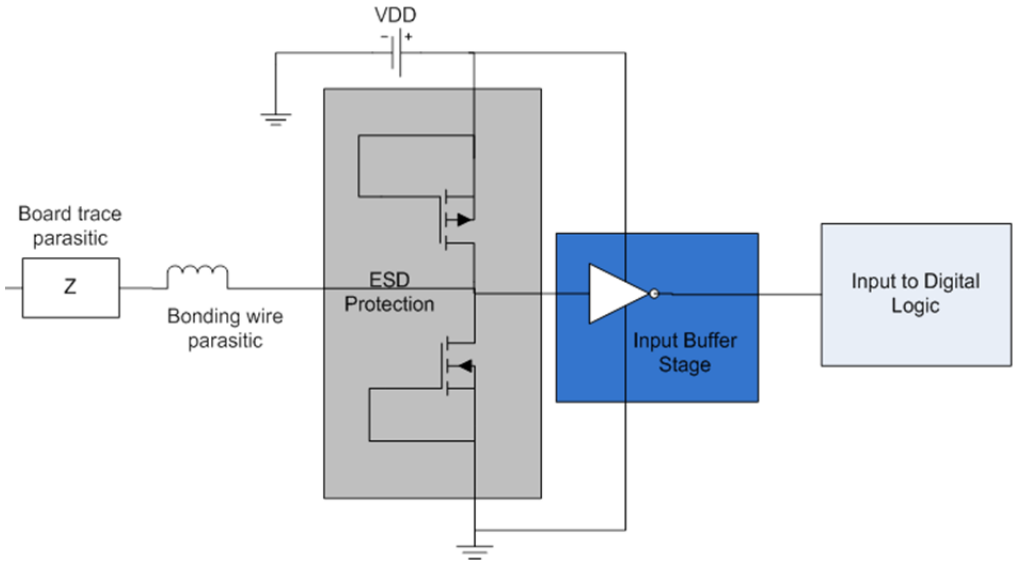
Bias Shifting



Instabilities

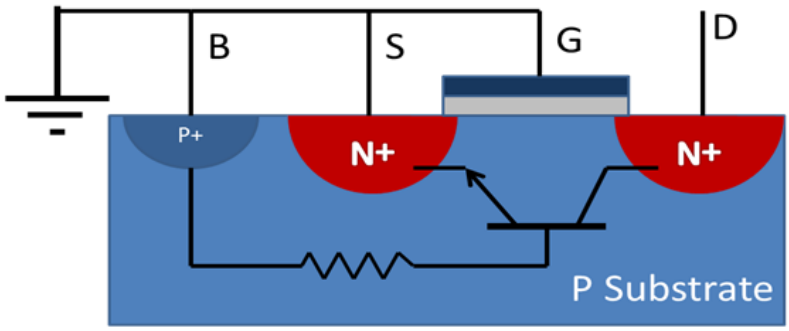


Typical Input Topology for digital IC's



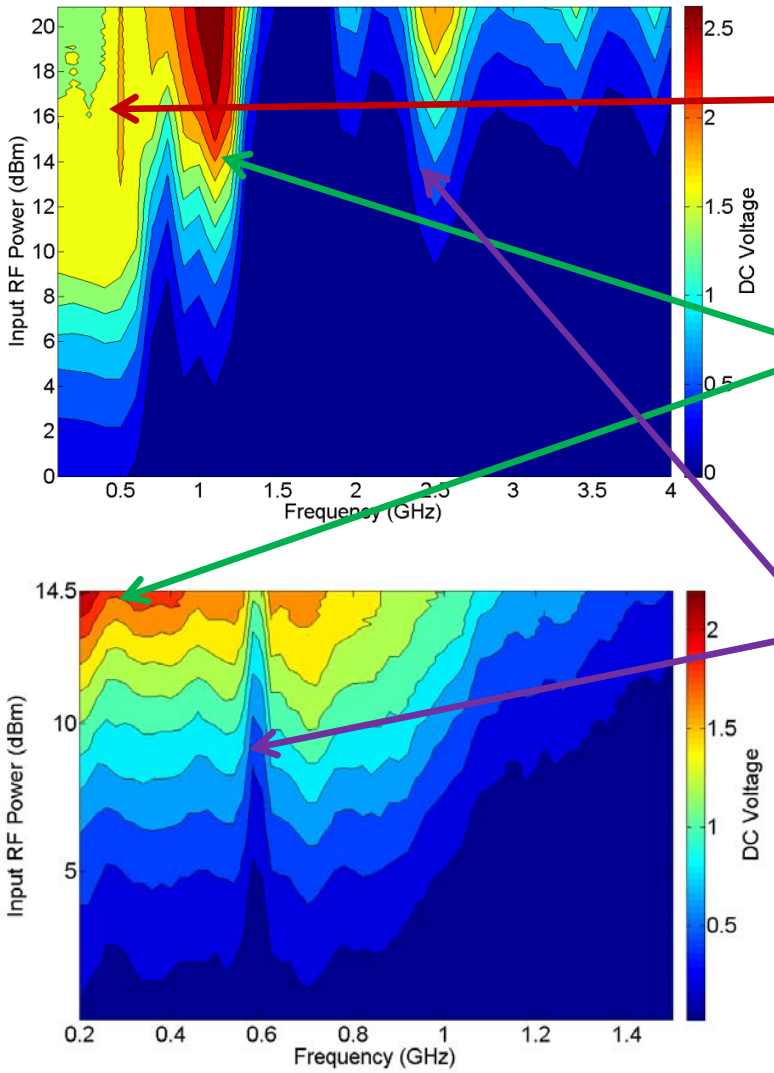
- Typical input includes circuit trace, the ball bond wires, which connect the silicon chip to the pin, ESD protection devices, and a buffer stage typically made up of some combination of inverters.
- ESD protection devices provide protection from electrostatic discharge events (mostly during fabrication)
- Devices designed to sink large transients currents to ground to avoid gate breakdown
- Below is an example of a common ESD device (though many types exist).
    - ESD event triggers parasitic BJT in the devices which can sink large transient current to ground.
    - These devices are large and typically have parasitic pn junctions which can rectify HPM signals

Common ESD protection device – gate grounded nmos (gate coupled pmos)



DC Response at the input of typical IC

- Below are two contour plots which show the results of measurements of the DC response to HPM signals at the input of the digital ICs.
- The DC level is due to rectification by input ESD devices.
- The top plot is the input response of a custom IC fabricated for HPM effects studies using the 0.5 µm On Semiconductor process
- The bottom plot is the input response from a Fairchild semiconductor 74LVX14 hex inverter
- V_{dd} for both these chips was 3 V



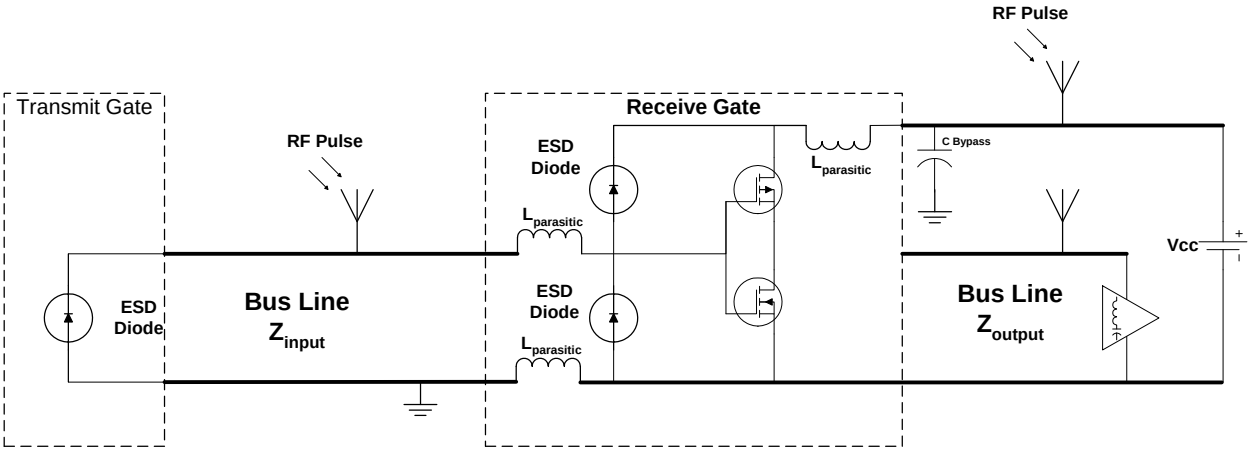
Up to 600 MHz DC response plateaus at about 1.5 V after 8 dBm

In other regions the DC voltage continues to rise as the input power increases

Peaks and valleys in the response indicative of resonances

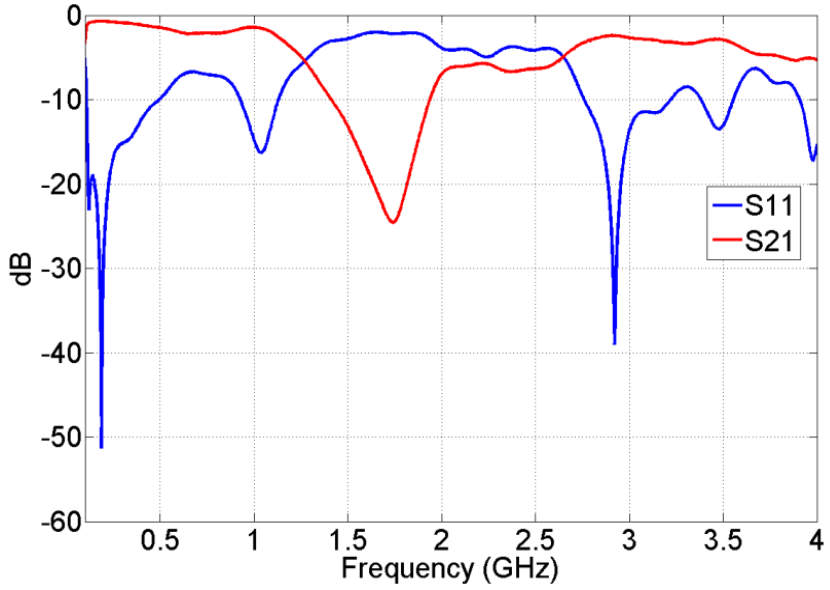
There is a general roll off in response with increasing frequency.

Resonances due to Parasitic Impedances

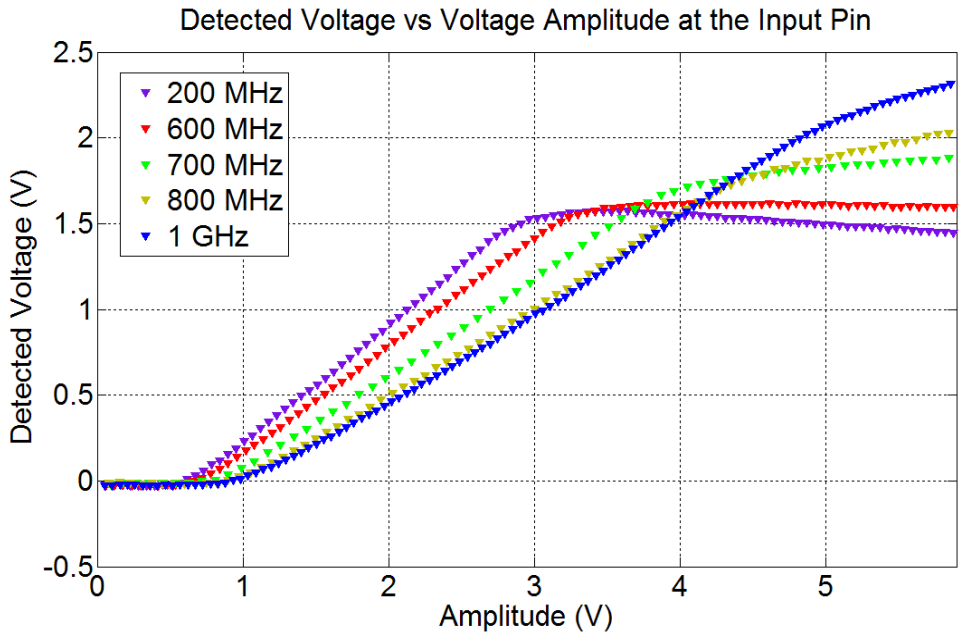


- Resonant circuits consist of lumped and distributed parasitic elements. For example:
  - Inductances from ball bond wires
  - Junction capacitances from ESD protections devices
  - Distributed inductances and capacitances from circuit board traces
- These resonances can potentially enhance a circuit's susceptibility.

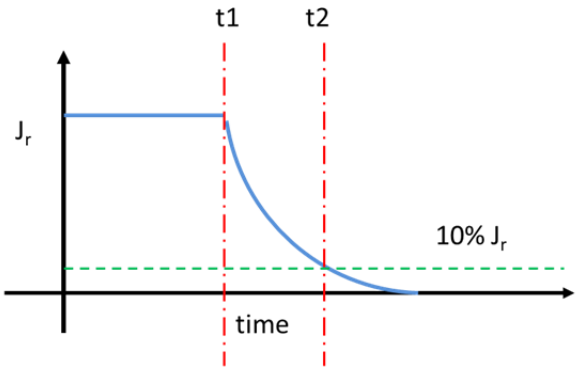
A plot of an S-parameter measurement of the input, including circuit board trace, pin and ball bond wire to the custom IC.



Quasi-static Diode Response vs. Non-Quasi-Static



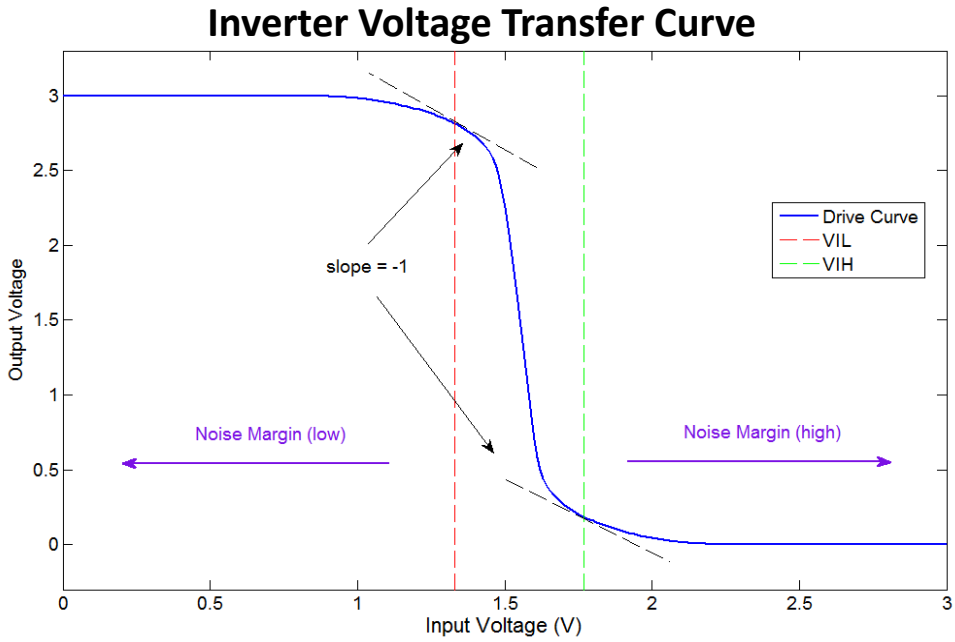
2D plot of Input voltage response of the custom IC



Approximate recovery time for a pn junction

$$\tau_{eff} = \frac{L_{eff}^{\ 2}}{D_{n,p}} \qquad D_{n,p} = \frac{kT}{q}\mu_{n,p}$$

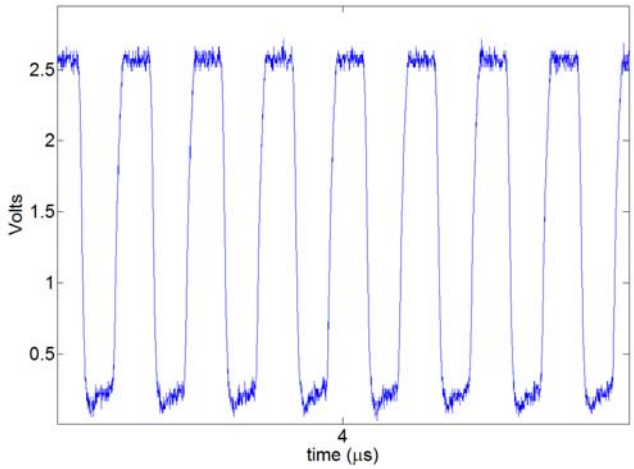
- In order for a diode to switch from on to off, minority carriers must diffuse away from the junction boundary
- Minority carrier lifetime determines diode frequency response
- Lifetime depends on carrier mobility Electron mobility is 2 to 3 times that of holes
- When the diodes of both ESD devices are in their quasi-static regions they counter balance each other. Once the RF amplitude reaches V_{dd} , the DC voltage is steady at $V_{dd}/2$.
- NMOS device has better rectification efficiency at higher frequencies which allows the DC voltage to increase beyond $V_{dd}/2$



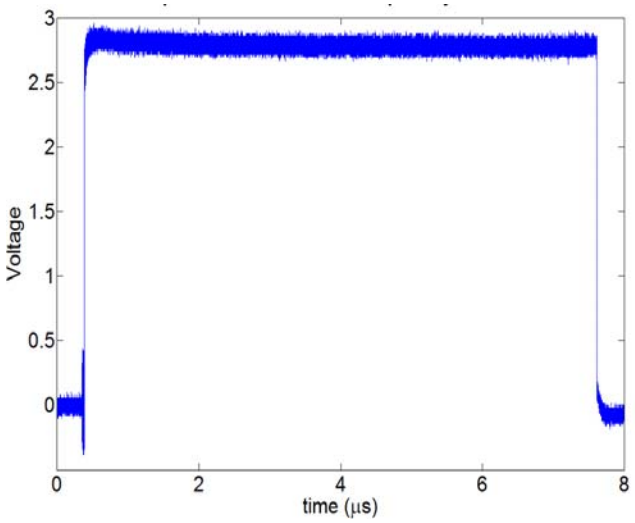
- Before looking at the output response to the HPM signals let's review basic inverter voltage transfer characteristics
- There are three regions to CMOS transfer characteristics
    - Input low- any voltage up to the low noise will not generate a change in voltage at the output
    - Input high- any input voltage above the high noise margin will switch the output low
    - High gain region- the transitions regions between the noise margins

In Band output response

- Within the operating bandwidth of a circuit, sufficiently large signals can switch the logic at the HPM frequencies producing bit errors
- Plot on the right is the output of the Custom inverter IC with an input excitation of 200 MHz

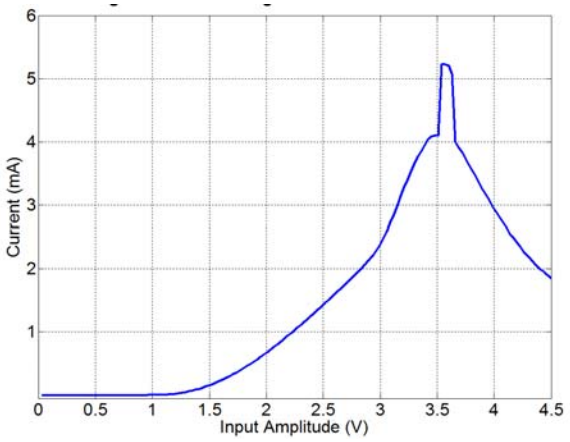


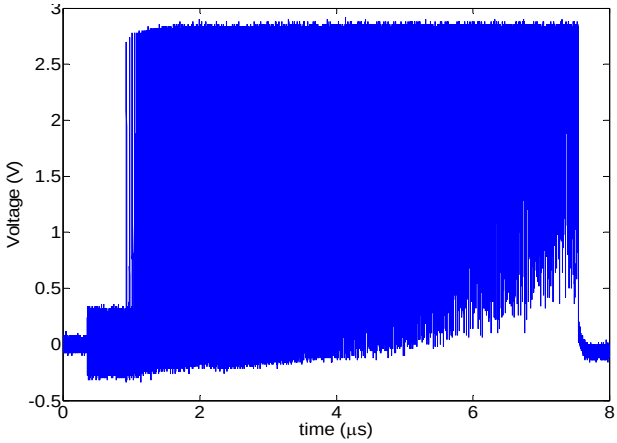
Out of Band Effects



Example of a prompt state error in the custom inverter IC due to an out of band HPM pulse. The frequency was 2.5 GHz and the input RF power was 19 dBm

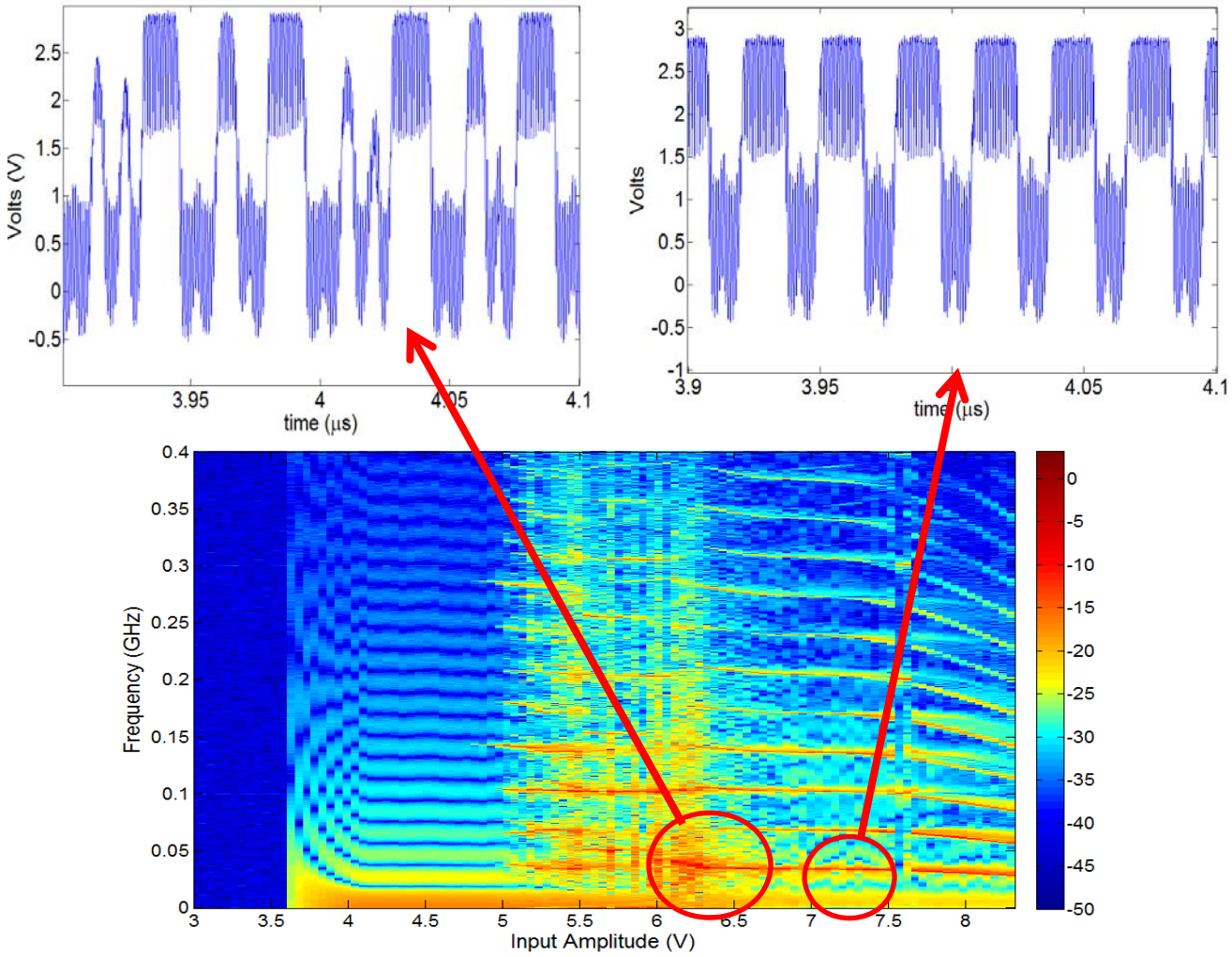
- Above the maximum operating frequency of a circuit, the output no longer switches with the RF frequency
- However, due to rectification at the input, the circuit will switch once the DC level rises above the high noise margin.
- When the DC voltage is within the high gain region, unstable spurious oscillations occur as shown below.





Output Instability due to HPM as the DC level at input reaches high gain region (right). The drive curve on the left shows the current spike as the input DC voltage transitions through the high gain region occurs

Another Interesting Out of Band Effect



Output spectrum vs frequency and input RF amplitude of the custom inverter IC when driven at 1 GHz

- When driven at 1 GHz the inverter circuit output began to oscillate after a certain input threshold power was reached. Oscillations continue to occur as the input power increased.
- These oscillations were low frequency around 35 MHz
- It was found that these oscillations occur due a parasitic resonance on the power distribution network.
- Fluctuations in V_{dd} was responsible for the almost chaotic like oscillations similar to what was also observed in the commercial inverter

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