



Fermi National Accelerator Laboratory

D0 Engineering Note #3740.000-EN-506

Document Template for Printed Circuit Board Layout

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Available on-line at

<http://d0server1/users/janderson/Public~1/default.html>

And

<http://d0server1/users/janderson/Public~1/a981203a.doc>

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PCB Layout Specifications

The purpose of this document is to list the information that may be required to properly specify a printed circuit board (PCB) design. You must provide sufficient information to the PCB layout vendor such that they can quote accurately and design the PCB that you need. Use the following information as a guide to write your specification. Include as much of it as is necessary to get the PCB design that you want.

1. Project Identification and Description

Identify the D-Zero project that this board is part of (include the WBS number if known), the formal name by which the board is identified and any D-Zero document numbers which define the device. Provide pointers to functional specification documents.

2. Mechanical Specification

Specify general mechanical details here. The sub-headings give more information. Again, reference any drawings you can by number. If necessary, provide a sketch or proper mechanical drawing. The following details are required:

2.1. *Dimensions and Tolerance*

Specify: length, width, thickness, allowable protrusions, allowable component height (on both sides), all clearances. Use consistent units and provide \pm tolerances on all dimensions. Verbally specify the shape of the PCB board.

2.2. *Cutouts*

If the board has slots, cutouts or any other feature which gives it more than four corners, specify dimensions and tolerances of all cutouts here.

2.3. *Thickness & Warpage*

Specify nominal thickness and tolerance. Specify allowable warpage tolerance in all three dimensions.

2.4. *Connector Placement*

Define reference datum from which all placements are measured and give at least one coordinate for each connector, including tolerance, from that reference datum.

2.5. *Conformance to Standards*

If board must fit into a standard chassis (e.g. VME, CAMAC) list the relevant standard here.

2.6. *Edge Milling and/or Corner Chamfers*

Most boards should have corners chamfered to ease insertion into crates. Some boards require edge milling to fit into card guides. Give all dimensions and tolerances for these here. If there is a spec (e.g. ANSI xx, IEEE 1101.1) that's applicable, reference it.

2.7. *Materials Specification*

Specify here the materials which are to be used. Include dielectric type (normally FR-4), allowed E_r for controlled impedance boards, any special requirements in weave. Note that in multilayer boards the E_r of the copper layers in the stack will usually vary from the E_r used for spacers. If board must withstand

radiation or temperature extremes, note so here. Also note if any special construction technique need be used because board is subject to high voltage or if in an environment where outgassing is a problem.

2.8. Layer Stackup

For any multilayer board, each layer must be uniquely identified. In controlled impedance applications, trace widths and the spacing between layers must be controlled.

2.9. Number of Layers and Order

Enumerate each layer in a table and show the order from component side to solder side. Note for each layer if layer is controlled impedance or not.

Specify the spacing between each layer of copper and show how it all stacks up to the total thickness specified earlier.

2.10. Copper Thickness of Each Layer

Specify copper weight (e.g. 2 oz, 1 oz, ½ oz, ¼ oz) on each layer. Insure that the thickness of the copper itself (typically 0.0018" per oz) is included in the total thickness calculation.

3. Component Placement

Specify rules here for which components go where. Include a drawing showing in general terms where parts are to be placed. Include any notes about parts that go on the solder side or orientation restrictions.

3.1. General Placement Diagram

Import a drawing here showing, with respect to the board datum, where things go.

3.2. Component Spacing (grid size, clearance)

Specify any grid required to keep parts in order (typically, through hole parts are placed on a 0.100" or 0.050" grid). Similarly, specify any grids to restrict via placement or trace placement. Specify clearances around components as required to insure smooth assembly.

3.3. Clearance from Board Edges

Specify all clearances from board edges, cutouts or mounting holes to insure that no component clashes with a mechanical mounting rail, retention screw or other non-electronic part of the board.

3.4. Components on bottom (solder) side

Specify which, if any, components may be placed on the solder side of the board. Insure that component height restrictions are observed here as they are for parts on the component side.

3.5. Restrictions on Placement due to Thermal Considerations

Specify any areas which must be kept low density to insure no hot spots; mark out the hottest components so the layout vendor knows to steer clear of them.

3.6. Restrictions on Placement due to Electronic Considerations

Discuss component placement to minimize crosstalk. Be wary of things like lots of power supply current flowing through a sensitive analog area. Discuss any special shielding requirements.

3.7. Orientation and/or Airflow Requirements

Discuss the cooling methodology and insure that no component will block another from the airflow. Specify any restrictions on orientation of components (e.g. all resistors must lay flat, all ICs must have pin 1 towards the top of the board, etc.).

4. General Routing Requirements

This section lays down the rules for traces and planes.

4.1. Nominal Trace Widths

Specify the default trace widths to apply to various signal types. Correlate these selections with characteristic impedance calculations as required. Insure that fine-pitch components are routed with a trace width conforming to the pin spacing.

4.1.1. Digital Signals

4.1.2. Analog Signals

4.1.3. Connector I/O

4.1.4. Power Feeds

4.2. Spacing Between Traces (nominal grid)

Specify trace-to-trace clearances, normally limited by manufacturing rules. Define grids for autorouting. Include any calculations necessary to defend larger spacings based in crosstalk or high voltage requirements.

4.3. No-Route Areas of Board

Define any areas that are no-route or limited-route, typically to avoid noise pickup or to avoid mechanical obstacles. Make sure that traces are not placed underneath clamped components, relying upon the soldermask for insulation.

4.4. Copper Pours (Including pours used as planes)

Define any copper pours used for shield areas. Define also any layer-wide copper pours used as planes. Often, when defining a power or ground plane, using a copper pour to create a 'positive' image is better than using a plane layer that creates a 'negative' image. A pour allows a trace or two to be buried within the "plane" – often useful for fuses and such – and a pour can be controlled more easily when relieving the plane from the edge of the board. Good design requires that planes be relieved about 0.050" from all edges to insure against accidental shorts.

4.5. Plane Layers

Specify which layers can be simple planes.

4.6. Mitering/Rounding of Bends

For high speed signals, corners in traces can cause excessive noise. Specify any signals which must use 45 degree mitered corners and/or arc segment bends.

4.7. Allowed Via Types and Sizes

Specify what size vias may be used; also specify if buried or blind vias are acceptable.

4.8. Via Placement Restrictions

Specify any no-via areas, if vias must be on a grid, etc.

4.9. Routing Strategy Restrictions (Grid/no grid)

Specify whether gridded or gridless autorouting is acceptable. Specify if autorouting is acceptable at all. Define any groups of nets that must be hand-routed.

4.10. Special Routing Requirements

This section is for the more difficult boards, for calling out nets or groups of nets that merit special attention to detail.

4.11. High Quality Nets (prioritized routes)

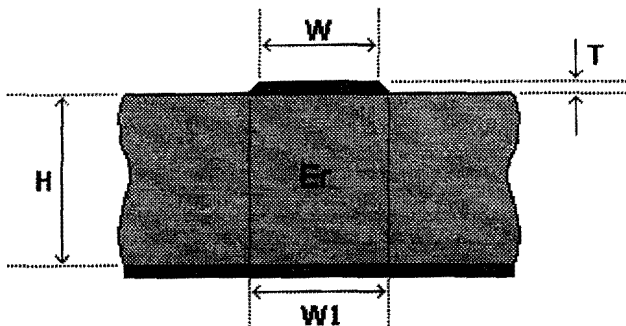
If certain lines (e.g. clocks) have to be routed first to insure they get the most direct paths, list them here.

4.12. Controlled Impedance Nets

Provide a list of the nets that have to be controlled impedance; in the sub-sections, provide the calculations of width and layer spacing for the type of signal. Note whether the impedance matching is differential-mode, common-mode or both.

4.12.1. Microstrip

Microstrip refers to the construction technique where the signal trace is on an outer surface of the board and the signal is referenced to a plane on an adjacent signal layer. The characteristic impedance is defined by the width of the trace, the thickness of insulator between the trace and the plane, and the dielectric constant of the insulator.



The impedance of an exposed microstrip can be expressed by the formula:

$$Z_0 = 87 / \sqrt{(E_r + 1.41)} \times [\ln(5.98H / (0.8W + T))]$$

where

Z_o = ohms

E_r = dielectric constant

H = the distance between the signal line and the reference plane

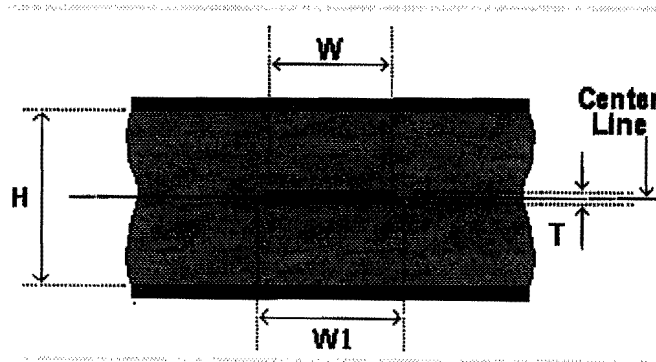
W = the width of the signal line and

T = the thickness of the signal line

Physical dimensions can be in mil., thou., mm., micron (i.e. inches or meters); it is, however, important to always use the same units throughout.

4.12.2. Stripline

Stripline is a geometry where the conductor is embedded between two return layers. Stripline offers reduced crosstalk and reduced susceptibility to external fields as compared to microstrip.



The impedance of a symmetric stripline can be expressed by the formula:

$$Z_o = 60/\sqrt{E_r} \times [\ln(1.9(2H + T)/(0.8W + T))]$$

where

Z_o = ohms

E_r = dielectric constant

H = the distance between the signal line and the reference plane

W = the width of the signal line and

T = the thickness of the signal line

Physical dimensions can be in mil., thou., mm., micron (i.e. inches or meters); ensure the same units are used throughout.

4.12.3. Other Geometries

Other geometries include offset striplines and variations upon both microstrip and stripline using two conductors for differential signals. A good place to learn is the web page of Polar Instruments at <http://www.polar.co.uk/>.

It is important to note that for differential signals there are *two* characteristic impedance numbers: Z_{odm} is the *differential-mode* characteristic impedance, or the Z_0 between the two traces of a differential pair. Z_{ocm} is the *common-mode* characteristic impedance, and is the Z_0 of either one of the two traces in the differential pair with respect to the common return. When terminating a differential signal, care must be exercised to insure that the correct impedance is used.

In very low noise applications a complex termination network may need to be applied to differential signals which provides termination of both characteristic impedances. This is because all differential drivers are imperfect and the mismatch in rise/fall times or propagation delay between the + and - halves of the signal becomes a common-mode signal which is returned through the common return. Thus, correct termination of the common-mode component may be required in addition to correct termination of the differential-mode component.

4.13. Clock Nets

Detail all the clock signals to insure they are routed correctly. Describe preferred paths and/or hand-route instructions.

4.14. Nets Restricted to Certain Layers

If some nets need to be restricted to certain layers (e.g. signals that must be accessible), detail them here.

4.15. Via Restrictions

For impedance or speed reasons, some nets may not be allowed vias. Note those here.

4.16. Matched-Length Nets

Clock nets and/or data buses must often be matched-length to control skew. Note such nets here.

4.17. Power and Return

If the path of power flow is important (e.g., no +5 current through the analog section), detail those restrictions here. Insure that no loops or big inductors are formed by board cuts or islands in planes.

4.18. Test Points and Probe Ground Lugs

Critical nets should have test points. All boards should have an array of ground lugs to facilitate probing. Note locations of these here.

4.19. Soldermask and Legend

A good soldermask insures clean assembly. A good legend insures accurate assembly and easier testing.

4.20. Soldermask Requirements

Solder mask can be either deposited image (screen printed epoxy or acrylic); or Photo defined image (liquid or dry film). Circuit spacing will define the technology required. You will need to know How much clearance off the pads? What color? Consult with your PCB vendor.

4.21. Component Side Legend

Describe what information should be included on the board on the component side. At minimum, specify enough data to insure all parts are stuffed correctly and that the board is fully identified (reference designators and part values).

4.22. Solder Side Legend

Include sufficient legend to identify solder-side mounted parts (reference numbers). Add debugging hints if appropriate.

4.23. Text In Copper

Typically frowned upon, but sometimes invaluable to insure correct layer stackup. Specify what, if any, is to appear.

5. CAM Files

In this section define what outputs the vendor must provide to complete the job.

5.1. Gerber Format Required

Gerber output is a set of X-Y coordinates plus movements where a shape (called an aperture) is 'drawn' along a coordinate path or 'flashed' at a single coordinate. Gerber formats are 274-D (coordinate data with apertures in separate file) or 274-X (coordinate data with aperture data embedded within data). The coordinate system is interpreted in inches. Two precisions of numerical data are common: 2.3, where the 5-digit coordinate is interpreted as two digits to the left of the decimal point and 3 to the right, or 3.4, where a seven digit value gives increased range and resolution. Leading zeroes in coordinates may be suppressed or not.

The most typical Gerber output used is 274-X, 2.3, non-suppressed; check with the board manufacturer if they need something else.

5.2. Drill Tape Format Required

The drill tape is a list of coordinates where holes in the board are placed. Computer-controlled drilling machines use two formats, ASCII and Excellon. ASCII is far more common.

5.3. Aperture List Required

If Gerber 274-D is used, an aperture list is required.

5.4. Assembly Drawing Requirements

Specify file format required, adherence to any ANSI specs, etc.

5.5. Required Alignment Markers

Put at least three on each layer.

5.6. Required Layer Identification Markers

Always require these to insure the layers are stacked by the board house the way you want.

5.7. *Check Plots*

Vendors should always supply check plots in some form to inspect their work before boards are built.

6. Information Transfer

6.1. *How will source files be provided*

6.2. *How will outputs be sent back*

6.3. *Technical Contact for Questions*

6.4. *Signoff and Approval Procedure*

An Example

This is an example file written from the template above. As an exercise, look through and find the omissions.

MCM Test Board Layout Specifications

This document describes the specifications for the printed circuit board layout of the "MCM Test Board". (hint: the preceding doesn't say what D-Zero project or WBS this is!)

Mechanical Specification

The MCM Test Board shall be 14.437 (+0/-0.012) inches wide (VME 9U) and 10.774 ± 0.004 inches (280 mm) high. The board shape shall be a simple rectangle with no cutouts. The finished thickness shall be 0.093 inches. Although generally intended to be compatible with IEEE 1101.1 and 1101.10 specifications, conformance to these specifications is not required. All corners shall be chamfered no more than $1/16^{\text{th}}$ inch after manufacture.

Materials Specification

Standard FR-4 material shall be used throughout.

Layer Stackup

The MCM Test Board shall be an eight layer, controlled impedance design. All layers shall be one ounce copper. The layer ordering shall be as in Table 1.

Layer Name	Layer order	Spacing requirements
Top Signal	Topmost layer	Determined by impedance to Return 1.
Return 1	2 nd from top	
Power 1	3 rd	Minimum spacing between Return 1 and Power 1.
Inner 1	4 th	Determined by impedance to Power 1.
Inner 2	5 th	Determined by impedance to Power 2.
Power 2	6 th	Minimum spacing between Return 2 and Power 2.
Return 2	7 th	
Bottom Signal	Bottom-most layer	Determined by impedance to Return 2.

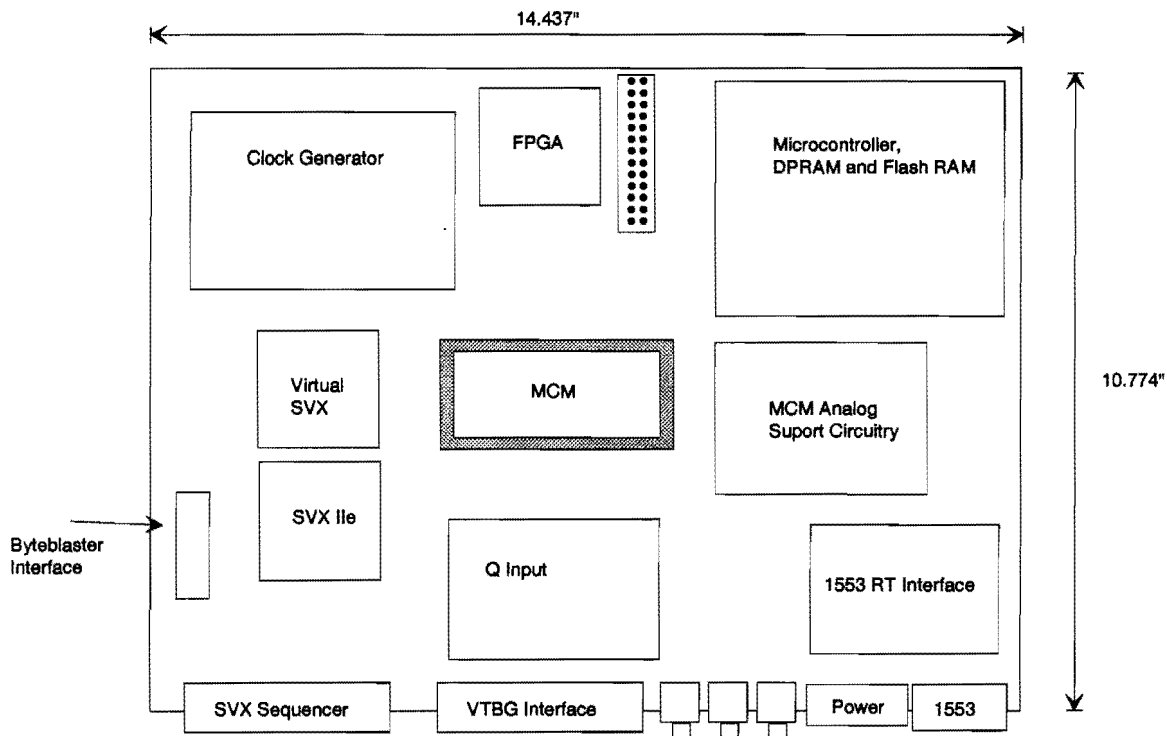
Table 1

Impedance considerations will determine the spacing between the four signal layers and the various power/return layers. Whatever space is left over to fill the board thickness of 0.093" defines the layer spacing between the Power 1/Return 1 and Power 2/Return 2 pairs.

Component Placement

Component placement will follow the general orientation as given in Figure 1. Parts are grouped by function and parts within a group shall all be kept close together. As the MCM component in the center is socketed, maximum clearance around that component should be reserved. All integrated circuit components and connectors are mounted from the component side. Names of blocks in Figure 1 correspond to pages in the schematic diagram.

Wherever possible, decoupling and bypass capacitors should be mounted on the solder side to minimize trace length between power pins of components and the bypass capacitors. No component other than a connector or LED shall be closer than 0.050" from the board edge. Wherever possible, all components should have the same orientation. The board will be passively cooled by convection; therefore, allow no less than 0.050" between components. Wherever possible, pin 1 of all components with more than 2 pins shall be identifiable by a rectangular as opposed to ovoid pad.



Rough Layout Scheme, MCM Test Board

Figure 1

General Routing Requirements

Nominal trace rules for the MCM Test Board shall be 8 mil traces with 8 mil separation. Feeds from the power connector to fuses shall be scaled to handle the necessary current. Cutout obstacles in power planes may be used as fuse feeds so long as the obstacles are of sufficient width to safely carry 150% of the fuse's rated current. Traces shall be routed on grid, with bends mitered at 45 degrees. A via size no larger than 0.025" shall be used throughout. Vias shall be constrained to be on grid. All vias shall be "through" vias; no blind or buried vias shall be used.

Power and Return planes shall be relieved no less than 0.050" from all board edges. Power and Return planes may be implemented as copper pours to allow for fuse feed obstacles. Signals shall not be routed on power or return plane layers without written approval. A square area of 0.500" by 0.500" shall be reserved at all four corners of the board as a no-route zone to allow for four mounting holes.

Signals on the Top Signal, Bottom Signal, Inner 1 and Inner 2 layers shall be controlled impedance, designed for a characteristic impedance of 50 ohms to the nearest Power or Return layer. Note that signals on the Top Signal and Bottom Signal layers are Microstrip geometry whereas the signals on the Inner 1 and Inner 2 layers are Offset Stripline geometry. The layout vendor shall provide documentation of the calculations of layer spacing to achieve the necessary characteristic impedance.

Special Routing Requirements

All signals on the Q input page of the schematic shall be routed with minimum length and minimum number of bends. Vias shall be avoided for nets on this page.

All signals on the Clock Generator page of the schematic shall be routed with minimum length and minimum number of bends.

All clock signals shall be routed as single path routes, with no stubs and with the driver of the signal constrained to one end of the trace.

The Power 1 layer shall supply +5 volt power throughout the board, except in the Q input area where an island of Analog GND will be placed.

The Power 2 layer shall be split, providing +3.3 volt power to one section of the board and providing both +12 and -12 volt power to other areas, except in the Q input area where an island of Analog GND will be placed.

The Return 1 layer shall provide the Analog GND return over the entire area of the board.

The Return 2 layer shall be split, providing a connection to Analog GND underneath the Q Input area and providing connection to Digital GND everywhere else.

No signal other than those found on the Q input page shall be routed in the Q input area.

The Q_OUT bus from the Q Input page shall be constrained to the Top Signal and Bottom Signal layers only. A no-route area shall be established on the Inner 1 and Inner 2 routing layers in the Q Input section of the board.

Soldermask and Legend

Standard SMOBC soldermask shall be applied to both sides of the board. Any color may be used. The legend for all parts shall indicate the component mounting orientation, if the component has an orientation, on the side to which the component is attached. Identifying text showing the name of the component shall be placed within the body of the component to identify assembly location, if said text can be fit within the component body. All small SMT components shall be identified by reference designator as close to the body of the component as feasible.

A legend identifying this PCB as

MCM Test Board Rev A

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Drawing #3823-113-ED-330237

shall be placed on the component side of the printed circuit board.

CAM Files

Gerber output shall be provided as non-zero suppressed 274-X 2.3 format (embedded aperture). Drill tape data shall be provided in ASCII format. All layers shall have a dual layer identifier on them, consisting of the standard numeric layer marker plus the name of the layer in text written outside the body of the board. An assembly drawing shall be provided in Gerber 274-X format consisting of the board

outline, all drill holes, all component side pads and all component side legend. This assembly drawing will specify all required check dimensions. A minimum of three alignment markers will be placed, in the same locations, on all layers.

The Gerber files including the assembly drawing shall constitute the check plots.

Information Transfer

Source files for the design shall be transmitted via e-mail with attachments and also made available via FTP. Outputs may be sent back the same way. The technical contact for questions are:

John T. Anderson, (630) 840-8885 or janderson@fnal.gov