U.S. Department of Energy SBIR Final Report

Phase 1 SBIR (2007)
Phase 2 SBIR (2008)
Phase 2 Supplemental Program (2010)

"Improved Controls for Fusion RF Systems"

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1.0 Executive Summary

The DOE Fusion Energy Sciences program supports a number of objectives with the common goal of expanding the science of heating and controlling thermonuclear fusion plasmas for energy production. Among these objectives are further development of several methods for plasma heating and current drive using radio frequency (RF) energy - including Lower Hybrid Current Drive (LHCD). The promise of LHCD is high, as it is a means by which tokamak plasmas can be sustained non-inductively.

For typical tokamak parameters, a LHCD system must supply several MW of power at a few GHz frequency - and for current drive, this must be presented to the plasma as an array of sources with tightly constrained phase relationships. The controls are necessarily complex, requiring sophisticated timing, phasing, protection, and monitoring. As the understanding of fusion plasmas evolves and the experiments become more complex, the demands of the controls for such a LHCD system evolve as well. In parallel, as the numbers of subsystems in a fusion plasma experiment increase, the demands of reliability for each system must increase as well.

Existing fusion experiments have kept pace with, or often led, improvements in modern electronics to meet these demands of complexity and reliability. These improvements, however, are not always applied uniformly across all subsystems. In many cases, older technology is still in use for reasons of budget, priority, or simply the availability of legacy equipment. As the world fusion program moves towards ITER, the motivation is high to modernize all such complex controls to yield the optimum in utility, reliability, safety, and ultimately cost.

In this effort, we have addressed the specific requirements for the integrated systems

Figure 1. The suite of five complete TPS core units (front assemblies and rear transition module assemblies) on the test bench after final testing, ready to ship to MIT.

controlling an array of klystrons used for LHCD. **The immediate goal for our design was to modernize the transmitter protection system (TPS) for LHCD on the Alcator C-Mod tokamak** at the MIT Plasma Science and Fusion Center (MIT-PSFC). Working with the Alcator C-Mod team, we have upgraded the design of these controls to retrofit for improvements in performance and safety, as well as to facilitate the upcoming expansion from 12 to 16 klystrons. The longer range goals to **generalize the designs in such a way that they will be of benefit to other programs** within the international fusion effort was met by designing a system which was flexible enough to address all the MIT system requirements, and modular enough to adapt to a large variety of other requirements with minimal reconfiguration.

1.1 Extended Background

The legacy LH system on C-Mod was installed earlier using conventional hardwired protection logic. There were several known disadvantages with this type of a system, offset by the simplicity of adapting known circuitry from other similar (e.g. radar) facilities. Difficulties included inaccessibility of controls for parameter adjustments (e.g. fault thresholds), long runs of cables in and out of HV areas (both increasing noise pickup and adding risk of personnel safety), and large physical footprint in the experimental cell. The goal of this program was to adapt modern electronics capabilities and experience learned in other modern phased array radar facility design to directly address these issues, creating a compact and reliable superset of the existing controls functionality. As an additional bonus, the space savings resulting from retrofitting the existing 12 klystron array with these upgraded controls considerably eases the expansion of the facility in the upcoming addition of four more klystrons for a 16 klystron LH system.

This Phase 1 effort and the initial stages of the Phase 2 effort were used to fully specify the requirements of the upgraded controls. Initially, we left an open topic for consideration as to whether to use a fully digital architecture or a hybrid analog/digital signal path – a very early decision was made to opt for the hybrid architecture, as this is inherently more robust as the fault comparators are on robust and independent signal paths, thus key equipment safety sensing circuits are implemented in a nearly failsafe manner.

Another key early decision was that the architecture would service four klystrons per unit, following the "cart" topology of the physical installation. The sheer quantity of signals that must be serviced in a four cart protection system, however, is prohibitive, particularly for a compact central control unit. That, plus the desire to reduce long cable runs to the greatest extent possible led to another early decision – we would modularize a great deal of the input/output hardware, and site a much of it at remote stations which multiplex groups of signals and transmit this over fiber-optic isolated communication lines.

During the middle of the Phase II program, we thus finalized design of a number of different I/O stations which would serve as isolated communication links, and moved into manufacturing of these even before the remainder of the system was fully specified….this gave a parallel path for both design and manufacturing, and helped constrain the final design by adhering to the chosen architecture of the I/O systems.

The core transmitter protection system (TPS) for four klystrons (one cart) was chosen to reside in a cPCI crate topology for co-location with the fast dTACQ digitizers used for data acquisition in the LH system. We did not choose to utilize the digital backplane of the cPCI

crate as a computer backbone *per se*, but instead used it as a mechanical structure and power supply. Communications to the Alcator C-Mod data system (MDSplus) was over an on-board Ethernet port directly installed in the TPS hardware, thus bypassing the backplane of the cPCI crate. We did make use of the expansion architecture of cPCI – which allows for a "rear transition module" (RTM), plugged into the backside of the crate with direct access to auxiliary contacts on the backplane connectors. This is usually used for I/O expansion, and in similar spirit, we used this for nearly all F/O connections, feeding these strictly digital signals across the cPCI backplane to the main TPS unit.

1.2 Program Schedule Modifications

During the second half of the program, we had undergone a number of delays within the Alcator C-Mod program, not the least of which was the temporary downchecking of the motor/generator flywheel, resulting in both calendar delays and unavailability of the MIT half of the team for design of some of the interfaces, originally assumed to lie on the MIT side of the collaborative effort. As the Phase II effort drew to a close, we submitted a proposal, granted by DOE, for an additional year of funding. This supplementary program served both to extend support during installation and integration, and to shift the load of design and manufacturing of a number of these auxiliary interface circuits – customized for various remote substations to provide local signals, filter and sense inputs, and standardize to the remote I/O format for transmission to and from the TPS central unit. During the first half of this additional year, these aux interfaces were designed, manufactured, tested, and shipped to MIT for early phases of the install.

In the second half of the extension year, we finally accumulated all the minor specification changes we had defined along the way and froze the design of the central TPS units. The six board assemblies were fabricated, embedded firmware written, and hardware delivered to MIT. The completion of this install, coinciding with tokamak downtime in late summer and fall of 2011, provided the opportunity to uninstall the legacy LH control systems and complete the install of the new controls. As of this writing (early November 2011), all of this equipment has been delivered to MIT and installation is ongoing, with initial *in situ* operation to begin phasing in during December 2011 and January 2012.

Rockfield Research has committed to fully support this installation and deployment, in spite of the technical termination of contract during mid August 2011. In fact, underestimate of the scope of the auxiliary circuits led to spending out the contract during June/July 2011, and Rockfield Research has continued on internal funding during subsequent efforts. The separate financial final report details the breakdown of the extent of post-contract spending.

1.3 Program Impact & Commercialization

This effort has developed a general purpose modular protection system for multi-VED (vacuum electronic device) control systems. The specific implementation delivered to MIT for the Alcator C-Mod LH controls were configured to fit that application, yet the hardware architecture design is quite open-ended, and heavily software configurable.

Typical protection systems for high voltage VED systems are custom designed and application specific. These circuits are critical – in some cases providing the only line of defense

against single-point failures for VEDs with replacement costs of several hundred thousand dollars each.

We have designed a general purpose multi-VED system which is a superset of the usual capabilities of such protection systems, and is very reconfigurable. In the fusion community, application for any such heating system is likely to greatly reduce the overhead development costs of installation, reduce time to operation, and improve both personnel and equipment safety.

It is the Rockfield Research Inc. business model to offer sale and support of a limited smorgasbord of specialized high end electronics. The manufacture and testing of such items can be largely outsourced, thus the **primary product is the support consultation and intellectual property invested in the design.** A span of a few years with zero sales will not damp the enthusiasm for continued support of such products – a sentiment unlikely to be shared by conventional electronics manufacturing and sales firms. The TPS system (and auxiliary multiplexed communications devices) have now been added to the Rockfield Research catalog, and will be supported for future customers as needed.

2.0 Architecture of the TPS

Figure 2 on the following page shows the updated block diagram of the one-cart (four klystron) TPS. The distributed nature of the TPS topology is apparent in this view – the central vertical block is the core TPS, which contains the fault logic, analog signal buffering, fault comparators, timing, and Ethernet interface. Much of the I/O, however, has been located at remote locations – sited adjacent to the source (or receivers) of the appropriate signals, with isolated multiplexed F/O links between. These remote I/O links are noted and labeled in red here.

This architecture went through many iterations in the early part of the Phase II program, and it includes the detailed specification of the interface between Rockfield Research and MIT – in regards to both the signals *and* the responsibility for interfaces. The TPS was initially agreed to comprise the core unit plus the I/O links shown and labeled “Rockfield”. Several blocks, labeled “MIT” represented custom interface circuits (usually quite small and application specific) to be built by MIT.

These links, seven in total, were deferred by MIT due to resource limitations. One of them (HV Interface box) was designed by the MIT team, as it was needed for upgrades to the legacy LHCD system with the refurbished CPI tubes. The remaining hardware links were split between the MIT team and additional effort by Rockfield under the supplemental funding extension, and are discussed in more detail in later sections.

2.1 TPS Core Unit

The TPS core unit resides in a cPCI crate adjacent to the fast digitizers, with one TPS and one digitizer per cart (4 klystrons). This unit serves as the “brains” in the transmitter protection, receiving instructions from MDS-plus over Ethernet before each shot, monitoring status lines and PLC permissives in realtime during shots, and managing fault status with sub-microsecond response time. Even with the intense effort at distributing I/O among remote stations, the I/O to this unit is a significant constraint to size and function. It is designed as a triple-width cPCI unit, with additional I/O brought in through a triple-width RTM (rear transition module) in the back of the cPCI crate. Features include:

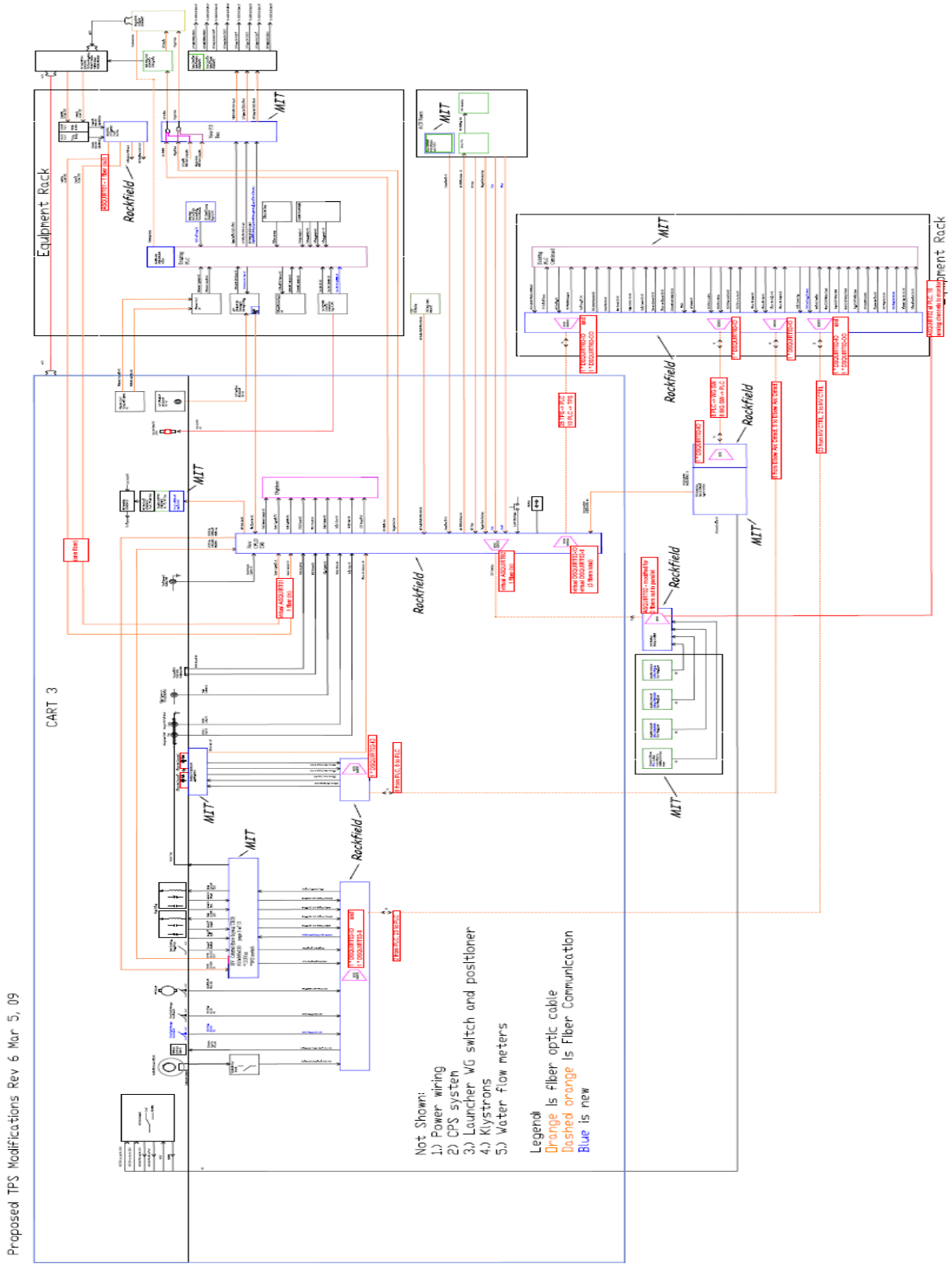

Figure 2. Block Diagram of a 4-klystron "cart" with TPS and interfaces.

- The main front board has 12 channels of analog input – these service two body currents per klystron, one ground current per cart, and three spare analog inputs. Each analog input has three comparators with programmable thresholds and inhibit delays.

Figure 3. Five of the main boards are shown above. Each of these boards services 12 analog channels (eight body currents, 1 ground current, and 3spares). In addition, there is a repeater port for MDSplus start and clock signals, an Ethernet port, and reset button and LED status display. Both the master CPU and Event Logger CPU, in addition to the programmable fault logic matrix are resident here.

- The main board (Figure 3) also has the fault FPGA matrix, the communications cpu, auxiliary memory for event logging, inhibit timing logic, Ethernet interface to MDS+, and cPCI backplane connections for power and interface to the RTM boards.

- The center front board (Figure 4) has 12 additional analog input channels – these service the one beam current per klystron, plus forward and reflected power sensors for each klystron. The beam current is processed similarly to body currents, while the forward and reflected power are compared ratiometrically for faults. Fiber optic inputs for the multiplexed analog data highways are on this board as well.

- In addition, the center board *digitizes* the beam current and forward power (albeit at relatively slow rates) for use in the COTS calculation. This is combined with the water temperature and flow measurements and the beam voltage measurement (received via analog links) for predictability of the realtime collector temperature. An analog temperature predictor is generated as a new data signal (to external digitizers), and sent to a fault comparator with programmable fault threshold.

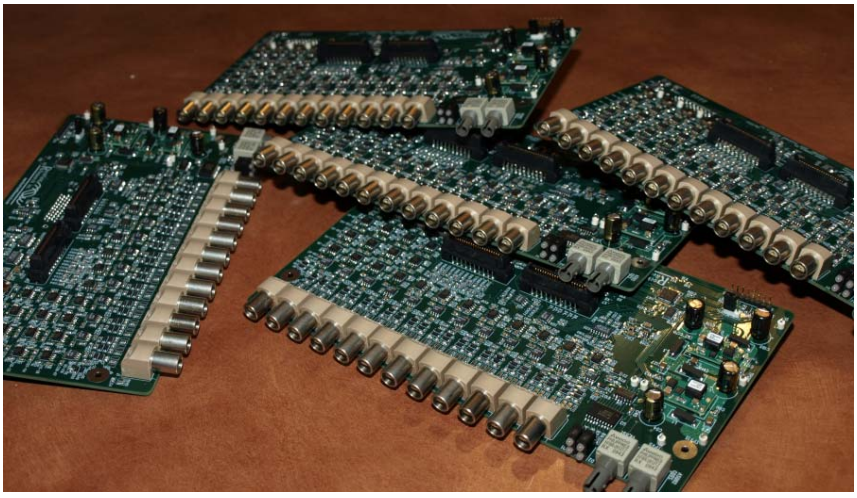

Figure 4. Five of the middle (COTS) boards are shown above. Each of these boards has 12 analog channels (four beam currents, and four pairs of RF diode inputs), as well as F/O inputs for the two ASQUIRT inputs. The COTS cpu is onboard here as well.

- The third front board (Figure 5) is an analog repeater board, which echoes

30 separate analog signals to front panel testpoints as well as to a 68-SCSI connector with pinout to match the input to the d-tAcq digitizer.

- The triple RTM module (Figure 6) has 42 F/O connectors – 36 of which have pre-allocated functionality, and 6 of which are spares (and configurable as either input or output).

Board-to-board mating uses hard connectors (not cables), which comprise part of the 3D assembly of boards. One of the three boards in each set (front and back) mate to the cPCI backplane for power and communications.

Figure 5. Five of the analog repeater boards (the third, or top board of the front assembly) are shown above. Analog signals, scaled and buffered are brought onto this board via board-board connectors, repeated via on-board buffers separately to single-pin LEMO test points and to a SCSI68 connector to mate with fast digitizer.

On the following page, Figure 7 shows the overall topology of the 6-board core TPS unit. On the left are the "front" board stack, from the bottom up:

- Main board, with Ethernet communications, fault logic, half the analog signals, data logger, and cPCI backplane connection to RTM modules,
- COTS board (middle), with the COTS cpu, and half of the analog signals,
- Monitor board (top), with buffered monitor points for debugging and SCSI68 connection to the fast digitizer.

On the right side of Figure 7, we see the three-board stack of the RTM, which contains little besides 42 fiber-optic I/O channels. All of the on-board intelligence to interface to these signals resides on the main "front" board.

In the following sections, we will discuss many of the key features of the core TPS unit, broken down by function rather than physical board location.

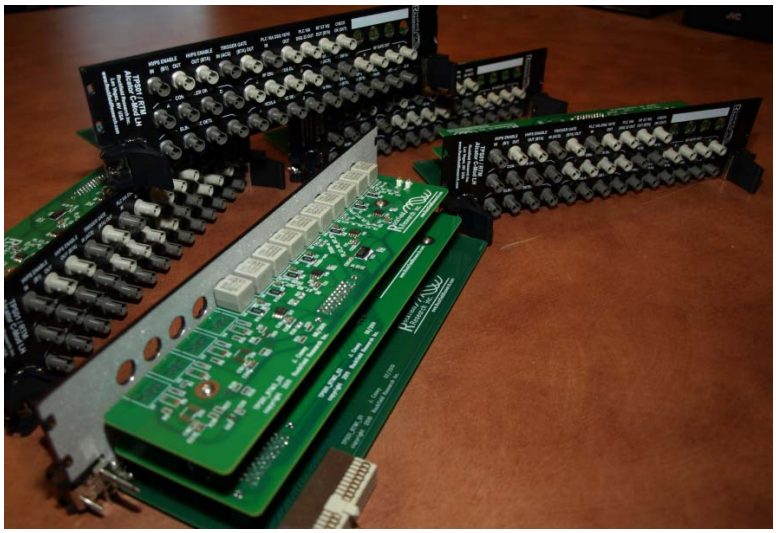

Figure 6.Five of the six three-board RTM assemblies manufactured are shown above. The lowest of the three boards mates to the cPCI backplane, as well as mounting board-to-board connectors to the other two boards. The panel hosts 42 fiber-optic I/O channels.

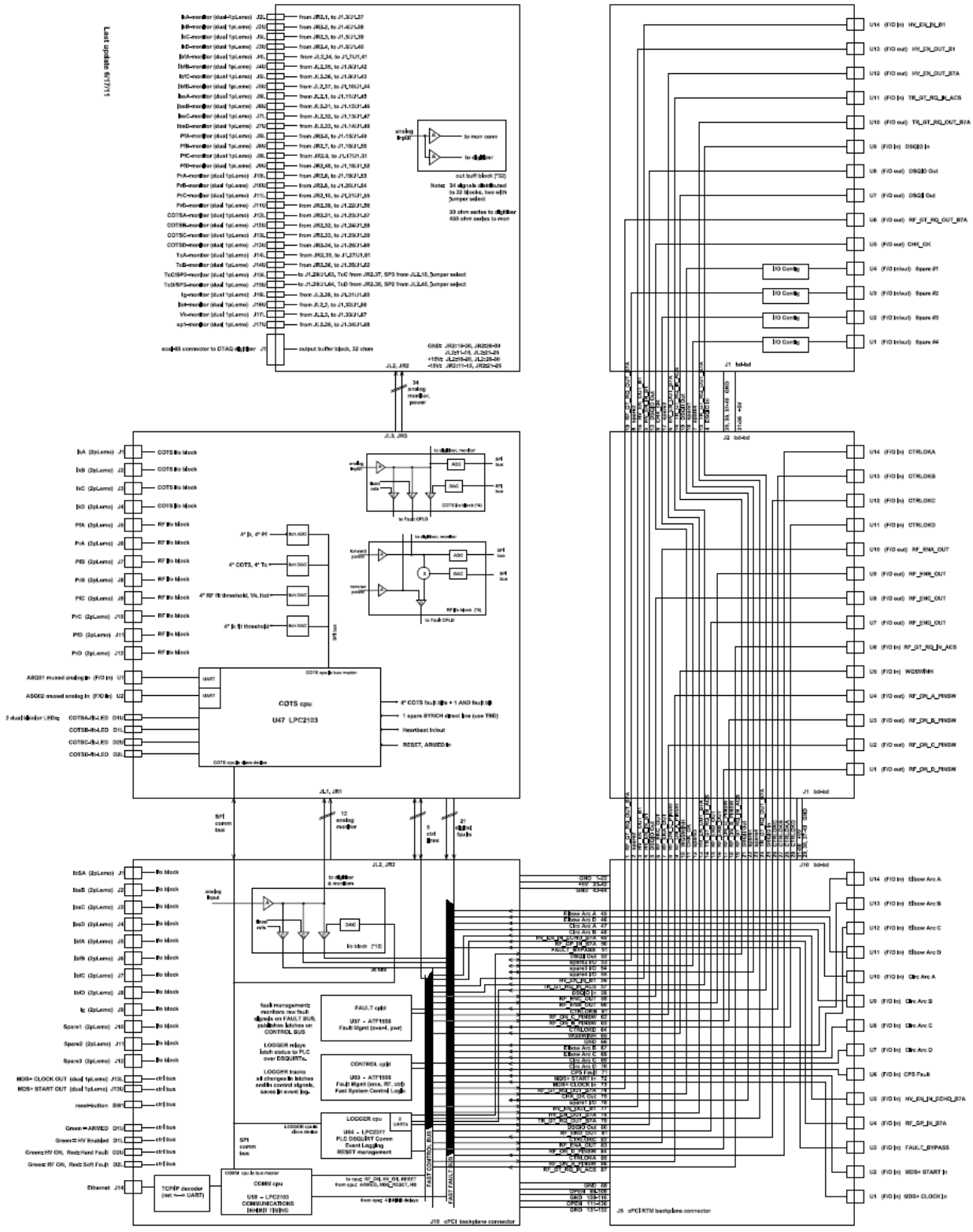

Figure 7. Block Diagram of the 6-board Core TPS architecture.

2.1.1 Collector Over-Temperature System (COTS)

The COTS – collector over-temperature system – is a digital model for the klystron collector temperature. It is necessary because the klystron vendor, CPI, notified MIT rather late in the game that the klystrons were in fact not sufficiently well cooled to accept full pulse-length unspent beam on the collector without incurring catastrophic damage. As the klystrons are quite expensive, this was deemed a serious matter. The klystrons are electronically vacuum diodes – high voltage is placed on the cathode, and a current is extracted towards the collector (according to the Child-Langmuir $V^{3/2}$ dependence, or perveance, typical for vacuum diodes). At full voltage (and thus current), this beam will present the full HV power on the collector surface, which must be removed by cooling water with neither copper vaporization nor water boiling. In fact, the klystron is an RF amplifier, and RF energy is emitted through the output coupler in proportion to the RF input. At reasonable efficiency, there is considerably less power presented to the collector than that emitted by the cathode, thus the cooling load is lessened.

There are several types of faults that the klystron must be protected against. Any internal arcing within the vacuum path must be responded to by immediately removing the HV power, which results in a shutdown of the HV. Lesser faults, however, such as air breakdown in the waveguides resulting in waveguide arcs, can be dealt with more easily by simply shutting off the RF input to the klystron. This is preferable, since we can wait a short time for the fault to clear (tens of ms), then re-establish the RF input to the klystron and continue operation after only a very brief interruption. Shutting down the RF, however, increases the energy in the spent beam, thus increases the energy load by the cooling.

At present, the MIT team must limit the RF pulse length to the worst case conditions – where RF is off for the entire shot, and the collector temperature is nevertheless safe. This is unsatisfactory, as longer pulsing is desired for physics experiments, and the cooling load is actually considerably less in practice since the RF is generally on. A collector temperature measurement would provide a simple answer, as we could interlock and shut down HV if the temperature approached the danger level – yet this is not possible, as the temperature is worst on deeply buried inside surfaces of the klystron. The difference between safe and disastrous are in fact contained within the time for water to transit from these deeply buried surfaces to the nearest available port for a thermal sensor – so we cannot safely measure downstream water temperature and shut off in time.

The COTS was thus designed as a predictor of the collector temperature. We gather all the inputs for power *into* the klystron: beam voltage and beam current, and calculate this load. We also gather all the inputs for power removal *from* the klystron: water temperature and flow, and RF power out. The difference must result in a net rise in the collector temperature – the rate of rise being determined by the heat capacity of the collector with its water load. Additionally, we can calculate the additional safety factor from the elevated boiling point of the water by measuring the water pressure as well. All of these signals are presented to the TPS in realtime, and the model maintained in realtime --- at all times, in fact, regardless of whether or not a shot is in progress. There are no adjustable parameters for the key power balance, and only the heat capacity of the tube is relative unknown, but that plays only into the dynamics, and is rather easy to match b y comparing temperature decay rates after a pulse once the system is installed.

As designed, we dedicated an ARM7 microprocessor just to accommodate the COTS calculations for the four klystrons serviced by a single TPS unit. This microprocessor talks to

two analog multiplexed remote I/O units (one which provides beam voltage, the other which provides 16 channels of water temperatures, pressures, and flowrates). It also directly digitizes the discrete beam currents and RF diode signals for each of the four klystrons. Gathering all this information, it updates the model for the klystron internal temperature at 1 msec intervals. MDSplus settable parameters, as well as fault trip points, are maintained in this processor – and it generates dedicated digital fault channels for each klystron to signify that the model temperature has exceeded the allowed setpoint. These fault bits are treated like any of the analog path hardwired comparator outputs – fed to the programmable logic matrix for sub-microsecond fault response, with removal of HV permissives as a response.

COTS Implementation

The COTS algorithm is coded in ARMASM to run in realtime on an NXP (Phillips) LPC2103 ARM7 microprocessor. No operating system or high level compiler is used, thus increasing speed and reliability (at the cost of coding effort.) This is a relatively fast 32 bit micro, but has no floating point math skills. Some pre-processing has been done in coding, and is necessary in converting from MDS+ setpoints to shot-loadtime setpoints in order to streamline the calculations. No divide or transcendental math are performed in realtime – all such calculations are pre-fit to polynomial expansions over the range of interest, allowing exclusive use of hardware instructions for multiply, accumulate, and shift.

The COTS calculation is performed on the 2nd (middle) of three boards in the front TPS assembly (Figure 8). There is one TPS assembly on each cart, thus each one services four klystrons. The beam current transducers and the RF diodes are processed on this same board for proximity to the COTS usage.

Each of the beam current (cathode current, klystron current) signals is generated by a FW Bell RS-100, with a raw signal calibration of 40 mV/A. It is oriented for positive signal under normal operations.

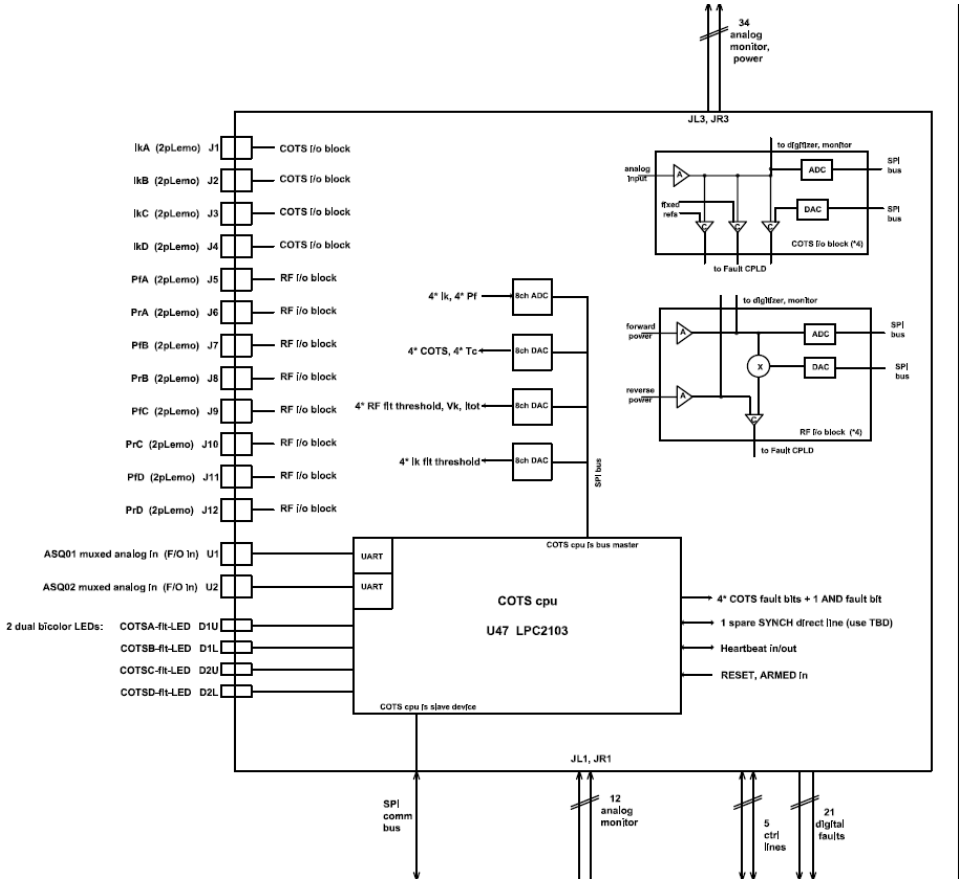

Figure 8. Expansion of middle-front board from Figure 7. The COTS model dominates this board, and the analog signals serviced on this board are the ones needed for the COTS calculation.

The analog processing section of the COTS board performs a clean-up (transient glitch protection, 1MHz *RC* filter), then buffers this through a 25 MHz op-amp (LT1358) with a differential gain of 5x. (The signal is treated differentially on input from a two-pin LEMO connector, although it is realized that the signal is technically single-ended). This buffered signal is fed to three comparators for fault detection (one to detect backwards-oriented installation, one with a pot-settable trip-point which is always active, and one with an MDS+ settable trip-point which is inhibited for a brief inhibit delay after the HV is turned on). The signal is then fed to several analog points of interest: 1) buffered and passed to a dTacq digitizer connector, 2) buffered and passed to a single pin LEMO testpoint, 3) routed to a local 8-channel 12 bit multiplexed digitizer. This last is digitized with a 12 bit scaling of 0-25A. The COTS microprocessor polls each ADC channel at 1 kHz.

Each of the RF diode pairs (forward, reverse), are provided by loop directional couplers with a default orientation for a negative signal. The directional couplers have a 50 dB attenuation, and the signal paths have an additional 15-20 dB attenuation. Typical signal amplitudes are about -2V.

Each detector input is again cleaned up (transient protection, 1 MHz *RC*), then buffered through a -2.5x gain differential amplifier, producing a positive signal with typical amplitude of about +5V. Each is similarly sent to the dTacq digitizer and to a single pin LEMO test point, and a ratiometric fault sensor is applied to each forward / reflected pair. This entails using an analog multiplier (AD633) with an MDS+ settable multiplication factor between 0.0 and 1.0 to attenuate the forward signal (and applying a 0.5V positive offset as well), and then faulting (via comparator) if the reflected power exceeds this calibrated fraction of the forward signal.

In addition, the forward signals (but not the reflected signals) are locally digitized by the same 8 channel 12 bit digitizer as the beam current. The scaling of this is such that the 12-bit range corresponds to 2.46V of the raw diode signal. This is also polled by the cpu at 1 kHz.

The main loop of the COTS code polls this digitizer at 8 kHz, with interleaved sampling of the four beam currents and forward powers ultimately sampled at 1 kHz each. The COTS calculation is called at 4 kHz intervals, with interleaving between the four klystron channels – and each klystron COTS calculation is done as soon as its relevant signals are acquired; thus the COTS calculation for each klystron is updated at 1 kHz. Benchmarking shows that the entire calculation update for a single klystron is performed in 26 μsec.

The TPS system makes extensive use of ASQUIRT and DSQUIRT modules, which are very similar to the in-house AFOL and DFOL links that Alcator C-Mod already uses. They differ in that they are fully digital, with complex messages passing via F/O both ways. These messages include dip-switch settable addressing, checksums, firmware version numbers, and other failsafes to help prevent erroneous operation of equipment. The ASQUIRT01 units transmit and receive 0-10V signals at 12 bit resolution, with two channels updated at 10 kHz. The ASQUIRT02 units transmit and receive either 0-10V or 0-20mA signals at 12 bit resolution, with 16 channels updated at 1 kHz.

One ASQUIRT01 unit placed in the LH HV control area of the Alcator C-Mod cell transmits the power supply voltage on channel 1, with a 12-bit range of 0-60 kV. The total supply current is on channel 2, with a 12-bit range of 0-500 A. The ASQUIRT01 units are made with four parallel F/O outputs (but only a single F/O input). This ASQUIRT01 unit feeds to all 3 (4 after the upgrade) LH klystron carts. There is no corresponding ASQUIRT01 mate to receive this

signal – the F/O receiver is on the COTS board, and the signal is decoded by a "virtual ASQUIRT01" routine within the COTS cpu. The ASQUIRT01 timing is controlled by the sending unit, and the receiving decoder is polled, thus is asynchronous with the COTS calculations. When complete and valid message packets are received, the "outputs" (buffers in SRAM) and status flags are updated. Timeout on receive, receive errors, or other faults revert the outputs to values of zero, and error flags are set.

Four ASQUIRT02 units are used at each cart. One normal ASQUIRT02 pair monitors the RTD temperature sensors on the klystrons, with these signals received only at the PLC station, and dealt with normally there. One more ASQUIRT02 – modified to have dual parallel F/O outputs (but no F/O input to copper output section) monitors fourteen signals associated with the klystron cooling on that cart. One fiber goes to a second ASQUIRT02 receiver at the PLC station, while the other goes to a "virtual ASQUIRT02" receiver on the COTS board, again decoded by the COTS cpu. This is treated similarly – the reception is polled and timing is controlled by the sender, thus asynchronous with the COTS calculation. Valid received packets are decoded and the messages are updated (packets are actually transmitted at 8 kHz, with two channels sent per packet). Any fault or timeout on reception zeros all received signals and sets fault bits. The channels include outlet water temperatures, pressures, and flows for each klystron, as well as temperature and pressure at the inlet manifold.

Since both ASQUIRT0x units operate asynchronously, updating the "outputs" – which are really just buffer memory in the cpu – whenever valid data is received, this data is treated as a simple lookup table for the COTS calculations, supplying the most recently received data.

The COTS system will produce a calculated model temperature for the water in the klystron collector cooling loop for each tube. The goal is to treat this as a realtime signal, and to latch a fault if it exceeds a given threshold. For verification purposes, we also convert this model in realtime to an analog signal and ship it out to the dTacq digitizer for acquisition by MDS+. These signals are updated at 1 kHz (as the COTS calculation is performed), and scaled with a 0-10V range corresponding to a 0-250C temperature. The analog outputs are generated by a muxed 12-bit DAC. (These analog signals are also available as single-pin LEMO testpoints on the TPS unit).

Additional analog outputs are provided for convenience in benchmarking performance of the system. We echo the two ASQUIRT01 signals (beam voltage, total current) to 0-10V signals with the same ranges (0-60kV, 0-500A respectively), updating these as the ASQUIRT01 packets are received, and sending to both dTacq digitizer pins and LEMO testpoints.

We also echo the *measured* klystron outlet water temperatures which are received from the ASQUIRT02 transmission. These are similarly sent to dTacq pins and LEMO test points. These are rescaled to have the same range as the COTS temperature signal – 0-10V range corresponds to 0-250C, and are updated as ASQUIRT02 packets are received.

COTS Calculation

The COTS calculation is quite simple. We determine *Power In – Power Out* , and divide by the heat capacity of the klystron collector cooling system to get the *dT/dt*, i.e. the rate of change of temperature. The power in is simply the beam voltage multiplied by the beam current. The power out is the sum of the forward RF power as determined by a calibration curve on the forward RF diode, and the power removed by the cooling water. The latter is determined by the

difference between the COTS temperature and the measured water inlet temperature, and multiplied by the water flow rate. Thus, for a timer interval *dt:*

$$dT = \frac{I_{beam}V_{beam} - P_{rf} - Q(T_{COTS} - T_{in})}{k}\ dt \quad .$$

The first part of the calculation requires us to calibrate the forward power diode signal. The C-Mod team[1] maintains calibration measurements, fit to a cubic with a calibration for the 50dB attenuator used. The form of these calibrations is defined as:

$$P = \frac{\left(a_1V^3 + a_2V^2 + a_3V + a_4\right) * 10^{\left(-a_5/10\right)}}{10^6} \quad ,$$

where V is the raw diode voltage in Volts, *and which is negative*, and the power P is given in kW. The coefficients were provided by calibrations done by the MIT team.

Note that this can be reduced somewhat, as the above calibration does not really represent five independent constants, but only four. If we fold the attenuator calibration into the other constants we get a simple cubic expansion. Furthermore, our forward diode signal is digitized with a 12 bit (0-4095) range of 0-2.456 V, and we must remember that we have removed the sign flip in the process. Rolling this all together, we now get something with a more tractable form:

$$P = b_1N^3 + b_2N^2 + b_3N + b_4 \quad .$$

N is now the number of raw counts of the digitized RF signal. (We will keep the unusual ordering of the coefficients, *vs*. the standard nomenclature where the subscript matches the exponent, to match Atma's calibration documents.)

Applying a few tricks to make this work well for 32 bit unsigned math, we can rewrite this as:

$$P = -c_1\left(\frac{N}{2^6}\right)^3 + c_2\left(\frac{N}{2^4}\right)^2 - c_3N + c_4 \quad ,$$

with N being the raw RF diode counts over a 0-4095 range, and the power P given in mW, the calculation and all intermediate steps maintain maximum accuracy while staying within a 32 bit range. All four of the calibration coefficients are now defined as strictly positive, and the sign is maintained in the form of the calculation.

We will load the coefficients c_1 through c_4 for each klystron via MDS+ tables. These can be loaded prior to each shot, or written into flash memory within the cpu to become power-up default values – confirmatory writing prior to each shot is of course recommended.

The conversion from Atma's calibrations to these numbers is as follows:

$$c_1 \equiv a_1 * 10^{\left(-a_5/10\right)} * \left(599.75 * 10^{-6}\ \mu\mathrm{V}/\mathrm{count}\right)^3 * 2^{18},\ \text{typical = default = 226,}$$

and c_1 will be constrained to be a positive integer $< 2^{12}$.

[1] Personal communication, Atma Kanojia

$$c_2 \equiv a_2 * 10^{\left(-a_5/10\right)} * \left(599.75 * 10^{-6}\ \mu V/\text{count}\right)^2 * 2^8, \text{ typical = default = 5400,}$$

and c_2 will be constrained to be a positive integer $< 2^{14}$.

The temperature model is maintained in a similar fashion – we roll the intermediate coefficients up into single unsigned integers, with care to maintain the range of all intermediate terms as well as the final result. We repeat the COTS calculation at 1 kHz, so the value of *dt* is fixed. The form of the calculation is:

$$\Delta T = k_1 N_V N_I + k_2 N_Q N_{Tin} - k_3 P_{cal} - k_4 N_Q N_{COTS} \quad .$$

We have already discussed most of these terms (N_V is the raw counts of the ASQUIRT01 beam voltage measurement, N_I is the raw counts of the locally digitized beam current, N_Q is the raw counts of the ASQUIRT02 flow rate, N_{Tin} is the raw counts of the ASQUIRT02 inlet temperature, P_{cal} is the previously calibrated RF power, N_{COTS} is the model outlet water temperature, and ΔT is the incremental correction to T_{COTS}.

The calculation is performed as a chain multiply-accumulate-shift with 64 bit accuracy. The additional accuracy is necessary in that very small temperature changes must be allowed for the small (1 ms) time intervals, particularly at the tail end of the exponential decay as the tube cools back down towards the inlet temperature. The four constants, k_1 through k_4 are actually a factor of 2^{32} oversized, so that the extra accuracy is on the correct (LSB) end of the calculation, and so that we may simply harvest the top half of the result at the end of each calculation. (64 bit, or two word, multiply and multiply-accumulate instructions are also primitives for the ARM7 processor.)

This calculation is continuously iterated at 1 kHz, maintaining the COTS model temperature. Clearly, with no signal for beam current or RF power, the COTS temperature should always converge quickly to the inlet water temperature. Note that we maintain no synchronicity with the HV or RF controls which are separately maintained elsewhere within the TPS hardware – this calculation proceeds blindly and continuously as long as the TPS is powered, with no knowledge of whether or not a shot is taking place.

COTS Fault Threshold

The previous calculation generates a model for the outlet water temperature, thus making a calculated proxy for the actual internal water temperature (which we cannot measure). We would like to set a trip-point threshold which we use to shutdown the HV for the remainder of the shot – one high enough to allow the largest possible window of run parameters (particularly "picket-fence" operation with reasonable duty cycle of RF low or off) – but also within safe bounds to avoid damage to the klystron.

Literature from CPI has given us guidance on the water temperature at the skin layer adjacent to the copper surface in the collector – typically 25% higher than the bulk water temperature (in deg C), thus we need to depress the fault threshold below 100C to account for this. Pressurization of the water, on the other hand, elevates the boiling point, which thus elevates the fault threshold. Finally, prudence dictates that we allow an additional safety margin from the actual boiling point.

In equation form, this yields:

$$T_{fault} = T_{boil}(P) * k - \Delta T_{margin} \quad .$$

We've already discussed how the pressure is measured in the suite of signals received over the ASQUIRT02. This pressure measurement can be used to first calculate the boiling point of the water at the elevated pressure. Reducing steam table curves to a cubic fit, and using our usual technique for multiply-accumulate-shift with single 32-bit word internal accuracy, we use the massaged formula:

$$T_{boil} = \frac{\left[6312 \left(\frac{N_P}{2^7} \right)^3 - 18580 \left(\frac{N_P}{2^5} \right)^2 + 45371\ N_P + 55246848 \right]}{2^{15}} \quad ,$$

Where N_P is the raw pressure measurement (in counts) with the 819 count floor subtracted off (i.e. 0-3276 counts = 0-232 psig), and the boiling temperature is in units of 4095 counts = 250 C. All of these coefficients are fixed. This fit gives better than 1% error over much of the range 100-200C, with the worst error (about 3C) right at 0 psig.

The factor k has a default value of 0.8, and will be maintained by MDS+, either loaded every shot or overwritten in flash memory for future power-on defaults. It is entered as an integer, to be divided by 4096, e.g. the default value is actually 3277. (The MDS+ value loaded must be a positive integer < 4096).

The factor ΔT_{margin} is also maintained by MDS+. It is recommended that this have a minimum value of 5C, due to the errors in the boiling point approximation, and prudence dictates that it actually be considerably larger. The default will be 15C. This is entered as an integer on the 250C = 4095 count scale, thus the default is 246.

This fault temperature threshold is updated in realtime on every cycle that the COTS temperature is updated, and used for determining whether or not a fault condition has occurred.

COTS Fault Logic

The COTS cpu produces five fault (status) bits. There is one bit for each klystron (COTSAOK, COTSBOK, COTSCOK, COTSDOK) which give the status of the COTS temperature model relative to the fault threshold. If the fault condition is tripped for one of these, it will LATCH off, and will not reset until the main cpu on the TPS has issued a RESET command, *and* the over-temperature condition no longer exists.

These four bits are also hardwired directly to four bicolor LEDs on the front of the COTS board, and piped to the layer1 board of the TPS, where they are monitored by both the EVENT LOGGER and by the DSQUIRT communications which echo them to the PLC.

In addition, there is a single master fault bit of opposite polarity, COTSFLT. It is latched on if any of the COTSFLT latches go on, or if the local power supply monitor (this board only) shows a fault. It also will only reset on a master RESET with all fault conditions clear. The COTSFLT bit is transmitted to the layer1 board of the TPS, where in addition to the EVENT LOGGER and DSQUIRT communications, it is used in the CPLD logic matrix to generate a "hard fault" which takes down all HV immediately, and for the duration of the shot.

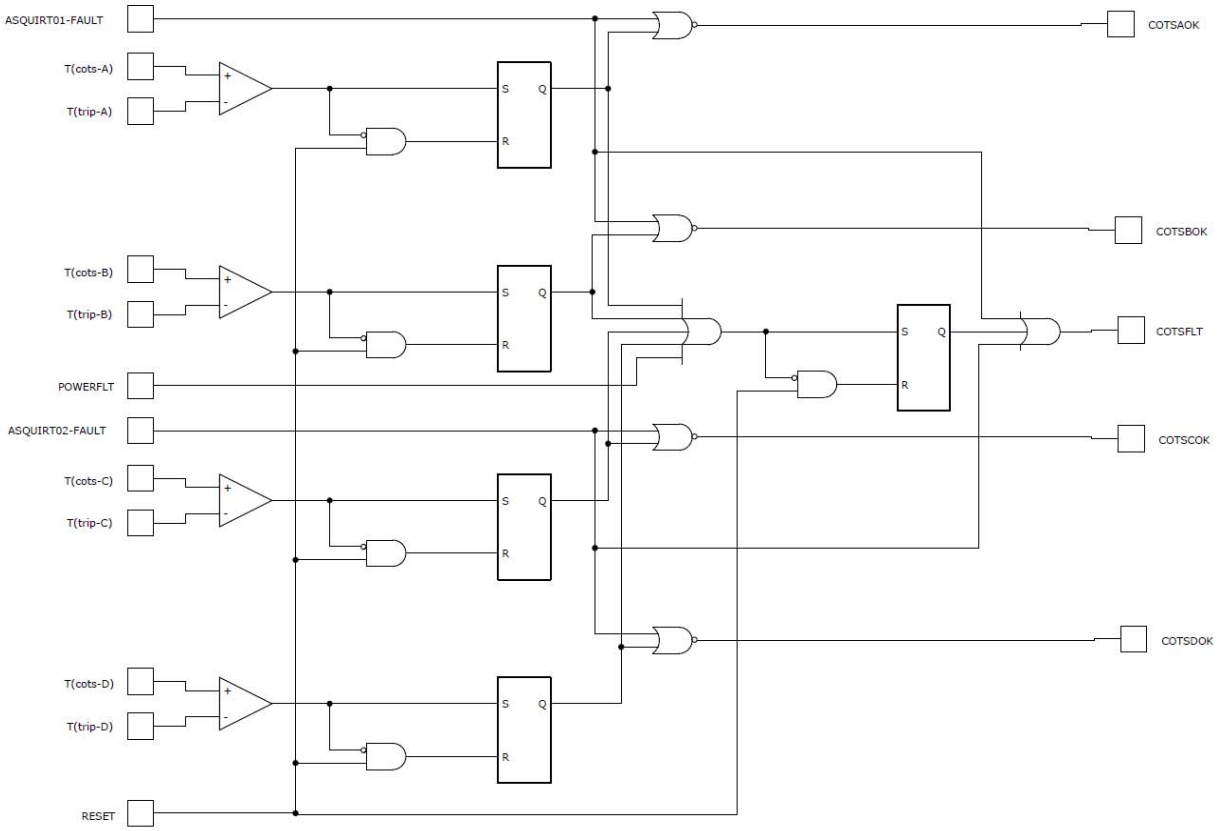

Figure 9. Logic diagram for the COTS fault determination.

We maintain a different logic for the faults on the ASQUIRT receiver routines. These will fault out if the receivers timeout without a valid packet, or if addresses or checksums don't match, or if there is a format error in the received packet. If either of these receivers fault out, we express the COTSFLT, but without latching. Similarly, we turn the COTSAOK and COTSBOK bits false without latching if the ASQUIRT01 faults out, and we turn the COTSCOK and COTSDOK bits false without latching if the ASQUIRT02 faults out.

This serves the following purpose:

- we generate a COTSFLT which inhibits all HV if there is any ASQUIRT failure, which is as it should be, as the COTS model temperature is no longer valid,
- we have an unlatched LED indicator at the front panel to indicate the validity of the communications link with the ASQUIRT01 and ASQUIRT02 senders – these will flicker red to green as the fibers are plugged in and the communications synchronize.

COTS Testing and Verification

For tests, we load in all the defaults mentioned above *except* for the fault threshold coefficients. For those, we assume a *k* multiplier of 1.0, and a margin of zero. We will thus begin with the fault trip point equal to the boiling point calculation.

In addition, we bypass the ASQUIRT02 readings, and superimpose fixed numbers for the following:

- T_{in} = 20C
- Q = 38 gpm
- P = 0 psig (thus the fault trip should be 100C)
- T_{out} = 40C

Similarly, we bypass the ASQUIRT01 readings, and superimpose fixed numbers for

- V_{beam} = 50 kV

We will apply no signal to the forward RF signal. Our only variable for this first test will then be the beam current. We will apply a signal from an arbitrary waveform generator to the I_{beam} input for channel A, and simultaneously monitor the analog COTS signal. We will also temporarily suspend the latching nature of the COTS fault bit, and echo the COTSA fault out to a spare pin on the cpu, which we also monitor.

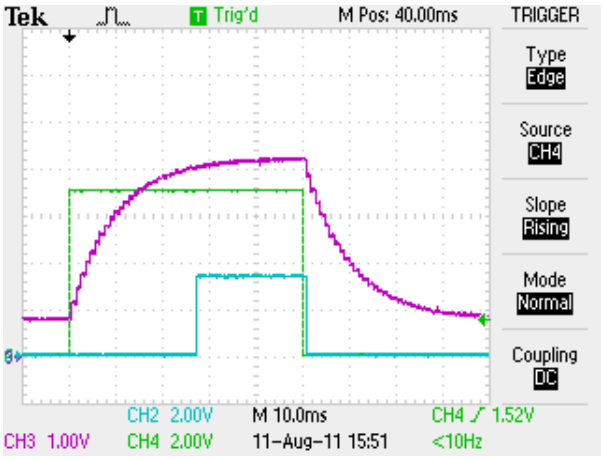

Figure 10. Test of COTS – the green trace is an emulation of 17.5A of beam current for 50 ms. The purple trace is the real-time COTS temperature model, and the blue trace is the overtemperature fault signal.

In Figure 10, we see a signal on channel 4 (green) applied to the I_{beam} input of the COTS board for channel A. It is a pulse 700 mV in height for 50 ms. This corresponds to 17.5 A, or at 50 kV, to 875 kW of input power.

The steady state cooled temperature has no free parameters at all - only the transients depend on our assumptions for the heat capacity. Applying the steady state relation that $V*I = Q\Delta T$, we quickly calculate an expected temperature rise between inlet and outlet of 88 degC.

The purple trace (channel 3) is the COTS model temperature for channel A, which rises from 800 mV to 4.20 V. At 10V = 250C, this translates as rising from a base of 20C to a steady state of 105C, for a rise of 85C. Check (close enough).

The blue trace, channel 2, is monitoring the temporary test point which echoes the (unlatched) \COTSAOK bit. Careful inspection shows that this is acting correctly – as a comparator for the COTS temperature relative to a reference of 100C. Check.

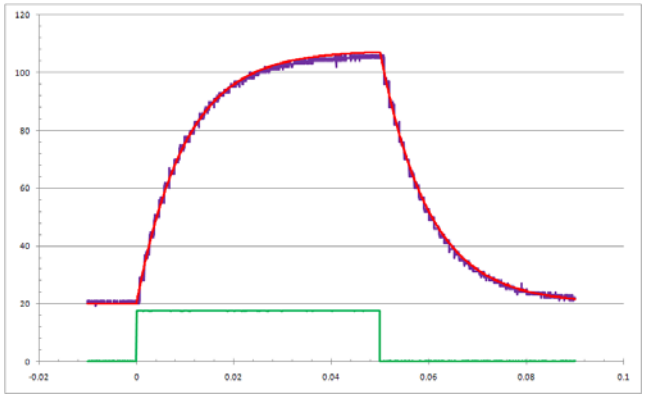

Figure 11. Test of COTS – same data as above, compared to a separate spreadsheet calculation for dynamics.

If we capture the same data to a spreadsheet and run the transient model, we can verify the dynamics of the rising and falling exponentials. In this case, we have the default coefficients derived from a heat capacity of 100 J/degC. The green and purple traces in Figure 11 are the

same (now in Amps and degC, respectively), while we have added a red trace calculated from first principles with the above numbers. Check.

Other contributions to the calculation are checked by, one at a time, removing the debug code which overwrites the input values from the source, and applying a signal to the appropriate input (in the case of the ASQUIRT0x modules, to the inputs on the remote sending unit).

- For a 10 psig signal (overwritten), the boiling point should rise to 116C. At k=1.0 and zero margin, we now observe the fault threshold at 116C
- Entering k=3277, for a factor of 0.8, we should observe the fault threshold at 93C. Check.
- Leaving k=0.8, we raise the margin to our 15C (246), which should drop the fault threshold to 78C. Check.
- Leaving k=0.8 and margin of 15C, we eliminate the overwrite of the measured pressure and use the ASQUIRT02 value. At 5 mA, corresponding to 14.5 psi, the boiling point should be elevated to 121C. That should raise the threshold to 82C. 81C observed. Check. At 15 mA, corresponding to 160 psi, the boiling point should be elevated to 187C. That should raise the threshold to 135C. 132C observed. Check.

We now leave zero signal into the pressure input, which should leave the boiling point at 100C (this however is the point of worst case error in the cubic fit, and it instead is about 103C). For k and margin as set, the fault trip point should now remain fixed at 67C. Check.

- We now remove the debug overwrites for all five of the temperature readings over ASQUIRT02. Supplying a signal to the input temperature channel, we now correctly see the baseline for the COTS model temperature shift up and down. At 8mA, corresponding to 25.3C, we correctly see a 25.3C baseline.
- Next, we remove the debug overwrites for all four of the flow readings over ASQUIRT02, and apply a signal to the remote ASQUIRT02. This, unsurprisingly, is the most profound change. At 18mA signal, which corresponds to 87 gpm cooling, a 100 ms 750 mV pulse into the I_{beam} input brings the temperature to only 40.5C (from a 0C baseline). 750 mV corresponds to 18.75A, or 938 kW at our fixed 50 kV. At 87 gpm, the steady state power balance requires a 40.8 degree ΔT. Check. At the other end, we crank the cooling way down, for only a 5mA signal, corresponding to 6.8 gpm, we must crank the beam current way down so as not to saturate the COTS model at 250C. Similarly, it takes much longer to reach steady state. We fix on a 300 mV pulse for 300 msec. This corresponds to 7.5A of beam current, or 375kW. The steady state power balance requires 210 degrees of ΔT. From a 0C baseline, we observe 210C. Check.
- Next, we put back the debug overwrites for flow at 38 gpm, and we remove the overwrites for beam voltage from ASQUIRT01. Applying 5V to the ASQUIRT01 input corresponds to 30kV. Pulsing the I_{beam} input with 500 mV (12.5A), or 375kW should give us a 37.4C temperature rise at 38 gpm. We measure 37C. Applying 9V to the ASQUIRT01 input corresponds to 54kV. For the same beam current, we should have 675 kW, and a 67.3C temperature rise. We observe 68C. Check.

- Finally, we apply a *negative* pulse to the forward RF diode input. This has the curious and unphysical interpretation of RF power being extracted when there is no beam, thus magically cooling the klystron. In Figure 12, we are applying a steady 8mA to the ASQUIRT02 input temperature terminal, thus giving us an elevated baseline of about 25C. We apply a 300 ms negative pulse of 1.5V (the green trace), which should calibrate to be 85 kW of RF power out. At our fixed 38 gpm, this should give us a ΔT of 8.5C. We observe 8.4C. Check.

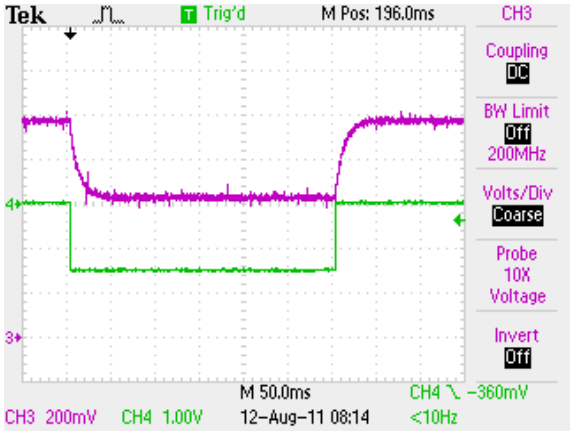

Figure 12. Test of COTS – a contrived test for pseudo cooling of the klystron via RF power extraction.

Additional Functions of COTS System

The COTS board is only part of the TPS assembly. The main TPS board serves the all-important function of monitoring all fault signals for conditions which require shutdown of RF, HV, or both. We process the RF and Beam Current signals on the COTS board because these signals are needed for local digitization for the COTS algorithm. In addition, these signals require fast comparators to sense fault levels, and the digital outputs are transmitted promptly back to the main board.

Additional functions that are provided by the COTS cpu, besides those discussed above, include:

- Controlling the multi-channel DACs which generate the MDS+ programmable fault-thresholds for beam current and RF reflected power ratio,
- Pass-thru of a master 'heartbeat" signal for watchdogging the TPS intelligencia,
- Communications (over a dedicated SPI port, which the COTS cpu is a slave to) with the master cpu on the main TPS board, and interpretation of commands passed by MDS+ (e.g. modification of setpoints, etc)
- Read/write of FLASH memory as needed, or as directed by MDS+ command.

2.1.2 Event Logger

The other novel feature in the TPS upgrade is an event logger. This is essentially a virtual logic analyzer, which tracks up to 96 channels of digital signals, and records an "event" whenever ANY of them change flag. This event is stored in local memory, along with a timestamp referenced to the 1 MHz shot clock used by the MDSplus data system. Post-shot, MDSplus downloads this event log, and thus can create a table or logic-analyzer-like plot of all status and fault bits, thus observing the sequence of controls and faults in a complex cause-and-effect situation. Since the timebase is the same as the MDSplus system, this plot can be overlaid with any physics signal from the MDSplus system for reconciling events across the C-Mod experiment.

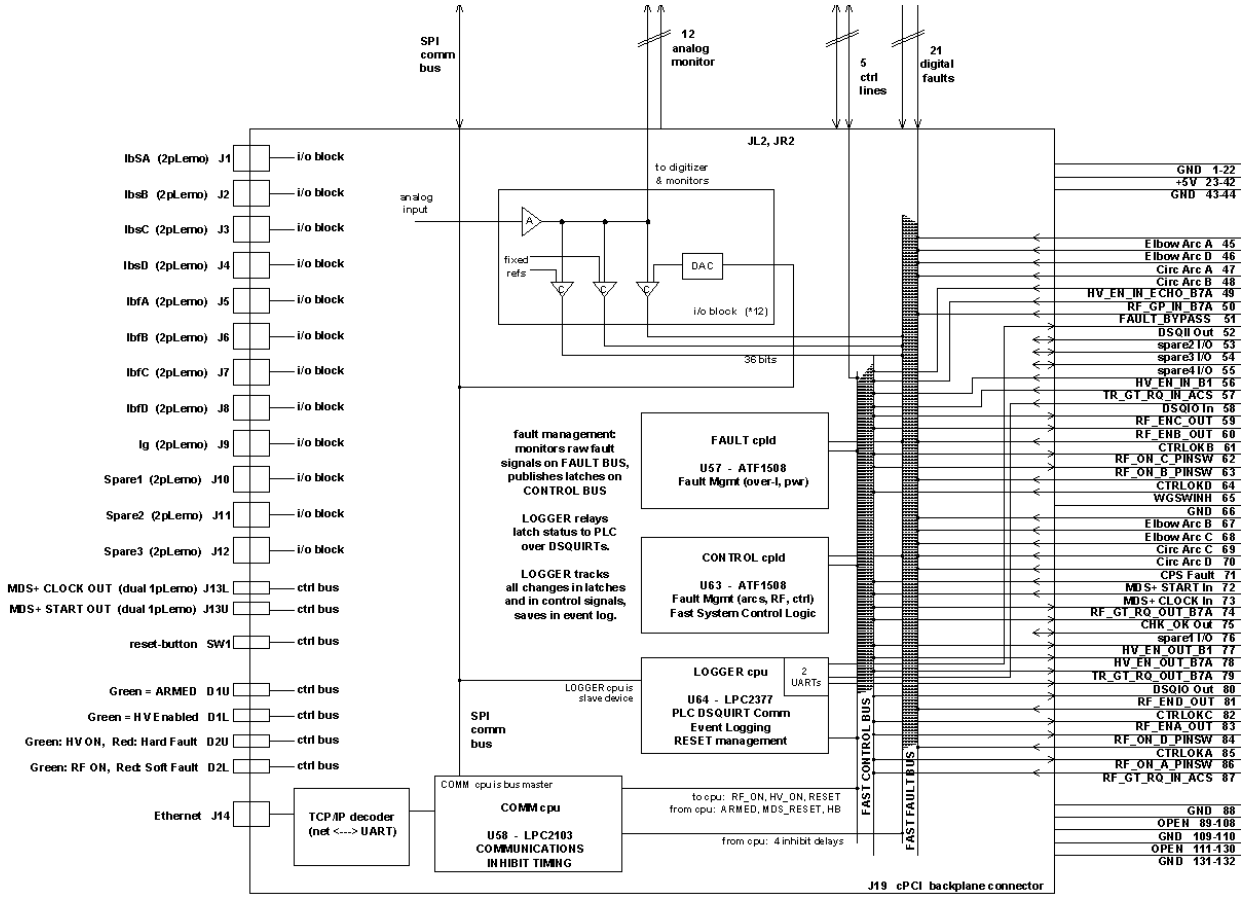

Figure 13. Expansion of main board from Figure 7. This board has 12 analog channels, plus the master/communications CPU, plus the Event Logger CPU. The Event Logger also serves as a dual DSQUIRT virtual transceiver for PLC communications.

This event logger is implemented on another dedicated ARM7 processor within the TPS on the main board (Figure 13). We have a 64 channel interface to the associated PLC, using two of the digital multiplexed DSQUIRT I/O units, and because so many of the fault bits and control signals are shared between the PLC I/O and the event logger, we perform both functions within this same ARM7. The high signal count requires that this be a very high pin-count chip – otherwise it is functionally very similar to the COTS cpu, sharing many architectural features.

Post-shot readout of the Event Logger allows comparison of complex fault-chains to compare to other tokamak activity, as well as to determine sequence of events (Figure 14).

2.1.3 ARM7 Programming

The coding of the ARM7 microprocessors was deemed to be highly sensitive and time-critical, and is thus not layered on an operating system or high-level language. All ARM7 coding is done in bare ARMASM, with full and absolute control over the microprocessor hardware. Interrupts are used for critical timing functions, and all chips are fully watchdogged against code errors which may hangup operation. In addition to conventional on-board

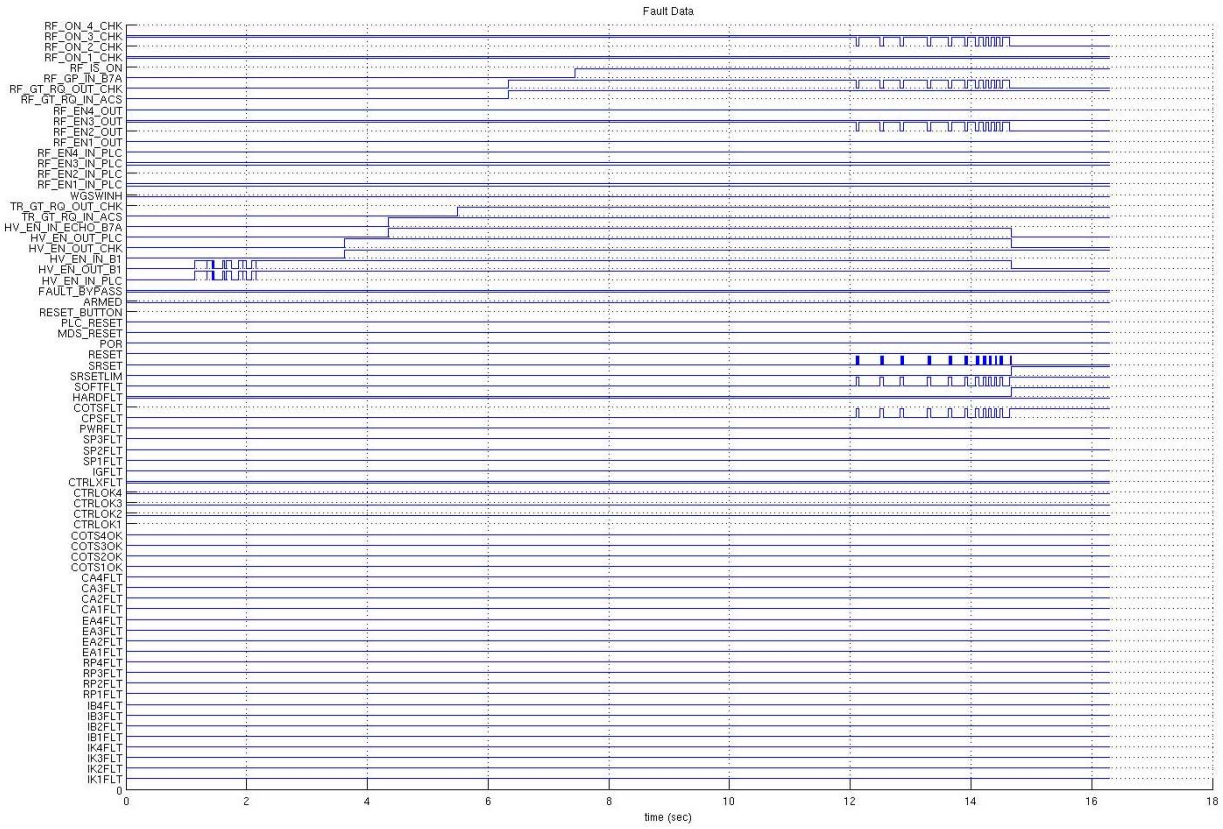

Figure 14. A readout of the Event Logger, post-shot, shows the time sequencing of all status and fault bits related to the TPS operation. The timebase is that used by the MDSplus data system. Events are defined as any change of any of the 96 bits – an event memory 2048 deep preserves a snapshot of all status/fault bits and a 32 bit timestamp on every event. (Readout plot provided by Atma Kanojia of the Alcator C-Mod team).

watchdogging of the cpus, we do an additional external "heartbeat" watchdog within the TPS system. This feature generates a 100Hz clock on one cpu, and passes it in turn through each of the other cpus and each of the programmable logic chips. In all cases, the "pass-through" is not interrupt driven, but is handled by polling at the highest level outer service loop – thus will fail at any hangup in the code. The output of the last stage is filtered, and two comparators detect if this filtered signal ever drifts off the middle towards either rail . The output of this fault-sense feeds a hardwired inhibit, the activation of which shuts down all HV and RF activity. Failure of any of the chips to service all features at the outermost service loop level thus results in a fail-safe shutdown of HV to protect equipment.

A third ARM7 microprocessor (on the main board) serves as a communications gateway from the TPS to the external Ethernet port. This processor is only "busy" with Ethernet between shots, and would otherwise be idle during shots. We thus keep it busy by assigning it the task of generating programmable inhibit delays, which we use to tune the sensitivity of the comparator faults with respect to leading and trailing edge of high voltage or RF commands.

While the COTS and MASTER cpus were demonstrated to operate with full functionality in default mode – running user code directly from onboard FLASH memory, we required more speed for the Event Logger. This program takes the additional step of copying itself from user

FLASH to SRAM on bootup, and transferring all operation (particularly interrupts) to run exclusively out of SRAM, resulting in about 3-4x speed improvement. The main loop, which services all polled functions, was redundantly programmed to repeatedly call the port polling function, keeping the latency to event detection down to ~1 μs.

2.1.4 Programmable Fault Logic

The internal architecture of the TPS breaks down into a conventional one used for modern radar controls. A network of programmable logic provides parallel and robust digital signal paths which ensure that HV and or RF are shut down promptly (sub-microsecond) in the event of a fault such as tube over-current or waveguide arc. At the same time, the use of programmable logic here allows for maximum flexibility and reprogrammability to accommodate specification changes.

This programmable digital fault logic is guided by a few state bits, which are indicative of the overall status of the system (i.e. idle, armed, debugging, etc). These state bits are set via slower, but higher level, controls, such as MDSplus commands or PLC commands. We thus have an interface which communicates with MDSplus, PLC logic, the ACS timing system, and the individual fault comparators and arc detection channels within the cart electronics, and performs the proper responses using all of the above as inputs as necessary. The TPS thus serves not just as its name implies (transmitter protection system), but also as a sequencer/interface for ross relays, HV supply turn-on, RF calibration/debugging, etc.

In Figure 15, we see a schematic representation of half of the programmable logic within the TPS CPLD array. This half is the crucial section for the above mentioned sequencing, and the logic shows the permissive structure which ensures that HV and RF are properly interlocked with all the safety and control features specified. (The other half of the programmable logic comprises a large repeating array of fault latches for many of the analog comparator channels – the net result being two fault bits which are treated as inputs to this page).

2.1.5 TPS Architecture Summary

The internal architecture thus consists of three interlocked ARM7 microprocessors, and a programmable logic array which is distributed between two Atmel CPLD array chips. The RTM contains 42 channels of Fiber-Optic I/O which feed directly to the logic array, and the front panel consists of 24 analog inputs for current transformers and RF diode inputs, 32 channels of analog monitor testpoints, and a port to directly connect 32 analog channels out to the dTACQ fast digitizer on a compact SCSI68 connector. The remainder of the front panel contains a few display LEDs, a manual reset pushbutton, F/O ports for the COTS analog mux links, and the Ethernet port.

A key additional task of this SBIR effort was to produce not just a specific solution for MIT's LH upgrade, but a general purpose transmitter control and protection system that could be easily installed for other applications – either in fusion, phased array radar, or other unanticipated needs. The design has discrete analog channels which are quite reconfigurable with respect to input termination, polarity, and initial gain, as well as to comparator filtering, thresholds, and logical dependence. The logical combination of fault signals is entirely contained within the programmable logic arrays, thus is easily reconfigurable for any foreseeable needs – and the

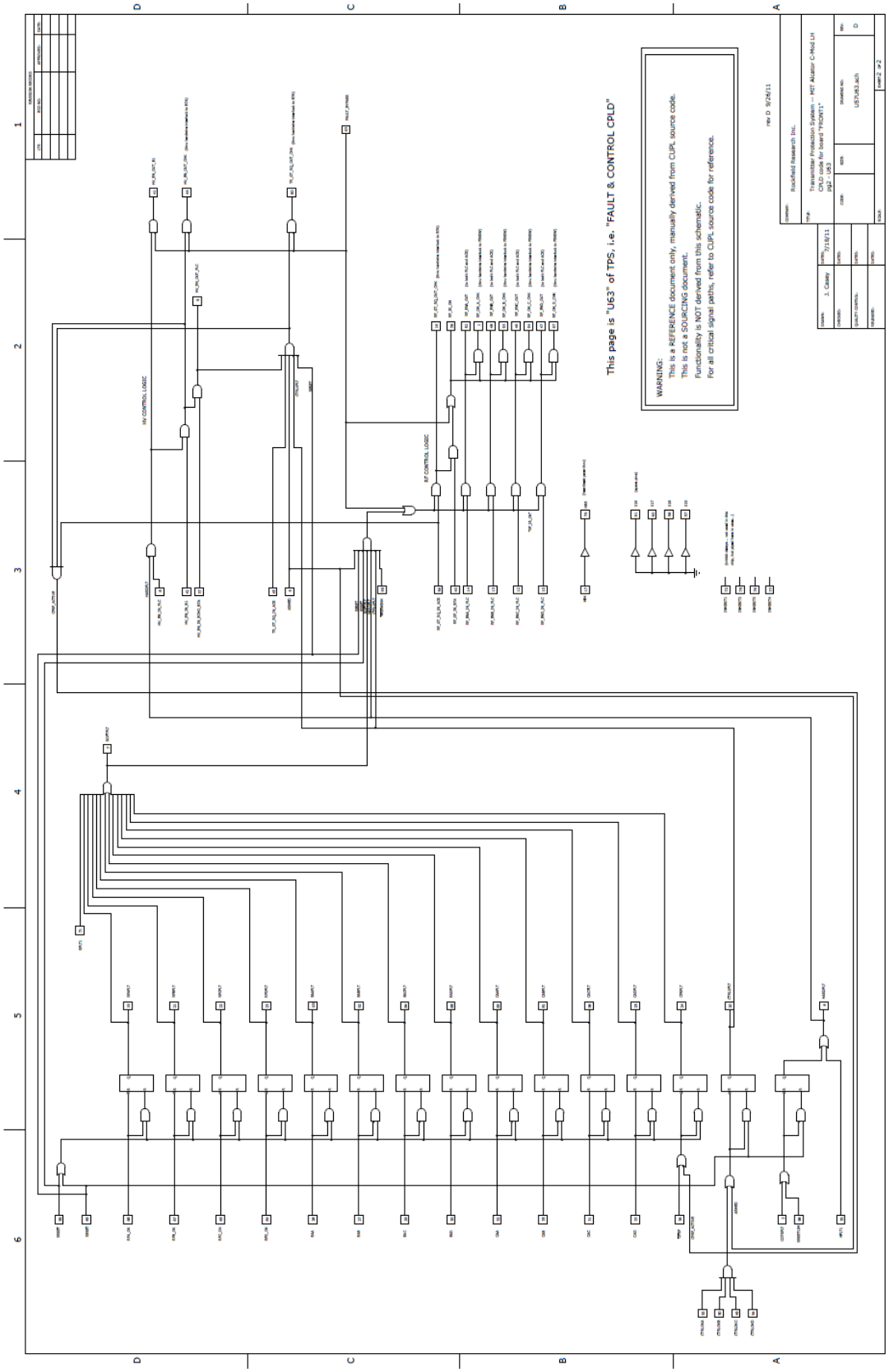

Figure 15. Half of the fault logic programmed into the CPLD array.

Figure 16. Five complete TPS front assemblies after testing and ready for shipment to MIT.

network resources within each of the programmable chips is considerably underutilized. Similarly, the possible uses of the onboard computational power are nearly limitless – they are quite interconnected, with spare pins allocated and unused for future expansion.

Essentially, we have designed a "kit" with a modular structure, containing a generous number of buffered analog inputs, fault comparators, and with all logical links reprogrammable for the application – easily adapted to nearly any fault-control use of similar scale.

Figure 17. One of the TPS assemblies, installed in cPCI crate and installed on the side of klystron cart on the Alcator C-Mod LH facility.

3.0 Review of Auxiliary Interface Components of TPS

Refer to Figure 2 for each of the following auxiliary interfaces and interconnect relations to the rest of the LH transmitter controls.

3.1 Box 1 – HV Control Box (Figure 18, Figure 19)

This interface resides within the high voltage restricted access area of the cart, and controls the action of the Ross Relays (which apply HV to the klystrons). In addition, a number of auxiliary services are performed: filament control, airflow sense, body current fault testing, Ross Relay positional sensing, cart panel safety switches, etc. This box is designed to be a key permissive element in the hardwired safety interlocks of the high voltage system.

The design for this closely emulated the functionality of the legacy controls for simplicity in

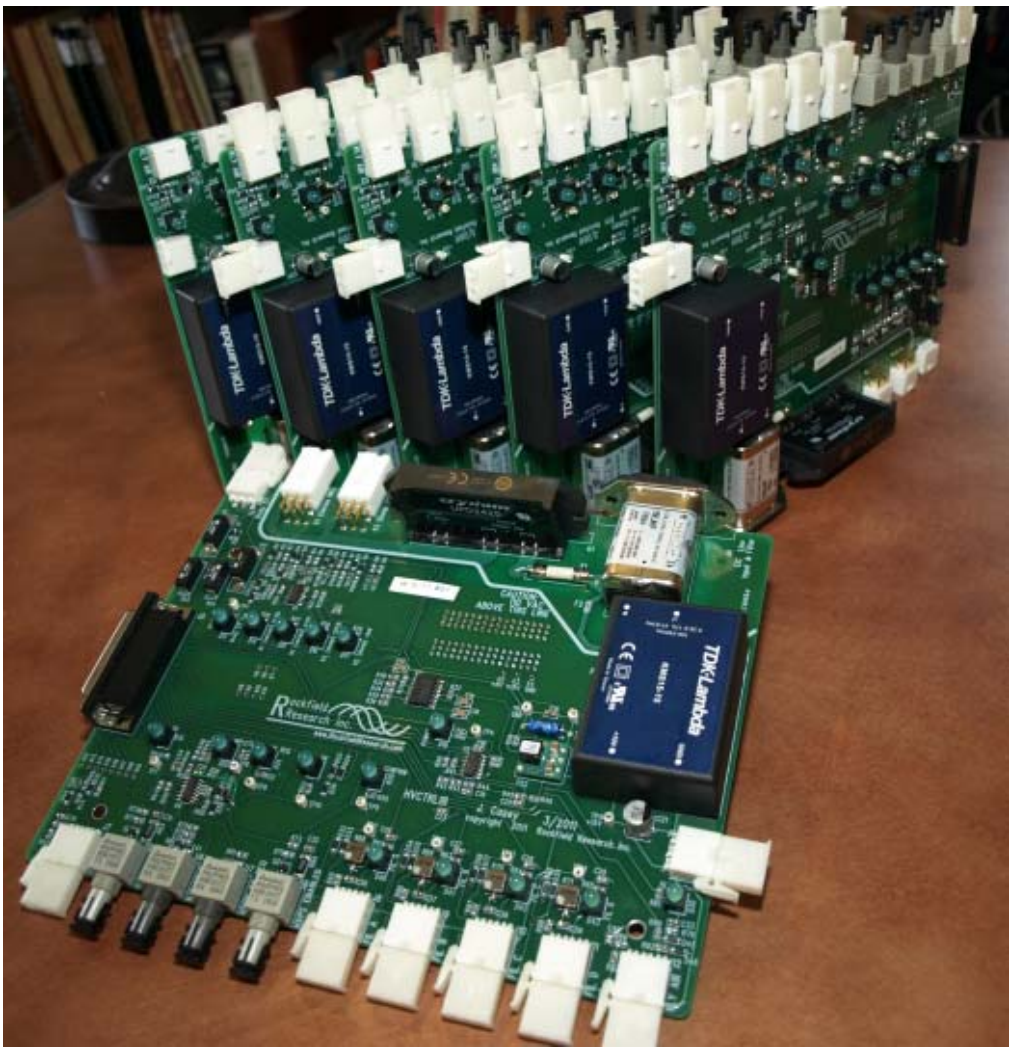

Figure 18. Six "box 1 HV control" units assembled and tested at Rockfield Research facility. Each of these boards interfaces to a DSQUIRT digital multiplexed fiber-optic I/O transceiver, and controls hardware in the HV area of the four-klystron cart.

wiring and interfacing. Cable runs external to the HV cart were largely eliminated by providing interface communications via fiber optics. Controls of the Ross Relays and filaments are managed by the PLC (under the responsibility of the MIT team), but the permissive reporting goes directly into the TPS as part of the interlock chain.

The block diagram specification and top-level design was performed by David Terry of the MIT team, and Rockfield Research did the detailed circuit design and all manufacturing, assembly, and testing under the supplementary Phase II program. One of these boxes is required for each cart, thus five were shipped to MIT (four carts plus one spare). One additional unit was retained at Rockfield Research for future support. The circuitry in each unit includes a DSQUIRT 16/16 channel bidirectional F/O transceiver, to provide non-galvanic connection to the PLC.

Figure 19. One of the "box 1 HV control" units is shown installed in the HV area of the cart, adjacent to the legacy filament power supplies, and underneath the klystron sockets.

3.2 Box 2 – Waveguide Switch Box (Figure 20)

This is a straightforward interface to operate the waveguide switches which alternate the klystron loading between the dummy load and the antenna. This box was the responsibility of the MIT team, although it did include one DSQUIRT 16/16 channel bidirectional F/O transceiver to connect to the PLC, which was provided by Rockfield Research under this effort.

Figure 20. Each cart has a "box 2 – Waveguide Switch Box", shown here installed in the C-Mod Cell. Opto-22 interface modules on the left, and a custom interface board at right interface to a DSQUIRT I/O board, mounted underneath at right.

3.3 Box 3 – Elbow Arc Detector Interface (Figure 21, Figure 22)

This is also a relatively simple interface box. Most of the functionality is to power and sense the waveguide arc detectors and echo the signals to the TPS over dedicated fibers for minimum fault response latency. Additional interfaces to solenoid water flow switches, and waveguide pressure transducers are provided here for convenience, due to the physical proximity to those sensor areas.

This box also powers and interfaces to the PIN diode switches, which gate the RF to the klystrons.

The sheer number and size of the connectors required a complex physical setup, even if the circuitry was quite simple. The Elbow

Figure 21. Each cart requires one "Box 3 Elbow Arc Detector Interface", which comprises two custom boards and two DSQUIRT fiber optic transceivers. The boards are physically constructed to 'wrap around" the DSQUIRTS to fit a stacked assembly in a compact box

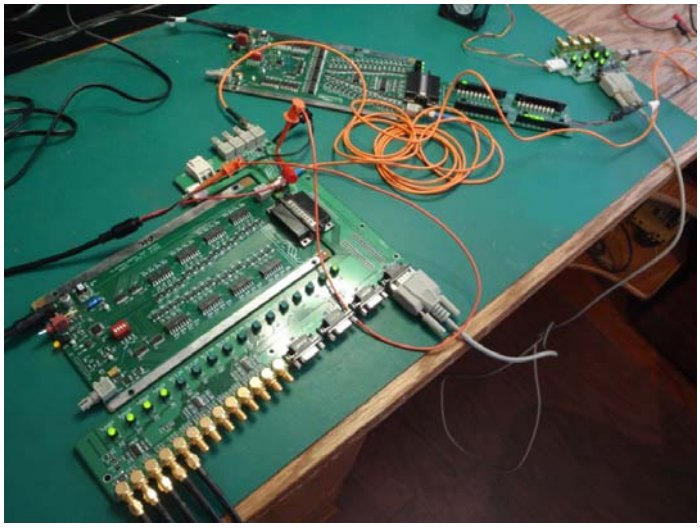

Figure 22. One of the Elbow Arc interface boards is shown on the testbench, plugged into its embedded DSQUIRT interface (above). One of the Elbow Arc units is shown mounted on the side of a cart, installed at MIT (right).

interface was built on two circuit boards which are stacked vertically to give two rows of detectors on opposite faces of a commercial enclosure. The boards are built to "wrap around" the embedded two DSQUIRT digital transceiver boards which link these controls to the PLC.

The LH system requires one Elbow interface for each cart, thus six were manufactured – four for install, one spare for MIT, and one to remain at Rockfield Research for support.

3.4 Box 4 – Analog Interface Box (COTS)

The water cooling system for the klystrons requires support of a number of transducers reporting water temperature, pressure and flow. In general, these report to the PLC for conventional analog logging and fault protection. For the upgrade TPS, we also report these signals directly to the TPS where they are used as inputs to the realtime collector overtemperature system. (Figure 23)

In Box 4, we power and interface these transducers, and bring the signals to a special version of the ASQUIRT 16 channel transceiver. This version omits the fiber-to-copper output section, but implements two parallel fiber outputs for a single 16 channel copper-to-fiber section. We also use the 0-

Figure 23. The analog interface box, Box 4, contains two ASQUIRT02 units to echo water cooling information to both PLC and TPS.

20mA option for the input scaling, so that the 4-20 mA analog outputs of the transducers interface easily to the ASQUIRT. The two output fibers separately feed the PLC and the TPS the same information on klystron cooling.

A separate additional ASQUIRT is used in each box for an additional number of RTD sensors that the newer CPI klystrons are outfitted with for improved diagnostics. These signals only feed to the PLC for monitoring and fault interlocking.

The Box 4 Analog Interface units – one per cart – were the responsibility of the MIT team. Each one used two ASQUIRT analog multiplexed transceivers, which were manufactured by Rockfield Research under this contract.

3.5 Box 5 – PIN Switch Diode Interface (Figure 24)

The klystrons are ultimately modulated via the input RF signal, which is gated via the PIN switches, mounted at the RF input coupler of the tube. These switches require DC power and a gating signal, which has been upgraded with the new TPS for galvanic isolation with a very simple fiber interface. The Box 5 PIN switch box performs these functions.

The fiber gating signal comes directly from the TPS for minimum latency, as the final end product of a long string of logic permissives and fault checks.

There is also an interface to the nearby Elbow Interface box, which supplies DC power, and reports back on power-ok and fan rotation status to the PLC via its embedded DSQUIRT interface.

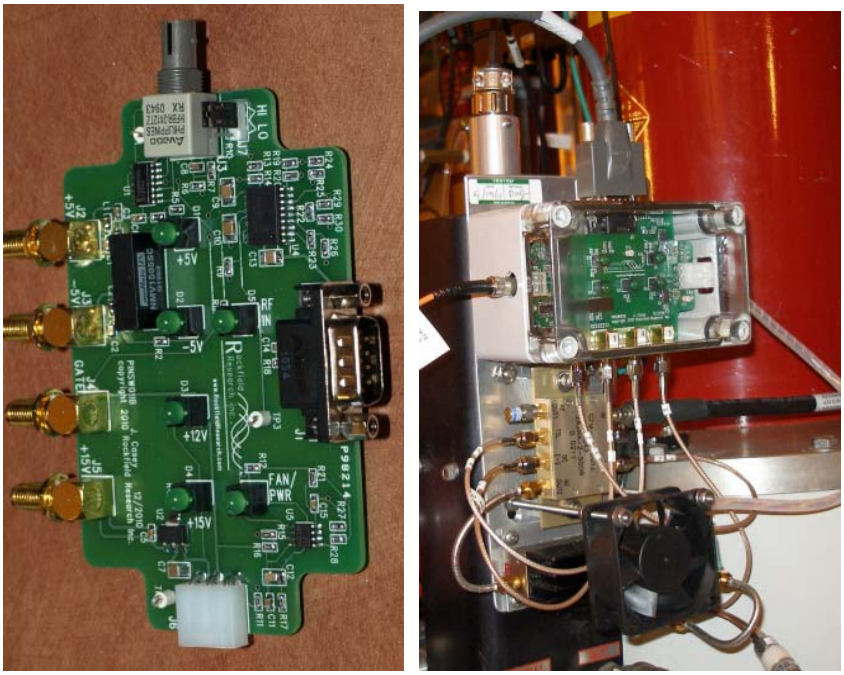

Figure 24. Box 5 is the interface to the PIN switch diodes – a very simple interface indeed. At left is the bare board, at right is the board installed in the protective case and mounted adjacent to the PIN Switch on the klystron body.

One PIN switch box is required for each klystron. Nineteen were thus built – sixteen for four carts fully populated with klystrons, two spares to MIT, and one spare remaining at Rockfield Research for support. These were manufactured and supplied by Rockfield Research under this program.

3.6 Boxes 6 & 8 – PLC Interface (Figure 25)

The "other end" of many of these isolated communications links are generally at either the PLC or the TPS central unit. While the TPS virtualizes the mating communications unit, the PLC does not and real physical mates are required to produce the proper signals on copper, which then route conventionally to the PLC for sensing.

Box 8 is a general interface holding six DSQUIRTs and two ASQUIRTs at the PLC. The fiber interfaces from these reach out to far flung remote sensing stations across noise and voltage barriers, isolating the signals and eliminating miles of cable in noisy and dangerous areas.

Each cart requires a fully populated Box 8. This was a group effort, with Rockfield Research providing the DSQUIRT and ASQUIRT units, and MIT housing them in a 19" rack mount frame, and wiring up the PLC cabling.

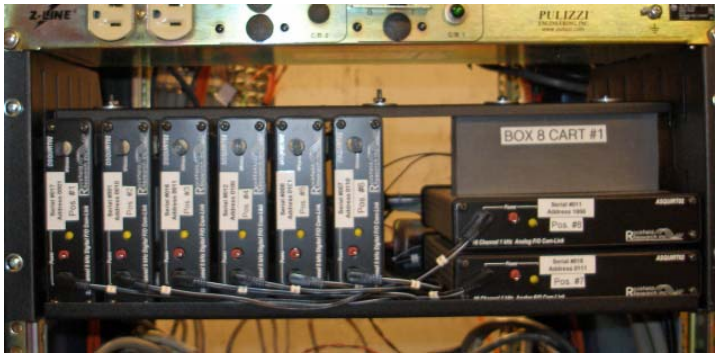

Figure 25. The Box 8 interface is primarily a rack mount housing for six DSQUIRT and two ASQUIRT modules.....

.....but with considerable wiring overhead, shown on the two trays between the Box 8 rack and the PLC.

Box 6 is a special case – a single higher bandwidth two channel multiplexed F/O transceiver, which monitors the Beam Voltage monitor point at the HV controls, as well as the total HV supply current. Both of these channels are pumped out over four parallel fibers, one to each TPS for use in COTS calculations.

Since there is only one Box 6 in the entire LH system it is added to the Box 8 assembly for Cart 3 only

3.7 Boxes 7

The nomenclature for Box 7 is somewhat confused, as it was broken into two separate interfaces during specification revisions. One of these is an interface to the pump controllers, and is relatively straightforward.

The other, Box 7A, is quite important. It is the control interface to the HV power supply, and it is also the "group control" for the suite of independent TPS controllers. We require that any RF fault on any one klystron immediately shutdown RF on all klystrons to prevent arcing on the antenna, and we also require that any hard fault which requires HV shutdown also immediately shut down the entire system. Box 7A gathers RF and HV "ok" signals from all TPS units and echos appropriate signals back to each of the TPS units – to confirm that group permission is given (or denied).

This box, by definition, must be reconfigurable to account for initial operation with the legacy 12 klystron system, but be easily upgraded to accommodate a 4th cart bringing the system to 16 klystrons at a later date. The TPS units have no such requirement – each controls 4 klystrons in an isolated universe.

Both the Box 7A and 7B assemblies were the responsibility of the MIT team.

3.8 Boxes 9, 10, 11

Boxes 9 and 10 do not exist, having been defined earlier in the specification, and later rolled into the previously described interfaces where convenient.

Box 11 is a small interface which includes the interlock keys and emergency stop button into the HV permissive chain associated with the HV controls (Box 1). It was the responsibility of the MIT team.

3.9 Two channel 10 kHz 12-bit Analog F/O Communication Link

In concept, this is a simple analog repeater – any signal presented at an input of one box is echoed at an output of the other box. Each box has two inputs and two outputs, making this a 2-channel bidirectional unit. The signals are transmitted over F/O link with 10 kHz update rates and 12 bit resolution. Shown in Figure 26, this was the first I/O unit designed.

Figure 26. The "ASQUIRT01" 2 channel 10 kHz analog F/O communications link, a sub-unit of the Alcator C-Mod TPS.

The link accommodates configurable options for 20mA input or 10V input, as well as an option for single-pin LEMO rather than 2-pin LEMO input and output connectors. Two have been delivered to MIT – one at the power supply/modulator monitor point, and one for spare/debug. (The complementary receiver for these

signals is virtual within the TPS).

Internally, the unit uses a 32-bit ARM micro-processor for both communication and internal logic, with UART interface to the F/O links, and local SPI interface to on-board digital-to-analog and analog-to-digital converters. The analog I/O sections use high-speed precision preamplifiers with 0.1% scaling resistors for absolute accuracy in signal reproduction at the far end of the link. The communications message includes an absolute tag for the starting byte of the message, a DIP-switch selectable address (to prevent activation if plugged into the wrong fiber), a code for the firmware revision, and a checksum for the entire message. Any failure (revision, address, broken fiber, broken wire, lost power at either end) results in a zero volt "safe" output. A watchdog reverts to "safe" if no signal is received over the fiber within a timeout period (a few msec). The unit is powered from a DC input – a commercial power "brick" with 6V output is supplied with the unit, but any DC voltage from 6V to 16V will serve – and installation at MIT will use the 15VDC local bus.

This unit is now a standalone product in the Rockfield Research offering, available as COTS for future program needs for the fusion community or elsewhere.
(See http://www.rockfieldresearch.com/products.html).

3.10 Sixteen channel 1 kHz 12-bit Analog F/O Communication Link

The 16-channel twin of the fast analog link (Figure 27) was designed using similar circuit fragments. A slower version of the ADC and DAC chips with onboard 8-channel multiplexers were used for data conversion, the analog front ends were similar, but micropower preamps were used at lower speed. The inputs are designed for a default of 0 to 20mA, with optional stuff for 0 to +10V.

The system overhead is nearly identical – the microprocessor is the same, and the firmware shares many features. The 1 kHz update rate is achieved by transmitting an entire message at 8 kHz, with all i.d. and checksum features and data from two channels. The 16 channels are thus updated in sequence for a net 1 kHz update rate per channel.

Five units were delivered to MIT (one per cart plus one spare). Late in 2009, a realization that we needed to echo pump station signals to *both* TPS and PLC required fabrication of a modified version – with dual F/O outputs, one way communication, and no analog output. Four of these were fabricated to reside at the pumphouse – the existing transceiver units will receive one output at the PLC, while the other output is received in a virtual unit in the TPS (and used for COTS calculations in the collector temperature interlock).

Figure 27. The "ASQUIRT02" 16 channel 1 kHz analog F/O communications link, a sub-unit of the Alcator C-Mod TPS.

This unit is also a standalone COTS product in the Rockfield Research offering, see above link.

3.11 Digital F/O Communication Link

Digital communication links were designed as close cousins of the analog units. The design settled on 32-channel multiplexed digital units in three varieties: 32 channel copper-to-fiber, 32 channel fiber-to-copper, and 16 channel (each way) bidirectional. The input and output sections were designed identically to Allen-Bradley PLC modules # 1771-IBN/B (10-30V high true input) and # 1771-OBN/B (10-30V high true output). 15V logic interfaces are used, and a number of these interface directly to mating PLC modules. This matching to the Allen-Bradley design extends to pin-for-pin compatibility on the I/O, output fusing, as well as the isolation circuitry of each group of eight channels within each module.

The modules operate with a 5 kHz update rate, although the actual signal risetime is a bit slower than this due to the implicit filtering of the PLC circuitry used. Addressing, communications algorithms, checksums, and safeties are all similar to those of the analog links. A "witness" fiber output is present on all modules (of all three varieties) for debugging and verifying signals without disconnecting existing fiber highways.

Six units are installed at the PLC station, packaged in a single 3U height rack-mount chassis adjacent to the PLC (along with the 16 channel analog receivers for pump station signals). Other remote units are in extruded boxes similar to the analog units, and many units will not have hardware counterparts, instead talking to counterparts "virtualized" within the TPS. The inventory of digital I/O units is quite large, reflecting the complexity of the TPS controls. For four carts, we have manufactured and delivered to MIT:

- 30 bidirectional units (7 per cart plus 2 spares)
- 6 copper-to-fiber units (1 per cart plus 2 spares)
- 10 fiber-to-copper units (2 per cart plus 2 spares)

Custom test fixturing was developed to aid in qualifying the large number of units, and a full set of this fixturing was delivered to MIT as well.

All three varieties of DSQUIRT02 units are now standard COTS products from Rockfield Research, available for future program needs for the fusion community or elsewhere. (See http://www.rockfieldresearch.com/products.html).

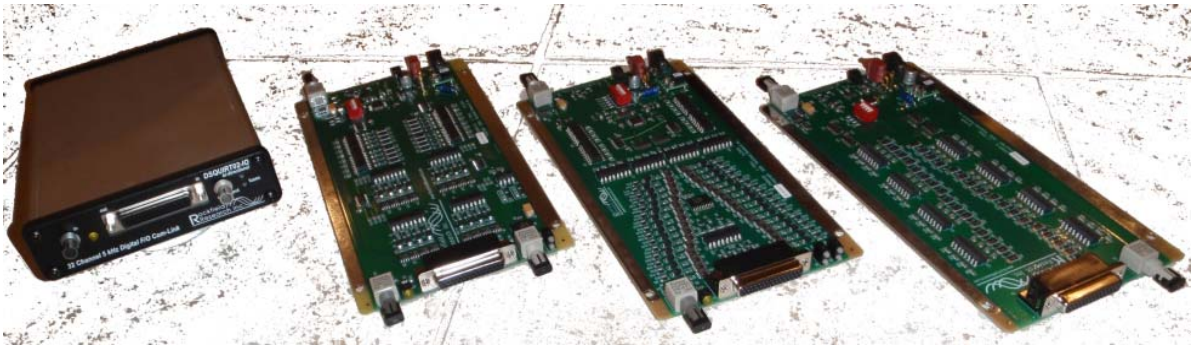

Figure 28. The DSQUIRT02 digital I/O modules come in three varieties. At left is an "IO" module – 16 channel bidirectional, and next to it is the assembled board for same. Center right is the "OO" module – 32 channel fiber to copper. Far right is the "II" module – 32 channel copper to fiber. Both "II" and "OO" modules assemble into boxes identical to the "IO" assembly shown.

Figure 29. The entire suite of DSQUIRT02 boards – II, OO, and IO varieties – are shown after testing. Some are installed in the extruded aluminum chassis for standalone installation, some remain bare boards for embedding within other assemblies.