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C. F. Lo[a], L. Liu[a], T. S. Kang[a], R. Davies[b], B. P. Gila[b], S. J. Pearton[b], I. I. Kravchenko[c], O. Laboutin[d], Y. Cao[d], W. J. Johnson[d], and F. Ren[a]

[a] Department of Chemical Engineering, University of Florida, Gainesville, Florida 32611, USA
[b] Department of Materials Science and Engineering, University of Florida, Gainesville, Florida 32611, USA
[c] Center for Nanophase Materials Sciences, Oak Ridge National Laboratory, Oak Ridge, Tennessee 37830, USA
[d] Kopin Corporation, Taunton, Massachusetts 02780, USA

The critical voltage for degradation of AlGaN/GaN high electron mobility transistors (HEMTs) employed with the Pt/Ti/Au gate metallization instead of the commonly used Ni/Au was significantly increased during the off-state stress. The typical critical voltage for HEMTs with Ni/Au gate metallization was around -60V. By sharp contrast, no critical voltage was observed for the HEMTs with Pt/Ti/Au gate metallization, even up to -100V, which was the instrumental limitation in this experiment. Both Schottky forward and reverse gate characteristics of the Ni/Au degraded once the gate voltage passed the critical voltage of around -60V. There was no degradation exhibited for the HEMTs with Pt-gated HEMTs.

Introduction

AlGaN/GaN high electron mobility transistors (HEMTs) show great promise for high power and high frequency operation [1,2] and for applications such as high frequency wireless base stations and broad-band links, commercial and military radar and satellite communications [3-5]. In recent reports, hot electron induced degradation has been observed in undoped AlGaN/GaN HEMTs on sapphire, SiC and Si substrate during DC and RF stresses [6-8]. Several degradation mechanisms that suppress device performance and reliability have been reported, ranging from hot-electron-induced trap generation to field-driven mechanisms [9-14]. Ni/Au metallization has been widely employed as the gate contact for AlGaN/GaN HEMT and consequently it has been used in most HEMT reliability studies to date.

Pt-based metal schemes have been used as p-Ohmic contacts on p-type GaAs to improve the reliability of AlGaAs/GaAs heterojuction bipolar transistors [15,16]. By alloying at low temperature, Pt diffused into GaAs and reacted with GaAs to form a thin $PtAs_2$ layer to achieve low contact resistance and excellent device stability. Pt-based metallization in the form of Pt/Ti/Pt/Au was also employed as the gate contacts for InGaP/GaAs, InAlAs/InGaAs [17,18], and AlGaAs/InGaAs HEMT to improve the device reliability, and an intentional annealing step at 250 to 350°C was used to sink the Pt into

the gate contact semiconductor layer to adjust the threshold voltage of the HEMTs [19]. This allowed both depletion and enhancement-mode mode HEMTs to be fabricated on the same wafer. Pt/Ti/Au metallizaton has also been used as the gate contacts on GaN and AlGaN. The thermal stability of Pt/Ti/Au was much higher as compared to Ni/Au gate contacts [20]. The thickness of the Ti layer in the Pt/Ti/Au played an important role in the resulting gate leakage current upon thermal stress [21].

In this work, we compared the critical voltages for off-state stress, Schottky gate forward and reverse current characteristics, as well as drain current-voltage (*I-V*) characteristics for HEMTs fabricated with the Ni/Au and Pt/Ti/Au gate metallization. X-ray photoelectron Spectroscopy (XPS) was used to examine the thermal stability of the Ni and Pt metal contacts deposited on GaN.

Device Fabrication

AlGaN/GaN HEMT heterostructures were grown on *c*-plane sapphire by metal–organic chemical vapor deposition (MOCVD). The epi-layers consisted of a 1 µm thick carbon doped GaN buffer layer followed by a 55-nm-thick undoped GaN channel layer, 21 nm of $Al_{0.25}Ga_{0.75}N$, and 2.2 nm GaN cap layer. The HEMT fabrication was started with Ohmic contact deposition by lift-off of e-beam deposited Ti/Al/Ni/Au multilayer followed by rapid thermal annealing (RTA) at 850°C for 30 s in a nitrogen environment. A typical contact resistance of 0.6 Ω-mm was measured using the transmission line method (TLM). For the device isolation, multiple doses and energies of nitrogen ion implantation were used to maintain a planar geometry in the fabricated device and reduce parasitic leakage current. Shipley Microposit STR-1045 positive photoresist was employed to protect the active region of the devices. Ni/Au (20 nm/80 nm) and Pt/Ti/Au (10 nm/20 nm/80 nm) based Schottky gate metallization was defined by optical lithography and followed with standard lift-off of the e-beam deposited metals. The gate dimension was 1 µm × 200 µm and the distances of gate-to-source (L_{gs}) and gate-to-drain (L_{gd}) were 1µm and 3 µm, respectively. The HEMTs were then passivated with plasma enhanced chemical vapor deposited 400 nm of SiNx at 300°C. The metal contact windows were opened with buffered HF solution. A schematic cross sectional view of the HEMT is shown in Figure 1.

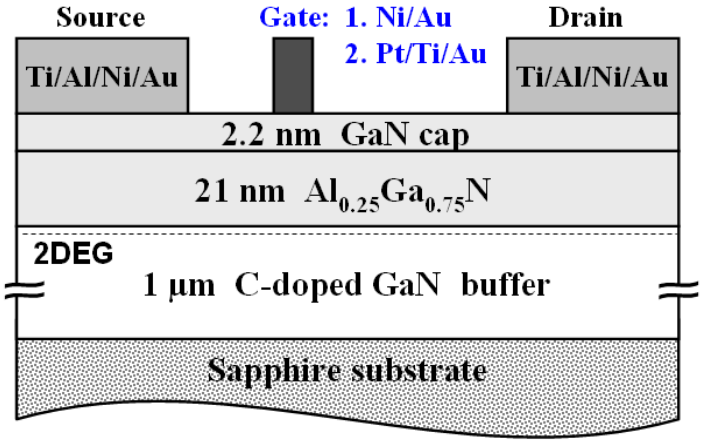

Figure 1. Schematic cross-sectional diagram of the AlGaN/GaN HEMT using Ni/Au or Pt/Ti/Au gate metallization.

Results and Discussion

15 separate HEMTs with Ni/Au or Pt/Ti/Au gate metallization were stressed for 60 seconds at each gate voltage step, while grounding the source electrode and maintaining +5 V on the drain. The off-state step-stresses were performed in the dark at room temperature using an HP 4156C semiconductor parameter analyzer and started from -10 V of the reverse gate voltage with -1 V of the voltage step up to -100 V. During the step-stress, besides monitoring I_g, gate-to-source leakage current, I_{gs}, and gate-to-drain leakage current, I_{gd}, were also measured. Between each step stress, the drain *I-V* characteristic, extrinsic transconductance, gate forward current biased from 0 to 1.5 V and gate reverse current biased from 0 to -5 V, source and drain resistance were all recorded with a Tektronix curve tracer 370A and an HP 4156 parameter analyzer. Self-heating effects were negligible based on the low drain-source currents under our test conditions, a fact supported by thermal simulations. The critical voltage of the off-state step stress was defined as the onset of I_g increase during the stress. The critical voltages of 15 Ni/Au gated HEMTs were varied from -45 to -65 V. As shown in Figure 2, the HEMTs with Ni/Au gate metallization exhibited a critical voltage around -60 V. The I_g suddenly increased and reached a compliance of 1 mA/mm, which was set to protect gate. It has been reported that once the gate voltage passed the critical voltage, a decrease of saturation drain current and increases of the source and drain resistance appeared [12]. Similar degradations were observed for the stressed Ni/Au gated HEMTs used here.

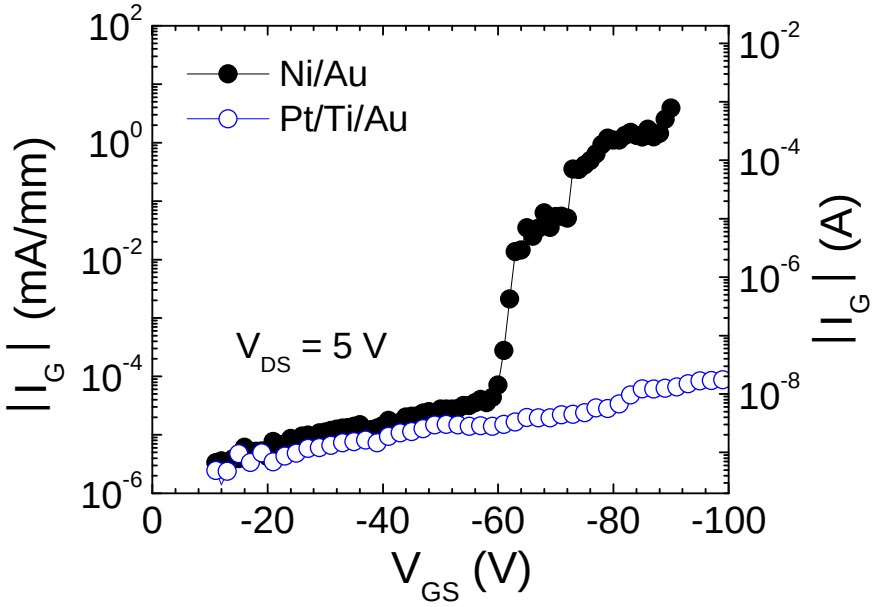

Figure 2. Off-state gate currents as a function of gate for the HEMTs fabricated with Ni/Au or Pt/Ti/Au gate metallization.

However, there was no critical voltage observed for the HEMT with the Pt/Ti/Au gate metallization up to -100 V, which was limited by the instrument used in this experiment. This suggested that the use of Pt based gate metallization could extend the operating bias conditions and improve the device reliability. The Schottky barrier height and ideality of the Pt/Ti/Au were 1.23 V and 1.21, respectively, which did not exhibit noticeable changes as a result of the bias stressing, as illustrated in Figure 3. On the contrary, the HEMTs with Ni/Au gate metallization showed significantly higher gate reverse bias leakage current and much lower breakdown voltage. The forward gate characteristics of

the Ni/Au gate contact appeared very leaky after the stress and the Schottky height reduced from 1.09 V to 0.66 V after stress. The lower Schottky barrier height of Ni due to the lower work function of Ni, as compared to Pt, resulted in almost an one order higher gate leakage current at the gate bias voltage, Vg, > -60 V. The excessive leakage current at the higher reverse biased Schottky gate contact was identified as a key indicator of poor device reliability.

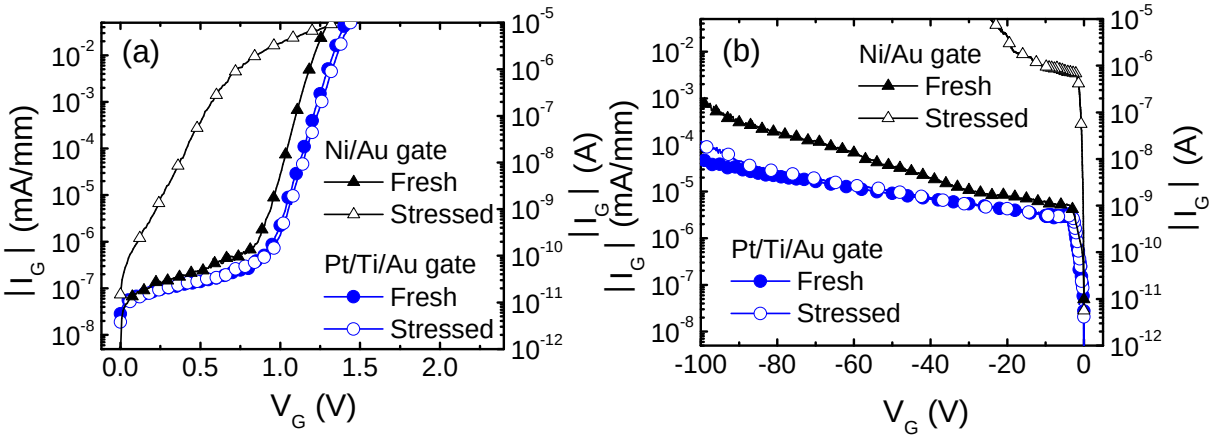

Figure 3. Forward (a) and reverse (b) Schottky gate characteristics before and after the off-state stress for the HEMTs fabricated with Ni/Au and Pt/Ti/Au gate metallization.

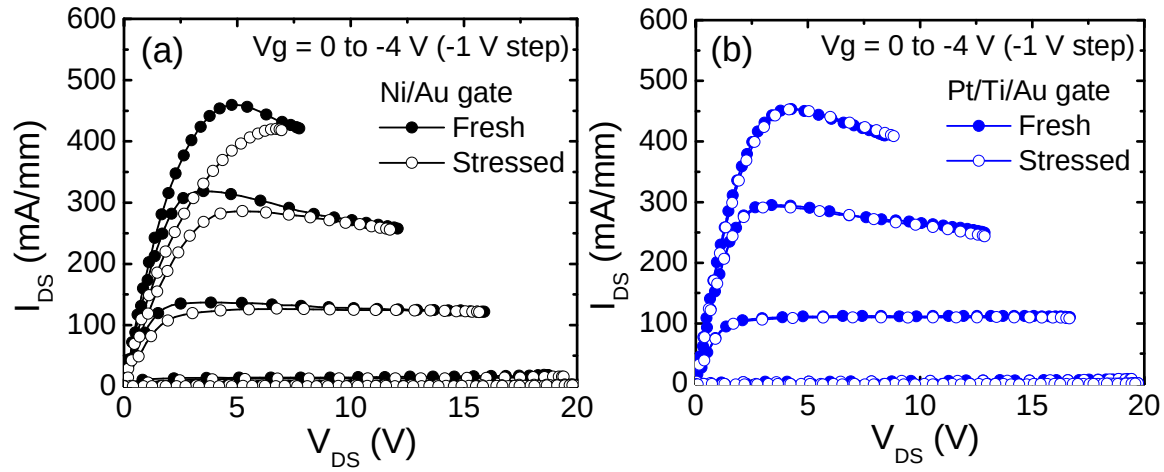

Figure 4. Drain IV characteristics of HEMTs before and after the off-state stress for the HEMTs fabricated with Ni/Au (a) and Pt/Ti/Au (b) gate metallization.

Besides the gate *I-V* characteristics, the drain *I-V* of Pt/Ti/Au gated HEMTs also exhibited a minimal change after the stress (less than 2% change) as compared to around 22% decrease of the saturation drain current for the Ni/Au gated HEMTs as shown in Figure 4, due to the increase of source resistance and drain resistance after the reverse gate voltage passed the critical voltage [12]. The threshold voltage of the Pt-gate HEMTs was around -2.3 to -2.4 V, which slightly shifted to the positive side as compared to -2.7 to -2.8 V for the Ni-gated HEMT, due higher Schottky barrier height of the Pt-gated HEMTs. There was no changes of the threshold voltage were observed for the Pt-gated HEMTs. However, the threshold voltage of the Ni-gated HEMTs shifted to -2.4 V. This positive threshold voltage shift of the Ni-gate after stress was attributed to gate metal interacted with the nitride, which was reported by several groups [22,23]. These results

were consistent with the gate *I-V* and off-state stress data that the reliability of the HEMTs was improved by using Pt/Ti/Au gate metallization.

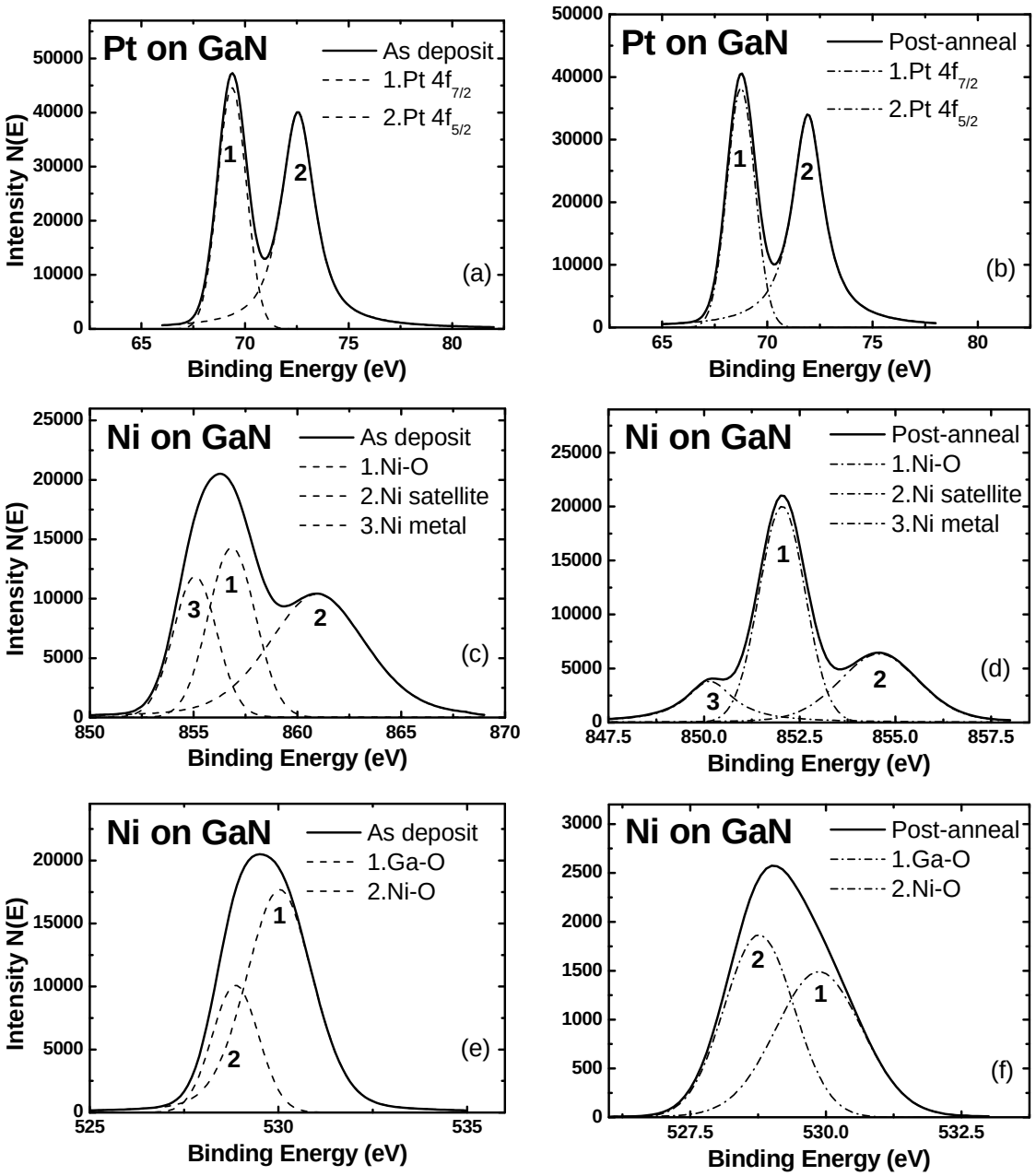

Figure 5. XPS spectra of (a) Pt 4f XPS spectra for as deposit Pt/GaN sample. (b) Pt 4f XPS spectra for the Pt/GaN sample annealed at 300°C for 30 mins. (c) Ni 2p XPS spectra for as deposit Ni/GaN sample. (d) Ni 2p XPS spectra for the Ni/GaN sample annealed at 300°C for 30 mins. (e) O 1s XPS spectra for as deposit Ni/GaN sample. (f) O 1s XPS spectra for the Ni/GaN sample annealed at 300°C for 30 mins.

For As- based HEMTs and HBTs, Pt based metallization is usually annealed at 250-350°C for 30 seconds to improve the gate contact stability and this process was also used to shift the threshold voltage of the HEMT for fabricating enhancement mode devices, as mentioned previously [17-19]. The Pt/Ti/Au gate contacts were heated up at 300°C for 60 mins during the silicon nitride deposition for the reliable device passivation [24,25]. In order to study the interaction between the Pt and GaN after 300°C annealing, special

XPS samples with 1 nm Ni and Pt deposited on 3 μm GaN were prepared. The metal films were intentionally kept thin so the metal/GaN interface could be studied in XPS. Prior to the metal deposition, the GaN samples were rinsed in 1:1 HCl:H_2O solution for 3 minutes, exposed to UV ozone for 25 minutes, dipped in buffered HF for 5 minutes and rinsed in de-ionized water. After the metal deposition, XPS was then used to examine the thermal stability between the as-deposited samples and the annealed samples. The in-situ annealing was performed in vacuum chamber (1×10^{-9} Torr) at 300°C for 30 minutes. The XPS system employed an Mg anode for the x-ray source; take off angle was kept at 45° for all measurements, and the pass energy was 35.75 eV.

As shown in Figure 5 (a) and (b), the spectra of Pt 4f XPS spectra for the as deposit Pt/GaN sample and post annealed sample, there were no changes observed in the spectra. This result confirmed the off-state stress results that the Pt/Ti/Au gate contacts were stable after electrical and thermal stress; no observable chemical reaction at the interface had taken place. By contrast, as shown in Figure 5 (c) and (d), by comparing the pre and post anneal spectra, the Ni-oxide peak increased and the Ni metal peak decreased significantly. The discrepancy of the Ni-O peak position for the as deposit and annealed samples was due to charging effect. These results indicated the Ni oxidized during the anneal in the vacuum chamber. By observing the O 1s peak, as shown in Figure 5 (e) and (f), and its changes between pre and post anneal, it was determined that the O-Ga bonding portion decreased and the O-Ni bonding portion increased. This led to the conclusion that the Ni film stripped oxygen from the native oxidized GaN surface and created a layer of NiO. The reaction between the Ni and native oxide could also happen during the on-state stress reported by Singhal et al. [26]. The Ni-O formation was just one the indications for the device degradation. It has been reported that the defects generated under the gate metal and pit formation along the gate edge close to the drain contact side [27]. All these defects would affect the gate leakage current, drain current and the efficiency of the gate to modulate the channel.

Conclusions

We have demonstrated significant improvement of nitride HEMT stability by using Pt-based gate metallization to replace the conventional Ni/Au contact. The off-state critical voltage was increased from -60 V to over -100 V. Minimal changes of gate and drain *I-V* characteristics were observed for the HEMTs with Pt gate metallization. The mechanisms for the dramatic change in critical voltage were established from combined electrical and chemical measurements.

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References

1. Y. F. Wu, A. Saxler, M. Moore, R. P. Smith, S. Sheppard, P. M. Chavarkar, T. Wisleder, U. K. Mishra, and P. Parikh, *IEEE Electron Device Lett.*, **25**, 117 (2004).

2. H. F. Sun, A. R. Alt, H. Benedickter and C. R. Bolognesi, *Electronics Letters*, **45**, 376 (2009).
3. N. X. Nguyen, M. Micovic, W.-S. Wong, P. Hashimoto, L.-M. McCray, P. Janke, and C. Nguyen, *Electronics Letters*, **36**, 468 (2000).
4. S. J. Pearton, J. C. Zolper. R. J. Shul, and F. Ren, *J. Appl. Phys.*, **86**, 1 (1999).
5. J. W. Johnson, A. G. Baca, R. D. Briggs, R. J. Shul, C. Monier, F. Ren, S. J. Pearton, A. M. Dabiran, A. M. Wowchack, C. J. Polley, and P. P. Chow, *Solid-State Electron.*, **45**, 1979 (2001).
6. H. Kim, V. Tilak, B. M. Green, H. Cha, J. A. Smart, J. R. Shealy, and L. F. Eastman, *Proceedings of IRPS 2001, International Reliability Physics Symposium*, 214 (2001).
7. H. Kim, V. Tilak, B. M. Green, J. A. Smart, W. J. Schaff, J. R. Shealy, and L. F. Eastman, *Phys. Status Solidi A*, **188**, 203 (2001).
8. D. Pavlidis, P. Valizadeh, and S. H. Hsu, *Proceedings of The European Gallium Arsenide and Other Compound Semiconductors Application Symposium 2005, European Microwave Association*, 265 (2005).
9. J. Joh and J. A. del Alamo, *Tech. Dig. - Int. Electron Devices Meet.*, 1 (2006).
10. J. Joh, L. Xia, and J. A. del Alamo, *Tech. Dig. - Int. Electron Devices Meet.*, 385 (2007).
11. G. Meneghesso, G. Verzellesi, F. Danesin, F. Rampazzo, F. Zanon, A. Tazzoli, M. Meneghini, and E. Zanoni, *IEEE Trans. Device. Mater. Reliab.*, **8**, 332 (2008).
12. J. Joh and J. A. del Alamo, *IEEE Electron Device Lett.*, **29**, 287 (2008).
13. J. A. del Alamo and J. Joh, Microelectronics Reliability, 49, 1200-1206 (2009).
14. S. Demirtas, J. Joh, and J. A. del Alamo, *Microelectronics Reliability*, **50**, 758 (2010).
15. E. F. Chor, R. J . Malik, R. A. Hamm, and R. Ryan, *IEEE Electron Device Lett.*, **17**, 62 (1996).
16. H. Okada, S.-I. Shikata, and H. Hayshi, *Jpn. J. Appl. Phys.*, **30**, L558 (1990).
17. J. R. Lothian, F. Ren, J. M. Kuo, J. S. Weiner, and Y. K. Chen, *Solid-State Electronics*, **41**, 673 (1997).
18. M. Dammann, A. Leuther, F. Benkhelifa, T. Feltgen, and W. Jantz, *Phys. Status Solidi A*, **195**, 81 (2003).
19. K. J. Chen, T. Enoki, K. Maezawa, K. Arai, and M. Yamamoto, *IEEE Trans. Electron Devices*, **43**, 252 (1996).
20. E. Monroy, F. Calle, R. Ranchal, T. Palacios, M. Verdú, F. J. Sánchez, M. T. Montojo, M. Eickhoff, F. Omnès, Z. Bougrioua, and I. Moerman, *Semiconductor Science and Technology*, **17**, L47 (2002).
21. J. Pedrós, R. Cuerdo, R. Lossy, N. Chaturvedi, J. Würfl, and F. Calle, *Phys. Status Solidi C*, **3**, 1709 (2006).
22. J. Kuzmik, D. Pogany, E. Gornik, P. Javorka, and P. Kordos, *Solid-State Electronics*, **48**, 271 (2004).
23. M. Ťapajna, U. K. Mishra, and M. Kuball, Appl. Phys. Lett., 97, 023503 (2010).
24. C. F. Lo, T. S. Kang, L. Liu, C. Y. Chang, S. J. Pearton, I. I. Kravchenko, O. Laboutin, J. W. Johnson, and F. Ren, *Appl. Phys. Lett.*, **97**, 262116 (2010).
25. C. F. Lo, T. S. Kang, L. Liu, F. Ren, S. J. Pearton, J. Kim, S. Jang, O. Laboutin, Y. Cao, and J. W. Johnson, *J. Vac. Sci. Technol. B*, **29**, 031211 (2011).
26. S. Singhal, J. C. Roberts, P. Rajagopal, T. Li, A. W. Hanson, R. Therrien, J. W. Johnson, I. C. Kizilyalli, K. J. Linthicum, *Proceedings of IRPS 2006, IEEE International Reliability Physics Symposium*, 95 (2006).

27. C.-Y. Chang, E. A. Douglas, J. Kim, L. Lu, C.-F. Lo, B.-H. Chu, D. J. Cheney, B. P. Gila, F. Ren, G. D. Via, D. A. Cullen, L. Zhou, D. J. Smith, S. Jang, and S. J. Pearton, *IEEE Trans. Electron. Mater. Reliab.*, **11**, 187 (2011).