Fabrication and Characterization of Self-Aligned InAlAs/InGaAsSb/InGaAs Double Heterojunction Bipolar Transistors

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Fabrication and Characterization of Self-aligned InAlAs/InGaAsSb/InGaAs Double Heterojunction Bipolar Transistors

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A trilevel resist system was employed to fabricate self-aligned, submicron emitter finger $In_{0.52}Al_{0.48}As/In_{0.42}Ga_{0.58}As_{0.77}Sb_{0.23}/In_{0.53}Ga_{0.47}As$ double heterojunction bipolar transistors (DHBTs). Selective wet-etchants were used to define the emitter fingers and to form an InGaAs guard-ring around the emitter fingers. Due to the low energy bandgap of the InGaAsSb base layer and type II base-collector junction, a low turn-on voltage of 0.38 V at 1 A/cm^2 and a high dc current gain of 123.8 for a DHBT with a 0.65×8.65 μm^2 emitter area were obtained. A unity gain cut-off frequency (f_T) of 260 GHz and a maximum oscillation frequency (f_{max}) of 485 GHz at J_C = 302 kA/cm^2 were achieved.

Introduction

Quaternary InGaAsSb based double heterojunction bipolar transistors (DHBTs) have attracted a great deal of attention because of their high speed and ultra low turn-on voltage compared to that of the conventional InAlAs/$In_{0.53}Ga_{0.47}As$ single heterojunction bipolar transistors [1-5]. These characteristics are due to their smaller base band gap and favorable type-I emitter-base (E-B) junction and type-II base-collector (B-C) junction. The higher valence band offset at the type-I $In_{0.52}Al_{0.48}As/In_{0.42}Ga_{0.58}As_{0.77}Sb_{0.23}$ E/B junction prevents the injection of holes from the base to the $In_{0.52}Al_{0.48}As$ emitter, leading to higher electron injection efficiency. Furthermore, the type-II staggered band alignment of the $In_{0.42}Ga_{0.58}As_{0.77}Sb_{0.23}/In_{0.53}Ga_{0.47}As$ (B/C) junction increases the current operation capability due to the postponed Kirk effect. Excellent dc performance of DHBTs with strained InGaAsSb as the base layer has been demonstrated [5]. To achieve even higher speed operation on InGaAsSb DHBTs, it is essential not only to decrease the carrier transit time through the base and collector layers through the structure design and wafer growth quality, but also to reduce both the emitter size and the parasitic resistance and capacitance through the layout design and device fabrication, simultaneously. Therefore, it is desirable to create submicron emitter fingers with a high resolution trilevel resist system and minimize the base resistance and capacitance by employing self-aligned processing for the device features.

In this paper, we report processing steps for self-aligned submicron-emitter finger InAlAs/InGaAsSb/InGaAs DHBTs and the resulting dc and rf performance of the devices. The submicron emitter formation with a trilevel stack using Polymethyl methacrylate (PMMA), germanium, and polydimethylglutarimide (PMGI) is described in detail. The characteristics of the selective wet-etchants for defining emitter and base mesa are illustrated for the reduction of parasitic resistance and capacitance. Guard-ring and ledge techniques were also employed to preserve the current gain at small emitter dimensions and passivate the sidewall of the emitter mesa for eliminating surface recombination. Finally, dc characteristics and small signal rf performance of 0.65×8.65 μm^2 emitter finger DHBT's are reported.

Material Growth

The layer structure of the InAlAs/InGaAsSb/InGaAs DHBT is listed in Table I. The epi-layers were grown on Fe-doped semi-insulating (100) InP substrates with a Riber 32P solid-source molecular beam epitaxy (MBE) system equipped with arsenic, phosphorus, and antimony valved cracker cells. Silicon and beryllium were the n-type and p-type dopants, respectively. The Sb_2 and As_4 flux were set to a beam equivalent pressure (B.E.P.) of 1.4×10^{-7} torr and 8.0×10^{-6} torr to control the antimony and arsenic composition, respectively. The DHBT layer structure consisted of a 300 nm n-type $In_{0.53}Ga_{0.47}As$ subcollector doped to 2×10^{19} cm^{-3}, a 150 nm n-type $In_{0.53}Ga_{0.47}As$ collector doped to 1×10^{16} cm^{-3}, a 44 nm p-type $In_xGa_{1-x}As_{1-y}Sb_y$ based layer doped with Be to 6×10^{19} cm^{-3}, a 40 nm n-type $In_{0.52}Al_{0.48}As$ emitter doped to 8×10^{17} cm^{-3}, a 5 nm n-type InAlAs doped to 8×10^{18} cm^{-3}, a 30 nm n-type $In_{0.53}Ga_{0.47}As$ emitter cap doped to 2×10^{19} cm^{-3}, and a 4 nm n-type InAs emitter cap doped to 8×10^{19} cm^{-3}. The substrate temperature was 490ºC throughout the entire growth except for the base layer. The junction characteristics showed that the dopants were well confined. During the growth of the base layer, the substrate temperature was decreased to 450ºC to prevent beryllium out–diffusion and antimony phase separation.

TABLE I. Epitaxial layer structure parameters of fabricated InAlAs/InGaAsSb/InGaAs DHBTs.

Layer	Material	Carrier concentration (cm^{-3})	Thickness (nm)	Dopant
Emitter Cap	n^+–InAs	8×10^{19}	4	Si
E.C. graded	n^+–$In_{0.53}Ga_{0.47}As \rightarrow InAs$	$2 \sim 8\times10^{19}$	16	Si
Emitter cap	n^+–$In_{0.53}Ga_{0.47}As$	2×10^{19}	30	Si
E.C. graded	n^+–InAlGaAs	8×10^{18}	25	Si
Emitter cap	n^+–$In_{0.52}Al_{0.48}As$	8×10^{18}	5	Si
Emitter	n–$In_{0.52}Al_{0.48}As$	8×10^{17}	40	Si
Base	p–$In_{0.42}Ga_{0.58}As_{0.77}Sb_{0.23}$	6×10^{19}	44	Be
Collector	n^-–$In_{0.53}Ga_{0.47}As$	1×10^{16}	150	Si
Subcollector	n^+–$In_{0.53}Ga_{0.47}As$	2×10^{19}	300	Si
Semi-insulating InP substrate				

Device Fabrication

The schematic cross-sectional view of a triple mesa $In_{0.52}Al_{0.48}As$/ $In_{0.42}Ga_{0.58}As_{0.77}Sb_{0.23}$/ $In_{0.53}Ga_{0.47}As$ DHBT and epitaxial layer structure are illustrated in

Figure 1. The process flow of the InAlAs/InGaAsSb/InGaAs DHBT fabrication is illustrated in Figure 2. The DHBT fabrication started with emitter contact metal deposition via the photoresist-assisted metal lift-off instead of the etch-back process used in the Si-based device fabrication [6]. This was mainly due to the complicated multi-metal contacts used for III-V materials and to avoid possible chemical reactions between the metals and the etchant used in the etch-back processes.

In order to achieve an almost 1:1 aspect ratio of emitter metal contacts, a trilayer resist system [7-10], Polymethyl methacrylate/Germanium/polydimethyl glutarimide (PMMA/Ge/PMGI), was employed to realize 0.62 μm tall emitter metal fingers with a dimension of 1 μm × 9 μm. The layer thicknesses of the trilayer system were 320 nm, 5 nm and 2.5 μm for PMMA, Ge and PMGI, respectively. The Ge layer was e-beam deposited on the PMGI and a spinner was used to coat the PMMA and PMGI on the samples. The PMMA was used to precisely define the emitter dimensions with a Raith-150 e-beam writing system; however, the PMMA was too thin to be used for lifting-off the 600 nm thick metal stack. The Ge layer not only served as a pattern transfer layer, but also alleviated the charging effect during the e-beam writing. The 2.5 μm thick PMGI layer was employed for lifting-off thicker emitter metal stacks.

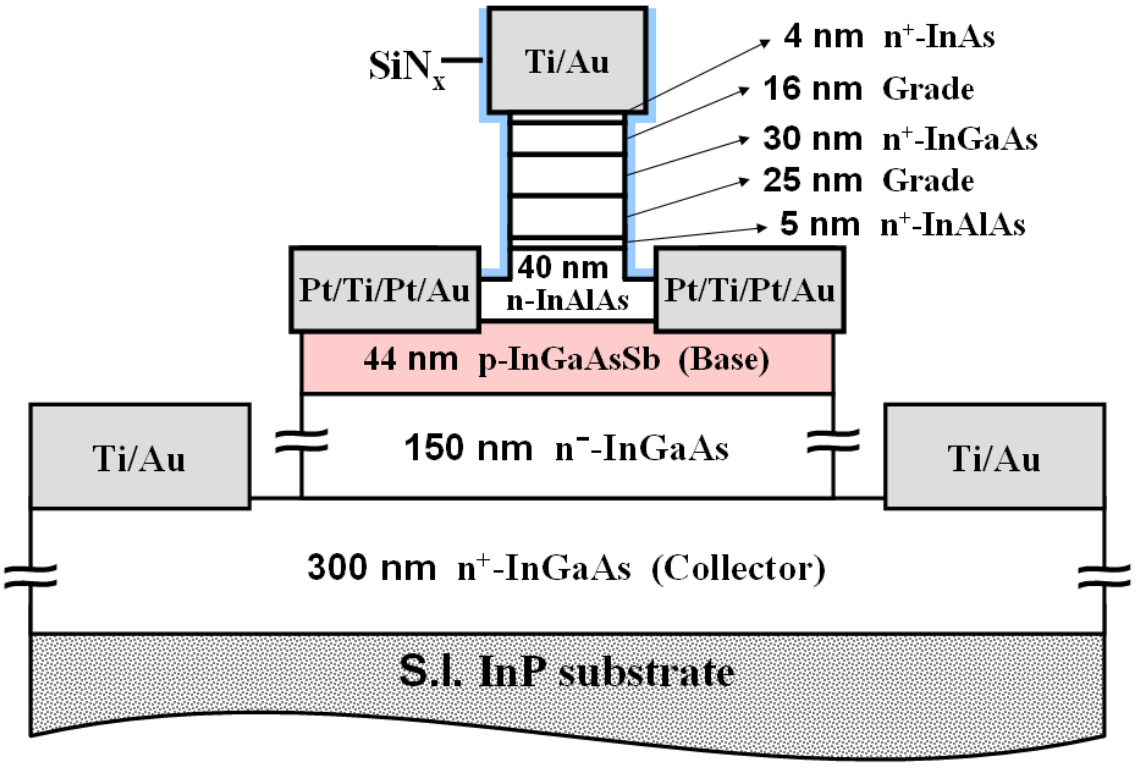

Figure 1. Schematic cross-sectional view of double mesa $In_{0.52}Al_{0.48}As$/ $In_{0.42}Ga_{0.58}As_{0.77}Sb_{0.23}$/ $In_{0.53}Ga_{0.47}As$ DHBT.

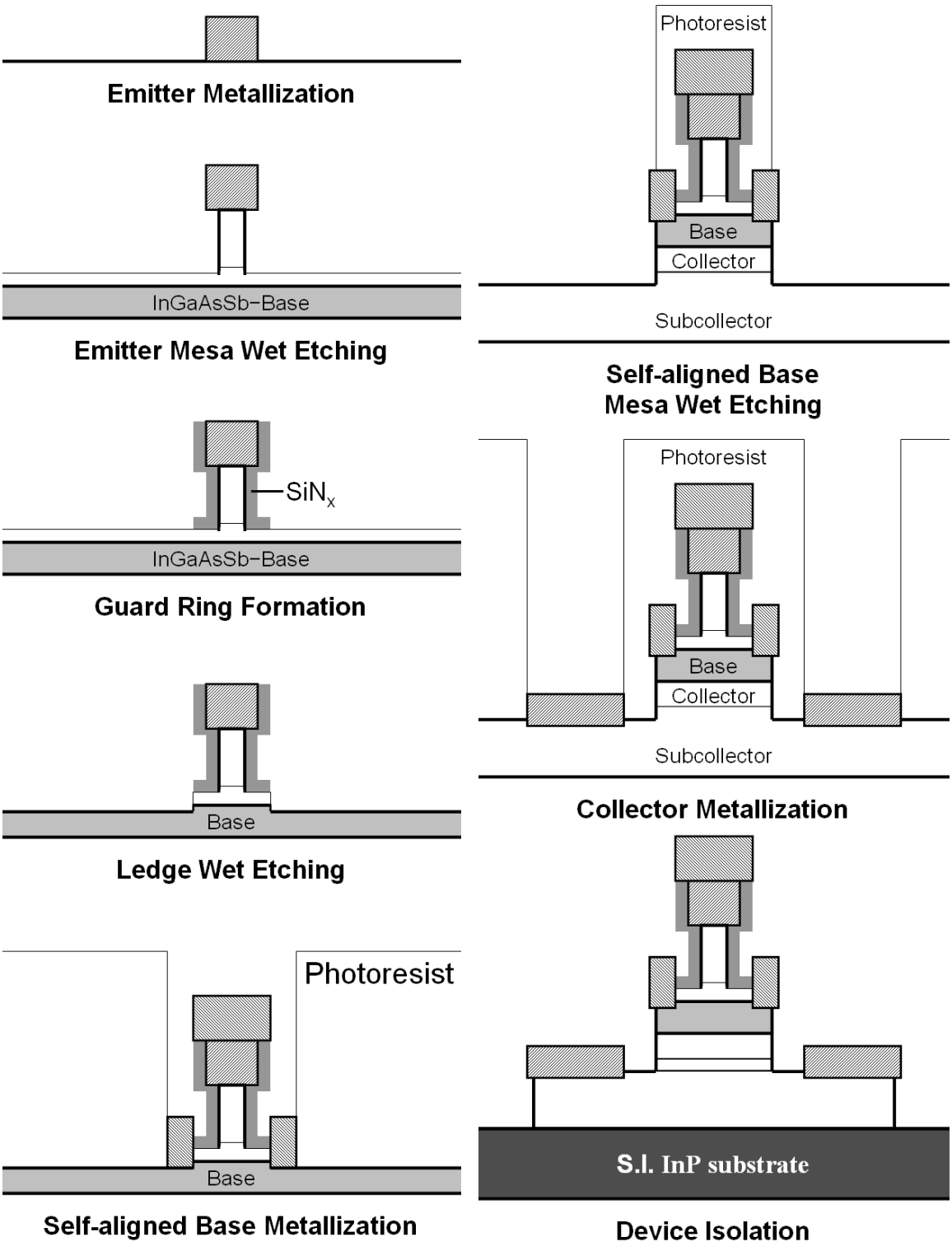

Figure 2. Schematic of process sequence of $In_{0.52}Al_{0.48}As$/ $In_{0.42}Ga_{0.58}As_{0.77}Sb_{0.23}$/ $In_{0.53}Ga_{0.47}As$ DHBT.

After the submicron emitter finger patterns been defined on the PMMA with the conventional e-beam lithograph, the emitter finger pattern transfer was achieved by using CF_4 plasma to etch through Ge layer at the emitter finger patterns opened on the PMMA

layer and the etch stopped on PMGI. To transfer the emitter finger patterns into the PMGI layer, an O_2 plasma was used to etch 2.3 μm of the 2.5 μm PMGI used in the trilayer system and the rest of the PMGI was removed with MF-321 developer. By using the wet-chemical method to finish up the PMGI removal, it prevented the ion bombardment damage of the emitter cap layer during the oxygen plasma etching and created an undercut of ~175 nm in the PMGI to assist the metal lift off. Figure 3 (a) shows a scanning electron microscope (SEM) picture of a test pattern created on the tri-layer system after the oxygen plasma etch, with about 200 nm of PMGI left on the surface. A rough bottom surface of the etched PMGI was observed due to the ion bombardment. Figure 3 (b) shows the SEM picture after the majority of PMGI had been removed by the MF-321 developer and an undercut on the sidewall of the PMGI was accomplished. There were some PMGI residues left along the edge of the openings, which were cleaned off with an UV ozone treatment, as illustrated in Figure 3(c). With the assistance of the trilayer system, 20 nm/600 nm of Ti/Au based emitter stacks were lifted-off. Figure 4 (a) and (b) illustrate the SEM pictures of the trilayer system after the emitter metal deposition and the lift-off emitter metal stack. A specific emitter contact resistivity of 4.6×10^{-6} ohm-cm^2 was obtained using transmission line measurements (TLMs).

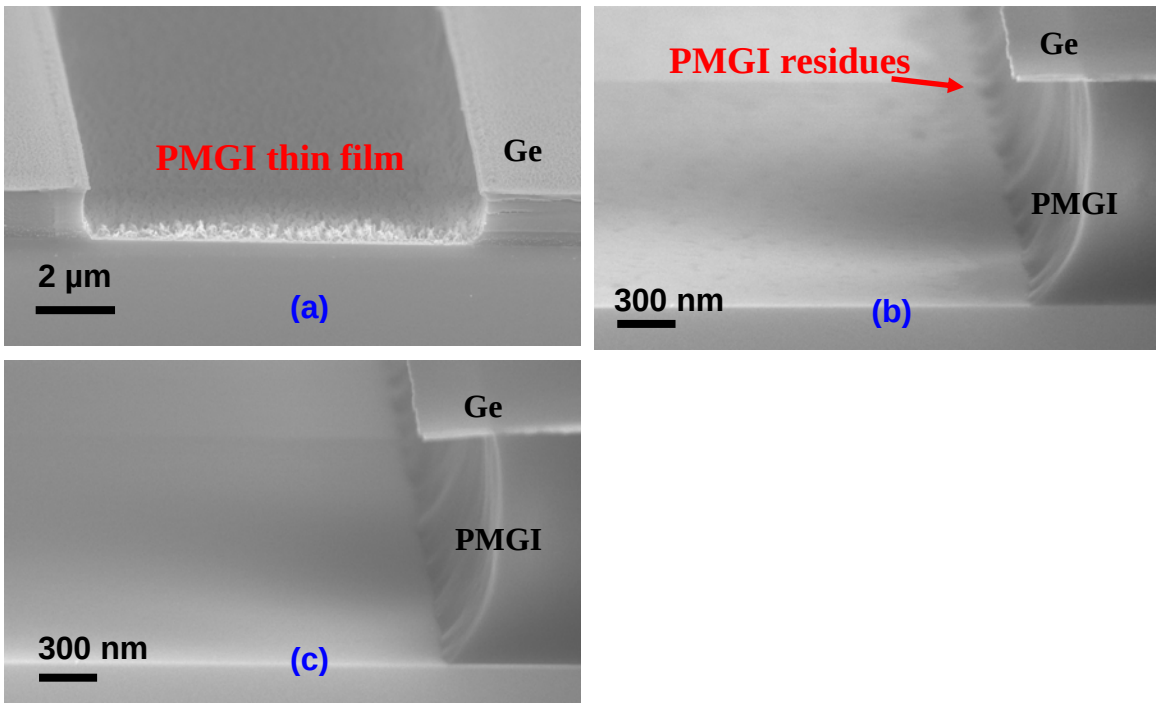

Figure 3. SEM micrographs of trilevel resist structure (a) after CF_4/O_2 RIE, (b) after soaking in developer, and (c) after UV-ozone treament.

With the emitter metal contacts in place, wet chemical etchants were used to form the emitter mesas. First, a citric acid/H_2O_2 solution was employed to selectively etch off the InAs as well as the InGaAs layer, and the selectivity of etching rate for InAs and InGaAs over the graded InAlGaAs beneath the InGaAs layer was 25 : 1. Then, $H_3PO_4/H_2O_2/H_2O$ was used to etch 25 nm off of the 45 nm InAlAs layer by timing. Since, the InAlAs etch rate was slow, 1.5 nm/sec, the etching depth could be controlled with the

$H_3PO_4/H_2O_2/H_2O$ solution. The reminding ~20 nm InAlAs was preserved for fabricating a guard ring around the emitter finger.

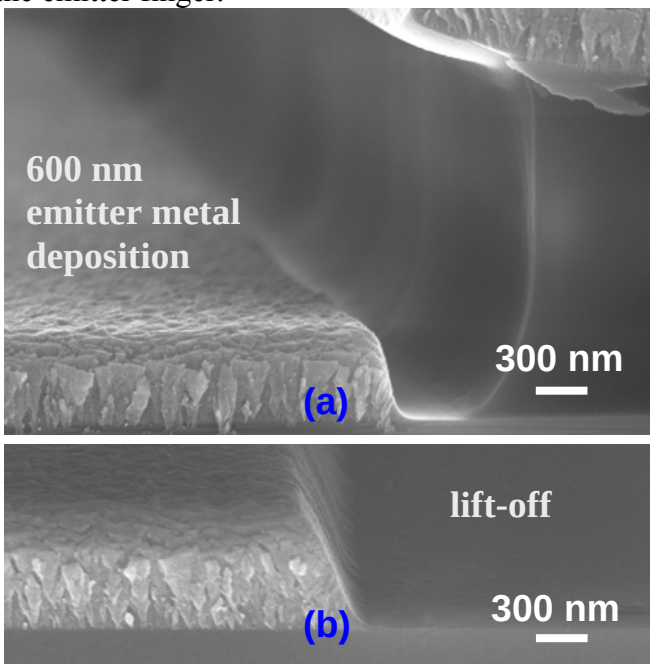

Figure 4. SEM micrographs of (a) as-deposited emitter metal and (b) emitter metal after lift-off process.

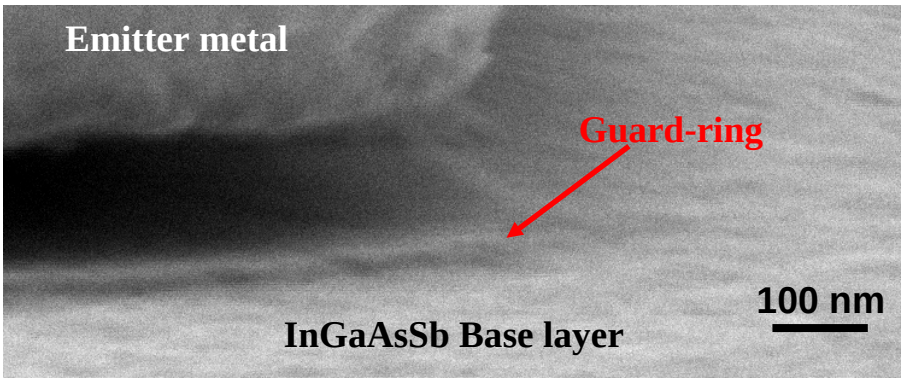

Figure 5. SEM micrograph of fabricated guard-ring structure.

The guard ring formation was achieved with a self-aligned plasma enhanced chemical vapor deposition (PECVD) SiNx etch-back process. During the wet chemical mesa etching, an ~170 nm undercut of the emitter mesa was produced below the emitter metal. Wafers with an InAlAs emitter layer of 170 nm were loaded into a Plasma-Therm plasma-enhanced chemical vapor deposition (PECVD) system for 100 nm SiNx deposition [11,12]. The SiN_x provided conformable coverage over the emitter contact, sidewall of the emitter mesa and the top of the un-etched InAlAs layer. Then, CF_4 plasma etching was used to etch-back the SiNx and expose the thin 20 nm InAlAs layer as well as the emitter metal. The SiN_x layer on the sidewall of the emitter mesa was protected by the overhang emitter metal and was not etched. This SiN_x layer not only prohibited the subsequent wet chemical etching of the emitter mesa-sidewall, but also protected a narrow area of the InAlAs layer around the emitter finger periphery. This narrow InAlAs acted as the guard-ring of the emitter, suppressing the electron surface

recombination and increasing the current gain of the DHBT. An HCl/H_2O solution was used to selectively etch the rest of the InAlAs layer and stop on the Sb-base layer, as shown in Figure 5. The etch rate of the InAlAs was 10 nm/sec and the etch selectivity for InAlAs over InGaAsSb was over 2000.

Pt/Ti/Pt/Au metallization was employed for the base metal contact using emitter metal as the mask and self-aligned deposited on the base layer. A specific contact resistivity of 3.7×10^{-7} ohm-cm^2 was achieved. $H_3PO_4 : H_2O_2 : H_2O$ was used again for the base mesa definition and both InAlAsSb layer and InGaAs collector were etched off to expose the InGaAs sub-collector layer. Ti/Au metallization was utilized for the collector metal and specific contact resistivity of 5.6×10^{-6} ohm-cm^2 was obtained. The layout of the DHBT is illustrated in Figure 6. The base electrode was self-aligned to the emitter finger. The double collector electrode was designed to reduce collector resistance. Device isolation was achieved with $H_3PO_4/H_2O_2/H_2O$ to etch off the InGaAs collector layer and stop on the InP substrate. An 1 μm wide metal bridge was formed to isolate the device active region and base contact pad to reduce the base-collector capacitance. Figure 7 (a) and (b) show the SEM picture of the triple mesa DHBT and a SEM picture of the enlarged metal air-bridge of the DHBT.

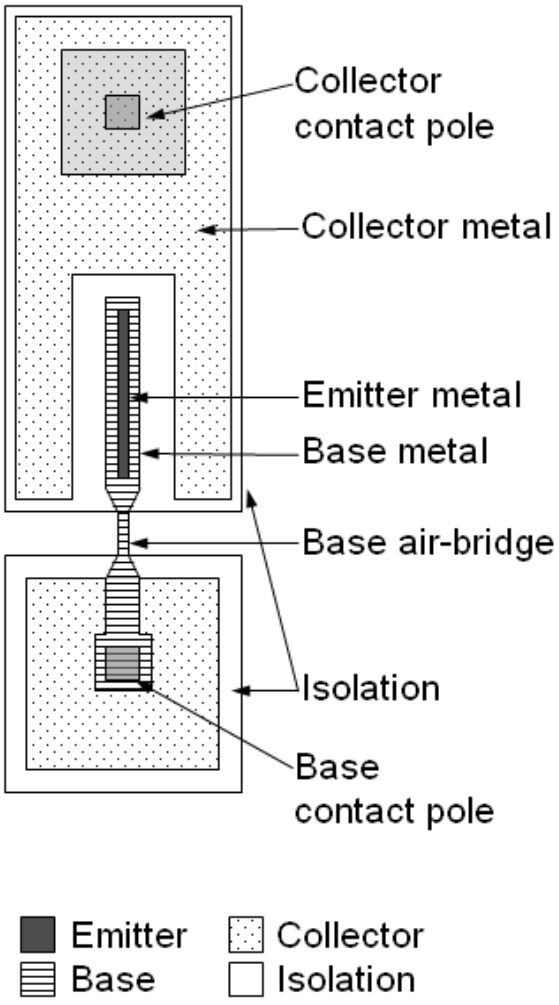

Figure 6. The device layout of an unit cell.

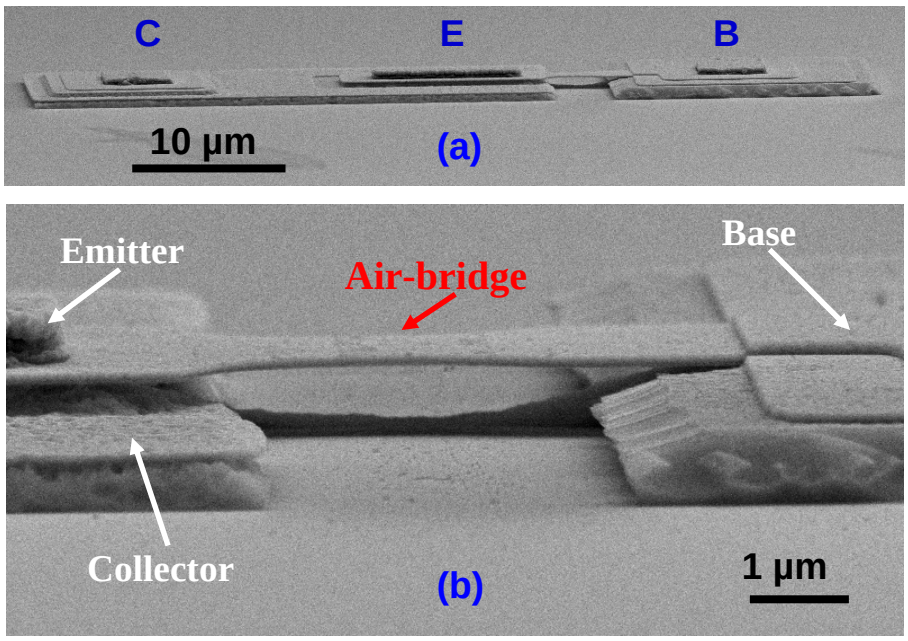

Figure 7. SEM micrograph of 0.65 × 8.65 μm^2 device prior to BCB planarization: (a) SEM micrograph of the DHBT with 1 μm air-bridge after isolation etch and (b) enlarged view of the base metal bridge.

Benzocylcobutene (BCB) was used as the planarization layer for the triple mesa DHBTs and as the insulator between individual DHBTs. The BCB coating was thermally cured in a tube furnace at 250ºC for 6 min. To expose the emitter fingers, base and collector contact pads, a BCB etch back process was performed using CF_4/O_2 based plasma and Ti/Au metallization was utilized for the interconnect metals for emitter, base, and collector electrodes, as illustrated in Figure 8.

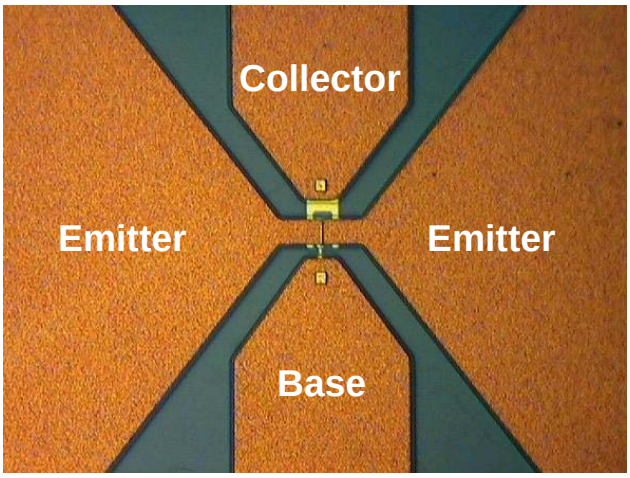

Figure 8. Top view optical microscope image for a fabricated device after Ti/Au interconnect metal deposition.

Device DC and RF Characteristics

Room-temperature Gummel plot and common-emitter current gains of the $In_{0.42}Ga_{0.58}As_{0.77}Sb_{0.23}$ DHBT are shown in Figure 9 (a). The ideality factors of emitter –

base junction and base-collector junction were $\eta_C = 1.28$ and $\eta_B = 1.41$, respectively. The low value of η_B confirmed the improvement achieved with the replacement of the type-II E/B junction by the type-I E/B junction, which helped to alleviate the electron pileup and reduced the tunneling recombination current. The turn-on voltage was reduced to as low as 0.38 V at a collector current density of 1 A/cm^2, as compared to the turn-on voltage of 0.505 V and ~0.45 V for the conventional InP/InGaAs SHBT and DHBTs at the same current density [3,13,14]. The challenge for reducing turn-on voltage was not to decrease the current gain. Due to the large valence band discontinuity at the emitter-base junction, the current gain was >50 at a collector current density of 35 kA/cm^2 and a maximum dc current gain of 123.8 at a collector current density of 364.73 kA/cm^2. Common-emitter collector current voltage (*I-V*) characteristics are shown in Figure 9 (b). The collector offset was 0.25 V and a common-emitter breakdown voltage of 2.6 V was achieved at a collector current density of 1 kA/cm^2.

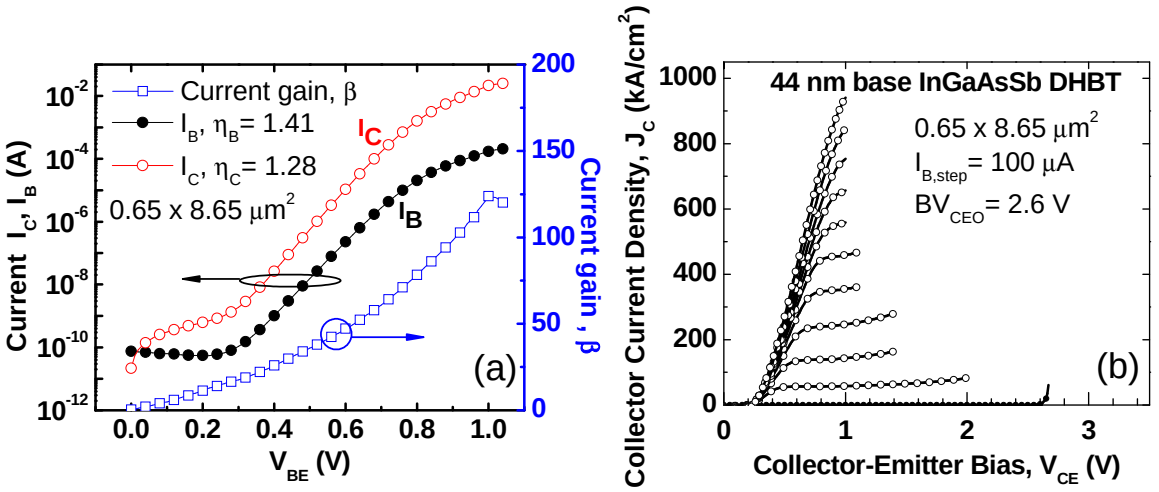

Figure 9. (a) Gummel plot and current gain β and (b) Common-emitter characteristics of the $In_{0.52}Al_{0.48}As$/ $In_{0.42}Ga_{0.58}As_{0.77}Sb_{0.23}$/ $In_{0.53}Ga_{0.47}As$ DHBT.

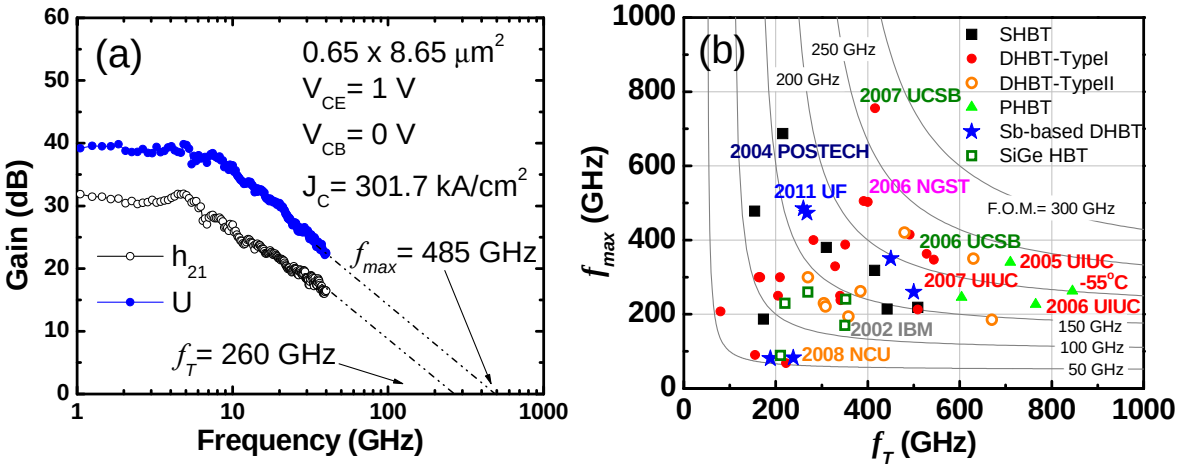

Figure 10. (a) Current gian h_{21} and Mason's unilateral gain U rf extrapolations of 0.65 × 8.65 μm^2 DHBT; (b) Overview of f_T and f_{max} data for high-speed InP- and SiGe-based HBTs. The figure-of merit (F.O.M) was defined as $f_T \times f_{max} / (f_T + f_{max})$.

The on-wafer *s*-parameters of the devices between 50 MHz and 40 GHz were measured using an HP8722C network analyzer. Both the unity gain cut-off frequency f_T and maximum oscillation frequency f_{max} were determined by the −20 dB/decade extrapolation from the common–emitter current gain h_{21} and Mason's unilateral power gain U curves, respectively. As shown in Figure 10 (a), the DHBT with an effective emitter area of 0.65×8.65 μm^2 showed f_T and f_{max} of 260 and 485 GHz, respectively, at a collector current density of 302 kA/cm^2. Figure 10 (b) compares the f_T and f_{max} of our InGaAsSb DHBTs with those taken from literatures [1-5, 13-26]. The DHBT with 0.65×8.65 μm^2 emitter area has delivered a comparable performance among InP-base HBTs.

Conclusions

High-speed $In_{0.52}Al_{0.48}As/In_{0.42}Ga_{0.58}As_{0.77}Sb_{0.23}/In_{0.53}Ga_{0.47}As$ DHBTs have been fabricated employing a trilevel resist system for the submicron emitter finger definition and using self-aligned processing to narrow the electrode separation and minimize parasitic resistances and capacitances. Guard-rings and ledges were formed to preserve the current gain at small emitter dimension for improving dc and rf performance. DHBTs with InGaAsSb base have been experimentally investigated to show a low turn-on voltage and high dc current gain. A peak f_T of 268 GHz and f_{max} over 450 GHz with an emitter size of 0.65×8.65 μm^2 were achieved. Scaled InGaAsSb DHBTs exhibit excellent potential for higher speed performance.

Acknowledgments

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