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COMMISSIONING OF THE IGP FEEDBACK SYSTEM AT DAΦNE

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Abstract

The iGp (Integrated Gigasample Processor) is an innovative digital bunch-by-bunch feedback system developed by a KEK / SLAC / INFN-LNF joint collaboration. The processing unit can sample at 500 MHz and compute the bunch-by-bunch output signal for up to ~5000 bunches. The feedback gateware code is implemented inside just one FPGA (Field Programmable Gate Array) chip, a Xilinx Virtex-II. The FPGA implements two banks of 16-tap FIR (Finite Impulse Response) filters. Each filter is realtime programmable through the operator interface. At DAΦNE, the Frascati Φ-Factory, two iGp units have been commissioned in the April 2007. The iGp systems have substituted the previous betatron feedback systems. This insertion has been very fast and has shown no problems involving just a substitution of the old, less flexible, digital systems, letting unchanged the baseband analog frontend and backend. The commissioning has been very simple, due to the complete and powerful EPICS operator interface, working well in local and remote operations. The software includes also tools for analyzing post processor data. A description of the commissioning with the operations done is reported.

INTRODUCTION

In lepton circular accelerators, nowadays digital bunch-by-bunch feedback systems are largely used to damp coupled bunch instabilities in both transverse and longitudinal plans. The need of this kind of systems and the continuous technology developments ask for always new powerful designs [1].

To avoid wasting efforts in term of manpower and budget, large international collaborations between high energy laboratories feedback teams have been carried on with very good results in several colliders and light sources [2][3]. Commissioning done on multiple machines makes much more simple and fast testing and debugging hardware and software of the systems.

The iGp feedback has been designed by joint efforts of feedback teams from high energy laboratories spread in three continents. At DAΦNE, the Frascati Φ-Factory, two iGp feedback units have been commissioned in the April 2007 and other two in this year. In the following, starting from a system overview, the commissioning operative procedures and results are described.

SYSTEM OVERVIEW

The iGp (Integrated Gigasample Processor) [4] [5] is an innovative digital bunch-by-bunch feedback system developed by a KEK / SLAC / INFN-LNF joint collaboration. The processing unit can sample at 500 MHz and compute the bunch-by-bunch output signal for up to ~5000 bunches. The feedback gateware code is implemented inside just one FPGA (Field Programmable Gate Array) chip, a Xilinx Virtex-II. The FPGA implements two banks of 16-tap FIR (Finite Impulse Response) filters. Each filter is realtime programmable through the operator interface. In the Fig. 1, the iGp block diagram is shown.

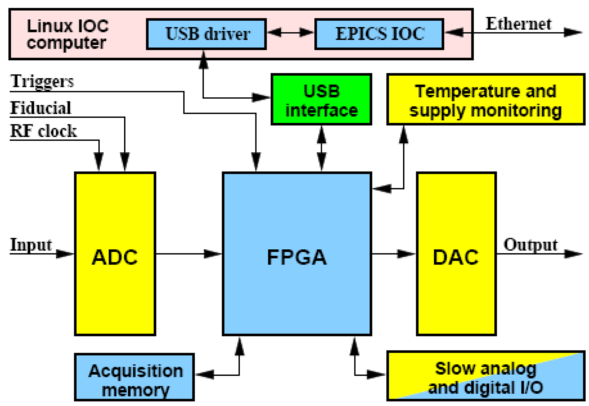

Figure 1: iGp block diagram.

The FPGA communicates by a USB interface with a commercial personal computer located in the iGp chassis. An EPICS IOC software package [6] is running in the internal PC Linux environment and by an Ethernet link can talk to the operator interface in the EPICS client PC.

In Fig. 2 the EPICS operator interface plotting two FIR filter coefficient sets is shown.

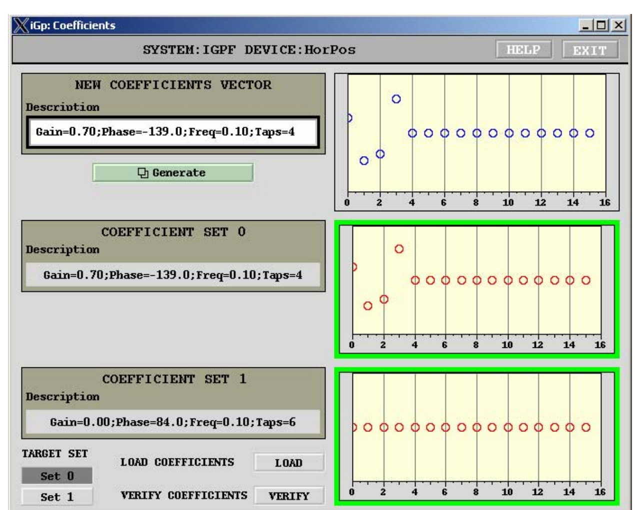

Figure 2: FIR filter coefficient set EPICS panel.

In order to produce a new coefficient set, the parameters to be chosen by the human operator are the following: gain (in the range from 0 to 1), phase (-180,

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180 in degrees), filter center frequency, number of taps (from 1 to 16). Other important parameters can be set using the Control panel shown in Fig. 3.

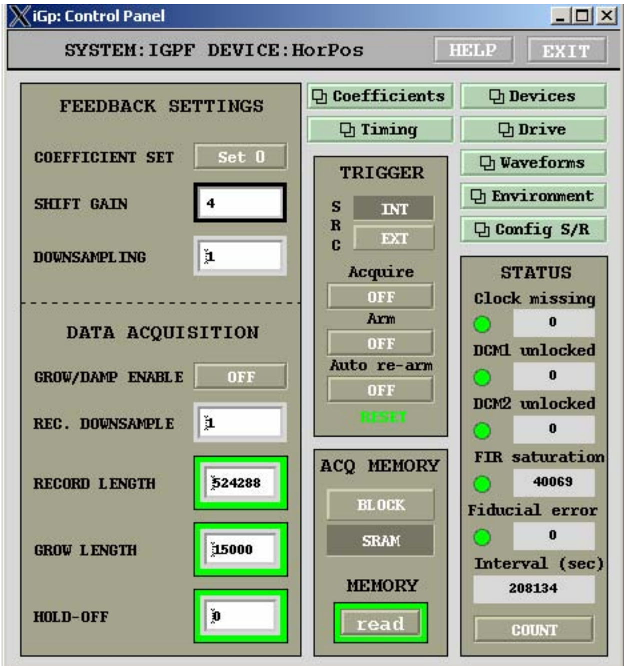

Figure 3: EPICS Control panel.

In order to operate on the feedback settings, the Control panel can allow choosing the coefficient set (1 or 2), the shift gain (0:7), meaning a binary shift by 0:7 position in the output signal, and the downsampling factor.

Other Fig. 3 command blocks manage data acquisition for offline analysis, internal or external trigger feature and internal memory size to be used for data acquisition. Diagnostics about feedback correct work is shown in the status block. Other important features can be called by seven subpanel pointers in the right top of the Fig. 3. In particular, the "Waveforms" panel shows the real time behaviour plot in time and frequency, the "Drive" panel can excite the beam or a specific bunch pattern by different waves generated by the system, the "Timing" module (see Fig. 4) can modify the front end or back end timing set, the "Environment" panel (see Fig. 5) shows internal temperatures for diagnostics purpose, the "Config s/r" panel is used to save or restore the feedback setup.

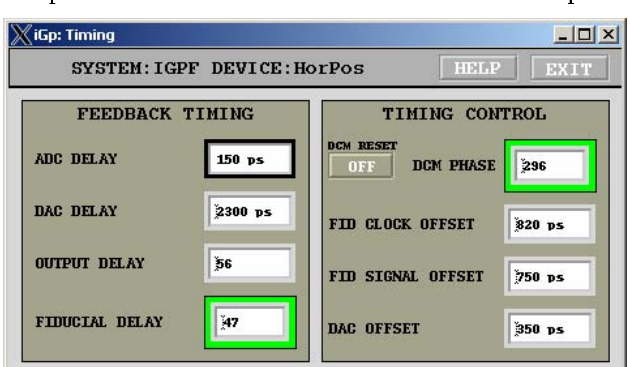

Figure 4: EPICS Timing panel.

COMMISSIONING AT DAΦNE

Two iGp units have been commissioned in the April 2007 at DAΦNE. The iGp systems have substituted the previous betatron feedback systems. The insertion has been very fast and has shown no problems involving just a substitution of the old, less flexible, digital systems [7], letting unchanged the baseband analog frontend and backend.

Commissioning, as it is well known, is the phase of installation and start-up of a technical supply, and of verification that it is complying with specifications.

The iGp commissioning has been very simple, using the powerful EPICS operator interface, working well both in local and remote operations. The software includes also tools for analyzing post processor data. A description of the operations done to find the best feedback setup and to complete the commissioning is reported below.

The iGp commissioning has been very fast and basically has been stepped in the following five operations:

1) front end timing (single bunch)
2) back end timing (single bunch)
3) best betatron phase response selection, with and without using white noise excitation (single bunch);
4) gain and shift gain selection (single bunch);
5) final tests with multibunch injected pattern.

Figure 5: EPICS Drive panel.

The first point (frontend timing) has been accomplished storing a single bunch in the ring, sweeping the f.e. delay value and finding the peak of the response (in the "Waveforms" panel) for a single bunch. The use of an orbit bump at the feedback pickup can be helpful.

The second goal has been achieved in two equivalent ways: selecting a single tap filter or using an output pulse generated through the "Drive" panel. In both cases, looking at the two kicker downstream ports by an oscilloscope and sweeping the b.e. delay value, it has been possible to find a precise overlap between the excitation and the bunch signals. A check on the signal equalization in magnitude and skew between the two kicker ports is always very useful.

The third point, i.e. to find the best betatron phase advance, has been accomplished experimentally, storing in the ring a single bunch, exciting it by external white noise, then closing the feedback loop and sweeping the feedback betatron phase on 360 degrees to evaluate the best value looking at the betatron sidebands by using a spectrum analyzer or directly in the “Waveforms” panel.

Feedback gain and shift gain have been set for a single bunch pattern and, after this step, injecting multiple bunches with progressively increasing beam currents. At high currents it is possible to find better and more precise setups. This ways to proceed is necessarily iterative because beginning with a “rough” feedback setup makes possible to store multibunch patterns and to increase the beam current. At this point it is possible to try a new, more suitable setup, changing feedback parameters in real time, without loosing the beam, by small steps. In particular it may be interesting to note that often the best filter center frequency at high beam current can differ from the best single bunch value in a range of 5%.

The first commissioning of the iGp feedback, after a fast hardware and software installation including the necessary Ethernet connections, has requested only two hours of dedicated machine time for each system.

Analysis off line tools [8] have used to study beam dynamic in DAΦNE: in the e+ horizontal plane, an extremely fast mode -1 limits the beam stability and the storable beam current.

2008 UPGRADE

During the year 2008 other two iGp system have been installed at DAΦNE, completing the transverse planes in both rings. A new software and gateware revision has been implemented in the four iGp units and tested with the beams. The EPICS client package, for Fedora-8 Linux environment, has been installed in a powerful dual core personal computer used as dedicated interface for the operators in control room.

With the last revision, new features have been tested as, for example, an off-line tool to measure the betatron bunch-by-bunch tune spread, as shown in Fig. 6.

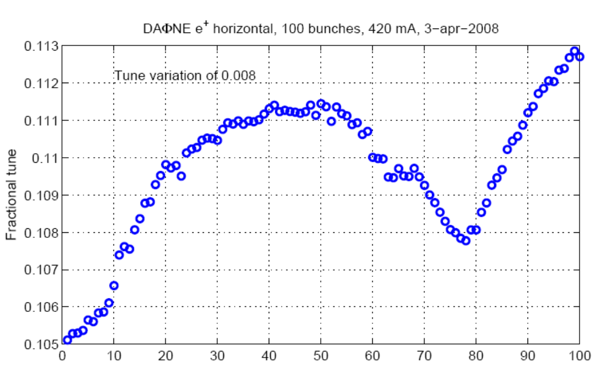

Figure 6: Bunch-by-bunch e+ horizontal tune.

CONCLUSION

Four iGp feedback systems have been commissioned in the transverse plane at DAΦNE. The insertion of these new systems has been done rapidly and has shown no problems requesting only a very little dedicated machine time. The commissioning has been very simple, due to the complete and powerful EPICS operator interface, working well both in local and in remote operations.

Powerful diagnostics inside the system help to understand beam current limits, to study beam dynamics and evaluate feedback performances. Analysis off line tools have shown an extremely fast mode -1 and a large tune spread in the e+ horizontal plane limiting the beam stability and the storable beam current.

REFERENCES

[1] A.Drago, “Trends in Fast Feedback R&D”, arXiv:0806.1864 , Jun 12, 2008.

[2] J.D.Fox, H.Hindi, I.Linscott, J.Olsen, G.Oxoby, L.Sapozhnikov, D.Teytelman (SLAC), A. Drago, M. Serio (INFN-LNF), J.Byrd, J.Corlett (LBL), "Operation and Performance of a Longitudinal Damping System using Parallel Digital Signal Processing", EPAC 1994.

[3] J.Fox, S.Prabhakar, D.Teytelman, A.Young (SLAC), G.Stover (LBL, Berkeley), A.Drago, M.Serio (INFN-LNF), S.Khan, T.Knuth (Bessy, Berlin), Y.J.Kim, M.K.Park (Pohang U.Sci.Tech.), "Programmable DSP Based Multibunch Feedback: Operational Experience from Six Installations", SLAC-PUB-8410, May 2000. Published in *Cambridge 2000, Beam instrumentation* 226-233.

[4] D.Teytelman, C.Rivetta, D.Van Winkle, R.Akre, J.Fox, A.Krasnykh, (SLAC), A.Drago, (INFN/LNF), J.Flanagan, T.Naito, M.Tobiyama, (KEK), “Design and Testing of Gproto Bunch-by-Bunch Signal Processor”, THPCH103, EPAC2006.

[5] D.Teytelman,“iGp-120F Signal Processor - Technical User Manual”, Rev.1.4, Jan.5, 2008.

[6] EPICS documentation: http://www.aps.anl.gov/epics/

[7] A.Drago, A.Argan, M.Serio (Frascati), "Fast Electronics for the DAFNE Transverse Feedback Systems", ICALEPCS-2001-WEAP048, Nov 2001. Published in eConf C011127:WEAP048, 2001. Also in *San Jose 2001, Accelerator and large experimental physics control systems* 376-379. e-Print Archive: physics/0111209.

[8] Shyam Prabhakar, **“**New diagnostics and cures for coupled bunch instabilities”. SLAC-R-554, SLAC-R-0554, SLAC-554, SLAC-0554, UC-410, UMI-99-86494-MC, Feb 2000. 188pp. Ph.D. Thesis.