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Low-Power, High-Speed InGaAs/InP Photoreceiver for Highly-Parallel Optical Data Links

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Abstract–Low-power photoreceivers based on InGaAs/InP heterojunction bipolar transistors (HBTs) and p-i-n diodes for highly-parallel optical data links have been designed, fabricated and characterized. The receivers are designed to operate from 980 nm to over 1.3 μm and interface directly with 3.3 V CMOS. SPICE was utilized to investigate circuit topographies that minimize power dissipation while maintaining large signal operation required to interface directly with CMOS. Low-power dissipation of ~10 mW/channel has been achieved at bit rates up to 800 Mbits/sec. Performance characteristics of discrete HBTs and of low-power photoreceivers fabricated with p-i-n/HBT circuits are reported.

I. Introduction

As clock rates increase and more channels are required, an alternative interconnect technology will be needed for interconnects in multichip-module (MCM)-based systems. Current backplane and ribbon technologies are limited in both speed and number of channels. High-speed necessitates transmission line interconnects such as coplanar ribbon cables which limits the possible number of channels between modules due to the relatively large connector size. Large numbers of channels in a highly-parallel configuration are desired because each channel can operate at the system clock rate to provide a high-throughput data link without the timing and power penalties of multiplexing/demultiplexing. Optical data link technologies promise high speed and high density, but power consumption must be reduced if they are to be viable technologies for MCM high-density data links.

In this paper we report the design, fabrication and characterization of low-power, high-speed photoreceivers based on InGaAs/InP HBT amplifiers and InGaAs p-i-n detectors that are suitable for both free-space and guided-wave, highly-parallel data links [1]. With SPICE simulations, several circuit topologies were studied to realize low-power dissipation with large-signal operation suitable for directly driving high-speed 3.3 V CMOS devices/ASICs. The circuit is implemented in two-dimensional arrays of photoreceivers.

II. System Requirements

Highly-parallel, high-density data link technology would greatly benefit systems such as image correlation processors. These systems are based on MCM technology where transfers of huge volumes of data between modules limits the throughput. The ability to rapidly transfer digitized images between modules would permit real-time image correlation that is critical in many image recognition implementations. Of course gigabit/sec data links could be used, but there is a time delay associated with multiplexing/demultiplexing operations and a power penalty with the additional circuitry.

Free-space optical interconnects would enable the realization of hundreds and even thousands of data channels between vertically stacked MCMs. In addition, these links offer greater flexibility in module design since they are not constrained to placement along the module periphery. Such a large number of parallel channels results in huge data throughput at a modest individual channel bit rate. With such a highly-parallel interconnect system, the per channel power budgets must be low for both electrical and thermal considerations. Furthermore, long-wavelength (>1.1 μm) data links are desired to eliminate the need for substrate via holes in silicon-based MCMs which is a common substrate material.

An additional requirement for this data link is that it interfaces with 3.3 V CMOS devices/ASICs without a separate buffer or line driver. This further minimizes the timing penalty and also minimizes valuable MCM area that is required for interconnect circuitry in conventional links. Propagation delays less than 1.5 nsec are required for this photoreceiver and are defined as the time lapses relative to the optical emitter turn on/off and when the output voltage level triggers a change in a CMOS logic. For a high-to-low transition, 1.4 V was the defined trigger level from a high to a low and 1.55 V corresponded to a low-to-high trigger level. The bitrate is limited by the CMOS circuitry which is 100 Mbits/sec in this application. Although the bit rate is only moderately high, the photoreceiver bandwidth must be high to achieve the fast rise and fall times specified for this system. As with any system, minimizing the number of rail voltages is an important consideration in this work, therefore, the

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photoreceiver is designed to operate with a single 3.3 V power supply.

A low-power optical data link includes the total power dissipation in both the emitter-source and photoreceiver. A study of receiver-power dissipation versus sensitivity versus emitter-source power was performed to set the photo-receiver power specification. Increasing the photoreceiver power budget meant less power was available for the emitter-source which meant higher receiver sensitivity was required. Conversely, a lower receiver power budget meant higher optical power could be realized and lower photoreceiver sensitivity was acceptable. The study yielded the specifications that 10 mW could be dissipated in the photoreceiver when ~0.5 mW of 980 nm light was incident on the detector.

III. Circuit and Device Design

The circuit design is based on HBT transistors and p-i-n detectors. The photodetector was chosen to be a narrow-bandgap InGaAs p-i-n detector to realize high sensitivity up to 1.5 μm excitation. To realize the high-current drive capability which is required to switch the CMOS load with subnanosecond rise and fall times, and for fabrication compatibility with the InGaAs detector, InP/InGaAs HBT amplifiers were chosen. A benefit to using HBTs amplifiers is the low input impedance as compared to FET technology. The low impedance results in rapid discharge of the p-i-n detector without a discharge resistor which lowers sensitivity.

Circuit performance and optimization was studied with SPICE simulations. Because an HBT model is not incorporated in SPICE, the standard BJT Gummel-Poon model with appropriate bandgap energies for the wide-bandgap InP emitter and narrow-bandgap InGaAs collector was utilized. Transistor model parameters were extrapolated from reported device performance [2,3] and were estimated from physical parameters. Shown in Fig. 1 is the model Gummel plot; other relevant performance parameters are f_T = 20 GHz, I_{sat} = 1e-16 A, base-emitter junction capacitance of 20 fF and base-collector junction capacitance of 8 fF. Several circuit topologies were studied including a cascode circuit combining common-base and common-emitter configurations. This configuration was investigated in an attempt to even further lower the input impedance of the amplifier; however, sufficiently low power dissipation could not be obtained with the cascode circuit. In all simulations a 4 pF load was considered to simulate the load of the input of a typical 3.3 V CMOS gate/ASIC.

The best performance was obtained with the circuit shown in Fig. 2. In this design the transistors operate in a switching mode. Transistors Q_{ch} and Q_{dch} charge and discharge the 4 pF load respectively when individual bias conditions are switched by Q_{sw}. The photocurrent controls the bias of switch transistor Q_{sw}. With photoexcitation, Q_{sw} is turned on by the photocurrent which turns off Q_{dch}. When Q_{dch} turns off, resistor R_{ch} strongly forward biases the base-emitter junction of Q_{ch} and the load is switched from a low to a high. When the photocurrent becomes extinct, transistor Q_{sw} turns off and Q_{dch} turns on when R_{dch} strongly forward biases the base-emitter junction of Q_{dch}. In this condition, diode D is also strongly forward biased and the load is rapidly discharged from a high to a low state through the diode and Q_{dch}. The load voltage is the saturated Q_{ch} voltage plus the voltage drop across diode D. With a purely capacitive load, the voltage across D is small since the current is small and V_{out} is roughly the saturated HBT voltage. The function of diode D is to limit the current through transistor Q_{ch} when Q_{dch} is turned on. With the base of Q_{ch} tied to the low side of diode D, the base-emitter junction of Q_{ch} is reverse biased to the forward bias voltage of diode D when Q_{dch} is turned on; the reverse bias condition of Q_{ch} limits the collector current when a low state is transmitted.

Using SPICE values of resistors in the circuit shown in Fig. 2 were optimized for low-power dissipation and high-speed switching. Other circuit parameters employed in the circuit modeling were a standard parallel-RC model for the p-i-n diode with 0.25 pF junction capacitance which dominated the p-i-n response characteristics, a 4 pF load, and a current source for the photocurrent. The current source characteristics included 0.5 nanosecond rise/fall times and the peak response was varied from 100 μA to 500 μA.

Optimization of circuit resistor values resulted in an ultra-low power photoreceiver design. Resistor R_{det} was included in the circuit design to achieve a sufficiently fast high to low transition. By adding R_{det} in parallel with the base-emitter junction of Q_{sw} the p-i-n discharged faster and the transition from high to low was brought into specification.

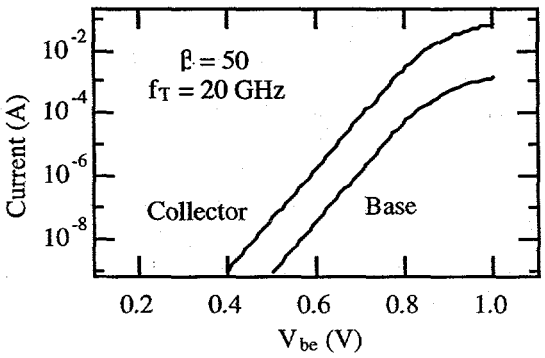

Fig. 1. Gummel plot and performance specification of InGaAs/InP HBT model utilized in SPICE simulations.

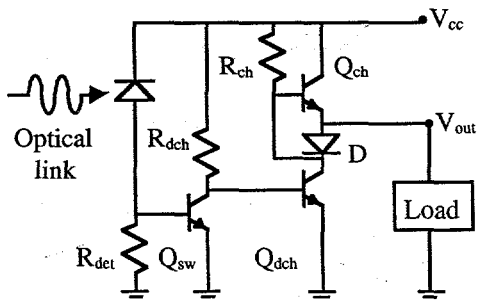

Fig. 2. Circuit design for low power photoreceiver integrating p-i-n detector and HBT amplifier.

The optimum resistance values are 2kΩ, 3kΩ, and 10kΩ for resistors R_{ch}, R_{dch} and R_{det} respectively. With these resistance values only 8.1 mW of average dissipated power occurred in the worst case where an alternating sequence of highs and lows occurred. A non-return to zero (NRZ) data format would lower the average power dissipation. The optimized simulated responses of both photocurrent and load voltage are shown in Fig. 2.

The low power dissipation results from exploiting the high speed of the HBTs. Power dissipation is governed by quiescent current through the resistors. This is shown in a simplified analysis of the circuit shown in Fig. 2 where the junction voltage is neglected. In a low-state Q_{dch} is on and most of the current from V_{cc} is through R_{ch}; the power dissipated is 5.4 mW. Similarly, in the high state most of the current is through R_{dch} and 3.6 mW is dissipated. The average power required to charge the 4 pF load is simply $fC_{load}V^2 = 2.6$ mW. The averaged sum is 7.1 mW which agrees well with the rigorous simulation result of 8.10 mW.

As shown the voltage swing is from 0.8 V in a low state to 2.6 V in a high state. This large swing is sufficient for directly interfacing with high-speed 3.3 V CMOS. In addition extremely short propagation delays are realized; the delay times, as defined earlier, are ~1 nsec. The high-speed, large-signal operation with low power is possible with HBT circuits because of the high-current drive capability and the low input impedance of HBTs. Both of the properties permit subnanosecond charging and discharging of the 4 pF CMOS load. In the simulations, the peak current is 50 mA with >1mA for ~0.7 nsec. The actual peak values are expected to be lower do to the idealized circuit components used in the simulations.

Extensive device modeling was performed to maximize p-i-n detector sensitivity and HBT speed. The two performance specifications were coupled because the base-collector junction of the HBT is utilized as the p-i-n detector. This processing scheme minimizes fabrication because the detector is fabricated for free when the HBT is processed [4,5]. Increasing the junction thickness increases the p-i-n collection efficiency but also decreases the HBT speed because the collector transit time increases. An additional constraint of the junction thickness is that the circuit is powered by 3.3 V which must completely deplete the reversed biased diode to maximize collection efficiency. Balancing these conditions resulted in the optimized structure which is shown Fig. 4.

The detector collection efficiency is further increased by utilizing backside illumination with a frontside metal mirror to achieve double pass absorption of the incident light. This approach required that the subcollector be a wide bandgap material to prevent attenuation of the incident light. This is possible with phosphide-based HBTs because the wide bandgap InP can be doped to highly degenerate levels which permits excellent contact fabrication.

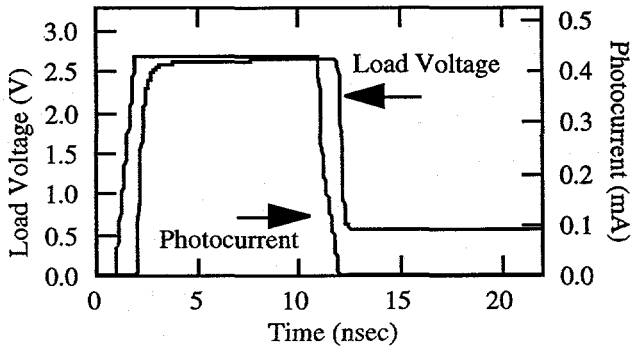

Fig. 3. Simulated performance of photoreceiver utilizing HBTs with characteristics shown in Fig. 1 and circuit topography shown in Fig. 2. The average power dissipation is 8.1 mW.

IV. Circuit Fabrication

The material for circuits was grown by MOCVD with zinc as the p-type InGaAs dopant, sulfur as the n-type InGaAs dopant and sulfur as the n-type InP dopant. Transistors with 2.6 x 5.2 μm^2 and 2.6 x 10.4 μm^2 emitters are used in the circuit for Q_{sw} and both Q_{ch}/Q_{dch} respectively. Non-alloyed Ti/Pt/Au contacts are used for emitter, base and collector contacts. The base contact is a self-aligned contact. To achieve good control of undercut, a combination dry-wet etch is used for both emitter and base mesa etching while the collector mesa is all wet etched.

Both discrete devices and two-dimensional (2-D) arrays of photoreceivers were processed. Planarization was performed with Dow Chemical benzocyclobutene (BCB). Two-level metal interconnects were also possible using the BCB as the dielectric. Tantalum nitride resistors were used in the circuit fabrication. In addition to circuits, discrete devices were fabricated and characterized to validate the device model used in the circuit modeling. A high-density, 2-D photoreceiver 4x4 array for free-space optical data links is shown in Fig. 5. Photoreceivers with various detector diameters were fabricated with 50 μm diameter p-i-n detectors determined to be optimum for this application. All detectors are on 500 μm spacing. The figure shows that the technology is easily scaled to higher density which is possible due to the ultra-low power dissipation achieved with this design.

V. Device and Circuit Characterization

Discrete HBTs exhibit current gain of 120, an f_T of 50 GHz and an f_{max} of 60 GHz which exceeded the specifications of the device model utilized in the circuit simulations. The

	1200 Å InGaAs	$1.5x10^{19}cm^3$
	500 Å InP	$2.0x10^{19}cm^3$
Emitter	1000 Å InP	$5.0x10^{17}cm^3$
Base	1000 Å InGaAs	$1.0x10^{19}cm^3$
Collector	8300 Å InGaAs	$6.0x10^{15}cm^3$
	100 Å InGaAs	$1.5x10^{19}cm^3$
	3000 Å InP	$2.0x10^{19}cm^3$
	S. I. substrate	

Fig. 4. Device structure for a low power photoreceiver utilizing a p-i-n detector and a Npn-HBT amplifier that are fabricated simultaneously with a self-aligned HBT process.

circuit is designed to interface directly with 3.3 V CMOS with a nominal input impedance dominated by a 4 pF gate capacitance. All measured results shown are with a 3.3 V power supply. Fig. 6 shows the eye diagram of the photoreceiver driving a 4 pF load at the system bit rate of 100 Mbits/sec. The noise properties are dominated by the measurement system which prevented sensitivity characterization. As shown, a large signal swing of 0.8 V to 2.6 V compatible with driving 3.3 V CMOS directly is achieved. The receiver delay when driving a 4 pF load is ~1.0 nsec with ~10 mW per channel power dissipation. The delay was independent of power above -10 dBm incident light. A high degree of optical noise immunity is inherent in the circuit design and low electrical noise is realized with the multilevel metallization used to access individual receiver channels.

Shown in Fig. 7 is the photoreceiver response to a laser being stimulated by a squarewave voltage source to yield a 200 MHz squarewave light-pulse train with ~600 μW/detector area maximum intensity. The slow fall in the response is an artifact of the laser characteristics which exhibited an intensity characteristic decay time of 1.2 nsec; higher speed is expected with higher performance emitter-sources. An average power of ~10 mW is dissipated when driving a typical 4 pF CMOS load with large signal voltage swing. Comparable low-power dissipation per channel has been demonstrated up to 800 Mbit/sec which is the limit of the emitter-source. At 800 Mbits/sec the voltage swing is slightly lower; however, it can be restored with increased V_{cc}.

VI. Conclusion

A photoreceiver design for highly-parallel optical datalinks was presented. The receiver is based on InP/InGaAs HBT amplifiers powered by a 3.3 V supply and is designed to interface directly with 3.3 V CMOS devices/ASICs. Validation of the design was completed by fabrication of 4x4 arrays of photoreceivers that exhibited the ultra-low power dissipation of ~10 mW/channel when driving a 4 pF load which is a typical 3.3 V CMOS input load. Low power dissipation is key to high-density optical data links for both thermal and electrical reasons; this low-power photoreceiver can be implemented in both free-space and guided-wave optical data links.

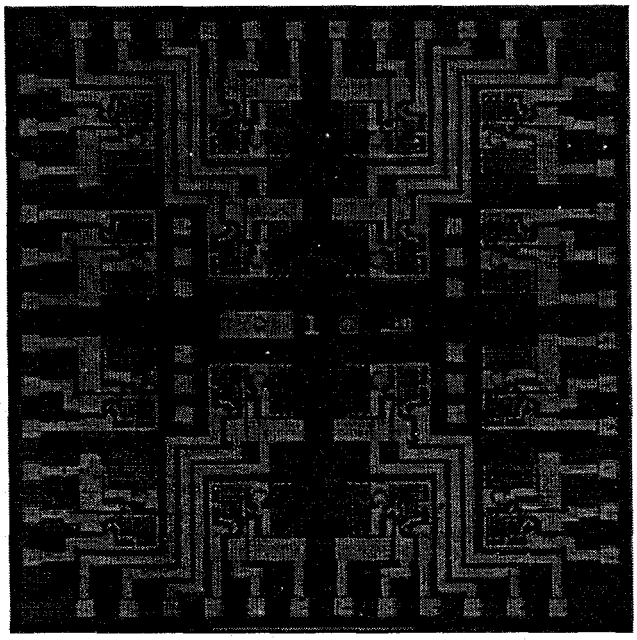

Fig. 5. 4x4 two-dimensional arrays of InGaAs/InP HBT/p-i-n photoreceivers for free-space optical interconnects.

Acknowledgment

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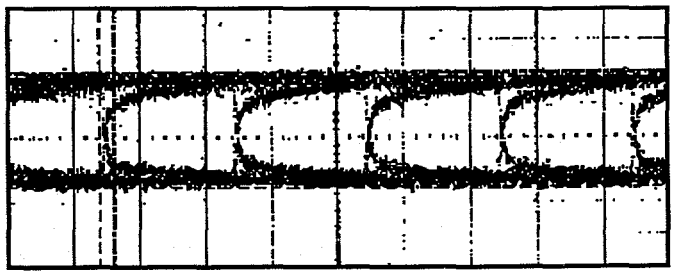

Fig. 6. Eye diagram for output of photoreceiver circuit shown in Fig. 1 operating at the system design bit rate. The data rate is limited to 100 Mbit/sec by the CMOS devices/ASICs that are connected directly to the photoreceivers; horizontal scale is 5 nsec/div and vertical scale is 0.5 V/div.

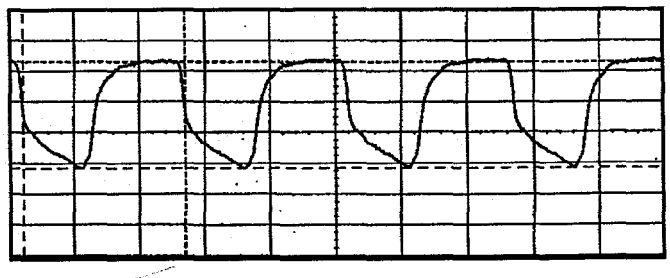

Fig. 7. Photoreceiver response driving a 4 pF load at equivalent bit rate of 400 Mbits/sec. The large voltage swing of 0.8 to 2.6 V which is suitable for driving 3.3 V CMOS; horizontal scale is 2.0 nsec/div and vertical scale is 0.5 V/div. The slow decay observed in the low-state is an artifact of the laser output.