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Electron and optical beam testing of integrated circuits using CIVA, LIVA, and LECIVA

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Charge-Induced Voltage Alteration (CIVA), Light-Induced Voltage Alteration, (LIVA), and Low Energy CIVA (LECIVA) are three new failure analysis imaging techniques developed to quickly localize defects on ICs [1-3]. All three techniques utilize the voltage fluctuations of a constant current power supply as an electron or photon beam is scanned across an IC. CIVA and LECIVA yield rapid localization of open interconnections on ICs. LIVA allows quick localization of open-circuited and damaged semiconductor junctions. LIVA can also be used to image transistor logic states and can be performed from the backside of ICs with an infrared laser source. The physics of signal generation for each technique and examples of their use in failure analysis are described.

1. INTRODUCTION

It is critical to develop new failure analysis techniques to keep pace with the continued development of increasingly complex ICs. Ideally, these improved analysis techniques should be easier to use, less damaging, more sensitive, and they should provide better spatial resolution. An ideal failure analysis technique would not only be simple, fast, and benign but would also use existing or readily available equipment and software.

The scanning electron microscope (SEM) is a necessary part of every failure analysis laboratory, commonly used for high resolution images with a large depth of field. The SEM has become a powerful failure analysis tool because of the electron beam's ability to interact with an IC and precisely localize the effects of this interaction.

Another instrument becoming more common in failure analysis laboratories is the scanning optical microscope (SOM). The SOM's confocal mode provides improved image resolution and depth of focus compared to conventional optical microscopy. Like the SEM, the SOM can be a very useful analysis tool because of the laser beam's interaction with the IC. The effects of light on the electrical properties of active ICs have been well documented [4-7].

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CIVA, LIVA, and LECIVA (charge-, light-, and low energy charge-induced voltage alteration) are three techniques recently developed for IC failure analysis that take advantage of the interactions between a scanning electron or photon beam and a biased IC. CIVA and LECIVA are used to quickly localize open interconnections. LIVA is used to localize junction related defects as well as to identify logic states from the die front and backside. All three techniques utilize voltage changes in a constant current supply as the beam is scanned across the IC.

The physics of signal generation, data acquisition techniques, and protocols for image collection are described in detail for each technique. The imaging results for the three analysis methods demonstrate their utility as failure analysis tools. A summary highlighting the similarities and differences of each techniques is given after the individual tool descriptions. The three techniques will be described in the order they were developed; CIVA, LIVA, and LECIVA.

2. CIVA

CIVA is analogous to electron beam induced current (EBIC) [4] and optical beam induced current (OBIC) imaging [5] in that the biased IC itself is the detector and amplifier. The signal monitored to produce a CIVA image is the power supply voltage of a constant current source used to bias the IC as an electron beam is scanned across the device surface.

2.1. Electron beam-IC interaction physics

To produce the CIVA signal the primary electron beam must penetrate to the conductors of the IC as shown in Fig. 1. If a conductor is electrically open, the charge injected into the conductor by the primary electron beam can reduce the voltage of the conductor and greatly affect the voltage demands of an IC supplied by a constant current source.

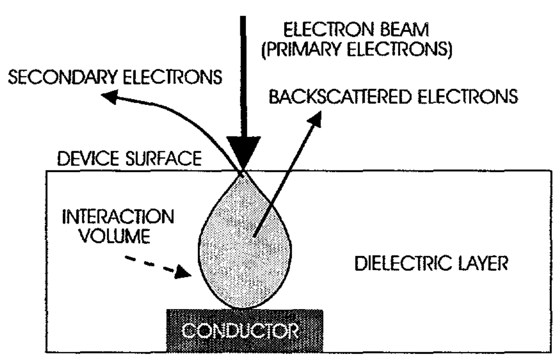

Fig. 1. For CIVA, the electron beam interaction volume must reach the conductor being examined.

The response of a CMOS inverter pair to various gate biases was examined (Fig. 2) to illustrate how changes in conductor voltages generate the CIVA signal. By using an inverter pair as our test structure the loading on the output of the first inverter would be representative of that found on an IC. The inverter pair was supplied with a constant current of 20 nA and a compliance voltage of 5 V. The results of a voltage sweep from 5 V to -1 V on the first inverter pair is shown in Fig. 3.

In Fig. 3 the power supply voltage drops significantly as the gate bias is reduced below 4.3 volts. An even more dramatic increase in power supply voltage occurs in Fig. 3 as the gate bias is reduced below 0.7 V. CIVA uses these changes in a constant current power supply voltage with changes in gate bias to produce an image. The CIVA images display the conductors which are susceptible to voltage change by small amounts of injected charge, i.e. open conductors.

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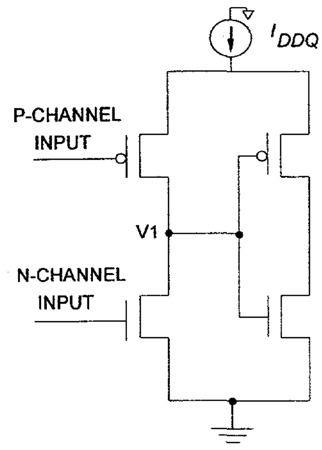

Fig. 2 Inverter pair used to demonstrate the CIVA signal.

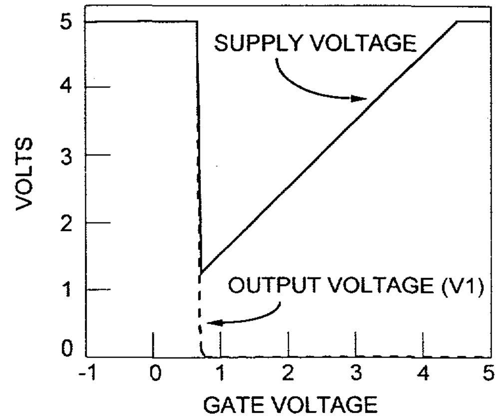

Fig. 3 Supply and output voltages of the inverter as a function of gate voltage with both input gates tied together.

The bias configuration of an IC for CIVA examination may be any non-contentive state. The static burn-in configuration used for IC burn-in and life testing is an example of an appropriate bias configuration.

While surface emission products like secondary electrons are not used to produce the CIVA image, they are a factor in image formation on passivated ICs. In order to penetrate through typical passivation layers the primary electron beam energy must be increased to 5 keV or above. At these beam energies more electrons are injected into the passivation layer than escape and a negative potential will build up on the surface [8]. This negative charge on the surface of CMOS ICs can effectively put all of the transistor gates into a low state, eliminating all IC functionality. As the primary electron beam energy is increased the interaction volume reaches buried conductors and a new current path is produced through the conductors. Charge can leave the passivation layer through the biased IC conductors and substrate. This additional current path reduces the negative charge of the passivation and permits normal operation of the IC. Voltage contrast observation may still be obscured by surface charging from areas with passivation thicker than that over the conductors, but the CIVA signal is not affected by this charging. The small added amount of charge from the electron beam has little effect on the IC operating characteristics of non-failing ICs, changing the power supply current by nanoamps [9].

2.2 Primary electron beam energy selection

To avoid radiation damage care must be taken not to use higher electron beam energies than are needed to reach the conductors of interest. The proper primary electron beam energy for CIVA imaging on passivated ICs is selected by first biasing the IC with a constant voltage source and the electron beam off. The IC current is then monitored as the primary electron beam energy is increased. The entire IC die is scanned at a rapid rate (TV scan rate) as the primary electron beam energy is increased. Initially the IC current will increase as the surface charges negatively. The IC current will decrease when the primary electron interaction volume intersects the buried conductors. Because most scanning electron microscopes change electron beam energy in 1 keV steps above 5 keV, there will be an abrupt energy at which the IC current falls.

For depassivated ICs the conductors are directly on the surface and very low primary electron beam energies (< 1.0 keV) are required to inject charge into these conductors.

Once the proper primary electron beam energy is selected, the IC current (I_{DDQ}) [6] under constant voltage conditions is recorded. For static CMOS ICs I_{DDQ} is normally several μA or less. A current value slightly (5%) less than this is then used to operate the IC with the constant current source. The resulting voltage powering the IC is very nearly that used under constant voltage source conditions. A compliance voltage limit prevents any accidental damage to the IC from the constant current source.

2.3 Types of open conductors

Open conductors can be grouped into two categories for CIVA imaging: (1) conductors that are open "completely" and communicate no significant electrical signal across the site of the open and (2) conductors that exhibit a significant amount of quantum mechanical electron tunneling across the site of the open [10]. "Complete" opens will slowly, over seconds, drift to various voltages. There is sometimes a preferred voltage that a "complete" open will drift to depending upon weak coupling from neighboring conductors and IC bias conditions. The voltage of "complete" opens can be dramatically changed when an electron beam is applied. After the electron beam is removed the "complete" open conductor will slowly (over seconds again) drift in voltage. For "complete" open conductors the change in power supply voltage is abrupt and large, 10% to 50% of the supply voltage, during the initial electron beam contact. To compensate for the slowly drifting voltage on "complete" open conductors after the electron beam is removed, the CIVA image is produced using the ac component of the power supply voltage.

Open conductors that exhibit a significant amount of quantum mechanical (QM) electron tunneling will function properly at reduced frequency but fail at higher speeds. The amount of charge conduction across QM opens varies exponentially with the voltage across the open until the QM open appears to be contiguous [10]. The time constant for charge conduction across QM opens can be on the order of milliseconds. Initial contact of QM open conductors with an electron beam will alter the open conductor voltage. The amplitude of voltage change and whether or not the open conductor remains at an altered voltage depends on the tunneling efficiency of the QM open and the amount of electron beam injected charge. When the electron beam is removed from the QM open conductor it quickly returns to its previous voltage. The dc or ac component of the power supply voltage can be used in CIVA imaging to examine QM type open conductors. In practice, only the ac component is used to eliminate any dc offset signals.

The optimum beam current for CIVA signal generation must be determined during image acquisition. Generally, several beam current conditions should be examined before concluding that no CIVA signal is present.

2.4 The "over-supply" method

One final note about CIVA acquisition concerns the use of the ac coupled amplification system. As alluded to previously, one advantage of using ac coupled amplification is the mitigation of any dc offset signals that can complicate data acquisition. Another advantage is the use of an "over-supply" approach which increases the effective bandwidth of the CIVA system. Increased system bandwidth permits faster image acquisition without a loss in spatial resolution.

The "over-supply" method involves increasing the supply current of the constant current source well above the maximum current needed to maintain the compliance voltage of the power supply. The compliance voltage (5 V for the examples in this paper) prevents damage to the IC from overvoltage. If the constant current supply had infinite bandwidth, no CIVA signal would be produced under "over-supply" conditions. Because the current source does have bandwidth (response time) limitations, there will be a momentary reduction in supply voltage as the current source attempts to "keep up" with power demands. The CIVA signal can be produced by amplifying the momentary voltage reductions with the resultant system bandwidth being determined by the constant current source. The "over-supply" approach enables image acquisition of an entire IC die while the electron beam is scanned at TV rates. ("Over-supply" is also applicable to LIVA and LECIVA imaging.)

2.5 Data acquisition system

A block diagram of the CIVA system used at Sandia is shown in Fig. 4. This is similar to the system used for LIVA and LECIVA.

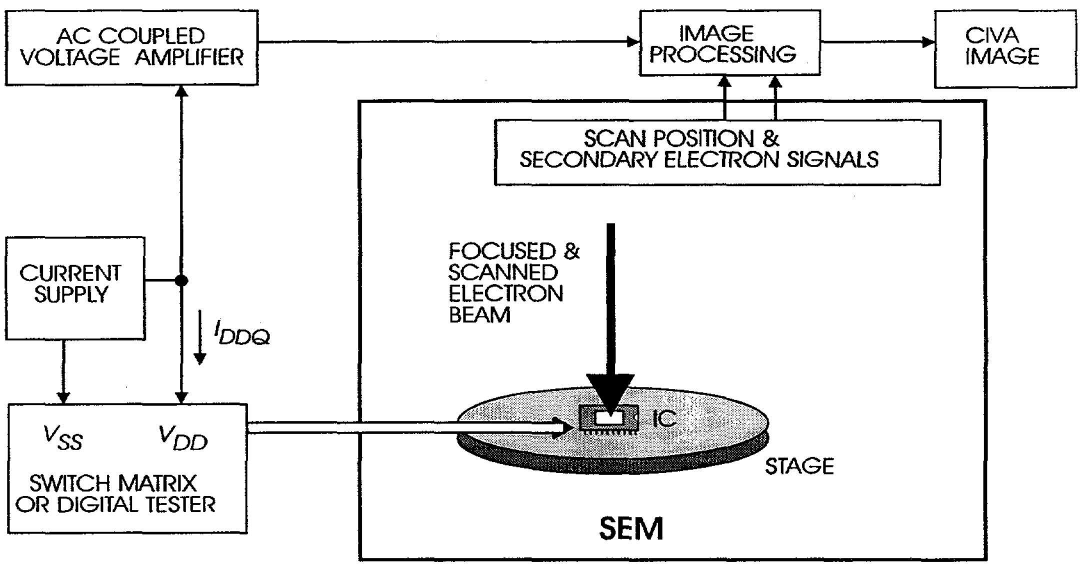

Fig. 4. CIVA acquisition/processing system.

Electrical stimulus to the IC (V_{DD} and V_{SS}) is provided by a Keithley 236 source measurement unit (SMU). During CIVA setup, the SMU is initially used as a constant voltage source to determine if the IC is operating properly and to measure the IC's power supply current (I_{DDQ}). The supply is then used as a constant current source for CIVA analysis. The compliance voltage is set (normally at 5 V) to prevent accidental overvoltage damage of the IC. The electrical state of the IC is controlled using a simple switch box to change the logic values of the inputs. A function generator or digital tester can be interfaced to the IC for higher frequency operation.

CIVA images are produced by changes in the operating power supply voltage (V_{DD}) of the IC. Voltage variations in the power supply as a function of electron beam position are amplified using an Ithaco 1201 voltage amplifier in ac coupled mode or by direct dc measurement of the supply voltage. The signal from the ac coupled amplifier is connected directly to the auxiliary input of the SEM. The amplifier gain and bandpass filters of the Ithaco 1201 are adjusted to optimize the CIVA image.

2.6 CIVA imaging example

Figs. 5a-c illustrate CIVA imaging applied to a passivated, 1.0 μm feature size, two-level metal CMOS gate array. The total dielectric layer was approximately 2.0 μm thick. The image was made using a primary electron beam energy of 15 keV and an initial magnification of 14X. The pattern in the upper left of Fig. 5a is the floating portion of a conductor fan-out network containing both metal-1 and metal-2 segments. Fig. 5b is a CIVA/Secondary Electron combined image for registration. Fig. 5c examines the floating conductor at higher magnification. The metal-1 conductor segments produce a CIVA signal when they are not covered by metal-2. In Fig. 5c the cause of the open conductor, an intentional focused ion beam cut, can be seen on the right.

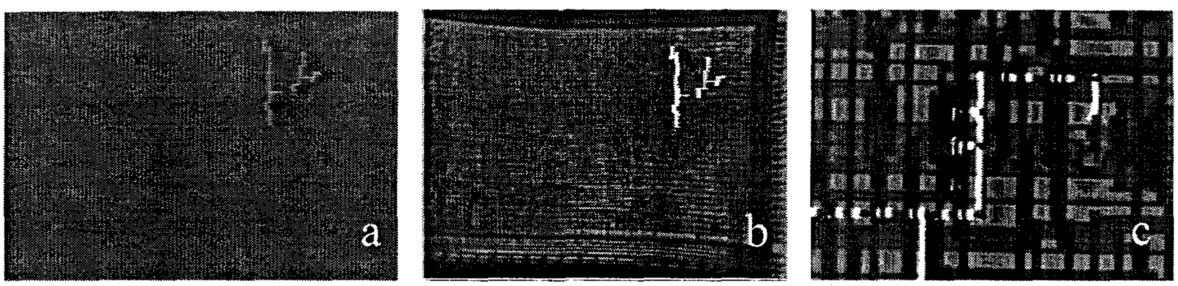

Fig. 5. The CIVA signal from a floating fan-out network is shown in 5a for this two-level metal, 1.0 micron technology. The overlay of the CIVA signal with a secondary electron image is shown in 5b. 5c is a CIVA-secondary electron image of the floating conductor at higher magnification. A focused ion beam cut producing the open conductor can be seen in 5c.

3. LIVA

LIVA is analogous to CIVA in that the biased IC is the detector. LIVA images are produced by monitoring the voltage change of a constant current source used to bias the IC as a focused laser beam is scanned across the sample.

3.1 LIVA system

The LIVA system used at Sandia is similar to the CIVA system in Fig. 4 with the SEM replaced by a SOM. The SOM used at Sandia is a Zeiss Laser Scan Microscope. In our system, three lasers are available: (1) the internal 633 nm, 5 mW HeNe laser; (2) an external 1152 nm, 5 mW HeNe laser; and (3) an external 1064 nm, 1.2 W Nd:YAG laser. Electrical stimulus for the IC, amplification, and input into the auxiliary port of the SOM are similar to that used for CIVA.

3.2 Photon-IC interaction physics for LIVA generation

LIVA takes advantage of photon generated electron-hole pairs to yield information about IC defects and functionality. When electron-hole pairs are generated near the interface between differently doped regions in an unbiased IC, the charge carriers are separated by the built-in potential between areas with different Fermi levels. Biasing an IC can increase or decrease the Fermi level difference between regions, thereby altering the magnitude of electron-hole pair separation. LIVA images are produced by monitoring the voltage changes of a constant current power supply as the optical beam from the SOM is scanned across an IC. Voltage changes occur when the electron-hole pair recombination current increases or decreases the power demands of the IC.

The LIVA measurement and imaging of voltage shifts has two advantages beyond directly observing the photocurrents or I_{DDQ}. First, the IC will act as its own current-to-voltage amplifier, producing a much larger LIVA voltage signal than photocurrent signal. This is in part due to the difference in "scale" for IC voltage and current. Fig. 6 illustrates this difference in "scale". For different illumination conditions Fig. 6 compares the increase in IC current under a constant 5 V bias (biased OBIC) with the decrease in IC voltage under constant current conditions. The supply current used maintained a 5 V bias with no illumination. Note that a 15 nA current under biased OBIC conditions produces a 300 mV voltage under LIVA conditions. Clearly the voltage signal is easier to measure (as it is in CIVA and LECIVA imaging).

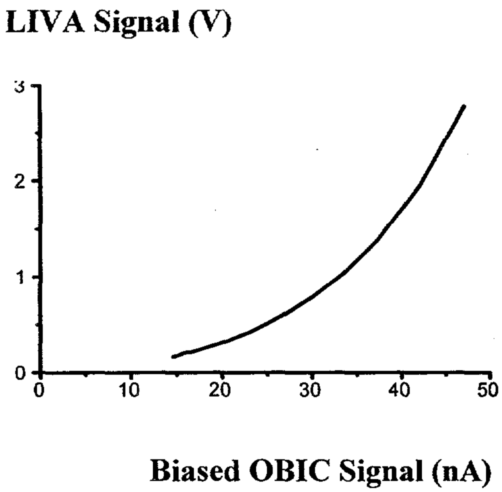

Fig. 6. A comparison of a biased OBIC signal with the LIVA signal under the same stimulus.

In addition to photon intensity, the amplitude of the LIVA signal will be dependent upon the logic state of a transistor. When a transistor is "off", there is a greater voltage between its source and drain than when the transistor is "on". This change in potential produces a difference in recombination current and in the LIVA signal.

The second advantage of the LIVA approach versus direct photocurrent observation is that IC voltages are simpler to use than IC currents. While this may not appear to be too great an advantage at first, there are several important ramifications. Direct photocurrent measurement is done in series. Most current amplification systems will have maximum current capability (typically 250 μA) that restricts the operational range without modifications. There is also the added complication of sometimes needing to measure a relatively small photocurrent against a large dc background current. Voltage measurements, on the other hand, are made in parallel, with none of the power limitations of current measurement. Small changes in voltage are easily measured using an ac coupled amplifier which is not affected by background dc voltages.

The simpler equipment setup and relatively large signal make LIVA more attractive than conventional photocurrent (OBIC) methods.

The LIVA signal generation described above considers photon interactions on nondefective ICs. Under identical illumination conditions, localized defects on ICs can generate LIVA signals 3 to 4 orders of magnitude greater than other LIVA signals from nondefective ICs. This difference in LIVA signal depends upon the defect type, but two basic mechanisms are responsible for the increase. First, the defect, because of its location in the IC amplifies the effects of normal photocurrents by altering the power demand of circuit elements connected to the defect region. Second, the defect region itself is a site of enhanced recombination compared to nondefective areas. In both cases the large increase in LIVA signals from defects facilitates rapid localization of the defective regions while scanning the entire IC die.

3.3 Backside LIVA Imaging Using IR (infrared) Illumination

The LIVA defect localization and logic state detection described in the previous section work well assuming photons can reach the junctions of interest. However, LIVA is not possible if an optically opaque layer is present that prevents photon transmission. Flip-chip packaged ICs and ICs with multilevel metal interconnection would be very difficult or impossible to examine with LIVA using a visible light source. The use of IR illumination for LIVA from a polished IC backside circumvents these problems. Backside examination of ICs has been well established and takes advantage of silicon's transparency to photons with energies less than the indirect silicon bandgap energy. Generation of LIVA signals from backside IR illumination is somewhat more difficult than reflected light IR microscopy, because the photon wavelength must be long enough to penetrate through the silicon substrate but short enough (have enough energy) to produce electron-hole pairs in the junction regions.

3.3.1 Backside IR Localization of Defects. A radiation-hardened version of the Intel 80C51 fabricated at Sandia was examined using IR LIVA. The microcontroller was made with a 1.25 μm, two-level metal, two-level polysilicon technology. Earlier failure analysis using CIVA had identified open metal-1 to silicon contacts resulting from a pellicle scratch. The contacts were completely obscured from surface optical examination by a metal-2 power bus.

Fig. 7a is a backside IR LIVA image of the entire microcontroller using the 1152 nm laser. The small LIVA signal indicated by the arrow is caused by an open metal-1 to silicon contact region. Fig. 7b is a reflected IR image showing the same field of view as 7a. Figs. 8a and 8b are backside IR LIVA and reflected IR images of the same defect site at higher magnification. The wide metal-2 bus obscuring front side observation of the contacts can be seen in Fig. 8b. Biased OBIC using 10^{10} gain and backside light emission were both attempted at the failure site identified with LIVA in Fig. 8. No anomalies were detected using either technique.

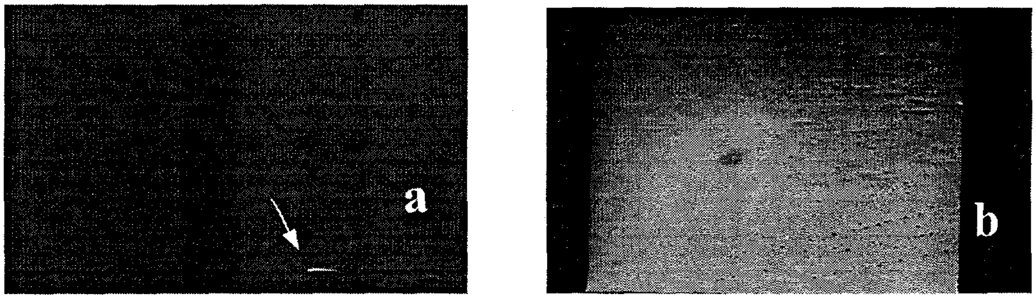

Fig. 7. (a) Backside IR LIVA and (b) reflected IR images of an IC with open contacts.

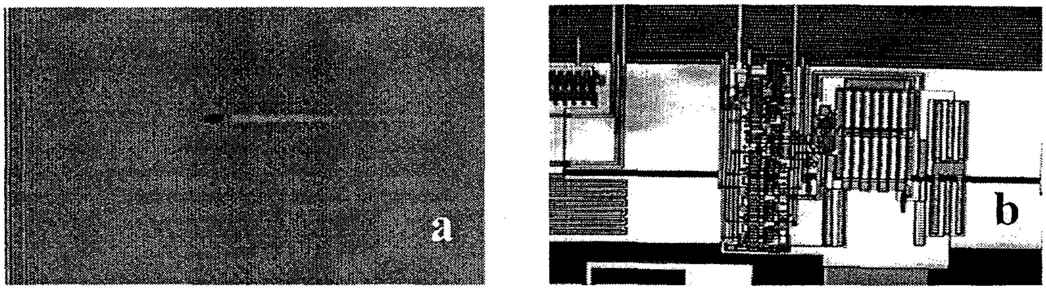

Fig. 8. Same as Fig. 7 but at higher magnification.

3.3.2 Backside IR Logic State Mapping. Even with the signal gain possible using LIVA, logic states could not be observed with the 1152 nm, 5 mW HeNe laser. The 1064 nm laser intensity is attenuated significantly more than the other IR lasers by Si, but this wavelength was recently shown to be successful in backside OBIC imaging of thinned, heavily doped silicon [11]. It was hoped that the added power of the 1.2 W laser would compensate for the increase in silicon absorption.

Fig. 9 demonstrates that the 1064 nm, 1.2 W laser was indeed successful in producing backside IR logic state maps using LIVA. In fact, the signal strength was sufficient to view logic states with the laser power reduced by a factor of 10 with a neutral density filter. Fig. 9a is a LIVA image of an I/O structure in a logical "1" state. The "off" transistors produce the dark contrast. Note that no metal masking obscures the LIVA signal from the transistor junctions as it would in surface LIVA imaging. Fig. 9b is a LIVA difference image between two logic states showing the transistors that change state when the output of the I/O structure goes from a logical "1" to a logical "0". Fig. 9c is a reflected IR image showing the same field of view as Figs. 9a and 9b.

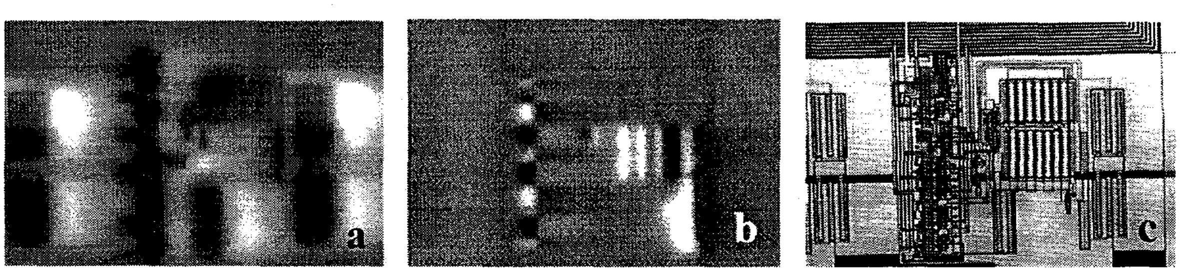

Fig. 9. Three backside IR images showing (a) a LIVA logic map of an I/O structure, (b) a LIVA difference image between a "1" and "0" state, and (c) a reflected light image for registration.

4. LECIVA

LECIVA produces images of open interconnections through interlevel dielectric and passivation layers similar to CIVA images. The main difference between the two techniques is that LECIVA is performed at low primary electron beam energies ~ 1.0 keV. LECIVA is a result of recent experimental work using high electron flux densities (high primary electron beam currents). The experiments indicate a dependence of the surface equilibrium voltage on the electron flux density at low primary beam energies. The equilibrium voltage changes from positive to negative as the electron flux density is increased. The change in surface polarity is used to produce LECIVA images.

4.1 LECIVA signal generation

4.1.1 High current, low energy secondary electron emission. The literature describing secondary electron emission at low primary electron beam energies indicates that the surface passivation of an IC reaches a positive equilibrium voltage when the beam energy is between two cross over energies, E_1 and E_2 [12]. Typical values of E_1 and E_2 for insulators are 100 ev and 3.0 keV, respectively [13]. The positive surface voltage (normally ≤ 3 V) is due to more secondary and backscattered electrons being emitted from the dielectric surface than are incident from the primary beam. The charge imbalance generates a net positive voltage that retards the escape of lower energy secondary electrons until an equilibrium between incident and escaping charge is achieved. Changes in the voltage of conductors below the passivation produce temporary changes in the surface voltage which are observed in capacitive coupling voltage contrast (CCVC) images. While the time to reach a positive equilibrium voltage is directly proportional to the incident electron beam flux density, the value of the equilibrium voltage has previously been thought to be dependent only on the primary beam energy, and therefore to be independent of the electron beam flux density [12, 13].

The positive surface voltage for electron beam energies E ($E_1 < E < E_2$) occurs because there are candidate electrons available to become secondary and backscattered electrons. Our recent experimental work has shown that at high primary electron beam currents (> 100 nA), the equilibrium surface voltage is negative at primary beam energies between E_1 and E_2. (For our experiments, only beam energies between 0.3 and 1.0 keV were examined.) The observed negative surface voltage at high beam currents is believed to be due to a depletion of available secondary electrons. More electrons are injected into the sample than can escape from the surface resulting in a negative charge imbalance. Note that the outer edge of the primary electron beam (beam spot) distribution, where the current density is lower, will still produce a positive equilibrium voltage.

The surface equilibrium voltage dependence on the incident electron flux density was probably not observed until now because the spot size of the low energy primary electron beam is relatively large (~ 0.1 μm) at currents greater than 100 nA, producing no observable CCVC decay times and poor spatial resolution images. The effect was observed at Sandia while positioning a sample for CIVA at low primary beam energy before increasing the beam energy. High currents may be required for CIVA analysis and the current was not reduced during low beam energy positioning.

4.1.2 LECIVA image acquisition. For LECIVA the primary electron beam does not directly interact with the buried IC conductors. As illustrated in Fig. 10, a positive-negative-positive surface equilibrium voltage will occur as the beam scans across the IC surface, dynamically polarizing the dielectric layer and producing a changing bound charge at the metal conductor-dielectric interface. The changing bound charge at the dielectric-conductor interface will introduce an ac voltage on the conductor. Similar to CIVA, the small ac voltage has little effect on nondefective conductors, but can change the voltage of open conductors. The change in voltage of the open conductor can alter the power demands of the IC under test. LECIVA images are produced by displaying the changing V_{DD} of the constant current supply powering the IC. As with CCVC, the thicker the dielectric layer between the conductor and the surface, the smaller the bound charge effect will be.

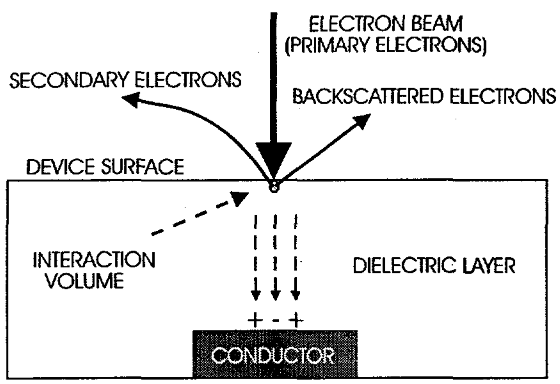

Fig. 10. For LECIVA, the electron beam interaction volume does not reach the conductor. A polarization wave produces a bound charge at the conductor-dielectric interface.

4.1.3 LECIVA operational guidelines. Depending upon the type of open conductor being examined (complete or quantum mechanical), LECIVA system parameters must be adjusted to optimize image acquisition. For both conductor types, low primary beam energies ($\leq$ 1.0 keV) and high beam currents ($\geq$ 100 nA) should be used.

ICs with open conductors that have a significant amount of quantum mechanical tunneling normally operate in a low frequency range and fail at higher frequencies. For LECIVA signal generation, the changing bound charge on the conductor induced by the changing surface equilibrium voltages must alter the voltage of the electrically floating conductor. This implies that the dynamic charge from LECIVA must be greater than the charge tunneling through the open site. One way to increase the frequency of the dynamic LECIVA charge is to use higher electron beam scan frequencies. Higher scan frequencies do produce a LECIVA signal, but defect and amplifier bandwidth limitations may make the image appear smeared. Higher spatial resolution may be achieved by slowing the electron beam scan and operating the IC at a clock frequency faster than the scan rate. At slow scan rates the power demand of the clocked IC will be different when the electron beam is scanned above the tunneling open conductor. Thus, slow scan rates that produce better spatial resolution images can be used.

The voltage of a "complete" open conductor changes almost instantly due to the dynamic bound charge in LECIVA imaging, but the recovery time (seconds) is much longer than in the tunneling open case. "Complete" open conductors are best viewed with LECIVA using an intermediate scan rate of approximately 2 image frames per second, and a supply current that maintains the IC voltage approximately 0.1 V below the compliance level.

4.1.4 LECIVA advantages and limitations. While LECIVA has the advantage over CIVA of virtually no irradiation damage [14] and has the capability of being performed on commercial electron beam test systems, there are two major limitations. First, LECIVA cannot be used to detect open conductors which are completely covered by an upper metal layer. The upper conductor will block any charging of the lower level conductor. Second, as alluded to above, the LECIVA response will be scan rate dependent. Commercial electron beam test systems usually scan only at a rapid TV rate producing a smeared LECIVA image across the field of view. Failure sites are localizable under these conditions but clear image recording of the floating conductor is difficult.

4.2 LECIVA imaging example

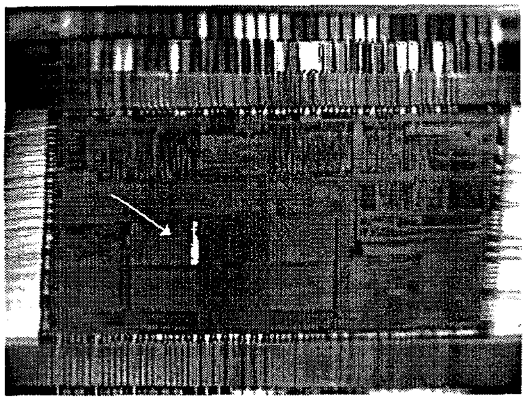

Fig. 11. Combined LECIVA and secondary electron image of a microprocessor with an open conductor.

An example of LECIVA imaging is shown in Fig. 11. The IC in Fig. 11 is a passivated 80486 microprocessor fabricated with a 0.8 μm, three-level metal technology. The primary beam conditions were 1.0 keV and approximately 150 nA. The LECIVA signal (white) has been superimposed with a secondary electron image. Fig. 11 demonstrates how the entire IC die can be examined using LECIVA. The conductor highlighted in Fig. 11 is a floating metal-2 segment with a "complete" open resulting from a defective metal-1 to metal-2 via.

5. SUMMARY

CIVA, LIVA, and LECIVA are three powerful new failure analysis techniques that take advantage of the increased sensitivity that results from operating an IC with a constant current source while monitoring the supply voltage. Each technique stimulates an IC in a different way; CIVA by direct electron injection, LIVA by photon injection, and LECIVA by a charge polarization wave. All three can provide rapid defect localization or, in the case of LIVA, logic state determination on complex ICs.

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