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Elimination of Gold Diffusion in the Heterostructure Core/Shell growth of High Performance Ge/Si Nanowire HFETs

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Abstract- **Radial heterostructure nanowires offer the possibility of surface, strain, band-edge and modulation-doped engineering for optimizing performance of nanowire transistors. Synthesis of such heterostructures is non-trivial and is typically accompanied with Au diffusion on the nanowire sidewalls that result in rough morphology and undesired whisker growth. Here, we report a novel growth procedure to synthesize Ge/Si core/multi-shell nanowires by engineering the growth interface between the Au seed and the nanowire sidewalls. Single crystal Ge/Si core/multi-shell nanowires are used to fabricate side-by-side FET transistors with and without Au diffusion. Elimination of Au diffusion in the synthesis of such structures led to ~ 2X improvement in hole field-effect mobility, transconductances and currents. Initial prototype devices with a 10 nm PECVD nitride gate dielectric resulted in a record maximum on current of 430 μA/V ($I_{DS}L_G/\pi DV_{DS}$), ~ 2X higher than ever achieved before in a p-type FET.**

I- Introduction

In addition to low dimensionality, semiconductor nanowires (NWs) offer the possibility of modulating alloy [1] and composition in the radial direction which has led to an intense interest to realize new device architectures. These novel materials and devices, however, cannot be achieved unless several obstacles currently present in the synthesis of radially engineered nanowires are resolved. At the foremost of these obstacles is Au diffusion during precursor switching for shell growth over Ge NW cores which leads to abundance of recombination traps, rough core/shell morphology, random NW kinking, and side-whisker growth. Attempting to solve this problem, previous works have used O_2 during growth [2] or ex-situ etching of the Au seed prior to growing Si shells [3]. In this contribution, we solve the Au diffusion problem in-situ and without oxygen contamination for Ge/Ge and Ge/Si core/shell NWs resulting in excellent surface morphology for all diameters. Au diffusion, which is found to be energetically favorable for smaller diameters at moderate temperatures, is solved by utilizing the catalytic effect of the liquid Au nanoparticle to deposit a thin Si barrier layer between the Ge NW and the Au growth seed. The Si interfacial layer stabilizes the Au seed atop at temperatures suitable for shell growth of both doped Ge and Si layers. We discuss the effectiveness of the Si barrier layer and the stability of the Au seed particle with time and temperature. Prototype Ge/Si core/multi-shell devices show that this growth procedure results in significant improvement of on-currents, transconductances and hole mobility. These improvements have resulted in our obtaining record high on-currents in p-type FETs.

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II- Core/Shell NW Growth

Growth of Ge NWs is typically carried out in a two-step temperature process in which the Ge NW growth is initiated near the Au-Ge eutectic temperature (~ 360 °C) and quickly ramped down to ~ 280 °C to reduce material deposition on the NW sidewalls and maintain only 1D growth mediated by the liquid Au-Ge seed particle (Fig. 1a & 1d). For core/shell NW growth, it is generally desired to stop the axial elongation of the NW and initiate vapor-solid or thin-film growth on the NW sidewalls. For this, the growth temperature has to be raised sufficiently for efficient decomposition of the precursor material used for shell deposition. This shell deposition temperature is typically well above the Au-Ge eutectic temperature, a condition that maintains a liquid Au-Ge particle atop the NW. As the temperature is ramped up, it is energetically favorable for Au from the Au-Ge alloy growth catalyst to diffuse along the NW sidewalls, leading to instability in the growth seed and Au nanoparticle decoration over the NW sidewalls (Fig. 1b & 1e). To overcome this problem, one would either need to solidify Au and etch it ex-situ [3] or change the surface energy by the introduction of O_2 [2] or dopants [4]. These techniques, however, can lead to detrimental effects during the growth process by introducing contaminants, defects, and oxidized interfaces that have direct consequences on the NW physical properties. In our work, we employed the catalytic effect of the Au nanoparticle to locally decompose SiH_4 at the Ge NW growth temperature (280 °C). This allows changing the interfacial energy difference from that of a Au-Ge alloy and a Ge NW sidewall to that of a Au-Ge-Si alloy and a Si segment sidewall which energetically favors the Au alloy to remain atop the NW. This situation is depicted in Fig. 1c and 1f in which the temperature was ramped to 410 °C after growing the Ge NW and depositing a thin Si interfacial layer where no Au diffusion occurred. This is in contrast to the NW in Fig. 1e which was subjected to the same temperature ramp, however with no Si interfacial layer

and showed Au diffusion that decorates the NW sidewall (dark contrast dots and growth seed sliding). Our energy dispersive

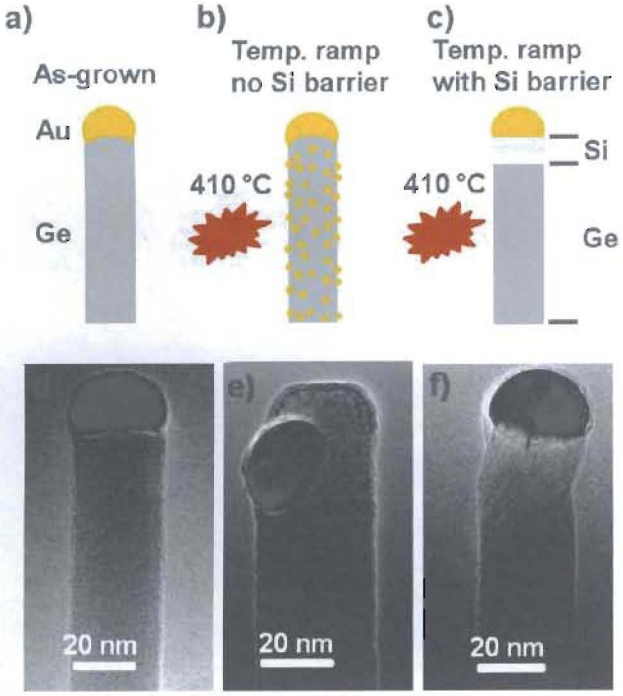

Fig. 1. a-c) Cartoon illustrating the stability of the Au nanoparticle atop a Ge NW when subjected to a temperature ramp to 410 °C without (b) and with (c) a Si interfacial barrier layer. d) TEM image of as-grown Ge NW from a 30 nm Au colloid. e-f) TEM images of a Ge NW grown from 30 nm Au colloid and subject to a temperature ramp to 410 °C showing that the Au colloid diffused over the NW surface (dark dots on NW surface and sliding over the NW sidewalls). f) TEM image of a Ge NW grown from a 30 nm Au colloid and subject to SiH_4 flow for growing an interfacial Si barrier layer underneath Au and then subject to a temperature ramp to 410 °C where no Au diffusion was observed.

X-ray analysis has verified the existence of a Si layer underneath the Au particle that helps in stabilizing it during the temperature ramp. The wires shown in Fig. 1 d-f are nucleated from a 30 nm Au colloid; similar behavior of blocking Au diffusion was also verified for NWs grown from 10, 60, and 100 nm Au colloids.

The stability of the Au NP atop the NW was found to be diameter dependent and total loss of Au was found for the smallest diameter NWs. Larger diameter NWs could also undergo total loss of Au if they were subjected to the high temperature for longer times. This situation is illustrated in Fig. 2 where a NW grown from a 30 nm Au colloid was subject to the 410 °C temperature (in-situ after growth) for 5 min (Fig. 2a-c) and another NW grown similarly but subjected to the same temperature for 10 min (Fig. 2d-g). It can be seen from Fig. 2 that the longer exposure time have led to total loss of the Au NP from the NW tip (Fig. 2g) and the spreading of the Au dots down to the NW base (Fig. 2e), whereas the shorter time caused Au to only partially spread over the top part of the NW (Fig. 1c). The diameter dependence is due to the increased chemical potential of the Au catalyst particle at very small diameters and the time dependence is controlled by the kinetics of Au release and diffusion.

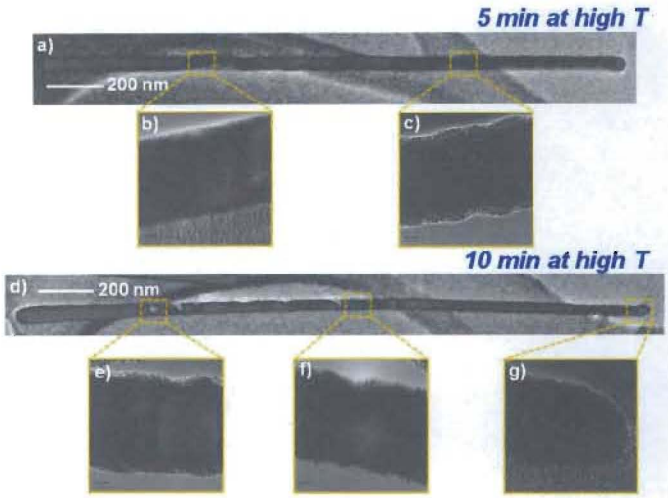

Fig. 2. a) TEM image of a Ge NW grown from a 30 nm colloid and subjected to a temperature of 410 °C for 5 min. Part of the Au colloid remained at the NW tip (dark contrast) and Au diffusion extended over ~ 700 nm in the vicinity of the NW tip (c) with no Au observed near or below the center of the NW (b). d) Same as (a) but for a NW subjected for 10 min temperature annealing where Au is spread all over the NW (e-g) and all the Au colloid volume was lost from its tip (g).

The effect of Au diffusion on the core/shell NW growth is important, given the spread of Au dots over the NW surface for NWs that do not utilize a Si interfacial barrier layer. Growth of radial Ge core/shell NWs is essential for the development of IR detectors and for optimizing the charge carrier density profile along the radius of the NW for transistor applications. Ge shells can be grown efficiently at ~ 410 °C. Fig. 3a shows a TEM image of an undoped Ge/Ge core/shell NW starting with a 30 nm Au colloid and growing the Ge shell for 2 min without a Si interfacial layer. It is evident from Fig. 3a that the Ge NW morphology becomes very rough due to the presence of the Au on the NW sidewalls that leads to local enhanced Ge deposition. This situation is similar to the observed faceting of Si NWs for long growth times under conditions that favor Au diffusion [5]. On the other hand, growth of the Ge shell after deposition the Si interfacial layer under the Au nanoparticle resulted in a very smooth interface as shown in Fig. 3b. For the same growth time and tempature, the presence of Au on the NW surface leads to an enhanced growth rate of ~ 3.75 Å/s whereas growth of the Ge shell with no presence of Au on the surface proceeds at a growth rate of ~ 2.1 Å/s further reflecting the effect of Au on catalyzing faster deposition rates. These trends in NW morphology control and elimination of Au diffusion are also observed in the growth of Ge/Si core/shell NWs as demonstrated in Fig. 3c-d. With Au diffusion, a rough

Si shell surface was observed (Fig. 3c) whereas in the case of no Au diffusion, a smooth single crystal Si shell was deposited (Fig. 3d).

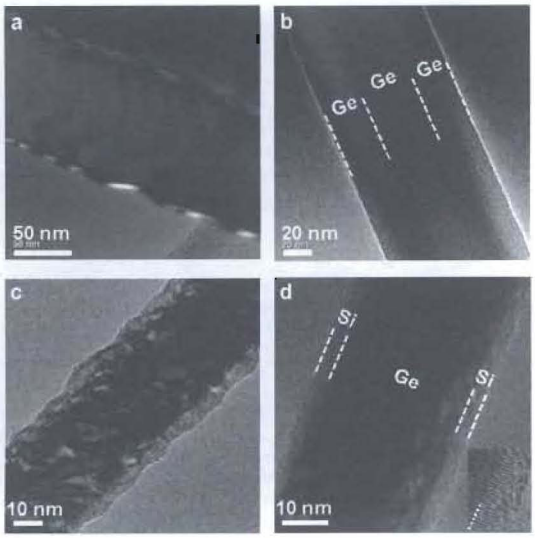

Fig. 3. TEM characterization of Ge/Ge core/shell NWs with (a) and without (b) Au diffusion and of Ge/Si core/shell NWs with (c) and without (d) Au diffusion.

III- Transport Properties of Ge/Si Core/Multi-Shell NWs

Growing Si shells on Ge NWs can help passivate the Ge surface and confine holes in a local potential well due to the valence band offsets between Ge and Si. As such, Ge/Si NWs have been previously proposed for high performance NW transistors [6]. The possibility of band-gap engineering in the radial direction and consequent charge carrier density control made possible in the present work provides an additional approach enhance the performance of Ge/Si heterostructures. For instance, an i-Ge/p^+-Ge/i-Si core/multi-shell NW heterostructure provides larger charge carrier density near the Ge/Si interface leading to a larger gate capacitance and therefore higher on-currents. This situation is illustrated in Fig. 4 a-b where a Schrödinger-Poisson self consistent solver (3D Silvaco-Atlas) has been utilized to calculate the charge carrier density profile across the radius of the NW for an i-Ge/p^+-Ge/i-Si core/multi-shell NW and for a uniformly doped p-Ge/Si core/shell NW where the integrated dopant density across the NW radius is the same in the 2 situations. Strain effects on the band structure were not included in these simulations. The simulated structure consists of a 14 nm diameter Ge core, a 2 nm Si shell, and a 2 nm Si_3N_4 gate dielectric simulated at thermal equilibrium conditions. It can be seen from Fig. 4 that for the core/multi/shell Ge/Si heterostructure, the charge carrier density is higher near the Ge/Si interface (Fig. 4b) than for the uniformly doped Ge/Si core/shell structure (Fig. 4c) which in turn leads to higher gate capacitance and higher drive currents. We have grown a core/multi-shell Ge/Si heterostructure similar to Fig. 4a in the presence or absence of Au diffusion to shed light on the effect of Au diffusion on the transport properties of these heterostructures as well as to investigate the drive-currents that can be obtained from such devices.

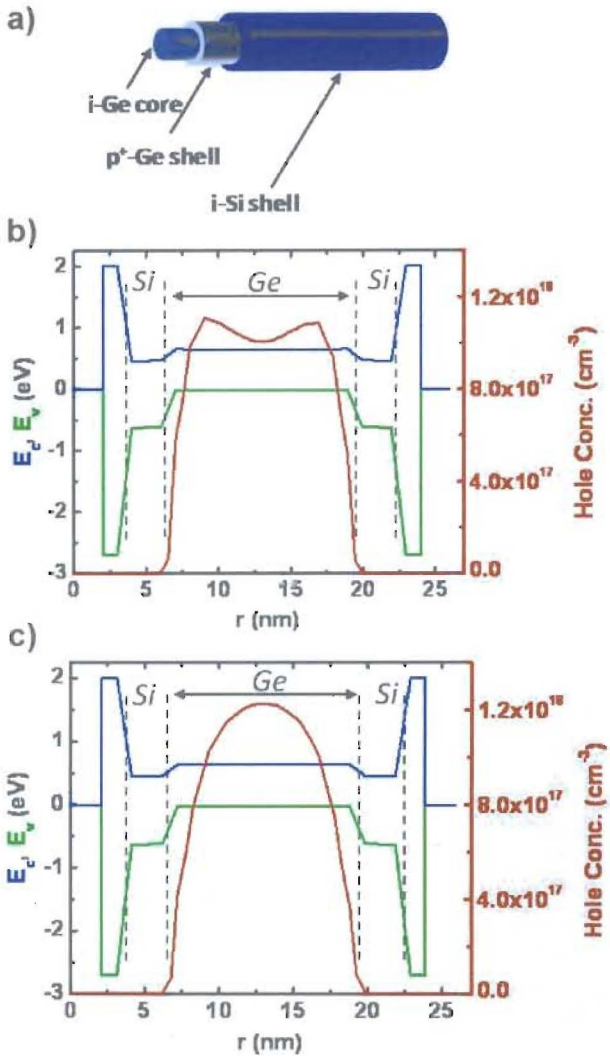

Fig. 4. a) Schematic of an i-Ge/p^+-Ge/i-Si core/multi-shell heterostructure NW used for Silvaco Atlas 3D Schrödinger-Poisson self-consistent solver. b) Band-edge diagrams (blue, green) and hole density profile (red) along the diameter of the structure in (a). c) Band-edge diagrams and hole density profile along the diameter of a uniformly doped Ge core with a total cross-sectional dopant charge density similar to that just used in the shell in (b).

The grown core/multi-shell structures were used for the fabrication of NW heterostructure field-effect transistors (HFETs). Contact electrodes were patterned using e-beam lithography and 100 nm Ni was evaporated using e-beam evaporation followed by lift-off. Plasma enhanced chemical vapor deposition (PECVD) was used to deposit 10 nm Si_3N_4 gate dielectric followed by another e-beam lithography step for patterning the gate electrode which consisted of a 100 nm/20 nm Ti/Au layer.

Fig. 5a shows typical output curves from a 500 nm channel length HFET device where the multi-shells were grown with conditions allowing Au (dashed) and no-Au (solid) diffusion.

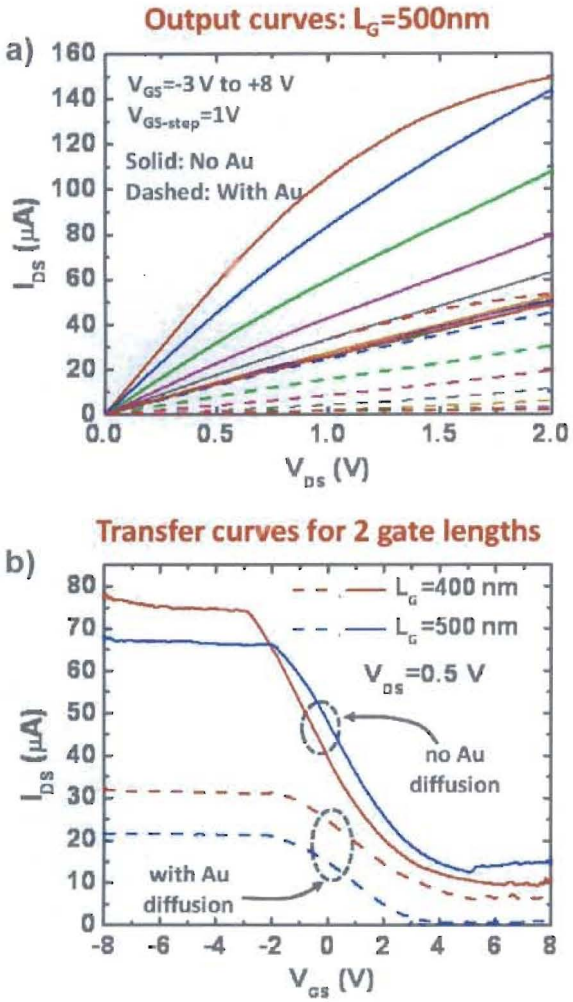

Fig. 5. a) Output curves from the same channel length Ge/Si core/multi-shell NW HFET with (dashed lines) and without (solid lines) Au diffusion. b) Transfer curves for 2 different gate lengths with and without Au diffusion.

Higher current drives are obtained in the case of no-Au diffusion. Fig. 5b shows transfer curves of the two sets of HFETs with 400 nm and 500 nm channel lengths. We can observe directly from Fig. 5b that the transconductance and the on-currents are higher for the case of no Au-diffusion. For the same V_{DS} and L_G, the transconductance is the product of the hole field-effect mobility and the gate capacitance. From TEM and SEM analysis, the gate capacitance for the 2 sets of devices is very similar indicating that the 2X lower transconductance in the case of Au diffusion is due to enhanced surface roughness scattering as expected from Fig. 3 c-d. To bench-mark the current results with earlier work on Ge/Si NW HFETs, we normalize the on-currents obtained here to the V_{DS} and channel length using $I_{max}=I_{DS}L_G/\pi DV_{DS}$. For a device channel length of 400 nm and maximum on-current of 205 μA, we obtain I_{max} of 430 μA/V compared to an earlier best result of 211 μA/V [7]. Despite using a low-k dielectric in this study, this initial result sets a record in the on-currents obtained from our engineered NW HFET devices. This approach is expected to be very promising for high-performance p-type FETs with improved sub-threshold characteristics when a high-k dielectrics are used.

IV- Conclusions

We have demonstrated the epitaxial growth of single crystal Ge/Si core/multi-shell NWs and high on-current NW HFETs using interface engineering to help eliminate Au diffusion issues during the synthesis process. A low temperature Si barrier layer was utilized to stabilize the Au growth seed during either Ge or Si shell growth. This allowed us to design and implement NW HFET devices beyond those demonstrated in earlier works. Elimination of Au diffusion has resulted in ~ 2X increases in hole field-effect mobility, transconductances, and on-currents of HFET devices and in the demonstration of a record on-current drives for a p-FET devices of 430 μA/V. Further enhancement of the device performance is expected with a high-k gate dielectric.

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