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High-Performance Computing for Airborne Applications

Heather Quinn, Andrea Manuzzato, Jeff Barton, Michael Hart, Tom Fairbanks, Nicholas Dallmann, Rose DesGeorges

Abstract— **Recently, there has been attempts to move common satellite tasks to unmanned aerial vehicles (UAVs). UAVs are significantly cheaper to buy than satellites and easier to deploy on an as-needed basis. The more benign radiation environment also allows for an aggressive adoption of state-of-the-art commercial computational devices, which increases the amount of data that can be collected. There are a number of commercial computing devices currently available that are well-suited to high-performance computing. These devices range from specialized computational devices, such as field-programmable gate arrays (FPGAs) and digital signal processors (DSPs), to traditional computing platforms, such as microprocessors. Even though the radiation environment is relatively benign, these devices could be susceptible to single-event effects. In this paper, we will present radiation data for high-performance computing devices in a accelerated neutron environment. These devices include a multi-core digital signal processor, two field-programmable gate arrays, and a microprocessor. From these results, we found that all of these devices are suitable for many airplane environments without reliability problems.**

I. Introduction

Unmanned Aerial Vehicles (UAVs) are increasingly being used for remote-sensing tasks that traditionally have been collected on spacecrafts. Since the price for these vehicles has been decreasing over the past decade, payloads on these platforms can be very cost effective. Besides being cheaper, UAVs have the advantage of being able to maneuver the sensor closer to the information target. For this reason, UAVs have been used to provide structural health monitoring of critical infrastructure [1] and disaster management [2]. UAVs also operate in more benign radiation fields, which increases the opportunity of using commercial electronics.

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The neutron environment for airplanes is very complex. Neutron flux is dependent on many factors, including the location of the airplane and the solar activity. As pointed out in [3] the neutron flux depends on latitude, longitude and altitude. Quiet solar activity can increase the flux by a factor of two to three times. As the airplane moves in relation to magnetic north, the neutron flux changes. Altitude is often the most significant factor in the neutron flux. In comparison to sea level rates of neutron radiation, the neutron flux in an airplane can be 2,000 times greater. As shown later in this paper, even the worst airplane environment is better than many space orbits.

As we are interested in high-performance airborne payloads, we studied the effect of neutron radiation on four high-performance computing devices — the Texas Instruments multi-core digital signal processor (DSP) (C6474), two Xilinx field-programmable gate arrays (FPGAs) (Virtex-6 and Spartan-6), and the Freescale PowerQUICC III Processor (MPC8548E). The feature sizes of all of these devices are sub-micron. The DSP was laid out on a 65nm process, the Virtex-6 on a 40nm process, the Spartan-6 on a 45nm process, and the PowerQUICC III on a 90nm process. All four of these devices have a significant amount of memory that could be sensitive to single-event effects.

The radiation effects on FPGAs and on FPGA user circuits has been studied on earlier devices [4]–[9]. These papers show that the configuration memory used to define the user circuit is susceptible to single-event upsets (SEUs), but that triple-modular redundancy (TMR) methods can be employed to mask the effect of SEUs in the system. In this paper, we will present results on two newly available devices.

There is a long history of studying single-event effects in microprocessors [10]–[13]. There are a number of recent publications studying more modern microprocessors [14], [15] with reduced feature sizes and multiple processing cores. Unlike FPGAs, determining the effect of radiation on DSPs and microprocessors is not as simple, as faults in the systems can remain dormant for several thousands of clock cycles before triggering an

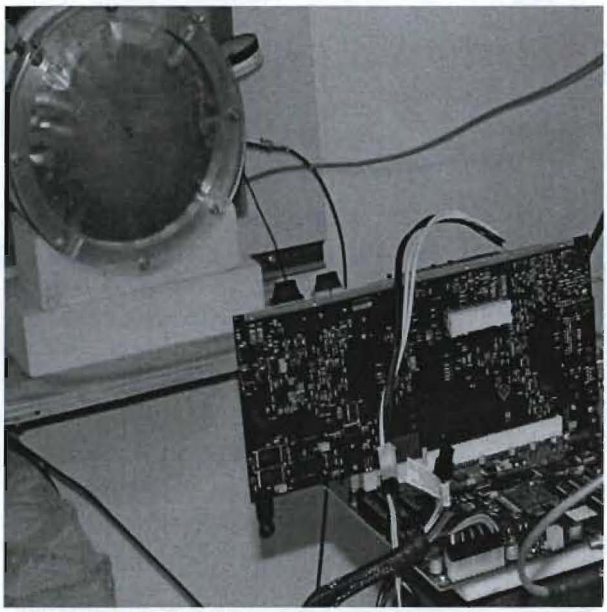

Fig. 1. PowerQUICC III at LANSCE

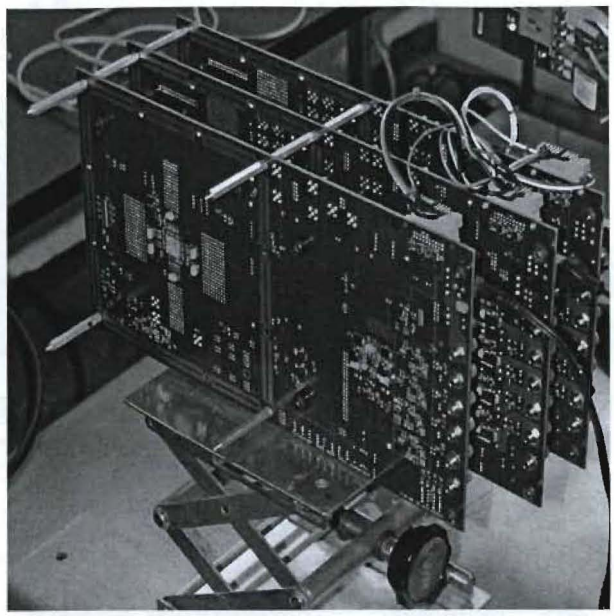

Fig. 2. Virtex-6 and Spartan-6 Harness at LANSCE

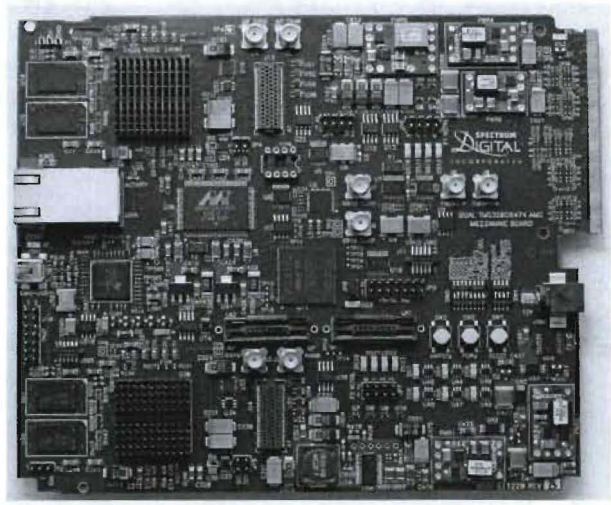

Fig. 3. C6474 Multicore DSP

error. On top of it, the operating system and the software can create noise in the system, making it hardware to determine static cross-sections. In [16] results from [10] are used to indicate the proton cross-section for the Pentium II and MMX processors was two to three orders of magnitude larger when tested with Windows operating system than without. The advantage of both the DSP and PowerQUICC III processors is that both devices can be tested without the operating system executing on the devices. Furthermore, the PowerQUICC III processor can also be tested without software executing, which makes it easier to measure the static cross-sections of the registers and the cache.

In this paper we will present a discussion of the static characterization of the four devices. Our test setups are presented in Section II. A discussion of the test results in presented in Section III.

II. Test Setup and Devices

We tested all four parts at the Los Alamos Neutron Science Center (LANSCE) neutron accelerator in July, October, and November 2009. The part numbers, board numbers, and adjusted fluence for all four parts can be found in Table I. For all of the tests we used a similar physical setup. All devices were tested at nominal temperature and voltages. For each test only the board with the part under test was in the beam area and the rest of the hardware test fixture was behind a concrete wall in the user facility. Pictures of the PowerQUICC III and the FPGAs at LANSCE are shown in Figures 1 and 2. In the remaining part of this section we will present information for the three test fixtures.

A. PowerQUICC III

A block diagram of the processor is shown in Figure 4. The e500 core processor executes at 1.33 Ghz and is a superscalar architecture with out of order execution [17]. The PowerQUICC III has 132,480 bits in register memory and 32 KB in both the L1 data and instruction cache memories. The cache and register memory spaces can be read and written to through the JTAG boundary scan port.

The PowerQUICC III board came encased in a standard computer case with a power supply. Much of the

TABLE I
TEST SPECIFICS

Part	Manufacturer	Part Number	Board Number	Number of Parts Tested	Average Adjusted Fluence Average per Part ($\frac{n}{cm^2}$)
DSP	TI	C6474	TMDXEVMC6474	1	1.94×10^{10}
Virtex-6	Xilinx	6VLX240T	AFX	2	4.94×10^{12}
Spartan-6	Xilinx	6SLX16C	AFX	1	5.38×10^{12}
PowerQUICC III	Freescale	MPC8548E	MPC8548CDS	1	3.48×10^{10}

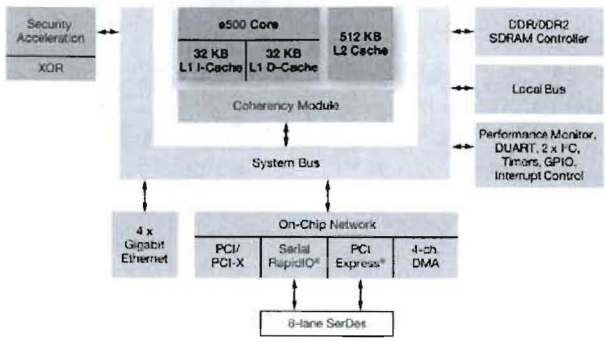

Fig. 4. Block Diagram of The PowerQUICC III Processor [17]

metal case was removed, so the beam would not have to pass through it. The board was connected to a control machine through an RS232 cable. The control machine was in the user facility and protected from radiation. By attaching the two systems together in this manner the software test fixture could be split into two pieces — the software executing on the PowerQUICC III in the beam and the software instrumentation executing on a control machine in the user facility. In this manner the PowerQUICC III can be executing software or not, and the instrumentation software should not skew the results.

The software test fixture was designed in guidance with the JPL Microprocessor standard [16]. We had two different software test fixtures for the test. One software test fixture did not execute software on the PowerQUICC III and the software instrumentation cycled between reading and reinitializing the registers and the L1 cache. The other software test fixture continuously executed the Whetstone benchmark software on the PowerQUICC III and the software instrumentation checked for incorrect output data. As the instrumentation software executed quickly, the instrumentation software performed reads and writes to the PowerQUICC III while the beam was on.

B. Virtex-6 and Spartan-6 FPGAs

Engineering samples for both the Virtex-6 and Spartan-6 device were used for the FPGA test. The devices have the same standard FPGA architecture discussed in [4]. User logic is implemented using programmable logic, programmable routing, DSP units (multiple/accumulate units), and BlockRAM (on-chip SRAM). The device is arranged in columns of programmable logic interspersed with columns of input/output blocks, clocking, DSPs, and BlockRAM.

For the Xilinx parts, AFX development boards were used to test the devices. The AFX boards were harnessed together so that all three boards could share one JTAG cable for reading from and writing to the programming data. Consequently, this setup could only read and write to one device at a time. The harness included three boards — two Virtex-6 AFX boards and one Spartan-6 AFX board. As the Virtex-6 devices had 73,859,552 bits in the bitstream, the process of checking for upsets and reinitializing all three parts took nearly thirty minutes and was done while the beam was off. In comparison, the Spartan-6 was much smaller with 3,711,248 bits in the bitstream. All of the FPGAs were executing a simple design, but the FPGAs were not checked for incorrect output data.

C. C6474 DSP

For the DSP we focused on testing the three DSP Megamodules that make up the processing aspect of the DSP, as shown in Figure 5. Each Megamodule has a fixed-point central processing unit, a parity-protected L1 cache, an error correcting code (ECC) protected L2 cache, and on-chip registers. Each DSP has 75,497,464 bits of memory in the L2 cache. It should be noted that the part also includes on-chip support for several peripherals. Many of these interfaces include memory and are likely to experience neutron-induced single-event effects, but were not tested during these initial tests.

Unlike the PowerQUICC III, the C6474 DSP did not have easy access to the register and cache space to do the traditional microprocessor test. To observe the sensitivity of the caches, we used test programs that used a large portion of the cache to store variables that were critical

TABLE II
SEU CROSS-SECTIONS WITH 95% CONFIDENCE INTERVALS FOR ALL FOUR DEVICES

Part	Bit Cross-Section ($\frac{cm^2}{bit}$)	Device Cross-Section ($\frac{cm^2}{device}$)
DSP L2 Cache	7.30×10^{-16} (4.45×10^{-16}, 1.12×10^{-15})	1.65×10^{-7} (1.01×10^{-7}, 2.54×10^{-7})
Virtex-6	$1.56 \times 10^{-16} \pm 1.31 \times 10^{-18}$	$1.15 \times 10^{-8} \pm 9.65 \times 10^{-11}$
Spartan-6	$1.52 \times 10^{-16} \pm 5.52 \times 10^{-18}$	$2.05 \times 10^{-10} \pm 2.05 \times 10^{-11}$
PowerQUICC III Registers	4.33×10^{-16} (4.33×10^{-17}, 1.56×10^{-15})	5.74×10^{-12} (5.74×10^{-12}, 5.07×10^{-10})
PowerQUICC III Caches	$8.54 \times 10^{-15} \pm 1.93 \times 10^{-15}$	$2.24 \times 10^{-9} \pm 5.07 \times 10^{-10}$

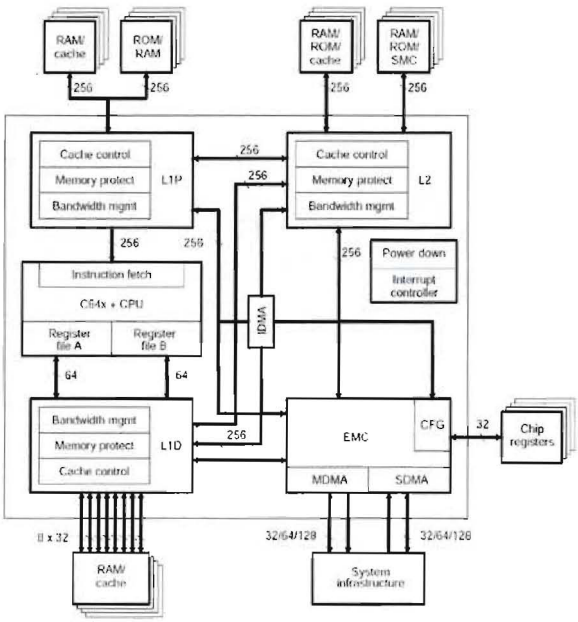

Fig. 5. Block Diagram of The C6474 Megamodule DSP [18]

TABLE III
SEFI CROSS-SECTIONS WITH 95% CONFIDENCE INTERVALS FOR ALL FOUR DEVICES

Part	Device Cross-Section ($\frac{cm^2}{device}$)
DSP	4.13×10^{-10} (1.76×10^{-10}, 8.16×10^{-10})
Virtex-6	1.01×10^{-13} (1.01×10^{-14}, 5.67×10^{-13})
Spartan-6	0 (0, 6.88×10^{-13})
PowerQUICC III	0 (0, 1.06×10^{-10})

to the computation. For these tests, we used a program for calculating Cyclic Redundancy Checks (CRC) that was optimized to use the memory for partial calculations. This code was instrumented to provide self-checking for incorrect output data. During the test the three DSP cores executed the same code using separate memory spaces, which allowed each of the DSPs to fail independently.

The C6474 DSP was attached to a host machine through the JTAG port using a USB cable. In this manner, the board could be placed in the beam area and the control machine could be placed in the user facility to reduce problems with the host machine interacting with the radiation environment. Data could be passed bidirectionally through the JTAG port, although for the sake of the test this was not done. The consequence of this decision was that the instrumentation software for the software test fixture executed on the DSP while being irradiated.

III. TEST RESULTS AND DISCUSSION

From this testing we were able to determine that all of the devices exhibited neutron-induced single-event effects. All four devices exhibited single-event upsets (SEUs) and two of the devices exhibited single-event functional interrupts (SEFIs). We will discuss these results in further detail in this section. We include a discussion of comparing the dynamic behavior between the C6474 DSP and PowerQUICC III processors and a more in-depth discussion of the Xilinx FPGAs results.

A. SEU and SEFI Cross-Sections

The bit cross-sections for SEUs listed in Table II show similarities across devices. While the Virtex-6 and Spartan-6 have nearly the same bit cross-section despite feature size differences, the bit cross-sections are also within an order of magnitude of the DSP L2 Cache and the PowerQUICC III registers. Only the PowerQUICC III cache is significantly larger at 55 times the Virtex-6 bit cross-section, despite the feature size only increasing by two times. The bit cross-sections for the Virtex-6 is 100-500 times smaller than the proton bit cross-section for the Virtex-5 device [7]. It should also be noted that since the DSP L2 Cache is ECC-protected, the SEUs seen during execution are likely only from multiple-bit upsets (MBUs) that are not corrected by ECC, which could indicate a need for better bit interleaving or a stronger code word.

The device cross-sections, though, vary widely, because the devices vary in the amount of memory in the

TABLE IV
FLUX RANGES IN $\frac{n}{cm^2-hr}$ FOR DIFFERENT LOCATIONS

Latitude	Solar Activity	Flux Ranges		
		10,000 ft	30,000 ft	60,000 ft
Equator	Active	54–66	609–806	1,776–2,533
	Quiet	57–72	667–907	2,038–3,020
45°	Active	105–141	1,604–2,723	6,362–15,016
	Quiet	121–178	1,969–3,832	8,541–24,261
Polar	Active	142	2,744	15,286
	Quiet	179	3,884	24,859

device. The two largest devices, the Virtex-6 and the DSP, have the largest device cross-sections. These results indicate that the PowerQUICC III processor is within one order of magnitude larger or smaller than some of the previous results [10]. Since the results are reported as device cross-sections, we are unable to determine whether the differences are caused by differently sized caches.

As shown in Table III, the Virtex-6 and the DSP experienced SEFIs. The SEFI mode in the Virtex-6 appeared to be a JTAG SEFI, which is similar to other Virtex devices [19], [20]. The SEFI mode in the DSP affected the use of the JTAG port and the ICEPICK [21], which allows multiple cores to be interfaced to one scan chain. The SEFI mode in the DSP is three orders of magnitude larger the Virtex-6 SEFI. It should be noted that the Virtex-6 SEFI can be cleared by reconfiguring the device, whereas the the DSP often needs to be reset or power cycled after experiencing a SEFI. System designs that do no use the DSP's JTAG port will likely be able to avoid the effects of the DSP's SEFI mode.

B. Comparing Dynamic Behavior

Unlike the FPGAs, the DSP and the PowerQUICC III processors executed software in the radiation environment. As stated previous, software can create noise in the measurement either enhancing or hiding the effect of SEUs in the system. We found that the two devices responded differently to the accelerated environment. When executing the Whetstone benchmark on the PowerQUICC III device we did not experience any execution problems. The DSP, though, exhibited a number of problems during execution, including incorrect output data or system crashes.

Part of this disparity can be explained by differences between the Whetstone benchmark software and the CRC software. The CRC software used the cache to store pre-calculated CRC tables and subroutines. Therefore, SEUs in the DSP cache often affected the output data or caused subroutines to crash. While the Whetstone benchmark includes some reads from arrays, the software's intent is measure how fast a processor can execute mathematical functions. Therefore, incorrect output data in the Whetstone benchmarks would be more likely from SETs in the processing unit or SEUs in the registers. Currently, there is no evidence that SETs affected the computation in the PowerQUICC III. In comparison the DSP caches were a much larger target in the beam than the PowerQUICC III registers.

C. Xilinx FPGAs

As the previous versions of the Virtex devices have been tested in similar environments, we would like to discuss the FPGA results in greater detail. This subsection will provide a comparison to earlier devices and to provide more in-depth analysis of the device.

When the Virtex-6 and Spartan-6 bit-cross-sections are compared to bit cross-sections listed in [4], [7], the results show a significant improvement from previous generations of devices. The bit cross-sections are on average 86 times smaller than the Virtex bit cross-section, 136 times smaller than the Virtex-II bit cross-section, 70 times smaller than the Virtex-4 bit cross-section, and 492 times smaller the the Virtex-5.

Next we looked at the difference between upsets in the configuration memory and the on-chip memory, called the BlockRAM. For the Virtex-6, the bit cross-section for the configuration memory is 4.3 times larger than the bit cross-section BlockRAM and upsets in the BlockRAM constitute 18% of all upsets on the device. For the Spartan-6 device, the configuration memory was only 2.7 times larger than the BlockRAM and upsets in the BlockRAM were 26% of all upsets on the device.

Finally, we compared the percentage of MBUs to the percentages listed in [4], [7] for the Virtex-6. The Virtex-6 experienced on average 40.86% MBUs out of all events. These results indicate a dramatic increase of MBUs from previous generations. The Virtex-5 experienced between 6–10% MBUs in protons, which indicates a four time increase in MBUs in the Virtex-6. While this increase was larger than expected, the problem is offset by the larger than expected decrease in bit cross-section from the Virtex-5. More testing will be needed to determine how the MBUs affect the user circuit on the FPGA.

D. SEU and SEFI Rates

Finally, we translated the SEU cross-sections into potential occurrence rates for airplanes. For the purpose

TABLE V

MEAN TIME TO UPSET FOR THE C6474 DSP

Latitude	Solar Activity	SEUs in Days			SEFIs in Years		
		10,000 ft	30,000 ft	60,000 ft	10,000 ft	30,000 ft	60,000 ft
Equator	Active	3,813–4,673	313–415	100–142	4,174–5,115	343–454	109–156
	Quiet	3,530–4,399	278–379	84–124	3,864–4,815	305–414	92–136
45°	Active	1,786–2,402	93–157	17–40	1,955–2,629	102–172	18–43
	Quiet	1,418–2,085	66–128	10–30	1,552–2,282	72–140	11–32
Polar	Active	1,779	92	17	1,947	101	18
	Quiet	1,407	65	10	1,540	71	11

TABLE VI

MEAN TIME TO UPSET FOR THE VIRTEX-6 FPGA

Latitude	Solar Activity	SEUs in Years			SEFIs in 1,000 Years		
		10,000 ft	30,000 ft	60,000 ft	10,000 ft	30,000 ft	60,000 ft
Equator	Active	149.9–183.7	12.3–16.3	3.9–5.6	17,068.1–20,915.1	1,401.8–1,855.5	446.1–636.5
	Quiet	138.8–172.9	10.9–14.9	3.3–4.9	15,798.9–19,690.8	1,246.4–1,694.6	374.2–554.7
45°	Active	70.2–94.4	3.6–6.2	0.7–1.6	7,993.3–10,750.0	415.1–704.5	75.3–177.7
	Quiet	55.7–82.0	2.6–5.0	0.4–1.2	6,346.9–9,333.2	294.9–574.1	46.6–132.3
Polar	Active	69.9	3.6	0.6	7,961.7	411.9	73.9
	Quiet	55.3	2.6	0.4	6,297.4	291.0	45.5

TABLE VII

MEAN TIME TO UPSET IN YEARS FOR THE SPARTAN-6 FPGA

Latitude	Solar Activity	10,000 ft	30,000 ft	60,000 ft
Equator	Active	8,409.2–10,304.5	690.7–914.2	219.8–313.6
	Quiet	7,783.8–9,701.3	614.1–834.9	184.4–273.3
45°	Active	3,938.2–5,296.3	204.5–347.1	37.1–87.5
	Quiet	3,127.0–4,598.3	145.3–282.9	23.0–65.2
Polar	Active	3,922.6	202.9	36.4
	Quiet	3,102.6	143.4	22.4

TABLE VIII

MEAN TIME TO UPSET IN YEARS FOR THE POWERQUICC III MICROPROCESSOR

Latitude	Solar Activity	10,000 ft	30,000 ft	60,000 ft
Equator	Active	767.6–940.6	63.0–83.4	20.1–28.6
	Quiet	710.5–885.6	56.1–76.2	16.8–24.9
45°	Active	359.5–483.5	18.7–31.7	3.4–8.0
	Quiet	285.4–419.8	13.3–25.8	2.1–6.0
Polar	Active	358.1	18.5	3.3
	Quiet	283.2	13.1	2.0

TABLE IX
MEAN TIME TO UPSET IN DAYS IN LEO AND GPS FOR SEUS

Solar	DSP		V6		S6		PPC	
	LEO	GPS	LEO	GPS	LEO	GPS	LEO	GPS
Active	0.40	144	1.79	648	37	13,234	360	130,140
Quiet	0.30	54	1.39	242	29	4,947	280	48,645

of illustrating SEU and SEFI rates for these devices, we have picked a few ranges of neutron flux based on three altitudes, three latitudes, four longitudes and two solar activities. To minimize the data set, we compressed the longitude variations into minimum and maximum values. These values are listed in Table IV. This table shows that there is an exponential increase in neutron flux with altitude. The table also shows that the higher altitudes are more affected by solar activity and latitude. For example, the flux at 10,000 feet varies by as much 3.3 times, whereas the flux at 60,000 feet varies by 14.0 times. The SEU and SEFI rates are shown in Table V, VI, VII, and VIII.

When comparing the devices to each other, one can see that the DSP L2 Cache's SEU rate is 74 times worse than the PowerQUICC III caches and nearly 29,000 times worse than the PowerQUICC III registers. While the bit cross-section for the DSP L2 cache is 1.7 times larger than the bit cross-section for the PowerQUICC III registers, a comparison of the two caches indicates that the bit cross-section for the DSP L2 cache is 12 times smaller than the bit cross-section for the PowerQUICC III cache. The real difference between these parts is the DSP has more memory than the PowerQUICC III device, which is reflected in the device cross-sections in Table II. In general, all of the SEU rates on sub-polar flights are very low.

We also translated the SEFI rates for the Virtex-6 and the DSP into potential SEFI rates. These numbers are reported in Tables V and VI. From these results, one can see that SEFIs will occur in the DSP in a time window of 11–156 years in the worst-case locations. For the Virtex-6, the time window is 45,466–636,488 year. Therefore, the chance a SEFI for an individual part in an airplane will be very rare.

These SEU and SEFI rates indicate that for many sub-polar flights an airplane could be flying these devices continuously between days and years without any problems. In situations where the UAV is able to maneuver into a lower altitude or away from the poles, the chance of an SEU or a SEFI will be rare. Therefore, not only are these devices well-suited for reliable computation in airborne applications, the devices will likely not even need mitigation for many applications.

For comparison sake, we were also interested in what potential space SEU rates would be. For this exercise, we used a low earth orbit (LEO) of 1,200 km with an inclination of 65.0 degrees and a global positioning system (GPS) orbit of 20,200 km with an inclination of 55.0 degrees. For both orbits most of the SEUs are from protons and not heavy ions. The SEU rates for these orbits are shown in Table IX. These results show that the SEU rate for these devices in LEO would be significantly higher than in airplane environment. For example, the SEU rates for the DSP are 33 times higher in LEO. Comparably, GPS has less proton flux that this particular LEO orbit, so the SEU rates are on the same order as the worst-case airplane environments. For the DSP the SEU rate would be 5 times lower in GPS than the worst airplane environment. While the SEU rates in LEO are higher than with the airplane environments, the rates are still reasonable, even without mitigation. With mitigation, these devices would be even more useful.

IV. CONCLUSION

In summary, we have presented results for neutron radiation testing for the Texas Instruments multi-core DSP, two Xilinx FPGAs, and the Freescale PowerQUICC III processor. These results showed that all of the devices exhibited SEUs with approximately the same bit cross-section. The Virtex-6 and DSP devices also exhibited SEFI modes. We also showed comparisons of the FPGAs to earlier generation devices, which show the devices are decreasing in bit cross-section and increasing in MBUs. Finally, we presented how the software affected in-beam execution failures. The expected SEU and SEFI rates in airplanes indicate that for many environments that these devices will not be affected by SEUs or SEFIs, making them useful for this type of work.

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