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# Survivability of Soldered Leadless Chip Carriers After Temperature Cycling

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## Abstract

*Temperature cycling evaluations were conducted on leadless chip carriers (LCCs) soldered to thick film networks (TKNs). Various temperature ranges, rates of change, cycle times, number of cycles, and sizes of LCCs were used. The TKNs were attached to metal backing plates with 63Sn/37Pb solder preforms using an infrared vacuum soldering process. The LCCs were attached to Pt/Au TKNs with 63Sn/37Pb solder paste using a belt reflow process. Visual examination and cross-sectional analysis were used to evaluate the survivability. Results were also correlated with finite elemental analysis. Considering the initial results, possible solutions included changing the solder from 63Sn/37Pb to 50Pb/50In, deleting the metal backplate, changing the rate of change in the temperature cycle, and/or adding leads to the large LCCs. Because of a system requirement, the rate of change in the temperature cycle could not be changed. Since there was no long term reliability information on the Pt/Au TKN with 50Pb/50In solder, this option was also dropped. Additional evaluations showed little difference in the survivability of large LCC solder joints with or without the metal backing plate. The only solution left, and one that worked very well, was to add compliant leads to the large LCCs. The final results indicated that LCCs beyond a certain physical size required compliant leads to survive the temperature cycle requirements.*

Key words: LCC, temperature cycle, J-lead

## Introduction

It has been noted for several years that a major concern in using leadless chip carriers (LCCs) was the limitation of the LCC solder joint when exposed to severe temperature cycles<sup>[1]</sup>. In addition, the trend has been towards larger LCCs as chips become larger and more dense<sup>[2]</sup>. It has also been stated that thermal cycling is an acceptable procedure for conducting reliability testing under accelerated conditions<sup>[3]</sup> and any accelerated test should be designed, as much as possible, on expected field conditions<sup>[4]</sup>. This paper describes the background and a solution to cracking solder joints on large LCCs when they have been exposed to an accelerated temperature cycle which is designed around system requirements.

## Background

For a military application, a hybrid microcircuit (HMC) which performed logic functions was required. The design required that a 68 pin ceramic leadless chip carrier (LCC) of size .950 inch x .950 inch x .095 inch along with smaller LCCs, chip components, and packaged active devices be soldered to a thick film network (TKN) of size 3.400 inches x 2.500 inches x .040 inch using 63Sn/37Pb solder. The TKN was initially soldered to a Kovar backing plate of size 3.400 inches x 2.100 inches x .040 inch also using 63Sn/37Pb solder. The assembled HMC, besides seeing an in-process temperature cycle and electrical testing across temperature, was required to withstand an accelerated system temperature cycle. The in-process temperature cycle consisted of 6 cycles (approximately 92 minutes per cycle) with extremes at -55°C and +100°C, no dwell at the extremes, and a rate of change of approximately 3.3°C per minute.

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Temperature testing was performed at -55°C, +25°C, and +90°C. The accelerated system temperature cycle consisted of 250 cycles (approximately 124 minutes per cycle) with extremes at -55°C and +72°C, a minimum of 30 minutes dwell at the extremes, and a rate of change of 4°C per minute.

Electrical failures occurred after as few as 50 accelerated system temperature cycles with cracks in the solder joint-Pt/Au interface, but only on the 68 pin LCC. Believing that the design layout may have led to a small percentage of single print Pt/Au in the solder areas, the solder pads were triple printed with Pt/Au. (The original solder pads were double printed.) The revised layout was subjected to all of the previous tests and cycles. This time cracks, which occurred in the solder joint, were detected visually as early as the 24th accelerated system temperature cycle. Again, the cracks only occurred on the 68 pin LCC. All other soldered LCCs and chip components showed no evidence of cracking.

Investigations were launched to determine the root cause(s) of the cracking and to develop a solution that could be incorporated very quickly in order to meet production schedules.

Two theories for the cracking were proposed: 1) a thermal mismatch between the Kovar backplate and the TKN ceramic, and/or 2) a mismatch between the large LCC and the TKN ceramic. Possible solutions included changing the solder from 63Sn/37Pb to 50Pb/50In, deleting the Kovar backplate, changing the rate of change in the temperature cycle, and/or adding leads to the large LCC.

A limited evaluation did indicate that the softer 50Pb/50In solder would eliminate the solder cracking. However, this solution was not further pursued because there were no long term studies on the compatibility of Pt/Au and 50/50 lead/indium solder available, and the time constraints of production schedules would not allow the time to characterize this compatibility.

The rate of change of the accelerated system temperature cycle could not be changed because of next assembly system requirements.

Therefore, the only two options remaining were removing the Kovar backplate and/or adding leads to the large LCC.

## Backplate and FEM analyses

The HMC configuration displaying premature failures with the LCC solder joints is shown in Figure 1. The system requirement is to

survive at least 250 cycles with no visual detection (<30X) of solder joint cracking or electrical open. To evaluate an assembly development failure, a test matrix of 18 test HMCs was assembled with triple print metalization and exposed to a number (1X to 6X) of solder reflows. Multiple reflows of the solder was done to window the worst case processing environment. All parts had their solder pads, via test components, electrically daisy chained to have continuous electrical continuity monitor during the temperature cycles. The HMCs were inspected visually every 25 cycles for the first 100 cycles and 50 cycles, thereafter.

The first failure occurred on the 24th cycle as an electrical open, and 5 more units failed below 100 cycles. The failure was always on the 68 pin LCC, and the open connection was predominantly on the corner pins (pins 9, 10, 26, 27, 43, 44, 60, and 61). The test results for the 68 pin LCC are shown in Figure 2. The data clearly shows the highest rate of solder joint failure on the corner pins of the LCC.

A finite element model (FEM) was constructed for the HMC assembly to predict the mechanical forces developed on each of the LCC solder connections. The material properties for the 63Sn/37Pb solder, 96% alumina TKN ceramic, 90% alumina LCC package and Kovar backplate are given in Figures 3 and 4. Two inputs, +25°C to +72°C and +25°C to -55°C, were used to profile the temperature cycling. All segments of the physical design were modeled as simple rectangular beams including the solder connections. The size of each beam (TKN, LCCs, backplate) was the size of the HMC design. The size of the LCC solder joints was 0.005 inch x 0.010 inch x 0.015 inch. All of the structures in the analysis were allowed to deform. The x, y, z, forces on the solder connections were calculated. Figures 5 and 6 graphically plot the resultant forces.

The FEM analysis showed that the forces on the solder connections occur primarily on the corner pins of the LCC packages, and the maximum forces occur on the corner pins of the larger LCC components. The direction of the forces twist and shear the opposing corners of the LCC when the thermal input varies from heat up (+25°C to +72°C) to cool down (+25°C to -55°C). This rocking action of the force enhances the joint failure.

The FEM analysis failed to validate a laboratory experiment that the removal of the Kovar backplate would not eliminate the solder cracking on the 68 pin LCC.

The empirical learned results of the laboratory experiment and FEM analysis are that the physical layout of the HMC (ceramic, component, and Kovar backplate) and the overall size of the components play an important role in the survivability of a LCC on an HMC.

## Leaded LCC evaluation

A quick and limited number of HMCs (4) were assembled with large LCCs which had leads soldered to the package (Figure 7). The leads were compliant J-leads on 0.050 inch centers manufactured for surface mount applications (Figure 8). Lead compliance has been found to be a critical parameter in optimizing the reliability of leaded surface mount components<sup>[5]</sup>. The 4 HMCs were subjected to the 250 accelerated system temperature cycles. After 250 cycles, there were no indications of any cracks in the solder joint as previously observed on non-leaded large LCCs. At this time, it was decided to incorporate J-leads on the large LCCs on process prove-in material and run a larger number of evaluation parts to validate the initial experiment. The larger evaluation consisted of 20 HMCs assembled with J-leaded large LCCs and 4 HMCs assembled with non-leaded large LCCs, to be used as a control sample. The pads of the LCCs were wire bonded in series inside the package so the LCCs could be monitored for electrical opens.

After 250 cycles, the non-leaded large LCCs visually had a great number of cracks in the solder joint, but no electrical opens. The leaded large LCCs also had no electrical opens, but they also had no visible evidence of any cracks in the solder joints. To have some idea what kind of margin either of these two groups of HMCs have to the 250 cycles, the two groups of parts were subjected to an additional 450 cycles. After 700 temperature cycles, the majority of the LCCs without J-leads exhibited some solder cracking. The J-leaded LCC solder joints did not exhibit any cracks in the solder. One electrical failure did occur at 600 cycles on a 20 pin non-leaded LCC.

## Conclusions

The following conclusions were reached from the evaluations and analyses performed:

- 1) A softer solder, such as 50/50 lead/indium, can eliminate solder cracking on large non-leaded LCCs.

- 2) Elimination of the Kovar backplate did not eliminate solder cracking on large non-leaded LCCs.
- 3) Incorporation of J-leads on large LCCs eliminated solder cracking.
- 4) For the specific system requirement, LCCs of size .460 inch x .560 inch x .102 inch and smaller did not require leads to survive.

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<sup>[1]</sup> R. N. Wild, "Some Factors Affecting Leadless Chip Carrier Solder Joint Fatigue Life II," *Circuit World*, Vol. 14, No. 4, pp. 29-41 (1988)

<sup>[2]</sup> J. Sauber and J. Seyyedi, "Predicting Thermal Fatigue Lifetimes for SMT Solder Joints," *Transactions ASME Journal of Electronic Packaging*, Vol. 114, pp. 473-476 (Dec 1992)

<sup>[3]</sup> J. P. Clech and J. A. Augis, "Engineering Analysis of Thermal Cycling Accelerated Tests for Surface-Mount Attachment Reliability Evaluation," in *Proceedings 7th IEPS*, pp. 385-410 (1987)

<sup>[4]</sup> R. Darveaux, "Crack Initiation and Growth in Surface Mount Solder Joints," in *1993 Proceedings, International Symposium on Microelectronics*, pp. 86-89 (1993)

<sup>[5]</sup> R. W. Kotlowitz and L. R. Taylor, "Compliance Metrics for the Inclined Gull-Wing, Spider J-Bend, and Spider Gull-Wing Lead Designs for Surface Mount Components," in *Proceedings IEEE 41st ECTC*, pp. 299-303 (1991)

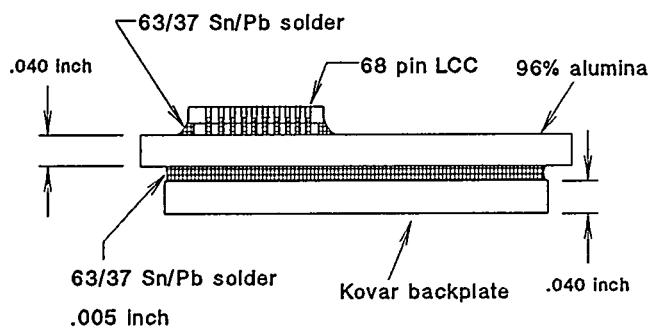


Figure 1. Cross-section of HMC assembly with non-leaded LCC

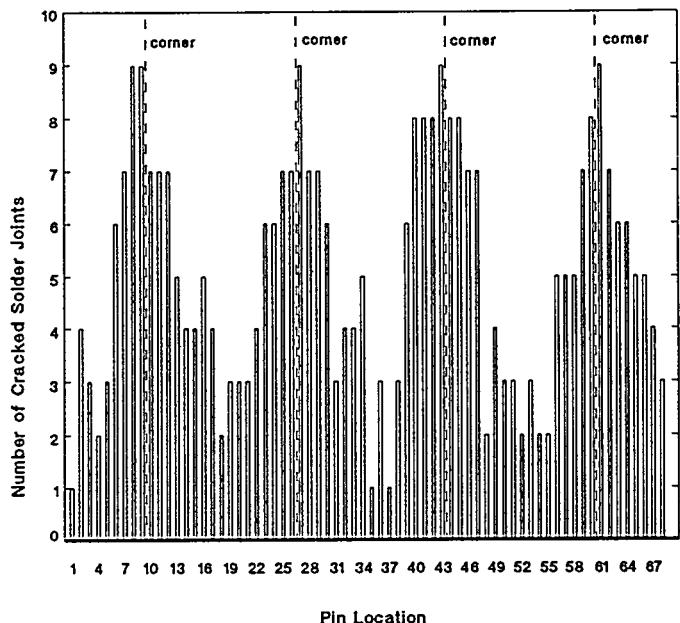


Figure 2. Histogram of solder joint failures on non-leaded 68 pin LCC by pin location

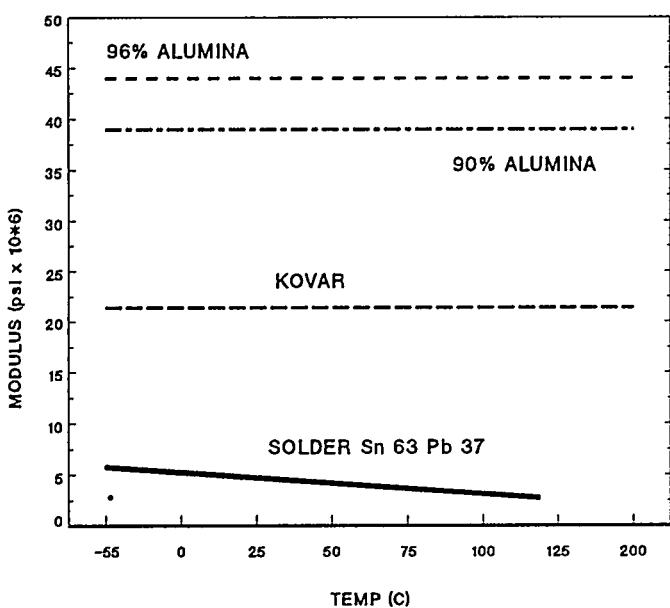


Figure 3. Modulus of Elasticity vs. Temp

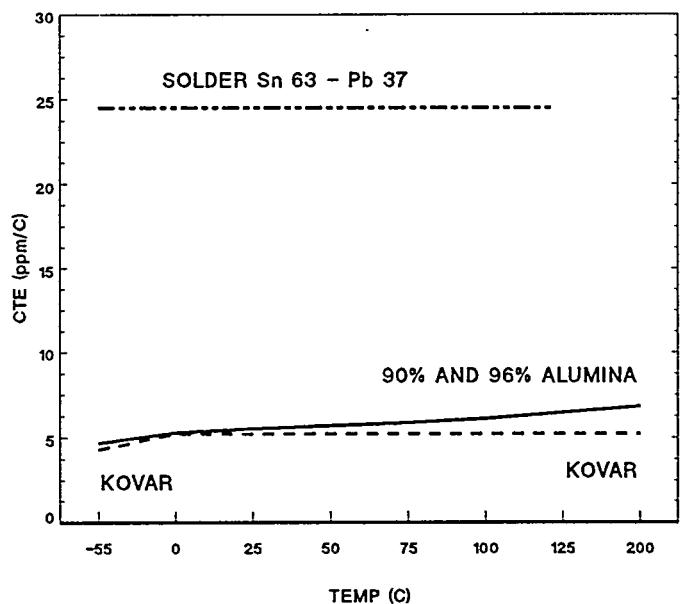
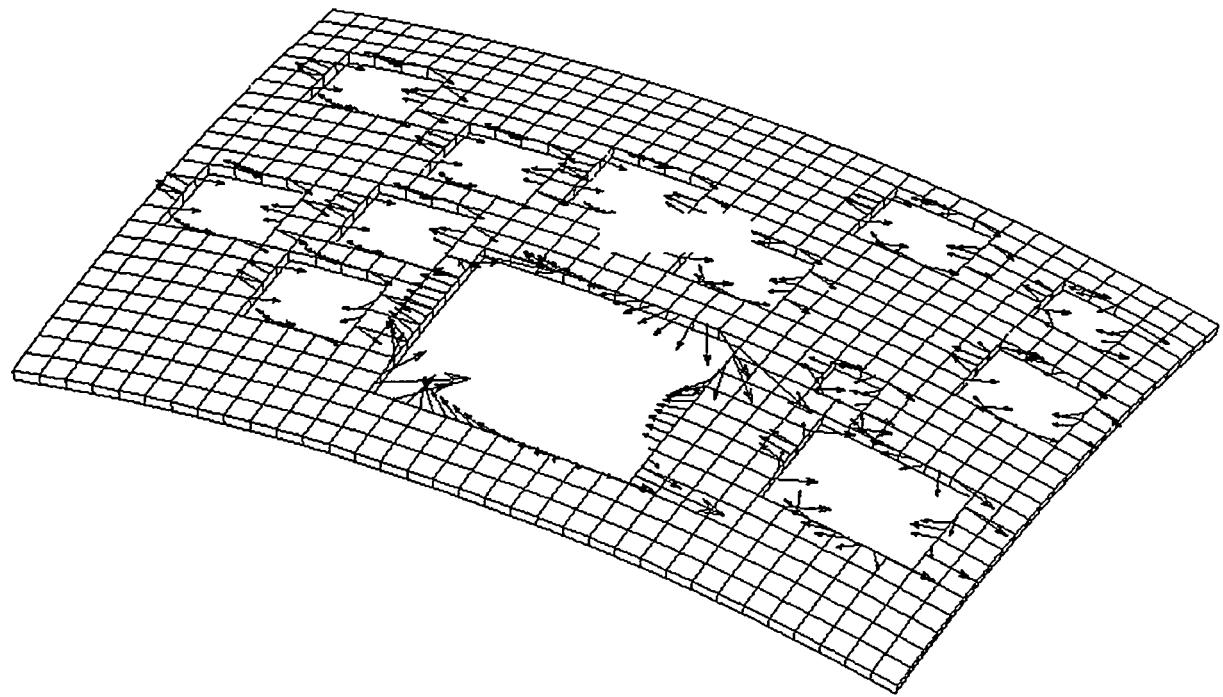
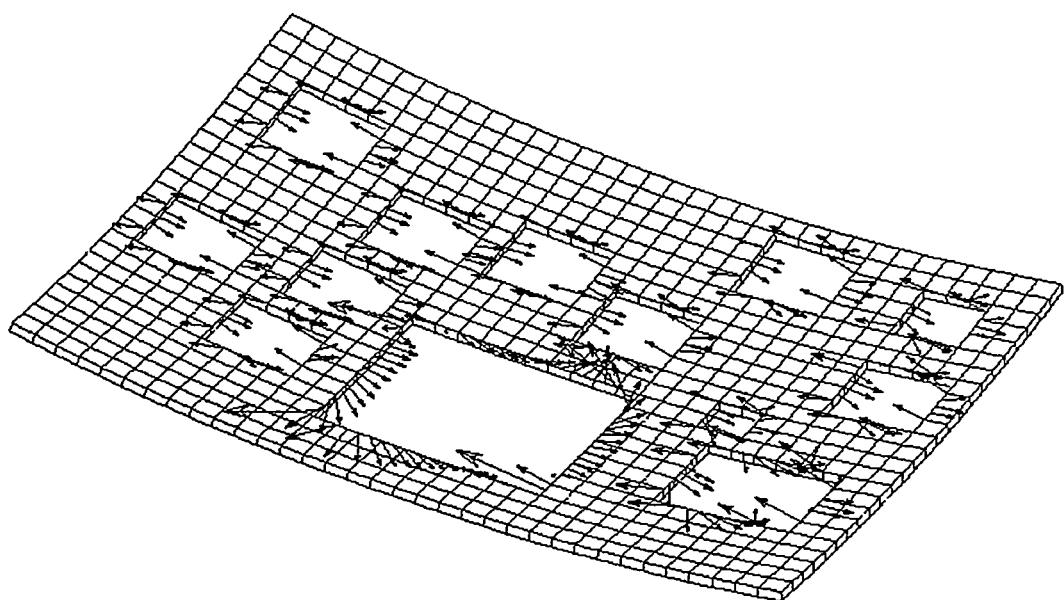


Figure 4. Coefficient of expansion vs. Temp



**Figure 5.** Resultant mechanical forces at  $+72^{\circ}\text{C}$



**Figure 6.** Resultant mechanical forces at  $-55^{\circ}\text{C}$

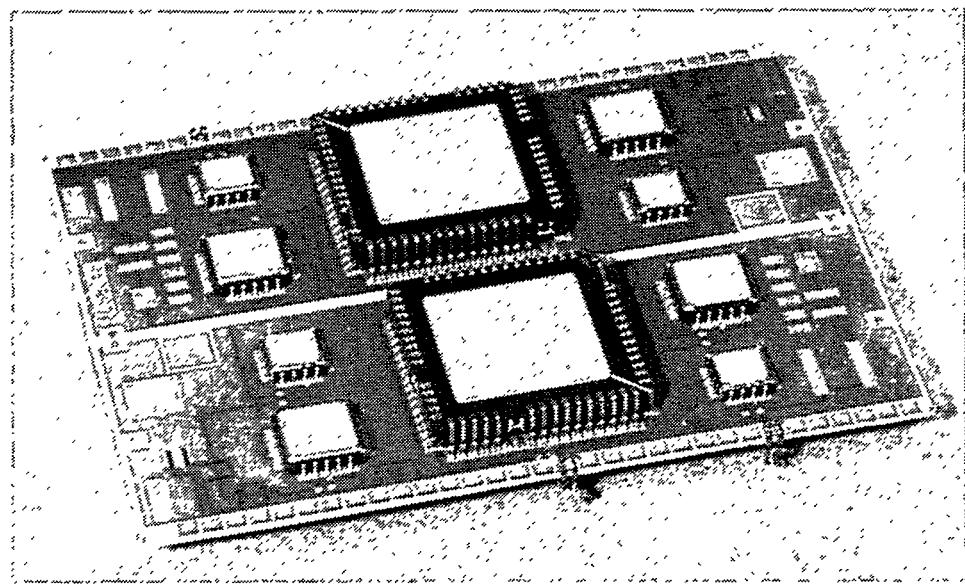


Figure 7. Evaluation HMC with leaded and nonleaded LCCs

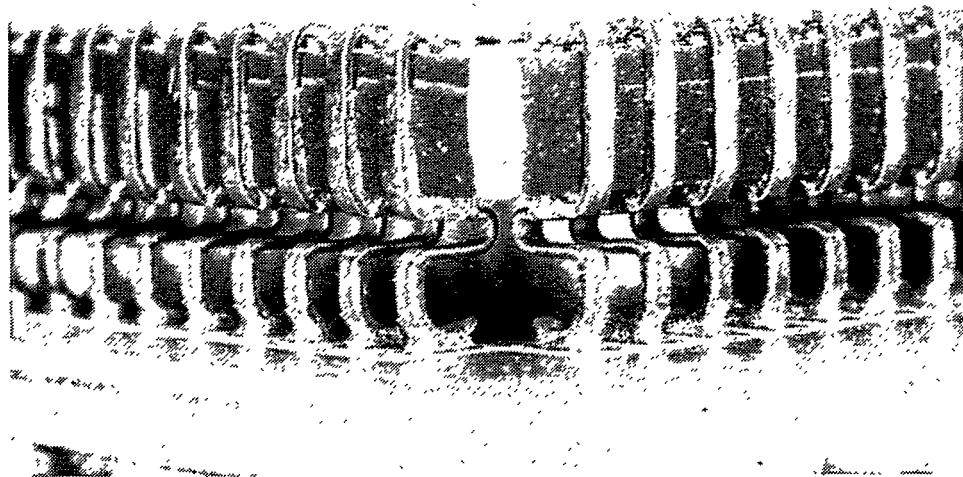


Figure 8. Leaded 68-pin LCC