COMPLEMENTARY GaAs JUNCTION-GATED HETEROSTRUCTURE FIELD EFFECT TRANSISTOR FABRICATION FOR INTEGRATED CIRCUITS

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A new GaAs junction-gated complementary logic technology that integrates a modulation doped p-channel heterostructure field effect transistor (pHFET) and a fully ion implanted n-channel JFET has recently been fabricated. High-speed, low-power operation has been demonstrated with loaded ring oscillators that show gate delays of 179 ps/stage for a power-delay product of 28 fJ at 1.2 V operation and 320 ps/stage and 8.9 fJ at 0.8 V operation. The principal advantages of this technology include the ability to independently set the threshold voltage of n- and p-channel devices and to independently design the pHFET for high performance. A self-aligned refractory gate process based on tungsten and tungsten silicide gate metal has been used to fabricate the FETs. Novel aspects of the fabrication include the simultaneous formation of non-alloyed, refractory ohmic contacts for the junction gates and the formation of shallow p-n junctions by ion implantation.

INTRODUCTION

GaAs complementary logic offers the potential for greatly reducing the power consumption of digital integrated circuits while maintaining speeds between those of conventional digital GaAs and Si CMOS. This can be especially important for integrating high-speed analog or microwave circuitry based on GaAs with low power digital electronics. While a number of approaches have been proposed for GaAs complementary logic [1-6], new approaches are worthwhile if they offer the potential for improved speed or reduced power consumption. In the present work, a new GaAs complementary logic technology is described and basic complementary integrated circuits are demonstrated. This technology extends the operation of the circuits below 1 V power supplies while maintaining good noise margins.

TECHNOLOGY DESCRIPTION

This new GaAs complementary logic technology integrates a modulation doped, junction-gated, p-channel heterostructure field effect transistor (pHFET) and a fully ion implanted n-channel JFET [7], as illustrated in Fig. 1. This approach permits the independent optimization of the p- and n-channel devices, including the ability to independently set threshold voltages. A weak link in GaAs complementary technology is the poor performance of the pFET relative to the nFET. Although modulation doping may make sense for pHFETs, this type of design has been little explored in other complementary technologies due to the competing p-channel and n-channel requirements in

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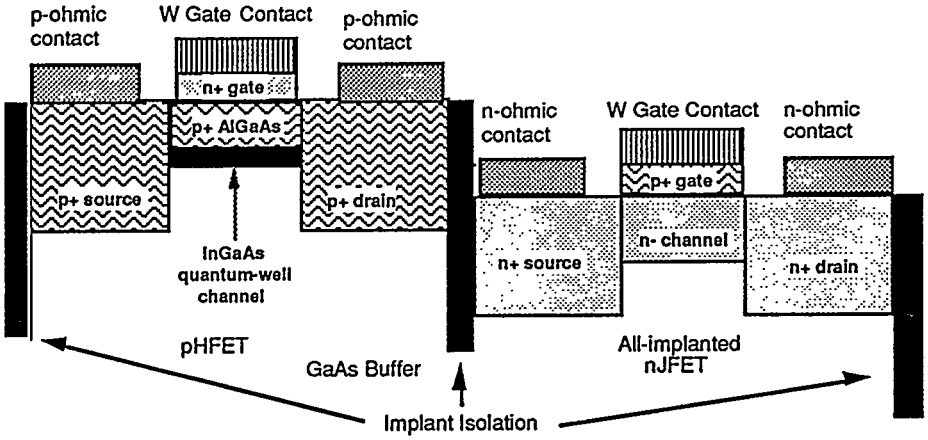

Figure 1. Schematic device cross sections of the complementary nJFET and pHFET devices. These devices are independently optimizable.

the common epitaxial layers [3]. In our approach, epitaxial doping, material composition, and layer design can all be varied to optimize the p-channel device, since none of these layers will be shared with the n-channel device. Thus, this weak link in III-V complementary technology can be addressed independently without affecting the n-channel device. A drawback of this approach is that n-channel performance will be sacrificed relative to n-channel HFET designs, but this may turn out to be a small factor compared to potential improvements in the pHFET.

The all GaAs n-channel device was chosen to be a self-aligned n-channel JFET [8,9] fabricated in the GaAs buffer of an epitaxially grown substrate for the following reasons. A JFET allows operation with low gate leakage up to 1 V, which is important in minimizing static power. In addition to the usual benefits of self-aligned processing, the self-aligned refractory JFET also offers important advantages over a conventional JFET as illustrated in Fig. 2. The conventional JFET suffers excess gate capacitance from metal

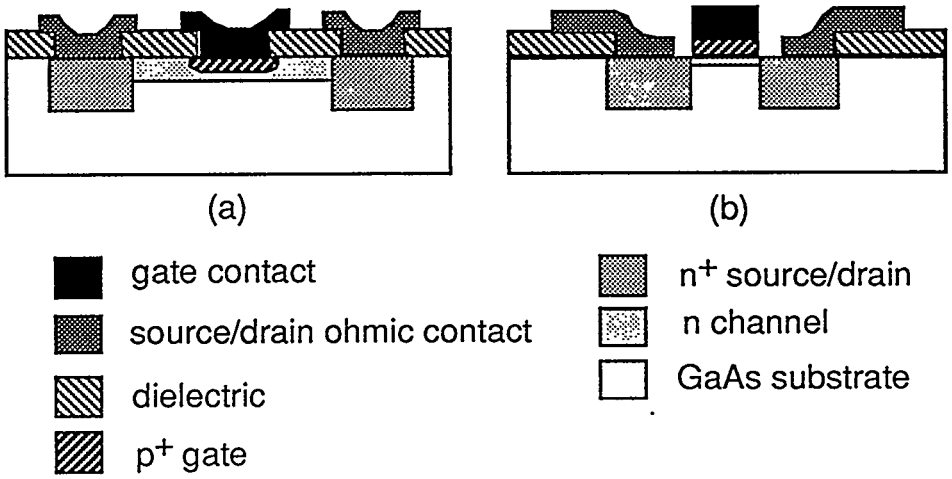

Figure 2. A comparison of self-aligned (a) and non self-aligned (b) JFETs. The self-aligned JFET results in reduced parasitic gate capacitance.

overhang as well as junction broadening. This typically leads to a rf-performance penalty in the conventional JFET compared to MESFETs of the same gate length. The self-aligned JFET with a coincident or slightly undercut junction gate region achieves comparable rf performance to a MESFET of the same gate length with the added advantage of a higher gate turn-on voltage [9].

Although the present design limits low static power operation to power supply voltages below 1V, low supply voltages are a big advantage for reducing dynamic power. The dynamic power is represented by $P_d = C_L(V_{DD})^2 f$, where P_d is the dynamic power, C_L is the load capacitance, V_{DD} is the power supply voltage, and f is the frequency. This relationship is the driving force for silicon CMOS technology aggressively reducing the power supply voltage to address high frequency portable electronics applications. For circuit operation below 1 V, GaAs-based devices should have an intrinsic advantage of higher speed at a given dynamic power consumption due to better current drive capability.

FABRICATION

The junction gate pHFETs are based on a modulation-doped AlGaAs/InGaAs/GaAs strained quantum-well material with 35% AlAs and 18% InAs grown by molecular beam epitaxy. The 100 Å InGaAs quantum well is designed to be thermodynamically stable to remain dislocation free during the high temperature processing. In the present design modulation doping on both sides of the quantum well is employed. A self-aligned refractory gate process based on tungsten or tungsten silicide gate metal is used to fabricate the complementary circuits. A 13 mask process begins with pHFET active area definition by wet chemical etching. Next, all of the nJFET active area implants (gate, channel, and backside) are performed together [9], followed by another photolighography step and a thermally stable isolation implant based on oxygen ions [10]. Gate definition follows with tungsten or tungsten silicide refractory gate deposition, patterning, and reactive ion etch in SF_6:Ar. Before the next photolithography step, a wet etch is used to remove the heavily-doped junction-gate semiconductor regions. This shallow wet etch defines the gate active region. The source and drains are then patterned and implanted, first with Si for the n^+ regions and then with Zn for the p^+ regions. A capless rapid thermal anneal with two GaAs wafers placed in proximity inside a SiC-coated graphite susceptor follows. The ohmic contacts are then formed with p-ohmic metal definition and alloy using AuBe and then n-ohmic metal definition and alloy using GeAuNiAu. A 2-level interconnect process then follows, based on silicon nitride dielectric and TiPtAu interconnect metal. Finally, circuit processing is completed with dielectric passivation. The devices and circuits are tested in wafer form. The minimum features are nominally 3 μm lines, 2 μm spaces, 1.0 μm gates, and 1.5 μm vias. The actual gate length was 0.7 μm as measured by scanning electron microscopy.

One novel aspect of this work is that a single refractory metallization has been used to define both the p- and n-FET gates. The electrical gates of the devices are defined by the p-n (n-p) junctions and the metal contact can be chosen for other properties. Choosing a refractory metal allows for self-aligned implants to dope the source and drain regions with the refractory metal acting as an implant mask for the channel regions and a non-reactive contact for the subsequent implant activation. This self-aligned process results in lower source resistances because of the self-aligned implant of the source n+ (p+) region to the gate. The refractory metal contacts transmit the electrical potential to the junction gates, which modulate the channel. Simulations of the metal to semiconductor contact show that the built-in voltage of the p-n junction is preserved if the metal-semiconductor contact is

ohmic and barrier lowering is encountered if the contact is Schottky. Figure 3 illustrates this point with a solution of the one-dimensional Poisson equation using FISH1D 2.2 [11] for a Schottky (assumed barrier height of 0.5 V) or ohmic contact. The potentially conflicting requirement of ohmic contacts for the high built-in voltage and refractory (non-reactive) metal for the self-aligned implant is resolved by fabricating non-alloyed, refractory metal contacts simultaneously to both gates.

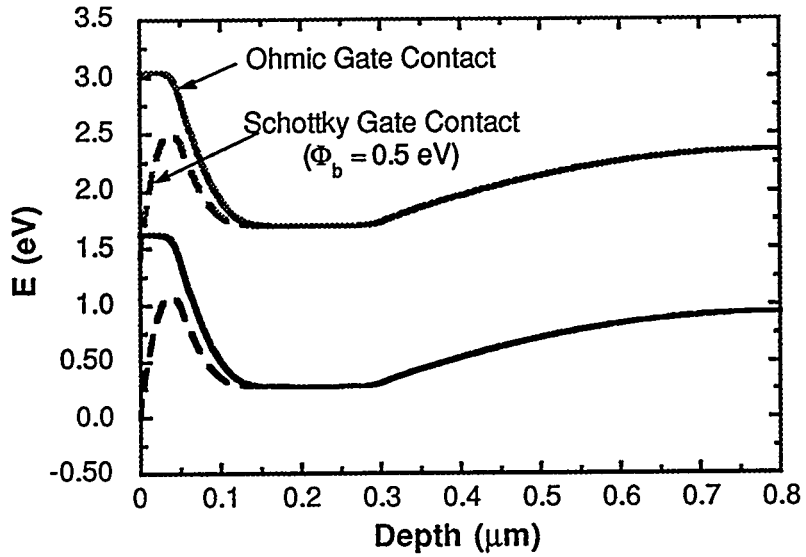

Figure 3. Plot of the calculated band diagram for an n-channel JFET with either a Schottky (assumed barrier height of 0.5 eV) or an ohmic gate contact. The plot is the solution to the 1-dimensional Poisson equation using FISH1D 2.2 [11] for a Schottky (assumed barrier height of 0.5 V) or ohmic contact.

For the pHFET, the ohmic gate electrode was achieved by employing a low bandgap n+ InGaAs contact layer at the surface of the epitaxial growth as has been done for refractory emitter contacts to heterostructure bipolar transistors [12]. The nJFET ohmic gate was first achieved by heavily doping the surface of the GaAs p+ with a shallow Mg implant so that a non-alloyed tunneling contact is achieved [8] and then later with a shallow Zn implant [9, 13]. Although Zn has been considered to be a fast diffuser, it was shown to diffuse little under conditions of heavy implant damage (creating abundant substitutional sites) and short anneal times [13]. nJFETs fabricated with shallow Zn and Mg implants for the p^+ gate have shown a clear advantage for the Zn-implanted JFETs with approximately 70% improvement in dc and microwave performance parameters [13].

DEVICE RESULTS

DC transfer characteristics are shown for both devices in Figs. 4-7. The nJFET shows a maximum transconductance (g_m) of 230 mS/mm and maximum drain current (I_{DS}) of 200 mS/mm. At a 1.0 V gate and drain bias typical of circuit operation, the g_m and I_{DS}

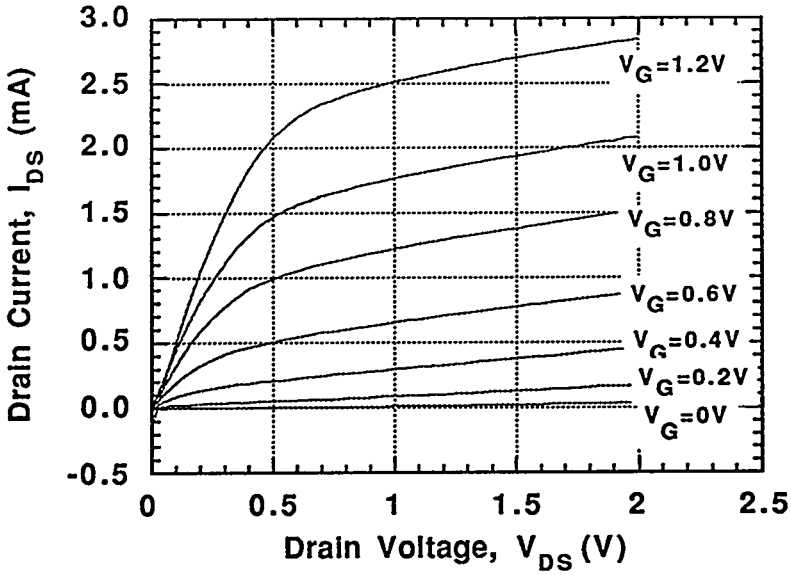

Figure 4. I_{DS}-V_{DS} for a self-aligned 0.7x20 μm nJFET.

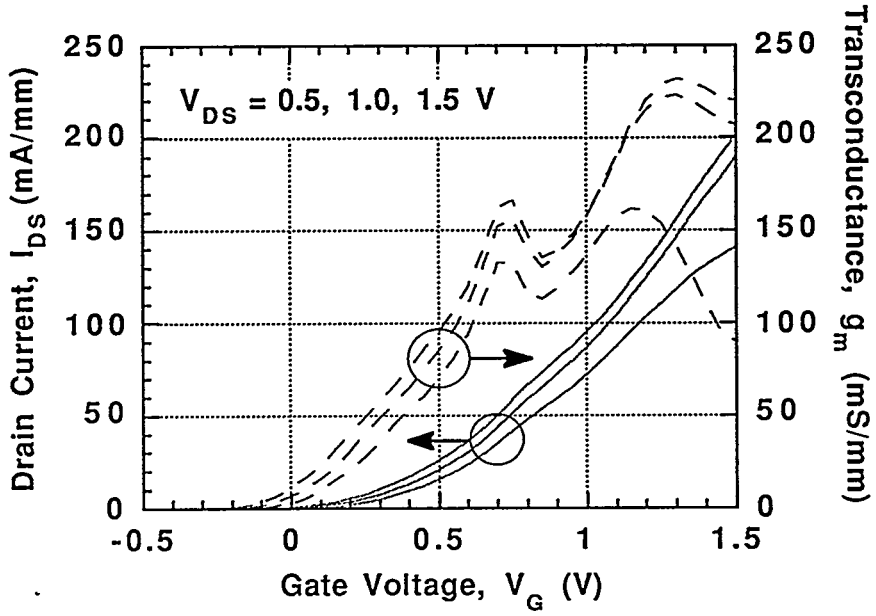

Figure 5. I_{DS}-V_G and g_m-V_G at drain biases of 0.5, 1.0, and 1.5 V for a self-aligned 0.7x20 μm nJFET.

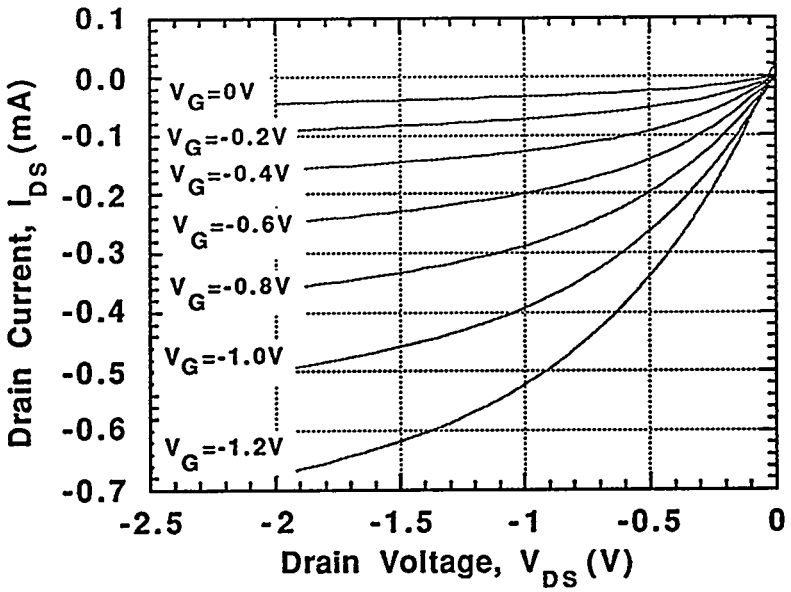

Figure 6. I_{DS}-V_{DS} for a self-aligned 0.7x20 μm pHFET.

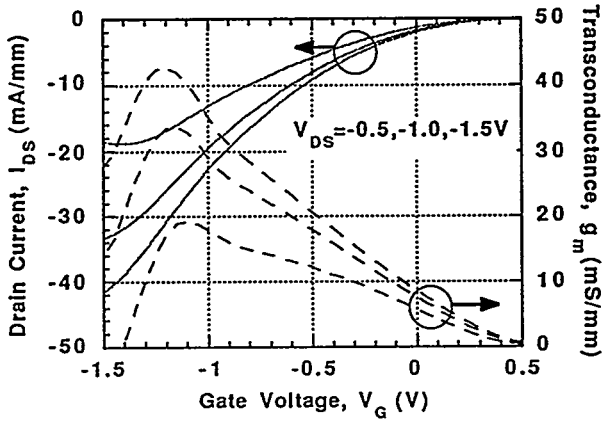

Figure 7. I_{DS}-V_G and g_m-V_G at drain biases of -0.5, -1.0, and -1.5 V for a self-aligned 0.7x20 μm pHFET.

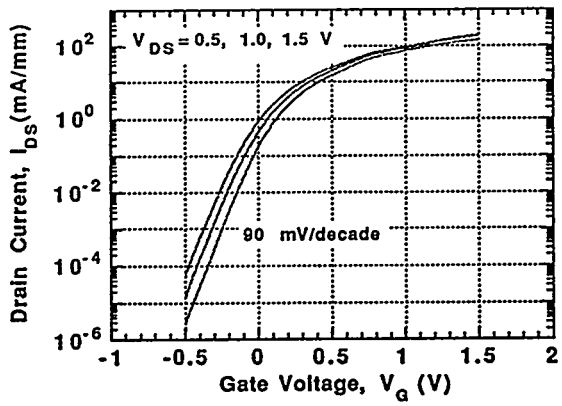

Figure 8. I_{DS}-V_G characteristic at drain biases of 0.5, 1.0, and 1.5 V for a self-aligned 0.7x20 μm nJFET.

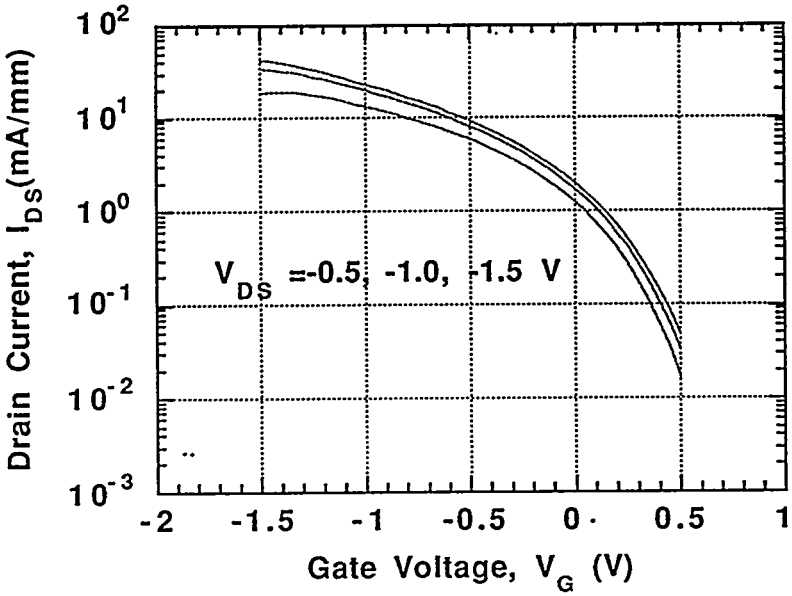

Figure 9. I_{DS}-V_G characteristic at drain biases of -0.5, -1.0, and -1.5 V for a self-aligned 0.7x20 μm pHFET.

are approximately 170 mS/mm and 90 mA/mm, respectively. Likewise, the pHFET shows a maximum g_m of 43 mS/mm and I_{DS} of 42 mA/mm and operating values of 29 mS/mm and 20 mA/mm. The nJFET shows f_t of 19 GHz and f_{max} of 36 GHz [9]. The pHFET shows an f_t of 3.5 GHz. The subthreshold characteristics for each device is shown in Figs. 8-9. The subthreshold slope is 90 mV/decade for the nJFET. The pHFET has not been fully optimized, as it shows soft pinchoff and excessive subthreshold current which contribute to higher than desired static power.

The junction gate turn-on voltages are -1.1 V for the p-channel device and 1.0 V for the n-channel device at 1 mA/mm of gate current. These turn-on voltages are adequate for low static power operation at 1.0 V power supply and below.

CIRCUIT RESULTS

Basic complementary circuits were fabricated including inverters, other basic logic gates, and loaded 31-stage ring oscillators. The inverters showed excellent noise margins in excess of 200 mV. The ring oscillators were loaded with 200 μm of wire in 2nd metal which was interdigitated with grounded 1st metal to provide a high capacitance load between each stage. Fan-in and fan-out are both 1 and the devices are 20 μm wide. Maximum speed was obtained at a supply voltage of 1.2 V with gate delays of 179 ps and a power-delay product of 28 fJ, as seen in Fig. 10. The maximum speed was obtained at a voltage beyond the onset of gate conduction and the power is dominated by gate leakage. A minimum power-delay product of 8.9 fJ was obtained at a power supply of 0.8 V and a speed of 319 ps/stage. The power consumption is largely static power due to soft pinchoff of the p-channel transistor. Under these conditions it is not yet possible to determine the dynamic power.

The modulation-doped pHFET does not offer state-of-the-art performance at this time with g_m only 29 mS/mm at operating circuit bias conditions. Yet these loaded ring oscillators demonstrate excellent speeds at low-power supply voltages and even better results are expected with a redesigned pHFET.

CONCLUSION

A promising new GaAs complementary logic technology has been presented and complementary ring oscillators have demonstrated excellent speeds at low power supply voltages, which is key for maintaining speed while reducing dynamic power consumption. This technology is promising for mixing low power digital functions with high-speed analog circuits.

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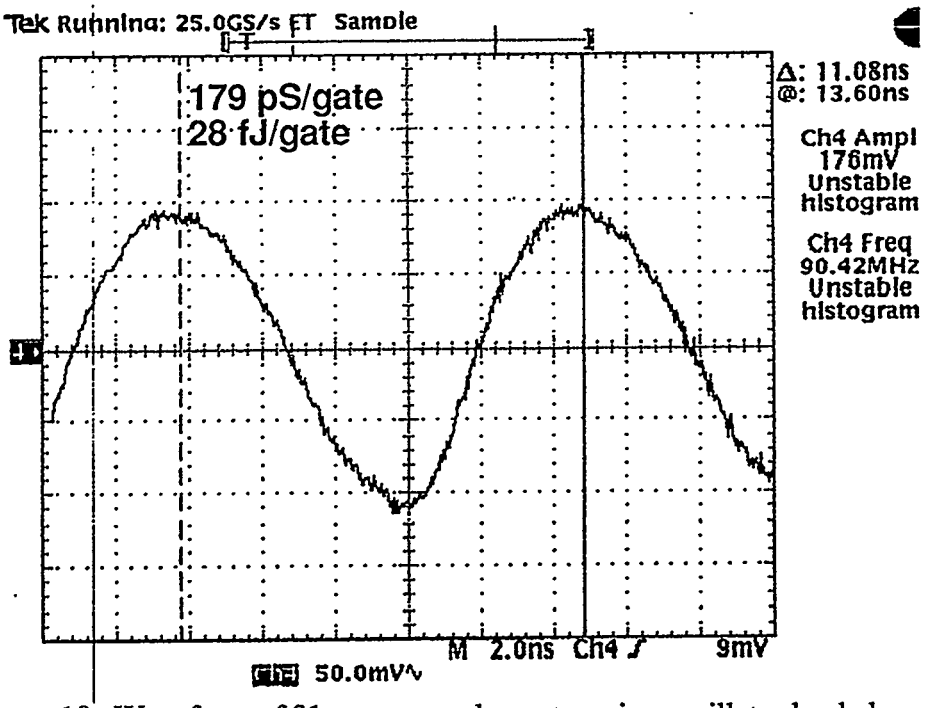

Figure 10. Waveform of 31-stage complementary ring oscillator loaded with 200 μm of wire and operating with a power supply of 1.2 V.

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