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CAMAC THROUGHPUT OF A NEW RISC-BASED DATA ACQUISITION COMPUTER AT THE DIII-D TOKAMAK

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ABSTRACT

The amount of experimental data acquired per plasma discharge at DIII-D has continued to grow. The largest shot size in May 1991 was 49 Mbyte; in May 1992, 66 Mbyte; and in April 1993, 80 Mbyte. The increasing load has prompted the installation of a new Motorola 88100-based MODCOMP computer to supplement the existing core of three older MODCOMP data acquisition CPUs. New Kinetic Systems CAMAC serial highway driver hardware runs on the 88100 VME bus. The new operating system is MODCOMP REAL/IX version of AT&T System V UNIX with real-time extensions and networking capabilities; future plans call for installation of additional computers of this type for tokamak and neutral beam control functions. Experiences with the CAMAC hardware and software will be chronicled, including observation of data throughput. The Enhanced Serial Highway crate controller is advertised as twice as fast as the previous crate controller, and computer I/O speeds are expected to also increase data rates.

OBJECTIVE

Tests at DIII-D of a new data acquisition computer and new CAMAC components have been prompted by the need for faster transfer of the rapidly rising quantity of diagnostic data and by the declining reliability of existing systems. Installation of an open systems platform running UNIX was expected to provide compatibility with DIII-D's network and also permit use of many hardware and software products on today's market. At the same time, DIII-D's large existing inventory of CAMAC data acquisition hardware dictated that compatibility with CAMAC be maintained.

TEST UPGRADE TO EXISTING DIII-D SYSTEMS

Existing System:

Fig. 1 illustrates flow of a single signal from a tokamak diagnostic to the local VAXCluster. In the existing DIII-D system, the Data Acquisition Computers block in Fig. 1 encompasses three MODCOMP CLASSIC and 32/85 computers with Kinetic Systems Model 2080, 2081, and 2083 highway drivers. The operating system on the MODCOMP computers is MODCOMP's proprietary 16-bit MAX IV. CAMAC data acquisition software was written at General Atomics (GA).

In each crate on the highway is a crate controller; the remaining slots of the crate may be loaded with

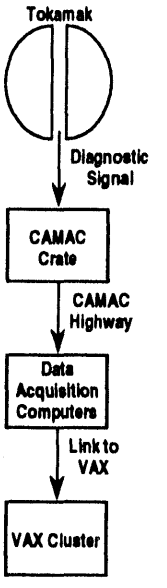

FIG. 1. DIII-D data acquisition path.

CAMAC-compatible modules including transient recorders, dual-port memories, programmable clocks, waveform generators, elapsed time counters and others. The serial highway in the existing system is a fiber optic link.

Digitizers, or transient recorders, comprise more than 96% of the existing CAMAC hardware linked to the MODCOMP CLASSICS and 32/85. Over 90% of shot data is obtained from two digitizer types: LeCroy 8212 32-channel Data Loggers and DSP Technology Traq 4012 systems. Each of these types provide 12-bit digitized samples which are padded to 16 bits and read by single-word or block read commands. Other non-digitizer CAMAC modules in the database include LeCroy 8801 dual-port memories.

Test System:

In the test configuration, the existing components of the Data Acquisition Computers block (Fig. 1) were replaced by a new computer and CAMAC highway driver. In 1993, GA purchased a MODCOMP RealStar 1000 computer incorporating a single-CPU Motorola 88100 RISC processor on a VME chassis. The operating system is MODCOMP's REAL/IX, an AT&T System V UNIX with real-time enhancements. The two-board Kinetic

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Systems model 2140 CAMAC serial highway driver plugs into the VME chassis. The test serial highway runs directly from the CAMAC crate controller to the highway driver without interposition of the fiber optic link. MODCOMP has supplied a CAMAC software driver with an interface library which provides C- or FORTRAN-callable routines similar to those available with the Kinetic Systems VAX-VMS CAMAC serial highway driver interface. Table I lists available CAMAC library calls. A complete description of the driver calls may be found in [1] and [2].

Test codes by MODCOMP and GA were written in C.

TEST SUMMARY

Requirements:

It was required that data stored in CAMAC devices be read without errors and that at a minimum the existing data transfer rate be doubled by the test combination of computer and highway driver. When the new enhanced serial crate controller was also installed in the test path, another doubling of the rate was expected.

Results:

The test computer and highway driver yielded transfer rates from three to more than ten times as fast as the existing components. Inclusion of the enhanced serial crate controller quadrupled these rates again, except for the LeCroy 8212 Data Logger, with which its enhanced mode was incompatible.

CAMAC MODULES TESTED

The modules tested included a LeCroy 8212 Data Logger, a Traq 4012 digitizer system and a LeCroy 8801 dual-port memory in three series of tests; first, functional tests to find sequences of commands to which the modules would respond correctly and consistently; second, tests of data transfer rate over the CAMAC serial highway; and third, a loop sequence which acquired about 1.5 Gbyte of data per test while accumulating error counts.

The tests included both the older standard Kinetic Systems Model 3952 L-2 crate controllers and the new enhanced model, version Z1-E. The CAMAC library commands, which are listed in Table I, included standard and enhanced block read services; both types could be used with an enhanced crate controller while only the standard commands were recognized by a standard controller. 16-bit data were both read and written during the test. The highway speed on the 2140 driver board was set to 5 MHz, byte serial.

FUNCTIONAL TESTS

Digitizer sequences followed the outline of; (1) set up, (2) start sampling, (3) stop sampling, and (4) read memory. Memory module sequences were: (1) write memory and (2) read memory.

Table I
CAMAC Commands Available

Command	Description
caopen	Open CAMAC highway; assign logical device name.
caclos	Close CAMAC highway; deassign logical device name.
cactrl	Send command to a CAMAC crate controller.
ccstat	Return crate controller status.
cam16	Read or write a 16-bit word to or from a CAMAC device.
cam24	Read or write a 24-bit word to or from a CAMAC device.
cab16	Read or write a block of 16-bit words to or from a device.
cab24	Read or write a block of 24-bit words to or from a device.
cab16e	Read or write a block of 16-bit words in enhanced mode (enhanced crate controller required).
cab24e	Read or write a block of 24-bit words in enhanced mode (enhanced crate controller required).
camsg	Output a diagnostic message to explain a status returned by a CAMAC command call.
cxlam	Enable interrupt to service LAM (look-at-me) event

The test software calls "cam16" to send all commands except the block read and write commands. A "cab16" call does standard block I/O, while a "cab16e" does enhanced block I/O when an enhanced crate controller is in the test crate.

The sequences shown in Table II were obtained, for the most part, from the modules' instruction manuals and from previous knowledge of using these modules on the older MODCOMP computers. Each sequence was tested, first by entering commands manually using an interactive diagnostic test program, and subsequently by writing and running test codes which incorporated the same commands. When writing code to run the Traq 4012 digitizer, it was necessary to provide the recommended 0.5 msec delay between commands; otherwise, errors frequently occurred.

ERROR CHECKING

Several tests checked for possible errors stemming from CAMAC calls.

First, the test codes reviewed the returned status from every call and displayed a message if any abnormality occurred. This type of message appeared if, for example, too many passes through a digitizer read loop were attempted. The memory address register automatically increments when each data word is read, and a "No-Q" or "No-X" status occurs in response to an attempt to increment this register past the programmed memory per channel of the digitizer.

Second, test codes preloaded known values into read buffers and then overwrote the buffers with data from CAMAC. If the correct number of data samples were written into the buffer, a test then revealed that the preloaded values had been overwritten as desired.

Table II
Command Sequences for Tested CAMAC Modules

Function	Description
LeCroy 8212 Digitizer	
F10	Clear LAM (look-at-me).
F17	Set post-trigger samples, clock rate, and number of channels.
F9	Start sampling.
F25	Stop sampling.
F10	Clear LAM.
loop over channels:	
F16	Select channel to read.
read loop:	
F2	Read data (an argument specifies the number of samples).
end read loop	
end loop over channels	
Traq 4012 Digitizer	
F17	Repeat this command six times to set these six parameters: Remote access Number of channels Post-trigger samples Clock selection (two internal clocks are available) Clock frequency Memory per channel.
F10	Clear LAM (look-at-me).
F9	Start sampling.
F25	Stop sampling.
F10	Clear LAM.
loop over channels:	
F17	Select channel to read.
F17	Select memory block zero (block size is 1024 samples).
F10	Clear LAM
read loop:	
F2	Read data (an argument specifies the number of samples).
F17	Select memory block for next read (pass this command is required only with the enhanced crate controller and enhanced block read command: see text).
end read loop	
end loop over channels	
LeCroy 8801 Memory Module	
Write memory:	
F19	Disable external port.
F25	Enable autoincrement.
F18	Load memory address register.
F16	Write block of data (argument specifies number of words).
F11	Enable external port.
Read memory:	
F19	Disable external port.
F25	Enable autoincrement.
F18	Load memory address register.
F2	Read first word of memory (required step before block read).
F2	Read block of data (argument specifies number of words).
F11	Enable external port.

Third, the dual port memory module was tested by writing a known sequence of data to it, then reading it back and looking for discrepancies.

Fourth, the output of a waveform generator was fed into digitizer inputs. The digitized values were scanned to verify that samples were not skipped, duplicated, or corrupted. This test method aided us in finding and correcting a problem we encountered when reading the Traq 4012 digitizer memory using a series of enhanced block reads.

ENHANCED BLOCK READS OF THE 4012 DIGITIZER

In testing of the Traq 4012 digitizer with the enhanced serial crate controller, a consistent error was found in the memory address register's updated value at the end of each block read pass. The error occurred only when using the enhanced "cab16e" call, never with the standard "cab16" call. Because of this, and because the digitizer memory can be repeatedly read after the "setup," "start sampling," and "stop sampling" steps are complete, the error can be detected and understood easily.

The procedure was to input a waveform voltage to an input channel and assign 256 ksample of memory to the channel. The input was sampled long enough to fill the memory and then the digitized data was read over CAMAC in blocks of 16 ksample, first using 16 standard "cab16" block read commands. Then the same digitized data was read again using 16 enhanced "cab16e" commands.

The "cab16" standard commands completed correctly, but the last "cab16e" enhanced command returned a "No-Q" error. A comparison of the returned data blocks, which should be identical for both types of read commands, showed that each "cab16" pass caused the memory address register to advance correctly, by 16384, but that each "cab16e" pass was advancing the register by three extra words. On the last pass, the register was reaching the limit of 256 ksample before the block read was complete. No samples were skipped within each pass; the three-word gaps were always between passes.

This situation was corrected by setting the Traq 4012's memory register address between read passes with an F17 command. The data rate penalty is small if a large read block size is chosen. The error does not occur at all if the read block size is equal to the memory per channel and only one read pass is required.

READING THE 8212 DIGITIZER

Under some conditions, the high speed of the test computer and highway driver sometimes exceeded the capability of the 8212 32-channel digitizer. A block-read command to read a single channel succeeded only if the module was set up for 4 channels, rather than 8, 16, or 32. Since channel data are interlaced in memory, response was too slow at higher channel settings and No-Q

status was returned. The problem was solved by using the 8212's stream-read mode, which returns sequential memory values from which individual channel data can be extracted.

The 8212 memory could not be read at all in enhanced mode with the enhanced crate controller. Errors occurred in data returned by either stream or channel read requests. However, the module could be read using regular (non-enhanced) software calls with the enhanced crate controller.

DATA THROUGHPUT TESTS

When testing data transfer rates over CAMAC highways, program overhead was minimized in order to attain the fastest possible rates on both existing and new systems. Read block sizes on the new system were larger than on the existing CAMAC, but neither system showed significant sensitivity to reasonable variation in block size. All rates are shown in kilosamples per second; a sample is passed in a 16-bit word. Error rates were zero.

Table III displays data rates of the existing GA acquisition system, while Table IV shows rates achieved by the new test computer and CAMAC hardware. All figures are maximum speeds over CAMAC serial highways, using block mode read commands, except for LeCroy 8212 digitizers on the existing MODCOMP system, which cannot be read reliably in block mode and thus are read in single-word mode. Read block sizes for devices other than 8212 digitizers on existing systems are 4 ksamples. Read block sizes on the new system are 256 ksamples for Traq 4012 digitizers, 16 ksamples for LeCroy 8801 dual-port memories, and 32 ksamples for LeCroy 8212 digitizers. Data rates for 8212 digitizers on the new system were the same whether reading memory in stream mode or reading a single channel with the module set up for four channels.

RELIABILITY TESTS

A test loop reads the three modules listed in Table IV in sequence; the code makes 1200 passes through this loop to simulate fifty "shots," each of 30 Mbyte. Error counts are accumulated throughout the run and reported on completion. The first three tests described under "Error Checking" above are performed at each read pass. A zero error rate has consistently been achieved.

CONCLUSIONS

The test data acquisition system has performed successfully and will provide capability for database expansion. The functional and reliability checking of other CAMAC modules will be performed. A further goal is to transfer all timing and control functions from the old acquisition system to the new in order to realize higher tokamak availability and, when desired, a more rapid shot repeat rate.

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[1] "Model 2160 CAMAC VMS Driver 6611-1B Software, Release 2.5," Lockport, Illinois: Kinetic Systems Corporation, March 1992.

[2] "CAMAC Library Reference Manual, REAL/IX Operating System," Ft. Lauderdale, FL: Modular Computer Systems, Inc., June 1993.

Table III
CAMAC Serial Data Rates on Existing Systems
(kilosamples per second)

	MODCOMP 7870 CPU	MODCOMP 32/85
LeCroy 8212 Digitizer	17	N/A
Traq 4012 Digitizer	25	60
LeCroy 8801 Dual-Port Memory Module	28	60

Table IV
CAMAC Serial Data Rates on Test System
(kilosamples per second)

Crate Controller:	Standard	Enhanced	
Block I/O Type:	Standard	Standard	Enhanced
LeCroy 8212 Digitizer	210	220	N/A
Traq 4012 Digitizer	200	210	850
LeCroy 8801 Dual-Port Memory Module	210	240	960

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