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Toward Low-Cost Display Assembly and Packaging: Precompetitive Challenges

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Abstract

Flat panel assembly and packaging are of growing importance in the electronic marketplace. Material, process, and equipment challenges extend beyond those of IC packaging.

Key Words: Displays, Packaging, Assembly, Flat Panel, COG

Difficulty of Display Packaging-- a Large Liquid Crystal Panel

For those that find single IC packaging often challenging and approach multichip module packaging with all their resources mustered, display packaging often seems beyond the realm of reason. From single IC to large displays, the dimensions jump from a few to 10-100 centimeters. In addition, all the fixturing necessary to perform assembly and bonding on these very large MCMs must be invented.

The material is no longer metal or robust alumina but rather 2 glass panels that must be kept separated with a constant 7 micron gap. The very long perimeter must be sealed to keep contamination out and special liquids or gasses in. This seal must withstand large panel flexing modes (similar to a kettle drum) and allow 640 column + 480 row + power feedthroughs. This seal must be the main line of defense for the 1 million thin film transistors and 2 miles of micron lines that may be inside. The packaging engineer must also be vigilant for any "inside" contamination innocently placed within the display by device engineers desperate for 100% pixel yield. The seal integrity must resist 10 years of temperature cycling, and severe shock and vibration that comes from handling by children and salesmen told to treat their display with respect. [1]

These large panels with many centimeters of line capacitance must often be packaged to switch voltages at microsecond rates to accommodate real time video. In addition, the packaging must not add to the power

demand because of battery and thermal management limits. All these requirements must be met at low cost and with attractiveness to the product customer, because the display packaging is becoming more and more the system packaging.[2]

Why display packaging is important

Depending on the specific product, the display plus assembly and packaging represents 5-50% of the value. For large manufacturing volume consumer products the 50% figure holds true. Moreover, the display is often the differentiating component in the system; that is, the customer is certainly driven by the brightness, color, resolution...all of which degrade somewhat with today's packaging. However, in addition, features determined directly by the display packaging such as the display robustness, lifetime, and operation time for a battery pack count heavily in product differentiation.[3]

The display packaging is growing in importance as the display panel is becoming the backbone of the system. Often the display is becoming the motherboard for all the integrated circuits as well as the external user interface. *For many products the display packaging is the system packaging.* Thus in both the good and bad meanings of the phrase, "display packaging has become too important to leave to the packaging engineer."

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Proprietary Caution

Many companies are involved in developing flat panel displays. Each company involved in displays has a particular targeted customer base and feels they have manufacturing solutions for this market. Thus each company has "solved" the challenges listed below. Their answers are often different, proprietary, and not often low cost and high yield. This article discusses the ongoing challenges which still benefit from pre-competitive shared development without divulging any of the many proprietary solutions.

Materials

The unique packaging materials are introduced in the following paragraphs, but will be discussed in more depth during the "processes" and "technical Challenges" sections.

Large panels of Corning optical glass are used for displays. Assembly equipment must be adapted to handle this large glass without generating particulate contamination or damaging the fine conductor patterns. The glass panels must be sealed along their perimeter without excessively heating the nearly finished display.

Component lead attach material consists of conductive low temperature cure adhesives, solders, and thermal compression Au-Au TAB bonds. The trend toward higher lead density and IC density requiring close packing on the display perimeter have weighed against TAB for this interconnect. Solders require high temperature reflow, fluxes, toxic disposal, and are not amenable to fine pitch I/Os. Thus solders are losing ground to anisotropic conductive adhesives pioneered by 3M.

Although displays in portable consumer products aim at only 3-10 year lifetimes, post-assembly coatings are advisable as both chemical and mechanical protective barriers. Today's IC chips and discrete components have intrinsic integral passivation, but the cleaning and post-assembly coatings prevent accumulation of condensation and ions from overwhelming this passivation. Coatings such as epoxy around and under flip chips have been recently shown to improve reliability during temperature cycles [4].

For many smaller display designs the signal electronics is not mounted directly on the panel but must be mass connected to the panel. Flex circuitry or flex connectors are often used. The connections can be made with z-axis elastomers, conductive adhesives, or solders depending on the pitch and conductivity required.

Processes

The glass panel material is "new" to packaging and thus the Chip-on-Glass (COG), Flip-Chip-on-Glass (FCOG), flex to glass, and rework on glass all must be approached as new processes that must be both optimized for manufacturability and for reliability. The growing size of the panels also challenges pick and place and chip assembly tools. Placement of parts must be within 1 mil over an area up to 30" on a side. This accuracy is needed for the 7 mil lead or solder bump pitch used by displays.

All assembly steps are aimed at low temperature and low generation of contamination. A single cure for adhesion and electrical connection and a second cure for a protective coating are the goal. Localized rework is a must for the high valued displays; one bad chip can not sink the pixel perfect large panel display. The perimeter seal generally takes place before chip assembly and is considered proprietary by each manufacturer.

Particular Technical Challenge:

The cleanliness needed on a large panel manufacturing line is considerably beyond the Class 1000 used in traditional packaging. The large areas and long sealing perimeter plus relatively long fine lines (2 miles of fine lines on a large panel) do not allow tolerance for contamination. For active matrix panels the thin film transistor matrix of up to one million must also be protected during packaging from contamination that will lead to reliability problems

The Assembly, rework, and sealing technology must be done at low temperature to protect the display devices and materials. This is one of the motivations to use low temperature cure conductive adhesives rather than traditional surface mount and flip chip solders which require higher temperatures.

The assembly and final packaging must provide robustness for the large thin panel under differential temperature expansion, vibration, and mechanical shock. The micro-attachments and large perimeter sealing must be resistant to microcracks and fracture propagation. Under abuse the seal must keep the appropriate liquid or gas within and the contamination out for up to 10 years.

The current yield on the most complex active matrix panels is low, thus the assembly and packaging must be very high yield, just as low yield ICs cause extra pressure on the packaging line.

For color displays the filters used in assembly are only 5% optically efficient and cost about 9% of the display; a clear need for better packaging material. Similarly the polarizing sheets needed for some display types degrade for extended periods above 85 C. This

limitation severely limits the processing and rework temperatures allowed after the sheets are applied.

System packaging is challenged by the power supplies for the display. They must be small yet efficient. The power supply also is the focus for thermal management for display based systems.

Although automation is common in assembly and packaging lines, automation for large panel manufacturing is not fully established. To become low cost, a high volume display line must have fully automatic pick and place, wire bonding/COB/FCOB, optical inspection, rework, and electrical test all capable of working on the whole panel with high speed and producing little contamination. Such equipment must have more extensive sensor feedback systems than are on current small unit assembly equipment.

Summary

Display panels are growing in size. Display packaging is becoming system packaging. In contrast with historical IC and PWB packaging, displays offer a glass substrate, large size, need for low temperatures and low contamination. There is plenty of room for display packaging improvement.

References

¹ O. C. Woodard, T. Long, "Display Technologies," *Byte*, July 1992, pp. 159-168.

² J. Shandle, "A Revolution is in Store for Flat-Panel Displays," *Electronic Design*, April 15, 1993, pp. 59-73.

³ L. E. Tannas, "Japanese flat-panel displays: what JTEC saw," *Information Display*, July/August 1992, pp. 18-22.

⁴ S. C. Machuga, S. E. Lindsey, K. D. Moore, A. F. Skipor, "Encapsulation of Flip Chip Structures," *1992 IEMT Symposium Proceedings*, IEEE Baltimore, September 1992, pp.53-58.

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