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Very Low-Power Consumption Analog Pulse Processing ASIC for Semiconductor Radiation Detectors

K.O. Wessendorf[1], J.C. Lund[2], B.A. Brunett[3], G.R. Laguna[1], and J.W. Clements[1]
[1]Sandia National Laboratories, P.O. Box 5800, Albuquerque, New Mexico 87185
[2]Sandia National Laboratories, P.O. Box 969, Livermore, California 94551
[3]Carnegie Mellon University, Pittsburgh, PA 15213

Abstract

We describe a very-low power consumption circuit for processing the pulses from a semiconductor radiation detector. The circuit was designed for use with a cadmium zinc telluride (CZT) detector for unattended monitoring of stored nuclear materials. The device is intended to be battery powered and operate at low duty-cycles over a long period of time. This system will provide adequate performance for medium resolution gamma-ray pulse-height spectroscopy applications. The circuit incorporates the functions of a charge sensitive preamplifier, shaping amplifier, and peak sample and hold circuit. An application specific integrated circuit (ASIC) version of the design has been designed, built and tested. With the exception of the input field effect transistor (FET), the circuit is constructed using bipolar components. In this paper the design philosophy and measured performance characteristics of the circuit are described.

I. Introduction

Conventional pulse processing electronics for radiation detectors consume relatively large amounts of power and are often unsuitable for use outside the laboratory. Lower power charge preamplifier circuits have been successfully developed [1,2]. However, for long term unattended monitoring applications, the entire pulse processing *system* [3,4] (preamplifier, shaping amplifier, sample-hold) must also consume very little power. We are interested in deploying circuits in a nuclear monitoring application in which long operating lifetime is critical. For the duty cycles that we envision in our application, this energy budget translates into an average power consumption of 14 mW for the pulse processing circuit.

II. Design Intent

The circuit we designed is intended to perform the same functions as a charge sensitive preamplifier, shaping amplifier, and a peak sample and hold circuit. However, to minimize packaging volume and power consumption, the three functions are integrated on one ASIC. The pulse processing ASIC is designed to interface to a flash analog to digital converter (ADC) for subsequent pulse height analysis. Low average power was achieved by making the high-current functions enabled only when the desired input pulse amplitude level is detected. Novel circuit design techniques were used to minimize power consumption while providing good linearity and moderately low-noise circuit performance.

The circuit was designed to operate off of a 7 V (±3.5 V) power supply and used with a CZT detector to provide pulse height spectroscopy from 0 to 1.0 MeV with an energy resolution of at least 20 keV FWHM. Assuming a mean electron-hole pair creation energy in CZT of 5.0 eV these design specification translate into a "charge gain" of 58.6 μV/keV (133 mV/fC) and an equivalent noise charge (ENC) [5] of less than 1700 electrons rms. By altering the effective feedback capacitance in the circuit, it should be possible to alter the gain for use with other detectors besides CZT. For instance, by increasing the "charge gain" of the circuit it should be possible to use the circuit as a readout for silicon p-i-n detectors attached to scintillators.

III. Overview of ASIC Design

The ASIC performs the three analog pulse processing functions used in a semiconductor pulse height spectrometer: charge amplification, shaping, and peak sensing. A simplified block diagram of the ASIC circuit is shown in **Figure 1.**

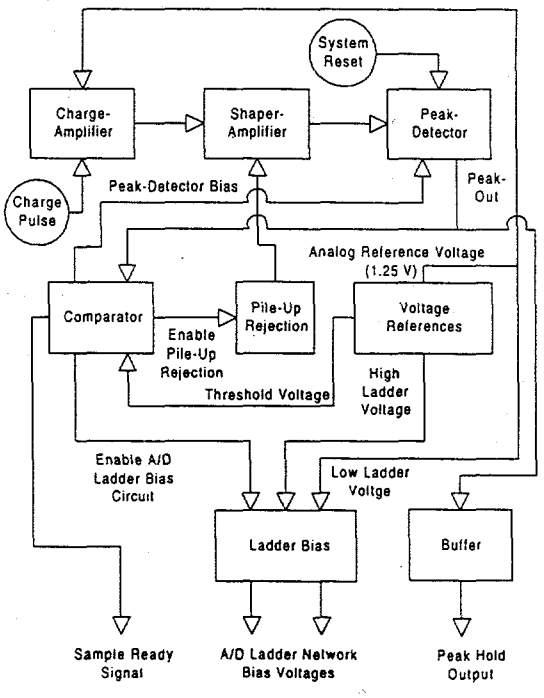

Figure 1. Block diagram of the pulse processing ASIC.

DISCLAIMER

The pulse processing ASIC is designed to work with a companion flash ADC and microcontroller to function as a complete ultra low-power gamma-ray pulse height spectrometer. In addition to its pulse processing functions, the ASIC also contains a circuit for biasing the external flash ADC reference input. Finally, the ASIC contains a circuit to provide common and precise reference voltages to all other circuits in the ASIC.

The ASIC was designed to draw approximately 2 mA of current in the "idle mode" (no valid pulses present). When a pulse of appropriate amplitude triggers the circuit, its current draw will double. The circuit will then continue to draw 4 mA for the remainder of the pulse acquisition time (< 10 μs). Additional current will also be drawn during pulse acquisition to provide a reference for the external flash ADC. The amount of additional current drawn will depend on the ladder network used in the external ADC.

This design uses a band-gap voltage reference to set the operating dc voltages of the entire system. Since the band gap voltage is very stable over temperature and power supply voltage, the system can be designed to exploit this stability. The voltage references block generates three dc voltages for the system. The 1.25 V analog reference voltage (V_{ref}) sets the steady state dc voltages for the charge-amplifier output. Since the dc gain of the shaper-amplifier, peak-detector and buffer amplifier is unity, the charge-amplifier sets the dc operating voltages of these function blocks. Therefore the output of the buffer is a peak-held dc voltage relative to V_{ref} (1.25 V).

The voltage reference block provides a threshold voltage to the comparator. This voltage is slightly above V_{ref} and is adjusted to reject circuit noise. When the peak-detector output rises above the threshold voltage (V_{thresh}) the pile-up rejection circuit and ladder bias circuit are enabled.

The voltage reference block also provides the high and low bias voltages to the ADC resistor ladder bias network. The high voltage is adjusted to approximately 6.0 V while the low voltage is V_{ref} (1.25 V). The ladder bias block takes these low-current voltage references and applies these voltages to the low-value ladder resistor of the ADC converter. For the sake of minimizing system power consumption, the ladder bias circuit is enabled by the comparator when a nuclear pulse of V_{thresh} is detected. The ladder resistor bias is maintained for the duration of the measurement which, in this design, is approximately 10 μs. After the sample has been digitized, the system is reset and returns to the lower power mode of operation (and remains in low power mode until another pulse of sufficient amplitude is produced by the detector).

The comparator block is used for four critical system functions: peak-detector bias control, ladder bias enabling, pile-up rejection and system noise rejection. These functions are enabled or disabled based on the sensing of a V_{thresh} pulse input. The comparator provides bias to the output of the peak-detector such that the circuit is bi-directionally linear until the comparator senses an input pulse of amplitude greater than V_{thresh}. When the comparator senses this input pulse, the peak-detector bias is removed and the peak-detector accurately follows the peak amplitude of the input. The peak-detector capacitor holds this voltage with very little change during the time interval required for ADC conversion.

The comparator also enables the pile-up rejection circuit. The pile-up rejection circuit controls the ac gain of the shaper-amplifier. The shaper amplifier ac gain is allowed to be relatively large (20 to 30) when waiting for a V_{thresh} input pulse. After a pulse has tripped the comparator the shaper-amplifier gain is allowed to stay high for a predetermined period of time (approximately 3 μs to 5 μs). This time is allowed to be long enough to completely capture one pulse. After this time, the ac gain of the shaper-amplifier is actively reduced to near unity. This gain reduction effectively eliminates the possibility of the desired pulse from being altered by a later arriving pulse greater than V_{thresh} in amplitude.

As stated earlier, the buffer is a unity gain amplifier. This amplifier is designed to drive relatively large capacitance loads of 20 pF. This is required because the flash ADC used in our system is essentially a string of paralleled gate inputs (vs. a single MOS input; which would be a relatively low input-capacitance). The base-currents of the input of the buffer stage were canceled by a current mirror arrangement. This technique minimizes the peak-detector droop caused by the base currents of the input stage. Base current cancellation typically results in very small effective input current although the sign of this current may be either positive or negative. Because it is nearly impossible to exactly cancel the input base currents, a very small net input current remains (though much smaller in amplitude than if one does not use a canceling technique at all).

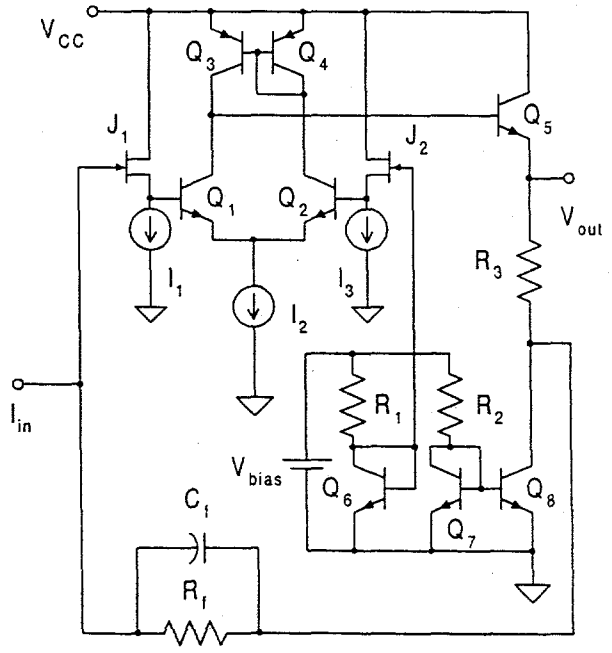

Figure 2. Schematic diagram of the charge sensitive amplifier section of the pulse processing ASIC.

IV. CHARGE AMPLIFIER

A simplified schematic for the charge amplifier in the pulse processing ASIC is shown in **Figure 2**. The design intention for this amplifier was to provide a large charge-gain to bias-current ratio and make the output dc voltage fixed to a band-gap reference voltage. This dc output subsequently becomes a reference voltage for the entire pulse-processing ASIC. The use of an active-load differential-amplifier provides a high-gain per unit bias current and allows for common mode noise rejection at the front-end of the amplifier. Current sources I_1 and I_3 use emitter resistors to minimize noise.

The external matched JFET pair (J_1 and J_2) is used as a differential-amplifier configuration with Q_1 and Q_2 as the heart of the differential amplifier. Q_6 sets the bias voltage of the base of Q_2, and- thus by feedback- the gate of J_1. The current-mirror, Q_7 and Q_8 allow for V_{out} to be biased by V_{bias}.

This amplifier was designed to operate at approximately 0.5 mA total current draw with 40 μA (I_1 and I_3) of bias in each of the JFETS. This amplifier is an inverting transimpedance amplifier with R_f/C_f as the feedback impedance.

The differential-amplifier (Q_1, Q_2, Q_3, and Q_4) is biased at 140 μA (I_2). Q_5 is a buffer transistor that also supplies a required dc bias shift from the collector Q_1 and the output, V_{out}. The amplifier output, V_{out}, is biased to the system V_{ref} (1.25 V) by the on-chip band-gap voltage reference. This bias voltage, represented by V_{bias} sets the dc voltage at V_{out}. Transistors Q_6, Q_7, Q_8 and resistors R_1, R_2, and R_3 comprise a current-mirror bias circuit through which the dc voltage at V_{out} is set. V_{out} will be equal to V_{bias} when R_1, R_2 and R_3 are equal values and Q_6, Q_7, and Q_8 are matched transistors. R_1, R_2 and R_3 were chosen to be 15 kΩ. These resistor values provides a good compromise between circuit performance and power consumption. Ideally, for good circuit performance, R_3 should be small to allow the emitter of Q_5 to control the collector of Q_8 and the associated capacitance at this node, but this would require more power given this ASIC topology. The bias voltage is selected to be relatively low for good dynamic range yet large enough to provide adequate bias voltages around the amplifier. Given these constraints, V_{bias} was chosen to be 1.25 V; a standard band-gap reference voltage. This amplifier is inherently very stable and of relatively high gain due to the single-stage of inverting-gain using high-impedance active loads. The amplifier circuit is phase-compensated by using a parasitic 1 pF capacitor added to the base-collector capacitance of Q_1. The external JFETS are n-channel epitaxial devices manufactured by Temic (part# SST404) and have a very small $V_{GS(off)}$ voltage of –2.5 V maximum and –0.5 V minimum. The SST404 is a dual monolithic part in a surface mount package. The feedback resistor, R_f, is a 20 MΩ surface mount resistor. To maintain a large system charge-gain with minimum power consumption, the feedback capacitor C_f is the parasitic capacitance of R_f; this capacitance is approximately 0.15 pF.

V. SHAPING AMPLIFIER

A simplified block diagram of the shaper-amplifier design used in this ASIC is shown in **Figure 3**. The feedback components, R1, C1, R2, C2 and the impedance of Q_1 control theacgain of this circuit. The dc gain of this circuit is unity due to C_2 which is a large value (0.1μF) capacitor. C_1 is chosen in combination with R_1 and R_2 to provide the desired gain and filtering characteristics of the shaper-amplifier function. V_{gain} is a digital "like" signal provided by the comparator and pile-up rejection block; V_{gain} either holds Q_1 in saturation or cutoff. The transistor impedance is very low when the device is in saturation (V_{gain} high) and therefore theacgain of the amplifier is set by the passive feedback components. When V_{gain} is low, the transistor is off and the collector to emitter impedance is very high forcing theacgain of the amplifier to unity. This gain control allows the rejection of charge- pulses after the initial sampling of a desired pulse. A gain ratio of approximately 20:1 to 40:1 is easily obtained using this technique. This range is typically enough to reject undesired pulses during the processing of a captured sample. In this design R_1 was chosen to be 30 kΩ with C_1 equal to approximately 10 pF. R_2 is set to 1.5 kΩ to provide the desired overall charge-gain of approximately 110 mV/fC and allow for a large,relatively high to low gain ratio.

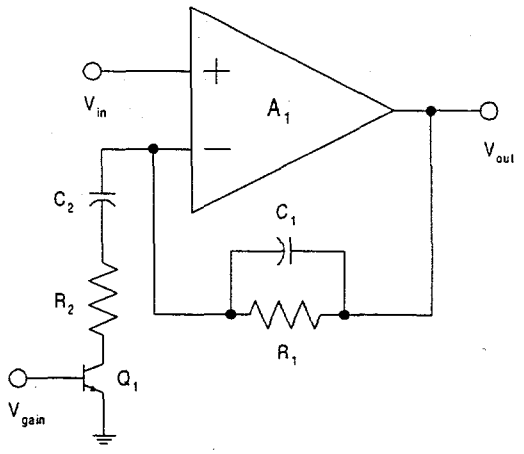

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Figure 3. Schematic diagram of the shaping amplifier section of the pulse processing ASIC.

The analog approach to pile-up rejection just described has one serious flaw. When Q_1 is turned off (immediately after a charge pulse has been peak-held) a small parasitic voltage pulse is generated at the output of the shaper-amplifier, effectively limiting the low-level sensitivity of this design. For this ASIC, the low-level limit due to this parasitic pulse is approximately 3 fC. Since this system uses a flash ADC, the system acquires a sample and resets in less than 15 μs. Thus, it is possible to use the ASIC without the pile-up rejection circuit if the rate of input pulses is relatively low. A redesign of the pile-up rejection block is being considered to eliminate the parasitic pulse. This new design leaves the shaper-amplifier gain constant but disables the peak-detector circuit instead. This new design appears to

have no parasitic glitches and may be a better solution than the one presented here.

VI. ADC Reference Input Biasing

The pulse processing ASIC is designed to work with another circuit module which incorporates an ADC and histogramming memory features. The ADC in the companion module is an 8 bit flash ADC which utilizes a rather low impedance resistor "ladder" network on its reference inputs. Thus biasing the ladder consumes a sizable amount of power. To minimize system power consumption, the ASIC described here incorporates a ladder bias supply which biases the ADC only when the comparator has detected a pulse of valid amplitude.

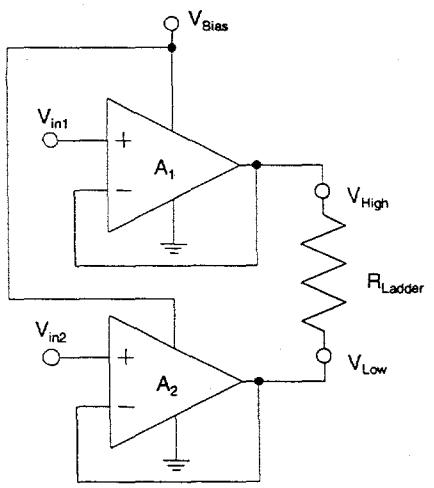

Figure 4. Diagram of the circuit used to provide biasing to the reference input of an external flash ADC.

A diagram of the circuit used in the ASIC to supply the required dc reference voltages for the flash ADC ladder resistor network is shown in **Figure 4**.

This circuit comprises two op-amp circuits, A_1 and A_2 performing a dual follower function. A_1 applies V_{High} to the top of R_{ladder} while A_2 applies V_{Low} to the bottom of R_{Ladder}. These voltages represent the highest and lowest measurable voltages the ADC will process at its input. Since the ladder resistor can range from 2 kΩ to 5 kΩ and the voltage range of the input will be approximately 5 volts, 2.5 mA (max) is required to bias this resistance. To minimize the system power requirements it is highly desirable to apply this bias voltage for the least amount of time possible. Thus this circuit is designed to apply V_{High}, and V_{Low} to R_{Ladder} only when a pulse has triggered the comparator and to be reset to zero bias shortly after the acquisition of the pulse. This is accomplished by using the comparator to bias the circuit via the V_{bias} node when a pulse trips the threshold voltage.

When biased "on", the opamps require approximately 160 μA of current each. They are designed to turn on quickly, have low-offset voltages and operate at minimum possible current.

VII. Peak Detector

The final stage of analog pulse processing that is performed by the ASIC is the peak sample and hold function. In conventional pulse processing systems the peak sample and hold is usually incorporated as part of the ADC, but we chose to incorporate as part of the pulse processing ASIC to minimize power consumption.

A simplified schematic of the peak detector used in this ASIC design is shown in **Figure 5**.

I_1 is approximately 120 μA and I_2 is approximately 50 μA. I_{idle} is 5 μA or 0 μA and is controlled by the comparator. I_{idle} is turned off when the output of the comparator senses an V_{thresh} input pulse. C_{peak} is an external 400 pF capacitor. A pnp (Q_1,Q_2) based differential-amplifier was chosen for this design. The input is biased at the system V_{ref} (1.25 V) from the shaper-amplifier. The input is on the base of Q_1 and the feedback from the peak hold capacitor, C_{peak}, is feedback to the base of Q_2. After a positive going peak has been held on C_{peak} and the input returns to base line dc, Q_2 will be cutoff and therefore the base current of Q_2 will be near zero and not discharge C_{peak}. Using this topology with an npn design would leave an active base on C_{peak} and allow a very significant discharge path. Q_3 is an emitter follower stage that guarantees that Q_2 cannot be saturated. When the circuit is idling or following a positive going signal Q_3 biases the collector to emitter voltage of Q_2 at approximately one diode drop. With I_{idle} "on" this circuit is essentially a low-offset, unidirectional

follower circuit. For good low-level accuracy and low overshoot I_{idle} is sourced from emitter of Q_5 until the threshold comparator trips and then I_{idle} is reduced to zero and a peak-hold is obtained. The offset of this design is also low because the Q_3 base-current is relatively small compared to the collector currents of Q_1-Q_2; allowing the differential amplifier to control the peak very accurately. The overshoot is essentially zero because the circuit is actively servoing the C_{peak} with all devices on and in the linear region of operation before V_{thresh} is sensed. When I_{idle} is turned off, the emitter current of Q_5 is determined by the charge current into C_{peak} and the circuit is very linear in operation. When the peak of the input has occurred and the input is decreasing, Q_2 and Q_5 are turned off and the current-leakage paths from C_{peak} are very low.

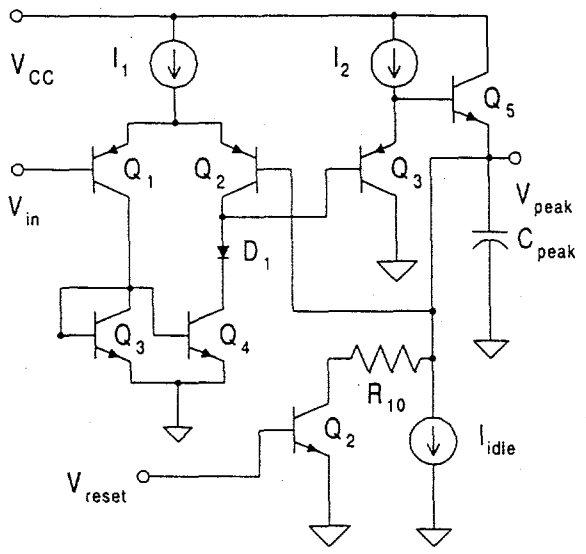

Figure 5. Schematic diagram of the peak sample and hold circuit used in the pulse processing ASIC.

One problem with this type of peak-detector design is that there is a limit to the amplitude of the detected signal. This limitation is the reverse breakdown voltage of Q_5 (approximately 5.6 V). To make this limitation have the least impact on the system performance, diode D_1 was added. This arrangement holds the collector voltage, Q_2, at one diode drop above ground plus the saturation voltage of Q_4 after a peak has been held and Q_4 is on hard. The addition of D_1 allows one diode drop greater peak voltage out before reverse breakdown of Q_5 occurs than if D_1 was not used (approximately 6.9 volts compared to 6.3 volts).

Finally, Q_2 and R_{10} make up a reset network. The system reset circuitry biases V_{reset} high to remove the charge on C_{peak} while R_{10} limits the current Q_5 can provide to ground during the reset process.

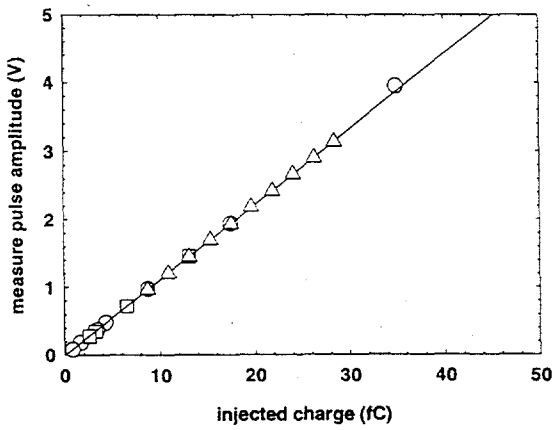

Figure 6. Measured output of the ASIC amplifier (charge and shaper) versus known charge injected to input.

VIII RESULTS

A version of the pulse processing circuit was built using Honeywell's ALB1A bipolar ASIC fabrication process. The resulting ASIC dice were 4 mm x 5 mm in size and were packaged in 40 pin leadless chip carriers (LCCs) for initial testing. The packaged ASICs were attached to a standard FR4 printed circuit board with surface mount external components for testing. Radiation detectors were attached to the ASIC test board using microdot and BNC connectors.

The gain and linearity of the ASIC module were measured by injecting a voltage pulse from an Ortec 419 Precision Pulse Generator into the input of the ASIC using an Ortec "charge terminator" (2 pF capacitor terminated 100 Ω to ground). The tail pulse generator and terminator had previously been calibrated with a silicon detector and the amount of charge injected into the ASIC was known to good precision. After injecting the fixed amplitude charge pulses into the ASIC input, the distribution of pulses produced at the output of the shaping amplifier was monitored with an Aptec Series 5000 multi-channel analyzer (MCA). The centroid of the peaks produced in the pulse height spectrum were used to determine the gain and linearity of the ASIC (**Figure 6**).

The output of the shaper amplifier was plotted versus a calibrated fixed charge pulse provided to the preamplifier input. Open symbols are measured laboratory data and the solid line is a linear fit to the data using a "least squares" algorithm. These data allow a determination of the overall system (preamplifier and shaping amplifier) gain and linearity. The slope of the least squares fit yields a system gain of 110 mV/fC (18 μV/electron), close to the original design specification. The correlation coefficient of the fit indicates a linearity of better than 0.1 %.

By measuring the width of the peaks in the pulse height spectra (using the apparatus just described), the noise of the circuit (ENC) was found to be 538 electrons rms (1270 electrons FWHM); well within the design specifications.

The ASIC was also operated in its intended mode- as a gamma-ray spectrometer- using two different detectors. The pulse height spectrum shown in **Figure 7** was obtained by irradiating a silicon p-i-n photodiode (Hamamatsu S1223) with a ^{57}Co source. The pulse processing ASIC was used to amplify and shape the pulses from the detector.

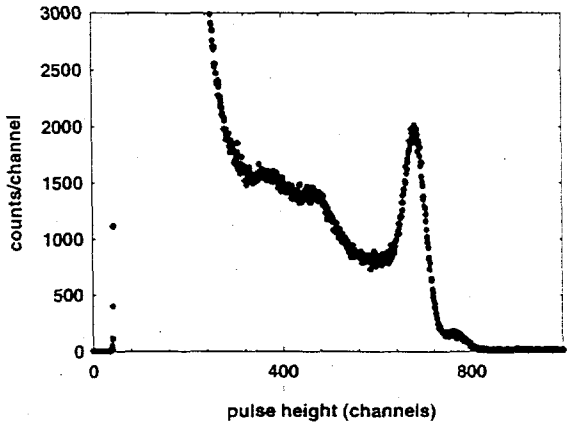

Figure 7. Pulse height spectrum of a ^{57}Co source taken with a silicon p-i-n detector and the electronics described in the text.

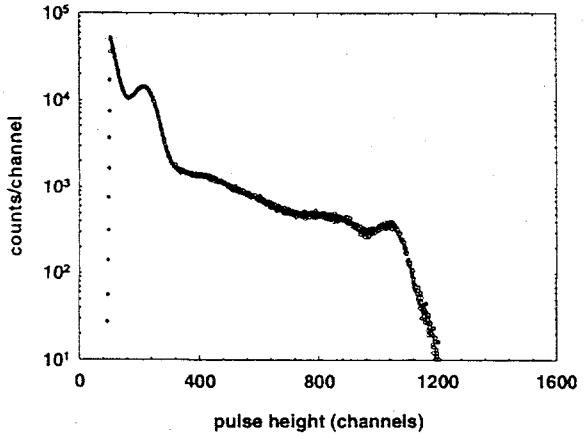

Figure 8. Pulse height spectrum of ^{133}Ba taken with a CZT detector and the electronics described in the text.

The same commercial pulse height analyzer (Aptec Series 5000) was used to histogram the pulse amplitudes and a ^{57}Co source was used to irradiate the detector. **Figure 8** shows a pulse height spectrum obtained with a CZT detector attached to the detector, and irradiated with a ^{133}Ba source.

The pulse height spectrum in **Figure 8** was obtained by irradiating a 15 mm x 15 mm x 2 mm CZT detector with photons from ^{133}Ba and reading out the detector with the ASIC described in the text. The CZT detector was of "spectroscopic grade" and was operated at a bias of 100 V.

The peak-detector circuit was also evaluated for droop (decay of the peak held voltage as a function of time), offset and overshoot. The droop measures approximately 100 μV/μs and the offset is less than 10 mV, this offset includes the buffer circuit. The peak-detector exhibits no measurable overshoot. The droop is caused by the comparator circuit input bias current. This droop is perfectly acceptable for our application due to the rapid digititization of the flash A/D. The peak detector need only hold the sample for approximately 10 μs before digitization, which implies a 1 mV maximum error; this is well below the overall system noise floor.

IX. SUMMARY

An ultra-low power consumption pulse processing circuit has been designed, constructed, and tested. The circuit is designed for use in an unattended monitoring application where multi-year operation from batteries is essential.

An ASIC embodiment of the circuit was constructed using Honeywell's ALB1A bipolar ASIC fabrication process. The resulting ASICs were tested and found to meet all of the design criteria necessary for use in the unattended monitoring application.

X. ACKNOWLEDGMENTS

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