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**A BREAKDOWN MODEL FOR THE BIPOLAR TRANSISTOR TO BE USED
WITH CIRCUIT SIMULATORS ***

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AUG 24 1993

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Abstract

A breakdown model for the output characteristics of the bipolar transistor (bjt) has been developed. The behavioral modeling capability of PSPICE, a popular SPICE program (with Emphasis on Integrated Circuits) was used to implement the macromodel. The model predicts bjt output characteristics under breakdown conditions. Experimental data was obtained to verify the macromodel. Good agreement exists between the measured and the simulated results.

Introduction

There is an increasing need for accurate modeling of the breakdown phenomena in bipolar transistors. None of the commonly available versions of SPICE have a breakdown model for the bipolar transistor. While the program is widely used as an electronic circuit design tool by designers, users can not rely upon SPICE for the calculation of breakdown voltages, even at a very basic level. The same deficiency exists with SABER, even though it is represented as a more powerful circuit simulator. Breakdown calculations for the bipolar transistor can become very complicated because of the interaction of external circuitry with the device breakdown phenomena. Even if the applied voltages are far below the breakdown level, there is a possibility of having large currents in the collector-emitter as a result of pre-breakdown effects. This may have significant effects on circuit operation. Cases of complete failure of integrated circuits, due to the lack of modeling the breakdown features, have been reported by industry [1]. The necessity for the development of an effective bjt breakdown model to be used with circuit simulators is thus felt.

Investigations into the physics of the breakdown mechanism and its mathematical

* This work was performed at Sandia National Laboratories supported by the US Department of Energy under contract number DE-AC04-76DP00789.

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formulation have been done by a number of researchers [2-5]. These works are based on the assumption that in a pn junction, the avalanche multiplication of carriers initiates the breakdown at a certain peak electric field. The value of the critical electric field determines the actual reverse breakdown voltage. A semi-empirical formula for the avalanche multiplication factor M is used in the calculations. The same approach is applied for the calculation of breakdown voltages in bipolar transistors. Although the approach supplies results of the right behavior, it is not in a form that can be easily implemented in circuit simulators. A macromodel, based on physical breakdown considerations has been developed and implemented in a circuit simulator program [6]. While the model predicts satisfactory results for the calculation of the breakdown characteristics of the bjt, it causes convergence problems in some practical circuit applications when it is implemented within the SPICE framework.

Considering all these limitations, there is a great need for a robust model which predicts bjt breakdown characteristics under any circuit arrangement and which does not cause convergence problems when implemented in common SPICE simulators. To determine if the model is robust several conditions need to be met. The family of output characteristic curves and the effect of the external base resistance on the breakdown voltage, BV_{cer} , should be simulated by the model. Typically, the circuit designer has a knowledge of the breakdown voltages, BV_{ces} and BV_{ceo} , measured at a specific current level I_{bv} (referred to as the breakdown current). The parameters associated with the breakdown model can be extracted from these values and the measured characteristic curves. Figures 1 and 2 show typical measured data for the breakdown voltages BV_{ces} and BV_{ceo} for an npn transistor for which the breakdown model parameters were calculated.

Description of the Model

The best approach is to develop a model based on the physical breakdown phenomenon of the device. To achieve this, two current sources are used to model the output breakdown effects (Figure 3). In the collector-base junction, the reverse leakage current is increased as the junction voltage increases and approaches the breakdown voltage. A current source flowing from the collector to the base is used to approximate this current. With the base terminal open, the current works as an effective base current that is amplified by the transistor action. In this case, the bipolar action of the transistor greatly increases the overall collector current and the breakdown voltage, BV_{ceo} , is lower than in any other configuration. On the other hand, if the base

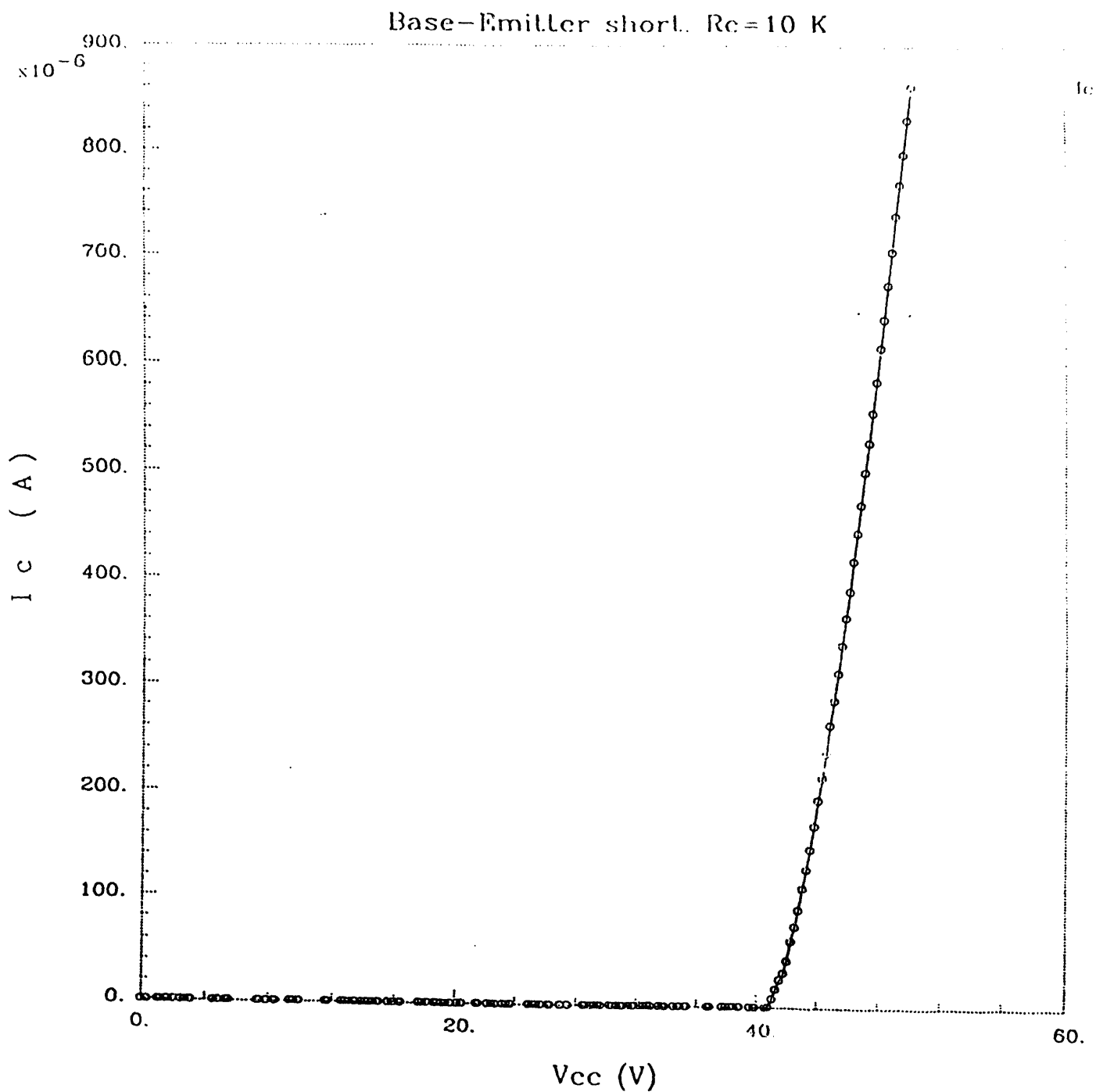


Figure 1. Typical measured breakdown characteristics with base-emitter junction shorted. The npn transistor of the linear array XQ2 was used.

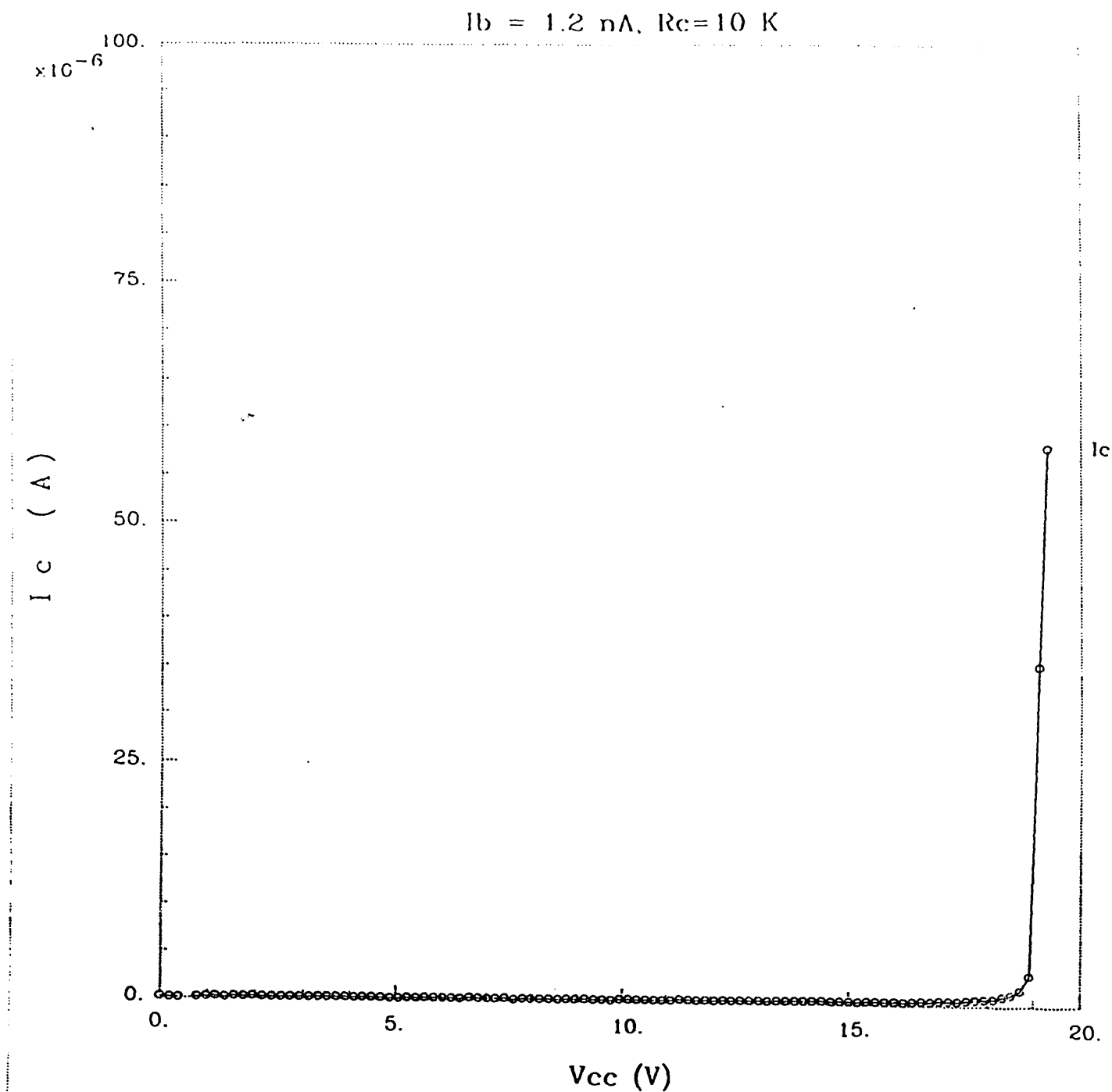


Figure 2. Typical measured breakdown characteristics with base-emitter junction open. A current source with a small input current of 1.2 nA was used to act as an open circuit at the base.

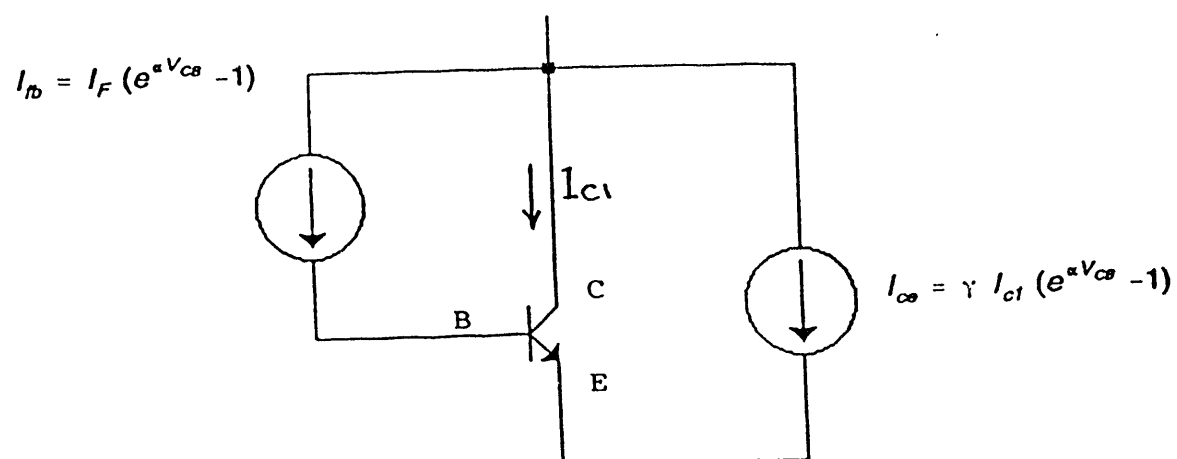


Figure 3. The bipolar transistor with additional circuit elements to model the breakdown phenomena.

is shorted to ground, the collector-base leakage current is not amplified by the transistor bipolar action. The increase in the collector current will then be limited to the increase in junction reverse current. For this reason, the breakdown voltage for this circuit configuration (BV_{ces}) is larger than BV_{ceo} . For other circuit configurations that have a net effective base resistance to the transistor, part of this current will be fed to the base. The result is that the breakdown voltage of the transistor will depend heavily on the resistive load seen by the base. Equation (1) shows the functional form of the current source used to model the breakdown effect in this junction.

$$I_{fb} = I_F (e^{\alpha V_{cb}} - 1) \quad (1)$$

However, the breakdown action of the transistor is not completely modeled by the inclusion of the reverse current for the collector-base junction. The forward collector current of the transistor, initiated by the emitter-base forward biased junction, gets amplified by the avalanche multiplication action of the collector-base junction. The additional component of the collector current is proportional to the collector current with no breakdown effects (I_{c1} in equation 2). This is the current that is initiated at the forward-biased emitter-base junction and injected into the collector-base depletion region. To model the effect of this additional avalanche effect, a second current source between collector and emitter is added.

$$I_{ce} = \gamma I_{c1} (e^{\alpha V_{cb}} - 1) \quad (2)$$

I_{c1} is the collector current without any multiplication effects. For any specific transistor, parameters α , γ , and I_F should be calculated from the measured breakdown characteristics. With small collector-base voltages, both current sources I_{fb} and I_{ce} will diminish and the transistor model will reduce to the normal Gummel-Poon model. At higher junction voltages, however, both current sources will contribute to the overall collector current. The extraction procedure for the breakdown parameters is described in an appendix at the end.

Results and Discussion

The breakdown parameters were calculated for an npn bipolar transistor used in the design of a linear IC designed at Sandia National Laboratories. The device characteristics were measured for a typical device and used for the breakdown parameter extraction procedures. A set of Gummel-Poon parameters extracted for the same transistor were also used for the SPICE

simulation. A PSPICE routine utilizing the complete macromodel of Figure 3 was then written and used for simulation purposes. Figure 4 shows a typical set of measured and simulated output characteristics of the device. More than one set of breakdown parameters can be calculated for any bjt. They all satisfy the breakdown voltage requirements, but exhibit different degrees of sharpness around the breakdown point. The calculated collector current does not actually go to infinity at BV_{ceo} because of the way the model is designed, but by proper choice of the breakdown parameters, the I-V curve at that point can have the desired shape and the necessary sharpness. Needless to say, the Gummel-Poon model would not predict any changes in the slope of the characteristic curves without the breakdown model added to the transistor. Equally important from a designer's point of view is the breakdown voltage of the transistor BV_{cer} with different values of base resistance R_b . Figure 5 shows the measured data together with predicted values of breakdown voltages by the model. It should be mentioned that in measuring breakdown voltages instabilities were observed for several resistor values and the data obtained was not very accurate. Similar types of difficulties have been reported by other researchers [1]. However, the overall features of the resulting curve are satisfactorily predicted by the simulated results, and an acceptable level of agreement exists between the measured and simulated curves. Both measured and calculated breakdown voltages decrease from a high value of BV_{ces} at $R_b = 0$ to a low value of BV_{ceo} at R_b open. The difference between the two curves is also partly due to the fact that the model is not entirely based on physical phenomena and is semi-empirical.

Applications

The breakdown model was tested in two application circuits to see the difference in circuit behavior response with and without the breakdown model implemented. Initially breakdown parameters were extracted for a linear array npn transistor with $BV_{ceo} = 18$ V and $BV_{ces} = 40$ V. The simulator used was PSPICE which is a SPICE based simulator. The first test circuit shown in Figure 6 is a Darlington configuration. A voltage pulse (5 Volts to 0 Volts) is applied to the base of the input transistor, and the collector voltage of the output transistor is monitored. The output signal is expected to go from a low level (saturation voltage) to a higher voltage level (off state). Resistor R_{B2} is varied from 1 kohm to 100 Megohm. Figure 7 shows the effect of R_{B2} on the output voltage waveform. If no breakdown model is implemented, the output voltage equals 50 Volts, the value of V_{cc} , irrespective of the resistance value for R_{B2} . This clearly is not the expected response, since in reality both breakdown voltages (BV_{ces} and BV_{ceo}) are below this

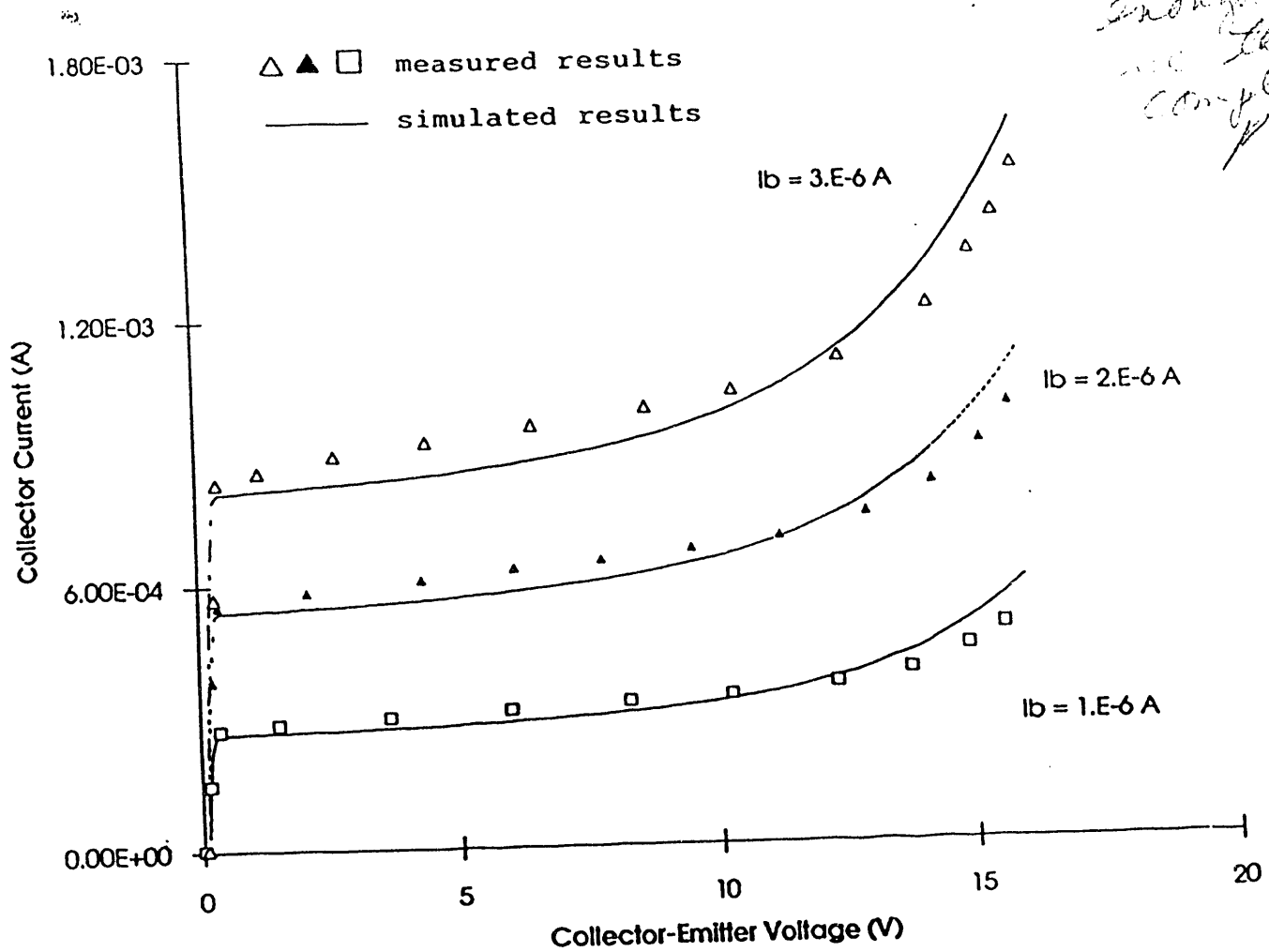
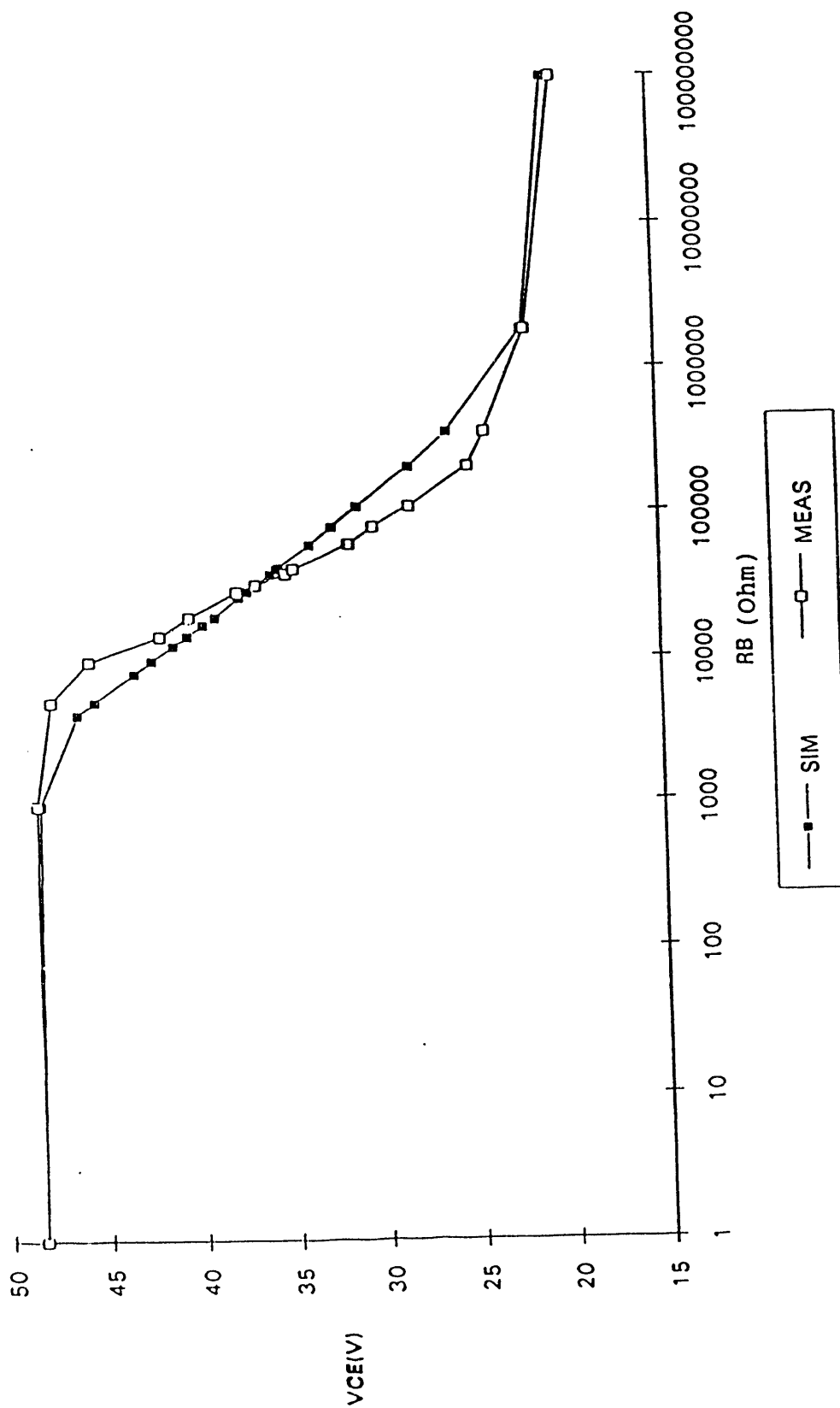


Figure 4. Typical measured and simulated output characteristics for the linear array npn transistor.

Figure 5. Typical measured and simulated results of the transistor breakdown voltage with different values of base resistors.

BVCER FOR LINEAR ARRAY NPN XQ2



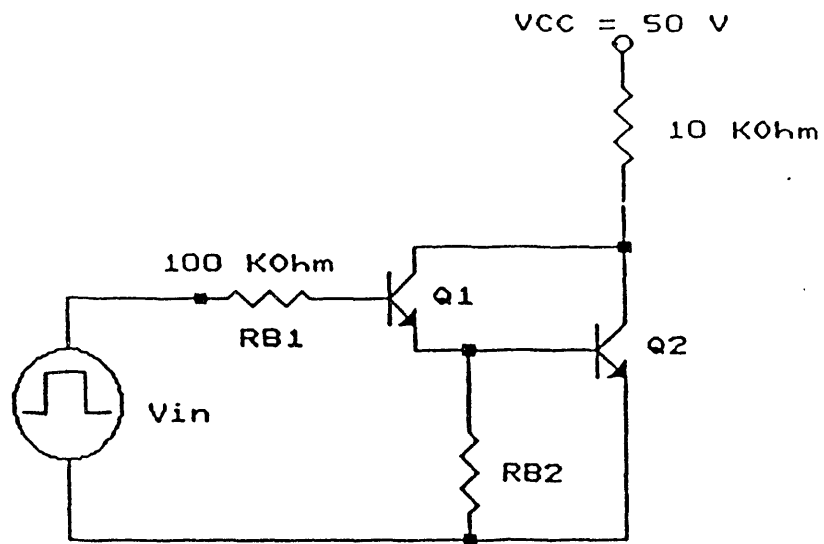


Figure 6. The Darlington amplifier configuration simulated using the breakdown model.

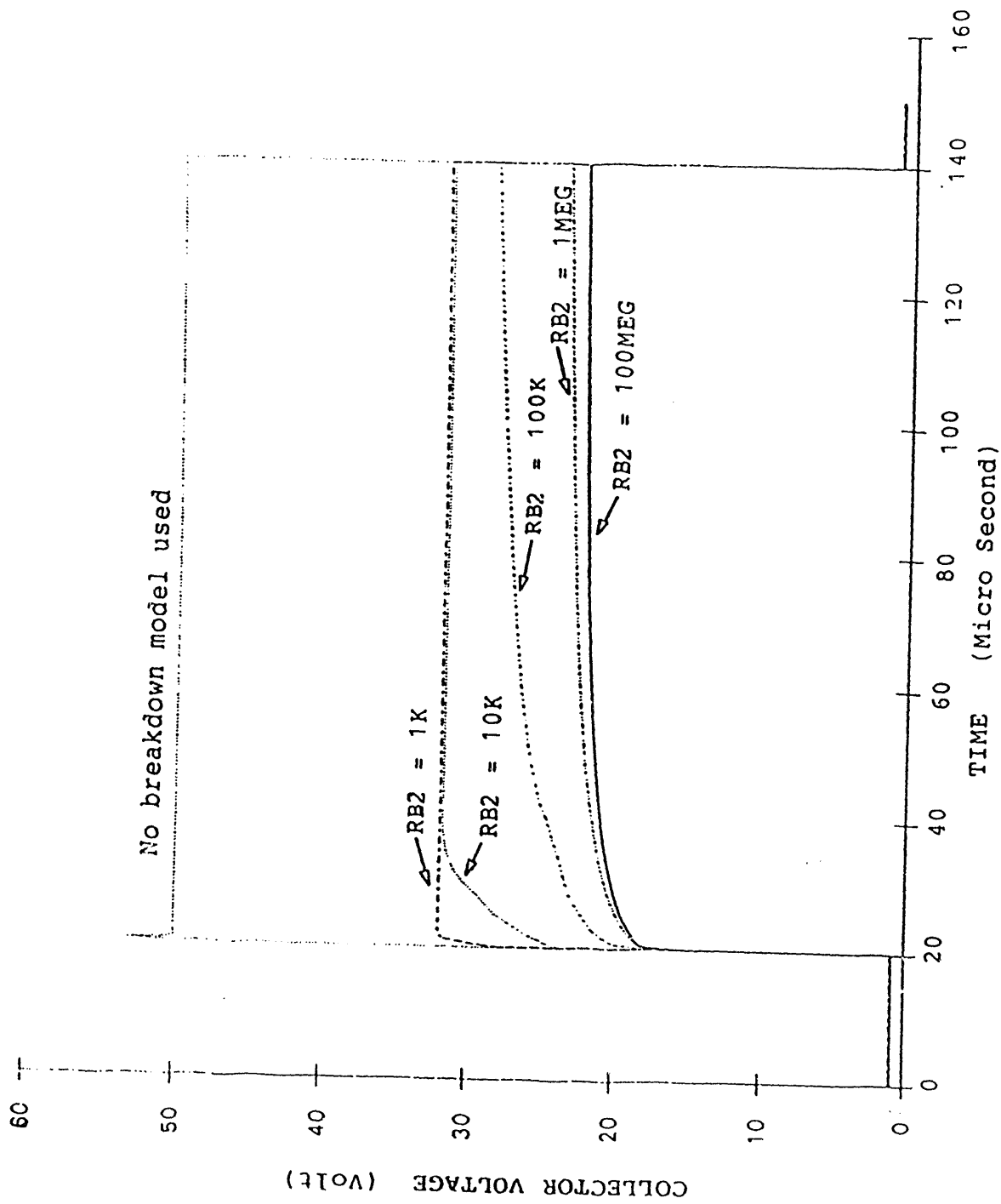


Figure 7. Simulation results showing the effect of RB2 values when the breakdown model is used. RB2 has no effect if no breakdown models are used (upper curve).

voltage level. On the other hand, when the breakdown model is implemented, the simulated output signal varies as one would expect. In this case, as seen in Figure 7, the output level strongly depends on the resistance values used. For smaller resistance values, the collector voltage settles to values below $BV_{ces} = 40$ V. As the value of R_{B2} is increased, the output voltage approaches $BV_{ceo} = 18$ V, as expected.

The second test circuit used for simulation was a current mirror circuit shown in Figure 8. A sinusoidal current source with a magnitude of 10 micro A in parallel with a 2.5 Meg Ohm resistance is applied at the collector of Q_2 . The sinusoidal current will then periodically change the collector voltage of the transistor. In the absence of a breakdown model in the simulation, the collector voltage obtains a high level as shown in Figure 9. In reality, Q_2 will reach a breakdown voltage at a lower level (which can be difficult to calculate due to the complexity of the circuit on the base side of this transistor). This behavior is predicted when the breakdown model is implemented. The peaks of the collector voltage in this case are much lower and closer to the expected results. In fact the initiation of breakdown at voltage levels below BV_{ceo} causes increases in the collector current of Q_2 which in turn causes a voltage drop across the large collector resistance and keeps the collector voltage below the expected breakdown level.

The two previous examples are typical indications of the differences observed when the breakdown model is used in simulations as compared to the cases when no breakdown model is implemented. Without a breakdown model, results can be significantly wrong and deceptive to the designer. The two examples indicate the impact of the breakdown model on the simulation results and clearly show the possible differences in results when the breakdown model is used.

Appendix

Extraction of the breakdown parameters

The breakdown model of the bjt, as defined by equations 1 and 2, requires three parameters to be extracted for each specific device. These are I_F , α , and γ . Different methods can be used for the extraction of these parameters. At least two methods were formulated and used for this purpose. Each method is based on a certain number of

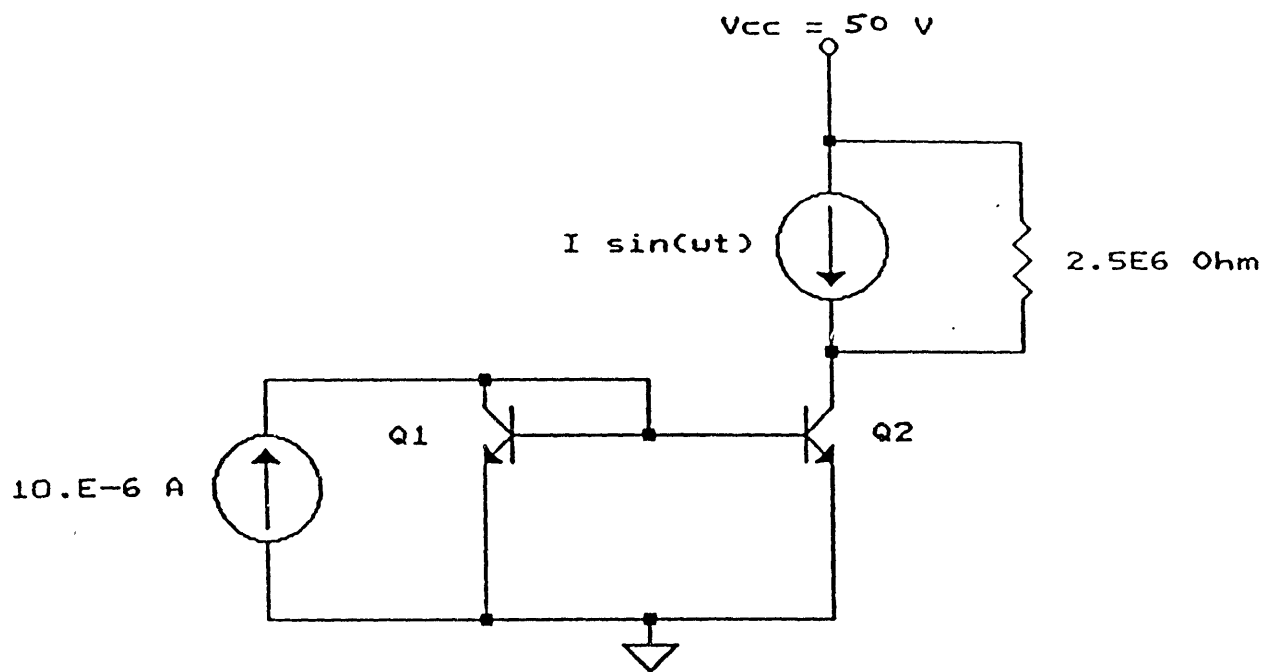


Figure 8. The current mirror circuit simulated to see the effect of the breakdown model on the circuit response.

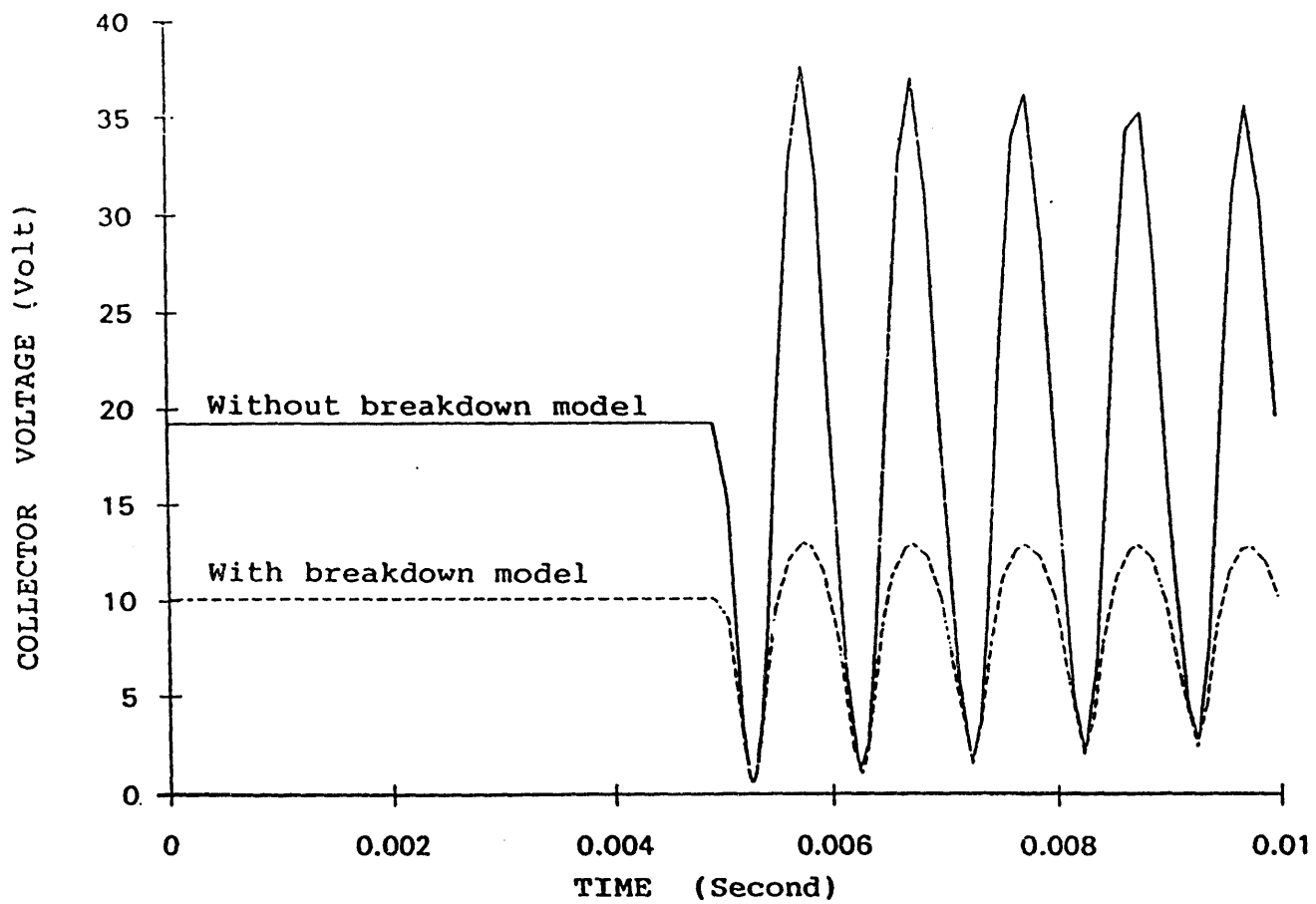


Figure 9. Simulation results for the current mirror circuit showing the effects of the breakdown model.

requirements on the breakdown model.

Method 1- This method was based on the requirements that BV_{ces} and BV_{ceo} at a specified current be satisfied and that the output characteristic curve should pass through a specified point near the breakdown point BV_{ceo} . The approach works, but a general concern was that the resulting output characteristics did not show the expected level of "sharpness" at the breakdown point and after that. In other words, the measured output characteristics increased at a faster rate after the breakdown point was reached. The shape of the output characteristics will depend on the point picked on the measured curve. After choosing the requirements for the model, the next step is to develop a method for the extraction of the breakdown parameters. Here is a description of the method used for the parameter extraction procedure using the above requirements.

To satisfy the BV_{ces} requirement at a breakdown current of I_{bv} we should have :

$$I_{bv} = I_F (e^{\alpha BV_{ces}} - 1) \quad (3)$$

Equation 3 is based on the assumption that at the breakdown point when the base is shorted to the emitter, the major collector current flowing is the breakdown current as shown in Figure 10.

To have the breakdown conditions satisfied with the base open, the breakdown voltage should be BV_{ceo} with a collector current of I_{bv} . Figure 11 shows the currents flowing under this circuit configuration and we have :

$$I_{bv} = I_{fb} + I_{c1} + I_{ce}$$

$$I_{bv} = I_F (e^{\alpha V_{cb}} - 1) + \beta I_F (e^{\alpha V_{cb}} - 1) + \gamma I_{c1} (e^{\alpha V_{cb}} - 1) \quad (4)$$

where β is the forward current amplification factor of the transistor. Making the simplifying assumption that $V_{cb} = V_{ce} = BV_{ceo}$ at the breakdown point (with base open), and noting that $I_{c1} \approx \beta I_F (e^{\alpha BV_{ceo}} - 1)$, equation 4 can then be written as follows :

$$\gamma = \left(\frac{I_{bv}}{I_F (e^{\alpha BV_{ceo}} - 1)} - (\beta + 1) \right) \frac{1}{\beta (e^{\alpha BV_{ceo}} - 1)}$$

This equation is simplified by substituting for I_{bv} from equation 3 and also assuming that $e^{\alpha BV_{ceo}}$

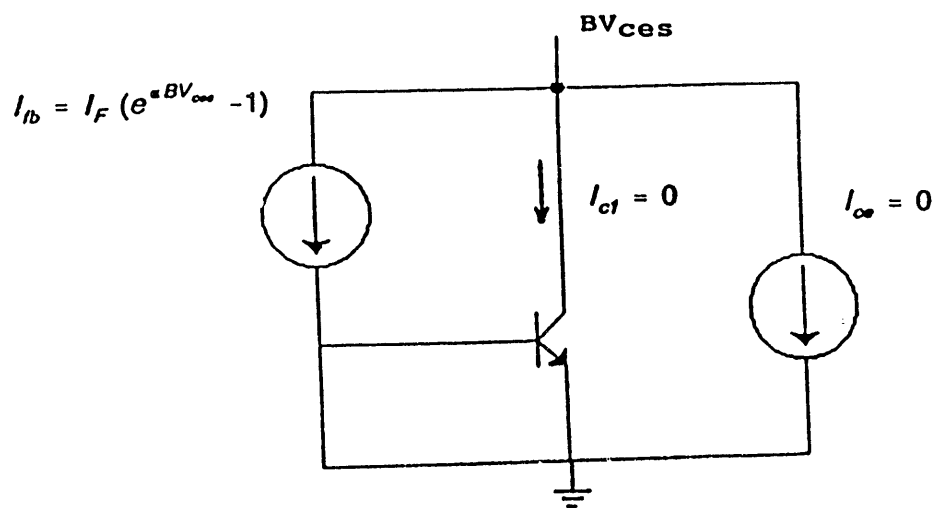


Figure 10. Major components of current under base-emitter short circuit conditions at the onset of breakdown (BV_{ces}).

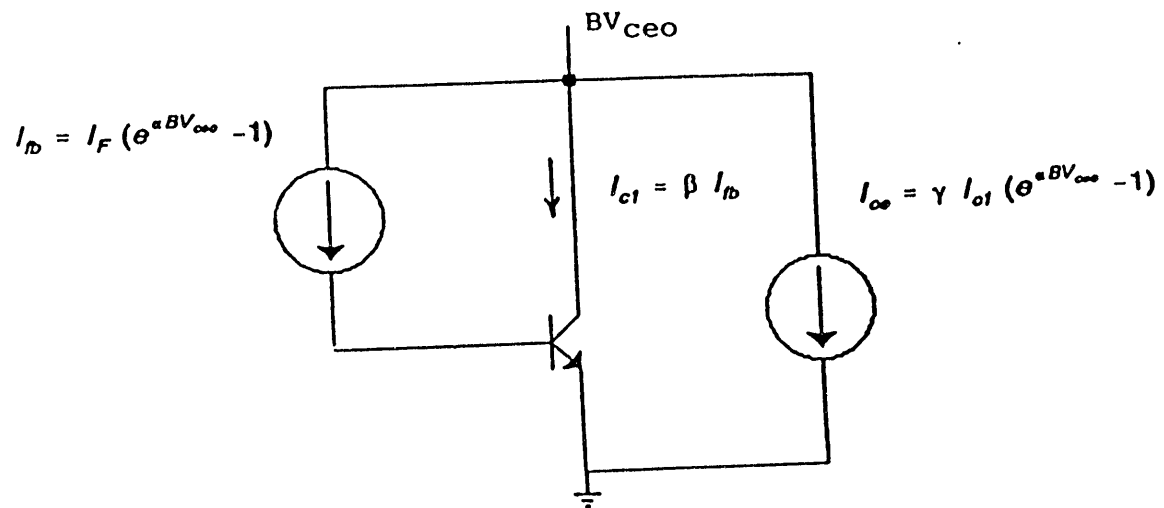


Figure 11. Major components of current under base-emitter open circuit conditions at the onset of breakdown (BV_{ceo}).

> > 1.0 which will justify ignoring the term 1 as compared to the exponential terms. The new form of this equation will then be :

$$\gamma = (e^{\alpha (BV_{ces} - BV_{ceo})} - (\beta + 1)) \frac{1}{\beta e^{\alpha BV_{ceo}}} \quad (5)$$

The third equation needed for the calculation of the breakdown parameters is formed by forcing the output characteristics to pass through a certain point. This point should be chosen close to the breakdown point so that breakdown characteristics will be dominant. We designate the device voltage and current corresponding to this point as V_{cem} and I_{cm} and write the general equation for the transistor current as follows :

$$I_c = I_{fb} + I_{c1} + I_{ce}$$

If the measured data points V_{cem} and I_{cm} are chosen so that the device is not deeply into breakdown, then I_{fb} can be ignored with respect to the other two terms. We also make the simplifying assumption that $V_{cem} = V_{cbm}$, that, is the base-emitter voltage is ignored with respect to the collector-base voltage. From the measured data, we have the value of the base current I_{bm} for the data point and the above equation can be rewritten as below :

$$I_{cm} \sim I_{c1} + I_{ce} = \beta I_{bm} + \gamma \beta I_{bm} (e^{\alpha V_{cbm}} - 1) \quad (6)$$

To solve for the three unknown parameters, the general approach is to delete the parameter γ from equations 5 and 6 which gives a nonlinear equation in the form of e^{I^α} . By defining a new variable $y = e^{I^\alpha}$, the equation will be changed to a new simpler form and can be written as

$$y^p = a + \frac{b}{y} \quad (7)$$

where a , b , and p are real variables depending on the breakdown voltages and breakdown current as well as the additional measured data point used in the calculations. This equation can be easily solved with numerical methods which supplies the value of y and hence α . No convergence problems were ever observed for several cases tried. The calculated value of α can then be used in equation 3 to calculate I_F and in equation 6 to calculate γ .

Method 2 - In order to improve the shape of the simulated curves in the vicinity of the breakdown point, a second approach was developed. In order to meet the breakdown requirements defined in the first method, equations 3 and 5 have to be used again. The third equation needed for the solution of the parameters, however, will be different from equation 6. Figure 12 helps understand how the next condition is imposed on the output characteristic curve. With the base open and no input currents, the collector current rises exponentially after BV_{ceo} . At a voltage point of $V_{cb} = n BV_{ceo}$, the current will be $I_c = m I_{bv}$. By choosing proper values for n and m , the sharpness of the curve after the breakdown point will be controlled. Both n and m will be larger than unity. Good characteristics were obtained from values of $n = 1.1$, $m = 2.5 - 3.0$. A simple program was written to supply sets of breakdown parameter values for $n = 1.1$ and m ranging from 1.1 to 4.0. As the m value increases, the curves will show more "sharpness" after the BV_{ceo} point. This method of parameter calculation shows more natural and acceptable breakdown characteristics.

The new condition supplies a new equation as shown below as opposed to equation 6.

$$\gamma = (me^{\alpha (BV_{ces} - n BV_{ceo})} - (\beta + 1)) \frac{1}{\beta e^{\alpha (n BV_{ceo})}} \quad (8)$$

Deleting γ between equations 5 and 8 and defining $y = e^{(n-1) \alpha BV_{ceo}}$, a new nonlinear equation will be obtained. This equation can be arranged as shown below and a simple numerical approach can solve it.

$$y^{P1} - my^{(P2-1)} = \beta + 1 - \frac{\beta + 1}{y} \quad (9)$$

where

$$P1 = \frac{BV_{ces} - BV_{ceo}}{(n - 1) BV_{ceo}}$$

and

$$P2 = \frac{BV_{ces} - n BV_{ceo}}{(n - 1) BV_{ceo}}$$

Typical calculated values for the breakdown model parameters are : $I_F = 1.3023E-9$, $\alpha =$

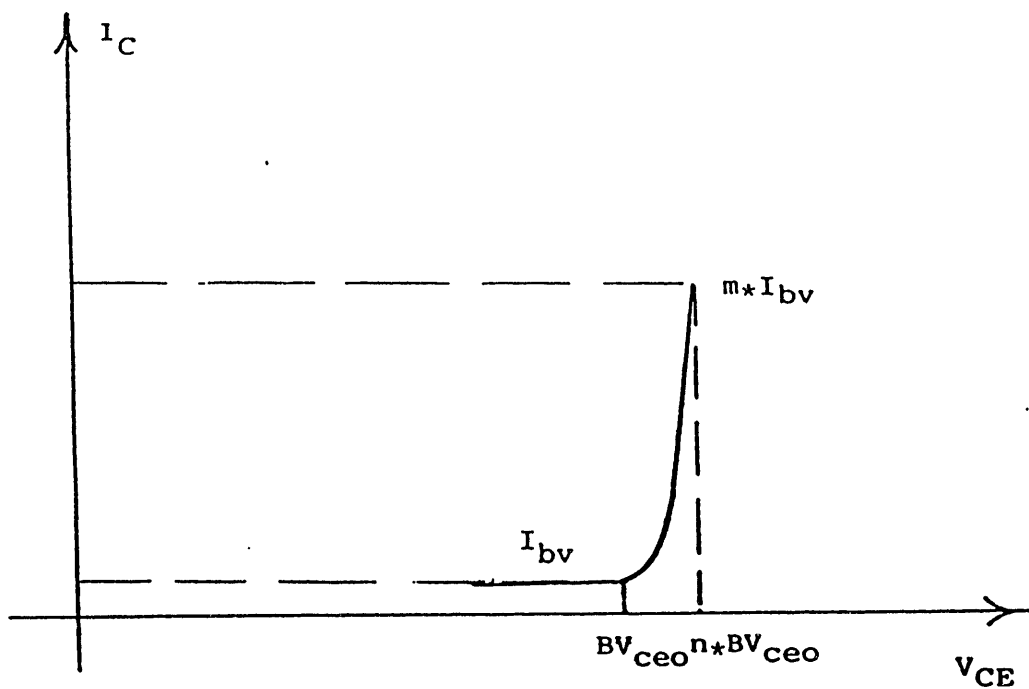


Figure 12. Definition of parameters m and n used to control the shape of the breakdown characteristics after breakdown. Both m and n are greater than unity.

0.30092, and $\gamma = 0.00766$. Figure 5, shown previously, is a typical comparison of measured and simulated results which use these parameters in the breakdown model. Figure 13 shows the effect parameter m has on the "sharpness" of the output characteristic curve. For $n = 1.1$, different breakdown parameters can be calculated as m is varied from 1.5 to 3. As indicated in Figure 12, sharper curves can be expected as larger values of m are used in the parameter calculations. Still, for each set of parameters, the breakdown voltages BV_{ceo} and BV_{ces} are the same. However, Figure 13 clearly shows the changes in the output characteristics for different values of m . For the npn transistor in the linear array used for extraction purposes, a value of $m = 2.5$ was chosen as the best value supplying the closest output fit between the measured and simulated results.

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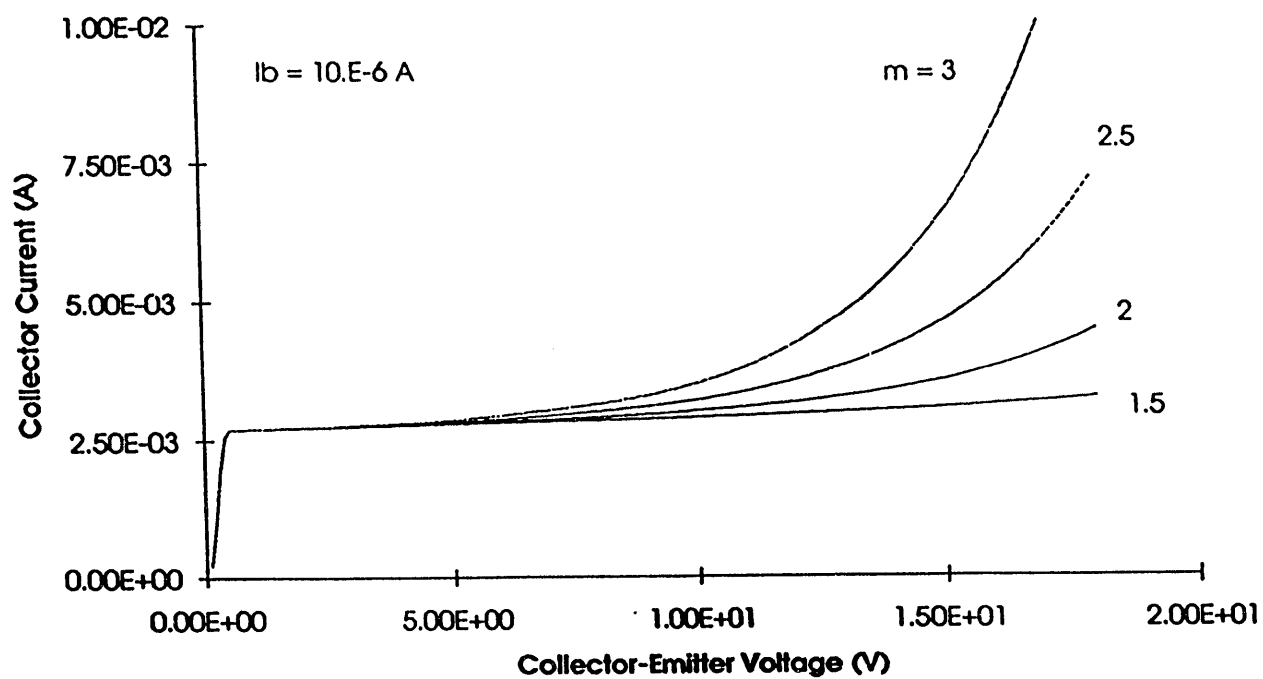


Figure 13. Effect of parameter m on the "sharpness" of the output characteristic curves. A constant value of $n=1.1$ was used for all cases.

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