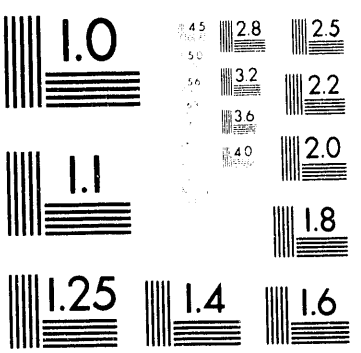
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Case History: Failure Analysis of a 16K ROM with a Polysilicon Gate Defect

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ABSTRACT

This case history presents the analysis of a very unusual CMOS 2K x 8 read only memory (ROM) failure. The IC failure was discovered after a 1000 hour, 150 °C static life test. Elevated quiescent power supply current (I_{DDQ}) was present that caused the IC to fail parametric testing, but the IC was fully functional at the specified operating power supply voltage of 10 V. Functional failures were "forced" by operating the IC at below nominal voltage. Electron beam probing and dynamic voltage contrast imaging performed while the IC was in the functional failing mode indicated the presence of an electrical open circuit in the polysilicon gate interconnect of a *p*-channel transistor. The IC was deprocessed down to the polysilicon and the defective gate was examined with a scanning electron microscope (SEM). An abrupt change in microstructure was observed at the location corresponding to the site of electrical discontinuity. Circuit simulations, performed using a series gate resistance to model the defective gate, showed that the gate signal to the *p*-channel transistor changed phase and high current (I_{DDQ}) was present if the gate resistance exceeded $1 \times 10^9\ \Omega$. The change in microstructure and increased gate resistance are consistent with a localized reduction of dopant (phosphorus) concentration. The reduction may have been initially caused by a particle masking that area during phosphorus implant. During the life test, it is speculated that phosphorus segregated to the grain boundaries resulting in a net reduction of dopant atoms and a corresponding decrease in the conductivity of the polysilicon gate. This IC failure is apparently due to dopant segregation and carrier trapping at the grain boundaries in the polysilicon during the high temperature life test.

The IC described in this case study was initially detected while monitoring the power supply current during the application of a functional vector set. For static CMOS design ICs, the monitoring of the quiescent power supply current, I_{DDQ} testing, is a sensitive method to detect defects in high reliability components [1]. This measurement was the first indication that the component was defective. The failing IC, a 2K x 8 ROM, was manufactured with a 3 µm, radiation-hardened, silicon gate CMOS technology, packaged in a 40-pin leadless chip carrier (LCC), and hermetically sealed with a Kovar® lid. The process and techniques used to diagnose this failure are described and the reliability implications are discussed.

HISTORY AND DESCRIPTION OF FAILING INTEGRATED CIRCUIT

A 1000 hour static life test at 150 °C was performed according to the product specification as part of the qualification of this IC. Prior to the life test, this IC underwent a dynamic screen (11 volts at 150 °C) with the IC operating for 24 hours and a static burn-in test (12 volts at 150 °C) with unchanging inputs for 168 hours. All electrical tests for qualification purposes were performed with Schlumberger's Sentry 20 tester. The electrical tests include both parametric (current and voltage) and functional testing.

Interim Sentry testing at 168 and 504 hours showed the IC passing all product specifications. I_{DDQ} failures of the component were detected at the completion of the life test (end-point testing at 1000 hours). Normally, I_{DDQ} for this component is less than 100 nA. On the failing vector, I_{DDQ} was greater than 200 mA. Correlation of the vector set to the electrical measurements showed that the high current occurred on vectors that activated or set to a logical high state the address latch enable (ALE) and read (RD) input pins.

FAILURE ANALYSIS OF THE ROM

For this IC, the nominal power supply voltage (V_{DD}) is 10 V. A modification was made to the Sentry test program that allowed a variable power supply voltage. For V_{DD} at 7 V or below, the IC not only exhibited the I_{DDQ} failure mode but also failed to function properly. Specifically, a "stuck-at-0" fault occurred for the address/data pin-4 (AD4).

The failing IC passed fine leak, gross leak, and x-ray tests before lid removal. Prior to lid removal, the IC package was examined for any external anomalies; none were found. After lid removal, the IC passed an initial optical microscope inspection of the internal package and die.

1.0 Light Emission Studies

Initially, light emission experiments were performed on the IC using KLA Instrument's Emission Microscope for Multi-layer Inspections (EMMI) while the IC was stimulated with the Sentry tester. The use of the Sentry tester and the product specification test program was necessary because the laboratory test equipment had not yet been assembled. Anomalous light emission was observed in the CMOS peripheral circuitry adjacent to the AD4 pin. (These data were not suitable for publication.)

A Hewlett Packard HP81810 tester was used throughout the remainder of the analysis to repeat the light emission inspections. Figure 1 shows light emission data obtained near the AD4 pin with V_{DD} = 7 V. The area of light emission is indicated in the image by the black region left of center (see arrow). The intensity of light emission increased when V_{DD} was greater than 7 V and detectable light emission ceased when V_{DD} was reduced below 7 V.

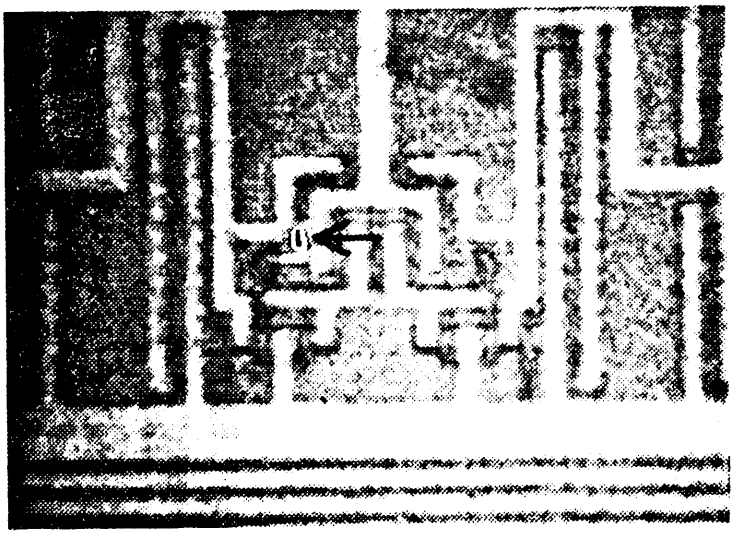

Figure 1. Light emission observed from AD4 port cell; V_{DD} = 7 V. The arrow denotes the location of light emission.

2.0 Electron Beam Studies

As mentioned previously, Sentry testing with V_{DD} = 5 V showed functional failures on the AD4 pin. Figure 2 is a simplified electrical schematic diagram of the AD4 port cell. While the IC was in this stuck-at-0 functional failure mode, the HP81810 and SEM tool of Schlumberger's IDS 5000 electron beam prober revealed that the output holding latch located in the AD4 port cell was not holding the data line (D4) at the proper pre-charge voltage. The output stage of the latch circuit that was found defective is shown shaded in the diagram.

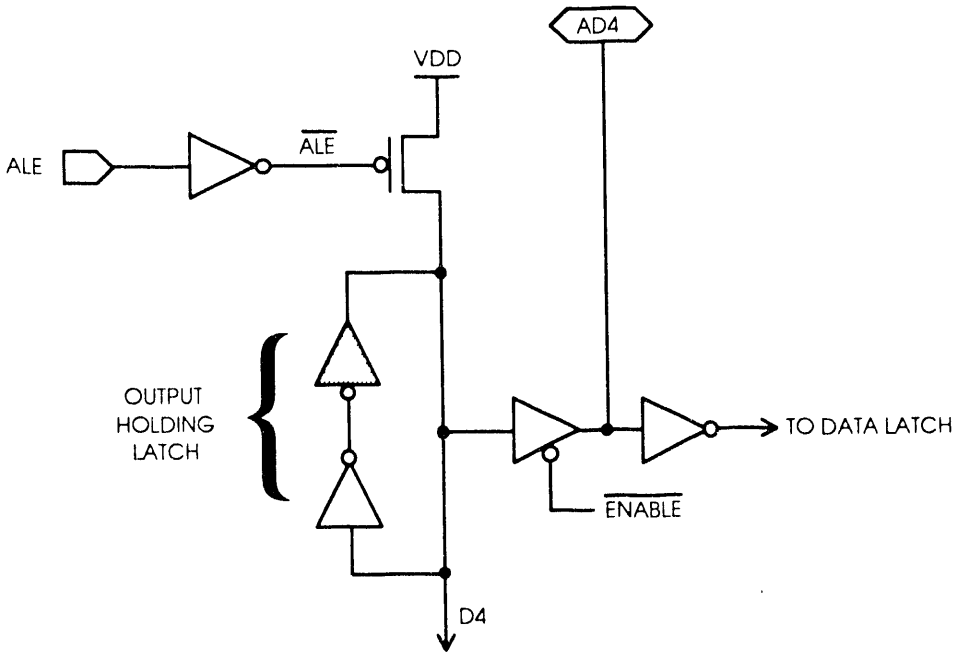

Figure 2. Schematic diagram of the AD port cell of the 16K ROM. The defective output stage of the latch circuitry is shaded.

A dynamic voltage contrast image of the AD4/AD5 output holding latches during the functional failure mode is shown in Figure 3. Voltage discontinuity is shown as an abrupt image contrast change on the *p*-channel transistor's polysilicon interconnect/gate of the AD4 latch output stage. The discontinuity is located in the center of the box in the left half of the image. The anomalous contrast of this interconnect can be compared with the uniform interconnect potential of the AD5 *p*-channel transistor's gate which is shown in the right half of Figure 3. (The AD5 latch layout is a mirror image of the AD4 latch layout.)

Figure 4 is an optical photomicrograph of the AD4 latch. The portion of the polysilicon interconnect where electrical discontinuity was observed is located inside the box. The field oxide step at which the potential change of Figure 3 occurs is indicated by the field oxide step arrow. The various metal (aluminum) and polysilicon interconnect layers are labeled in this figure. The nominal width of the polysilicon interconnect is 3 μm.

Electron beam probing of the gate area associated with the oxide step using the waveform tool of the IDS 5000 showed a marked change in the acquired waveforms of the polysilicon interconnect/gate. As we will discuss below, the voltage changed abruptly in magnitude and phase as a function of position along the length of the polysilicon interconnect. Figure 5 shows the section of the polysilicon that was probed. The numbers labeled on the image correspond to IDS 5000 acquired waveforms of Figure 6. In Figure 6, probe_1 through probe_3 correspond to the expected electrical potential of the polysilicon interconnect. (The full voltage swing of 10 V is not observed since attenuation of the signal(s) is due to the interlevel dielectric and passivation layers.) Wave_4 through wave_6 represent the region of transition. Wave_7 corresponds to the *p*-channel transistor's actual gate potential. It is clear that between wave_3 and wave_7 there is a dramatic change in the electrical waveforms, indicating a loss of electrical continuity. The gate signal becomes noisier and eventually becomes inverted. (Note that wave_6 shows the complete degradation of the *p*-channel transistor's gate voltage.) For a normal interconnect/gate, all waveforms would appear nearly identical to wave_1 regardless of the probe location.

3.0 Chemical Deprocessing

A series of experiments using both dry (CF_4-O_2 chemistry) and wet etch processes were performed on sample die to determine the best process for revealing the morphology of the polysilicon gate. Optimum selectivity and best results were obtained by using several selective wet etch processes with semiconductor grade chemicals for the different dielectric and conductor levels. All etching was performed in room ambient lighting.

A dilute glass etch (NH_4F:CH_3COOH:H_2O = 2:2:1 at 27 °C) was used to remove the passivation layer to expose the aluminum interconnects. An aluminum etch (H_3PO_4:H_2O:HNO_3 = 19:4:1 at 60 °C) was then used to remove the interconnects and bond wires. The dilute glass etch was used again to remove the majority of the interlevel dielectric and, finally, a buffered oxide etch (NH_4F:HF =7:1 at 27 °C) was used to remove the remaining interlevel dielectric layer and delineate the grain structure of the polysilicon interconnects.

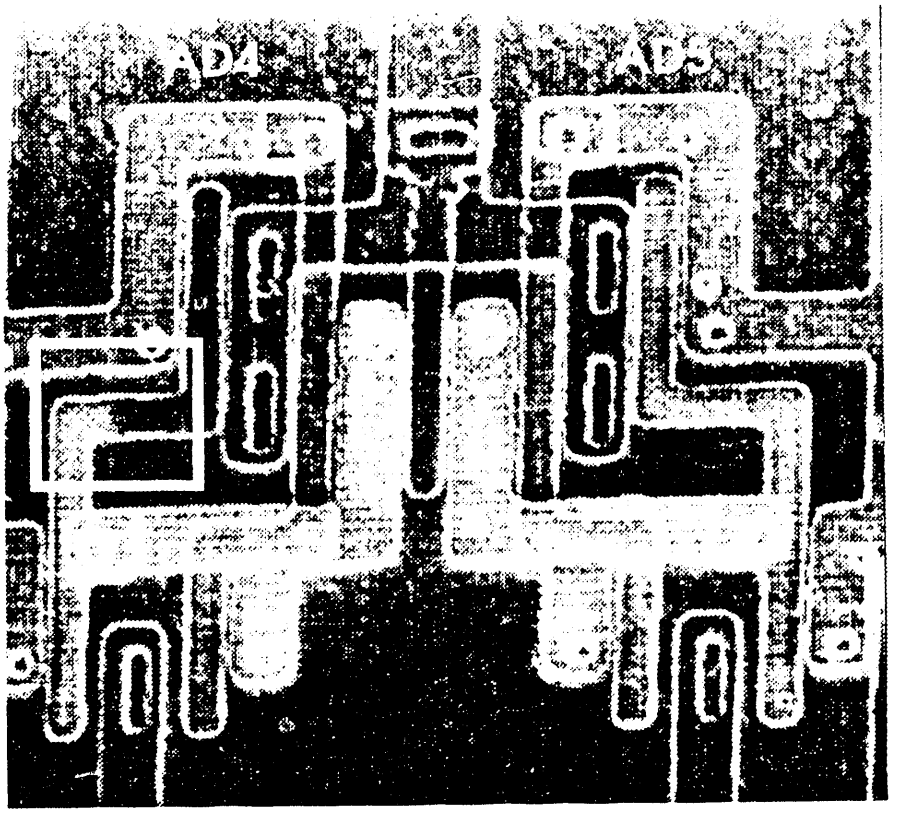

Figure 3. Voltage contrast image of the AD4 and AD5 port cell latches. The highlighted region in the left center of the image denotes the location of electrical discontinuity in the AD4 latch.

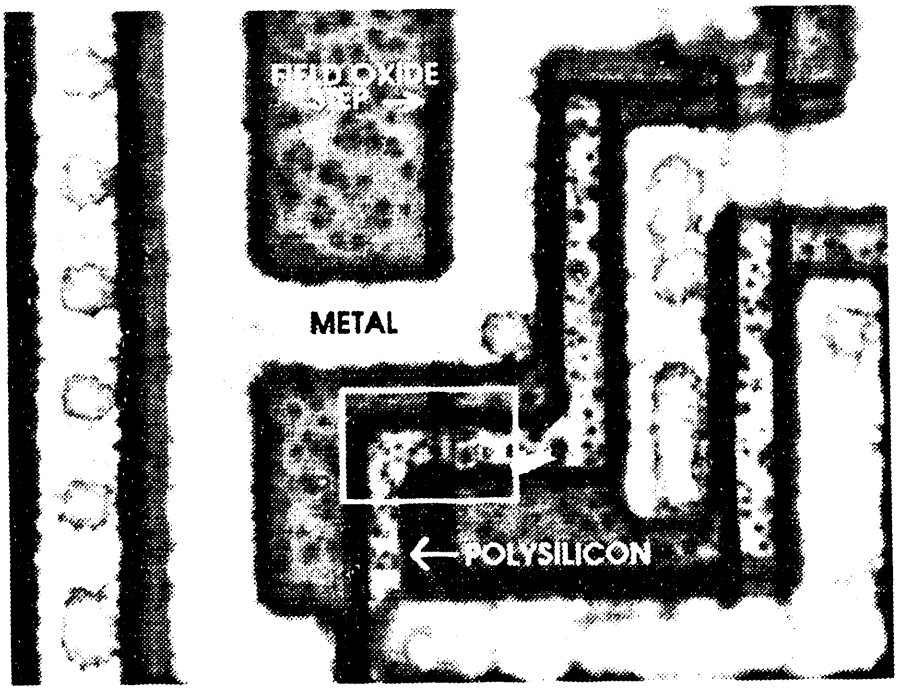

Figure 4. Higher magnification optical photomicrograph of the AD4 *p*-channel polysilicon interconnect. Nominal width of the polysilicon is 3μm.

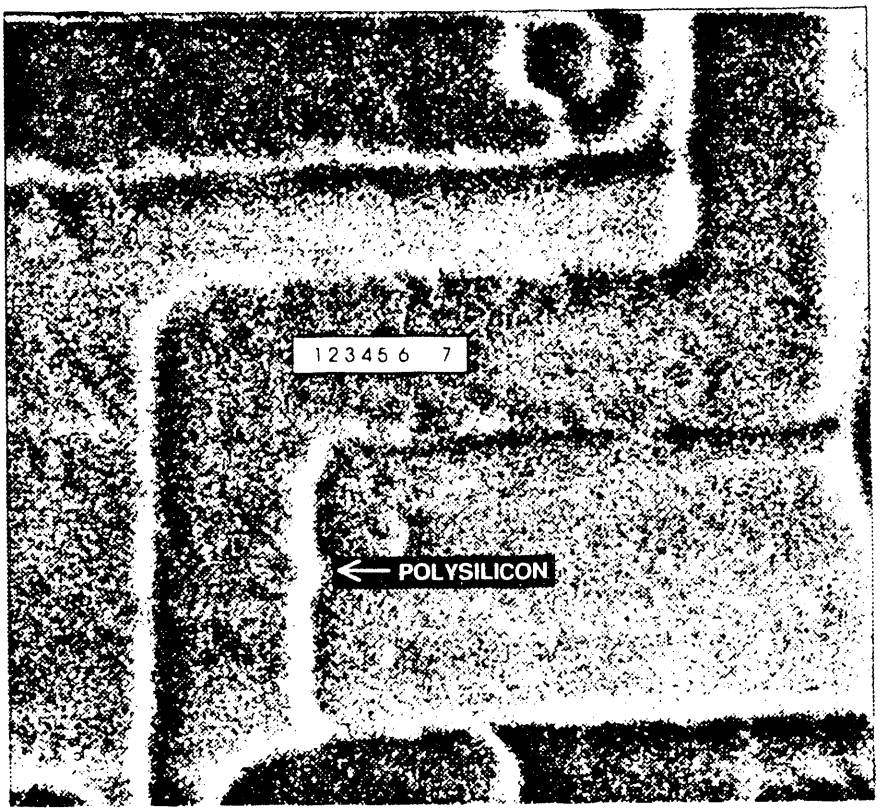

Figure 5. SEM image of the probed section of the defective polysilicon interconnect. The numbers denote the probing positions during IDS 5000 waveform acquisition.

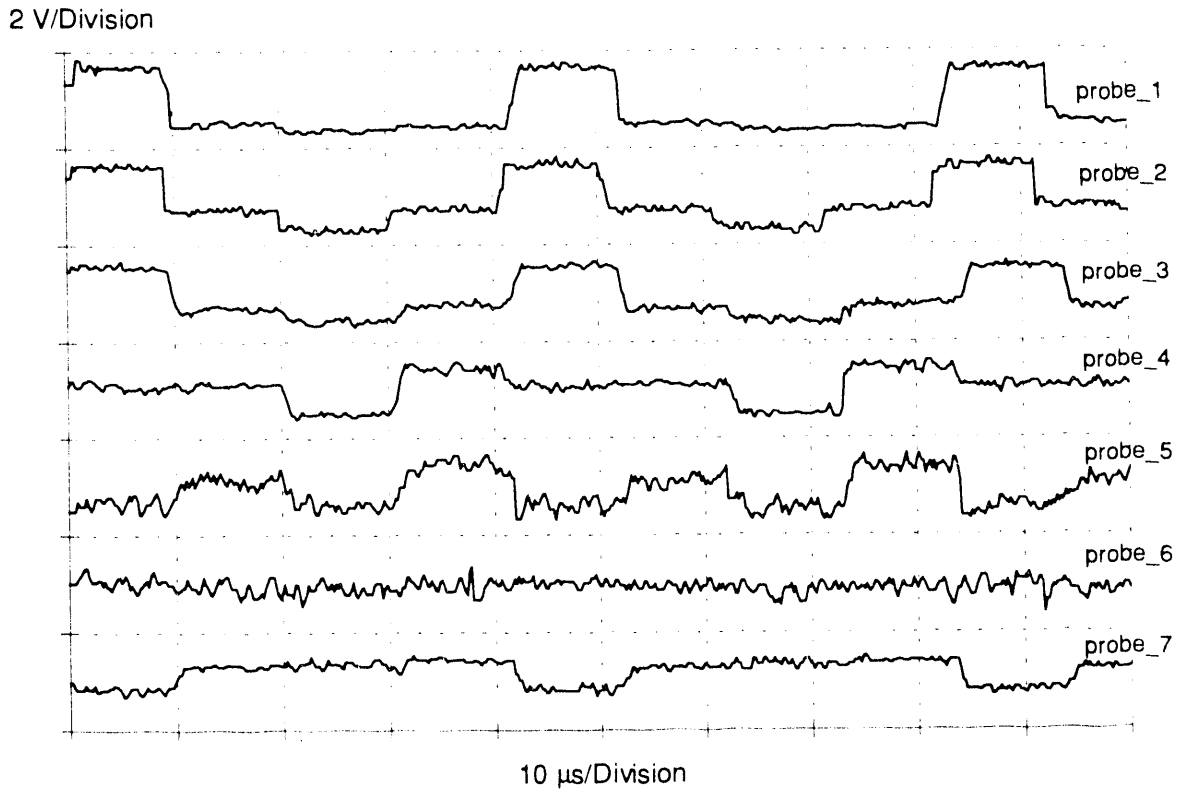

Figure 6. IDS 5000 waveforms obtained with reference to position on polysilicon gate (see Fig. 5).

4.0 Electrical Studies

After the polysilicon gate was exposed, DC current measurements were performed to assess the current-voltage characteristics of all the *p*-channel transistor gates that are associated in the output stage of the latches. An HP4145 parameter analyzer, a Keithley 616 electrometer, and a Micromanipulator mechanical probe station were used to acquire the electrical data. Current measurements on the *p*-channel transistor gates were obtained by placing mechanical probes on the polysilicon interconnect and applying the electrical stimulus. The current measurement for AD4 was extremely low when compared to the other seven. These data are shown as resistance measurements in Figure 7 for the eight AD ports. Note the high resistance value (3-5x10^8 Ω) of the *p*-channel transistor gate of AD4.

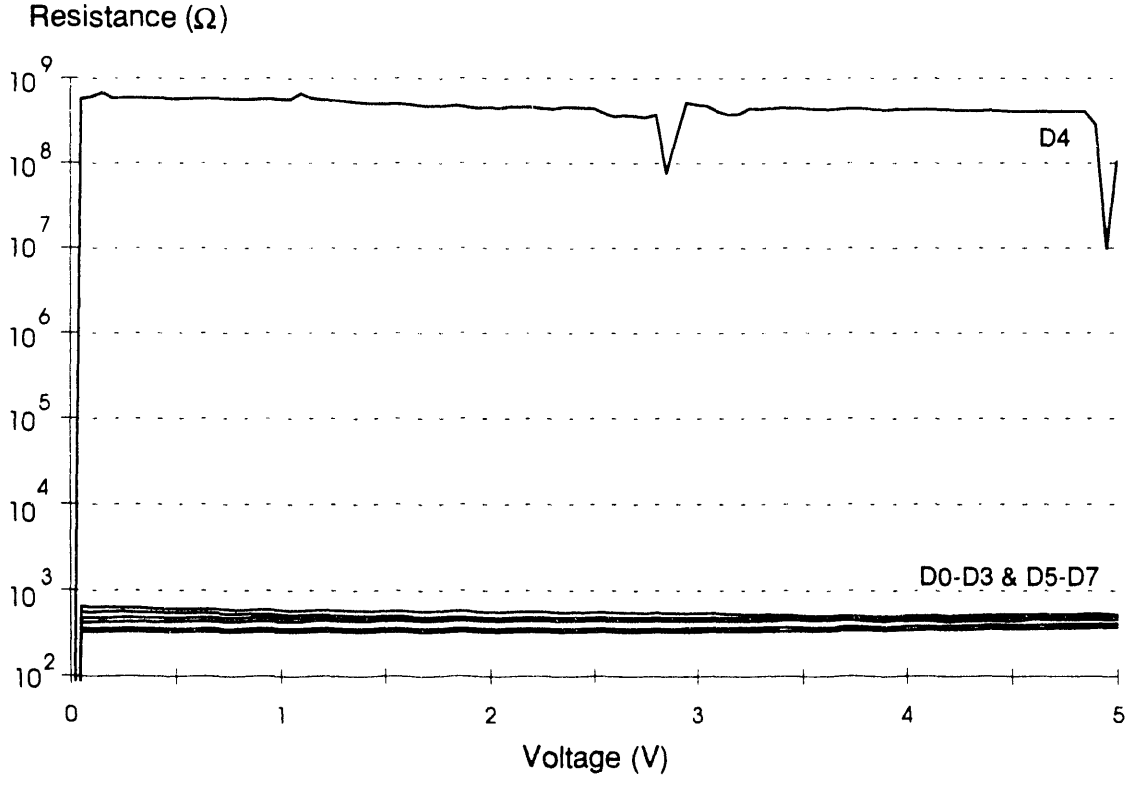

Figure 7. Resistance measurements of the eight AD port *p*-channel transistor interconnects.

Further probing was performed on the defective interconnect/gate of AD4. Figure 8 shows the results of using a maximum applied voltage of 10 volts. These data show clearly that there is an abrupt increase in interconnect current when 8.5 volts and greater is applied. This abrupt increase in current may account for why functional failures occurred at 5 V but not at 10 V. The grain boundaries in the polysilicon interconnect are assumed to behave as an intrinsic wide-band-gap semiconductor forming a heterojunction with the grains. The carrier transport mechanism in polycrystalline silicon has been proposed as quantum mechanical charge tunneling through the grain boundaries [2]. The abrupt current increase shown in Figure 7 is most likely due to an increase level of charge tunneling that occurs in the polysilicon interconnect at the higher voltages.

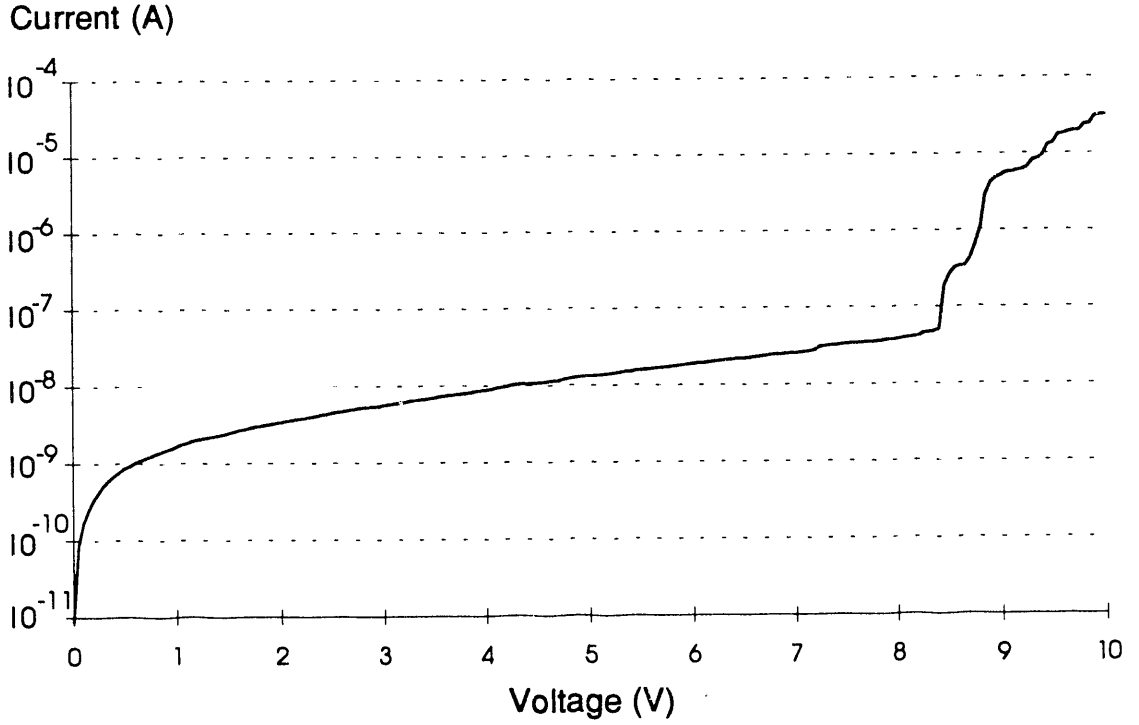

Figure 8. Current measurements (DC) on the defective interconnect of AD4 port. The magnitude of current for the other interconnects was approximately $1x10^{-2}$ A.

5.0 Scanning Electron Microscope Studies

High resolution SEM inspections of the AD4 gate indicated that the polysilicon is physically contiguous; however, a marked change in the grain structure was observed at a location corresponding to the edge of the field oxide step near the point of electrical discontinuity. To provide the highest resolution possible, the IC was coated with a Au/Pd conducting film (approximately 10 nm thick) to decrease the amount of charging during the high resolution SEM inspections.

Figure 9 shows the polysilicon interconnect of AD4 (0° tilt). Note the changing width of the interconnect at locations denoted by the arrows. The portion of the interconnect between the arrows appears less etched and is wider. Figure 10 is a higher magnification image of the AD4 interconnect region at the edge of the oxide step. The sides of the polysilicon appear to be vertical and well defined over the field oxide but less vertical and poorly defined over the gate oxide region.

Figure 11 shows a marked change in the polysilicon microstructure as the AD4 gate steps over the field oxide onto the gate oxide. The appearance of the polysilicon on the left hand side of the figure is typical. The polysilicon over field oxide located to the left of the oxide step has well delineated grain boundaries. By contrast, the polysilicon to the right of the oxide step appears less etched. It is wider and the grain boundaries are not well delineated. The location of morphological discontinuity corresponds to that of electrical discontinuity which was observed in Figure 3. Figure 12 is the AD5 neighboring interconnect for comparison.

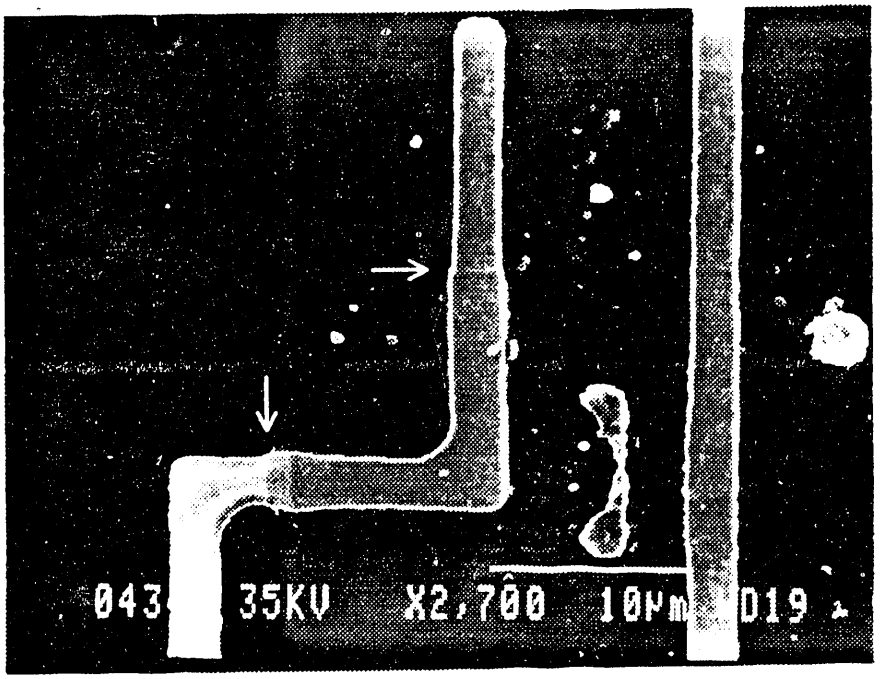

Figure 9. SEM image of the AD4 polysilicon interconnect after chemical deprocessing (0° tilt).

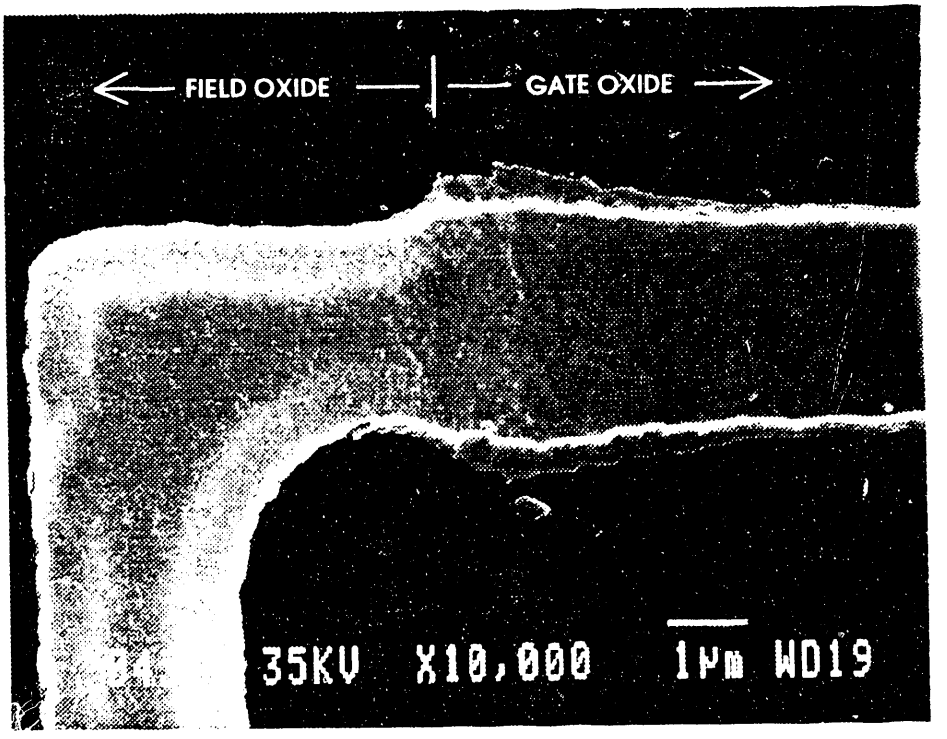

Figure 10. A higher magnification SEM image of the defective interconnect. Note the varying width and anomalous sidewall slope of the interconnect beginning at the oxide step.

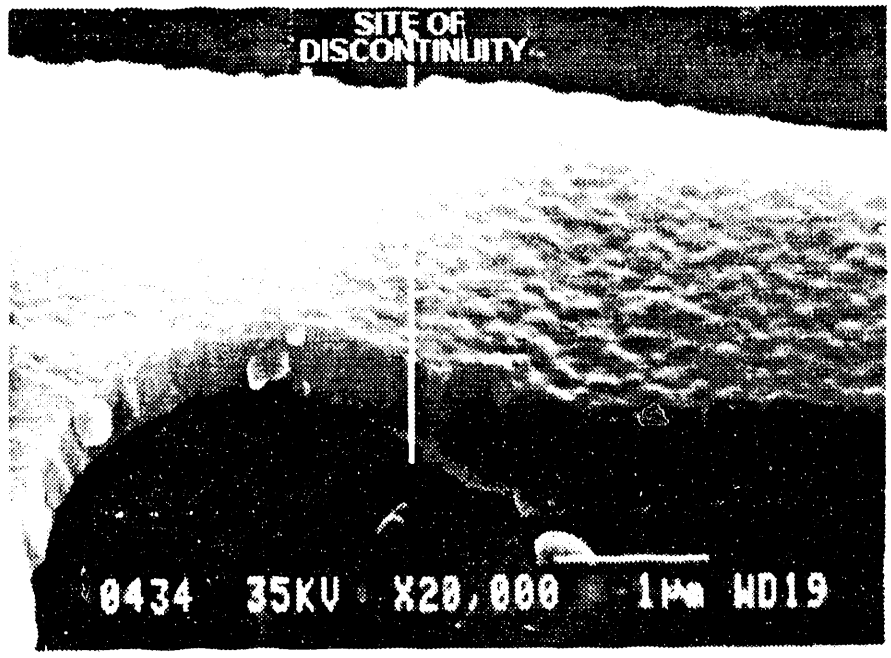

Figure 11. SEM image of AD4 polysilicon interconnect at field oxide step (45° tilt).

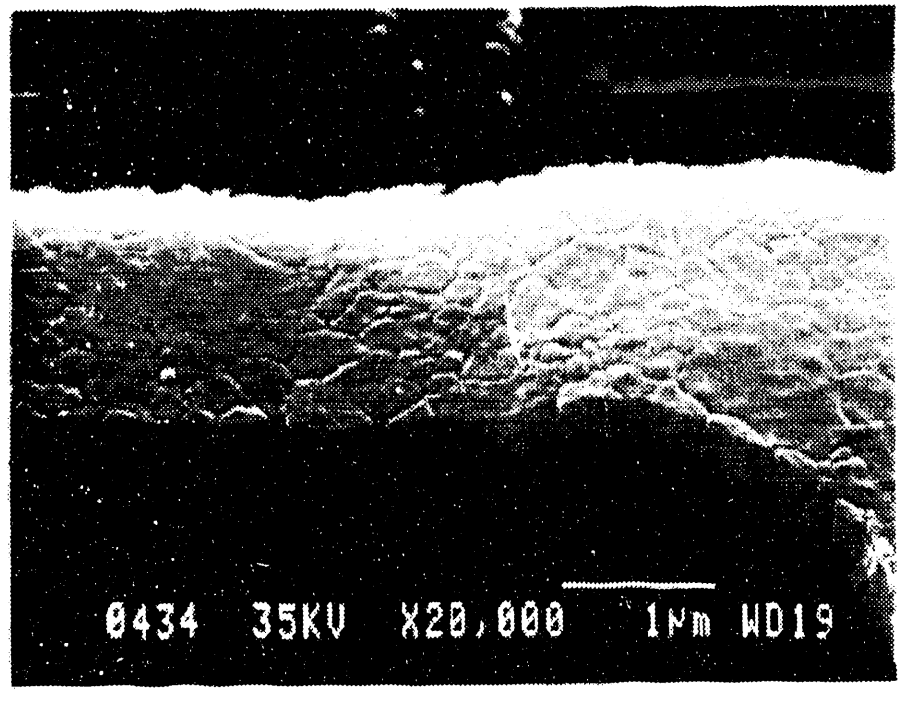

Figure 12. SEM image of AD5 polysilicon interconnect. Compare this image to the AD4 interconnect (Fig. 11).

Based on the etch rate of polysilicon which increases with increasing dopant (phosphorus) concentration, the region of the AD4 polysilicon to the right of the discontinuity apparently had an anomalously low phosphorus doping level [3]. The cause of the locally low dopant concentration is not known but could result from particulate masking during the phosphorus ion implantation of the polysilicon. The global or blanket ion implantation process step immediately precedes the lithographic patterning to define the polysilicon interconnects.

Following the discovery of this suspect area, the entire die was inspected for other anomalous areas of polysilicon patterning and grain structure, but none were found.

Note: Unfortunately, elemental (secondary ion mass spectroscopy, SIMS) and structural (transmission electron microscopy, TEM) analyses of the polysilicon were not practical at the time of failure analysis.

6.0 Electrical Simulation of the Failure Mode

PSpice simulations were performed on the output holding latch circuitry to investigate the effects of the gate defect [4,5]. The gate defect was represented by a series resistor in the interconnect path between the *n*- and *p*-channel transistors of the output stage of the holding latch. Figure 13 shows the electrical schematic of the holding latch simulation circuit with the series gate resistance and node numbers. The simulations were performed with V_{DD} = 10 V and V_{SS} = 0 V at a temperature of 27 °C. All *n*-channel transistors had a threshold voltage, V_{tn}, equal to 1.0 V. All *p*-channel transistors had a threshold voltage, V_{tp}, equal to -1.4 V. The model index for all transistors was three (LEVEL = 3). All SPICE parameters used in the simulations were obtained from wafer lot characterizations. Gate oxide thickness for this technology is nominally 45 nm. Since statistics of the gate oxide thickness were not available, variances of ±10% on the oxide thickness were simulated to account for process variations and the corresponding effect on gate capacitances.

Transistors MP1, MN1, MP2, and MN2 represent the latch circuitry. The combination of MP1/MN1 represents the input stage of the latch circuit. The combination of MP2/MN2 represents the output stage of the latch circuit. MP3 represents the pre-charge transistor that sets the data line (node 3) to a logical high state when the ALE signal is active. (V1 is the inverse of the ALE signal.) MN3 represents the pull-down transistor that sets the data line to a logical low level during a read operation when the bit information from the ROM is low. (V2 is the inverse of the bit information.)

The key nodes of the circuit analysis are nodes 4 and 5. Node 4 represents the output of the input stage of the latch and the gate potential to the *n*-channel transistor, MN2. Node 5 represents the gate voltage of the *p*-channel transistor, MP2.

By increasing the series gate resistance, RGATE, the simulations showed that when RGATE exceeded 1×10^9 Ω, the potentials at nodes 4 and 5 became 180° out of phase. Recall that DC current measurements showed the resistance of the polysilicon gate was approximately $3\text{-}5 \times 10^8$ Ω (see Fig. 7). The value of RGATE required for inversion of node 5 voltage is well within an order of magnitude of the measured interconnect resistance. (By varying the gate oxide thickness by ±10%, small differences were noted but the effects were not significant.)

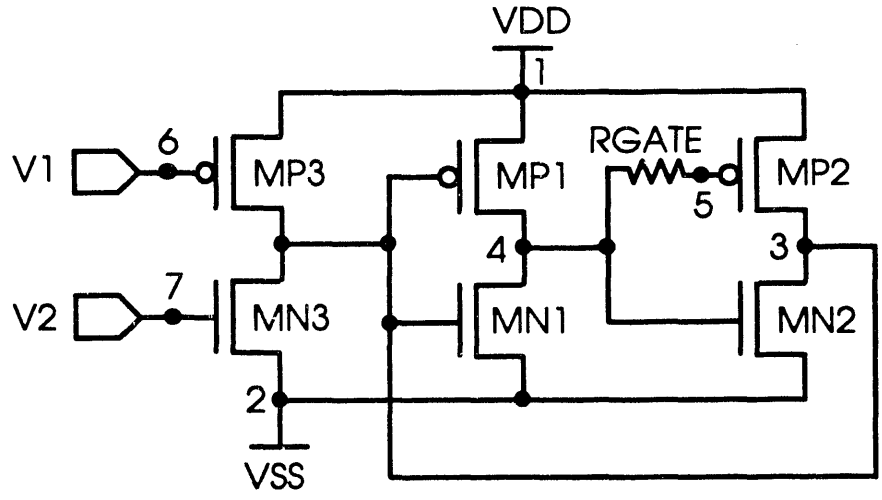

Figure 13. Electrical schematic diagram of PSPICE simulation circuit of holding latch circuitry.

Figure 14 shows the voltage waveform for node 4, the input node to the output stage of the holding latch. This waveform appears normal with a voltage swing of 0 to 10 V (V_{DD} = 10 V). This waveform corresponds to the "probe_1" waveform obtained during the electron beam probing (see Fig. 6) and represents the gate signal to transistor MN2 which is routed through a normal polysilicon interconnect. Figure 15 shows the potential waveform of node 5 which is the gate potential of the *p*-channel transistor, MP2. This waveform would correspond to the "probe_7" waveform obtained during the electron beam probing studies. Figure 16 shows the simulated power supply current response of the latch circuitry. By comparing Figures 14 and 15, high current exists when a high voltage is input to the output stage of the latch. Under these conditions, the waveforms indicate that both transistors, MP2 and MN2, of the output stage of the latch would be active during this stimulus. In addition, the magnitude of simulated current during this logic state exceeds the Sentry electrical test (I_{DDQ}) failure criteria of 200 μA.

DISCUSSION

1.0 Generation of the High Current State

The shaded inverter of the latch circuit, as shown in the schematic diagram of Figure 2, contains the defective polysilicon interconnect associated with the gate of the *p*-channel transistor. The purpose of this latch is to hold the data line at a high logic state when the ALE line is enabled; at a low logic state when the ROM data is low. Elevated currents were measured on the failing IC during a read operation when the ROM bit information was a low logic state. The voltage of the section of gate labeled as probe_7 in Figure 6 (node 5 of Figure 13) is such that it is 180° out of phase with probe_1 (node 4). Under normal conditions, MP2 would be off while MN2 was biased on. Because the gate voltage for MP2 is inverted, both MN2 and MP2 are biased on when node 4 potential goes high. This causes high current in the inverter circuitry of the output stage since both the *n*- and *p*-channel transistors are biased into conduction long after the application of the address latch/read vector. Thus, the polysilicon interconnect defect at MP2 causes the component to fail the I_{DDQ} tests when the ALE and RD pins are enabled.

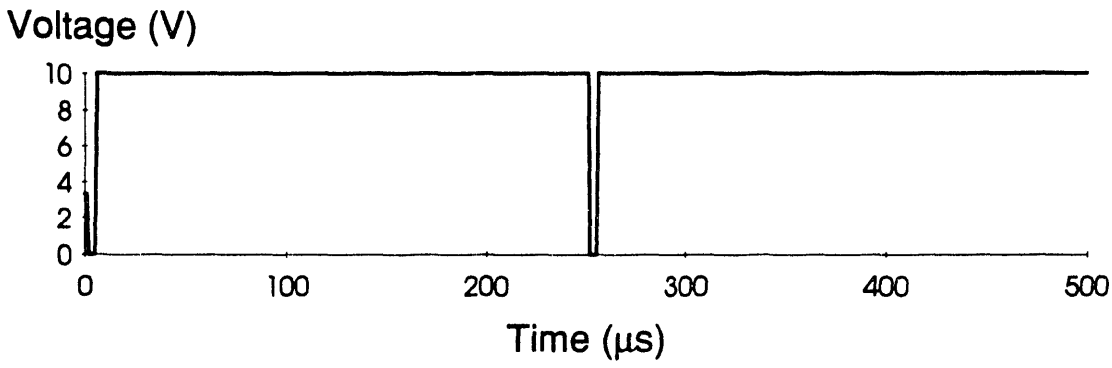

Figure 14. Simulation results of holding latch, node 4. This is the input node to the output stage.

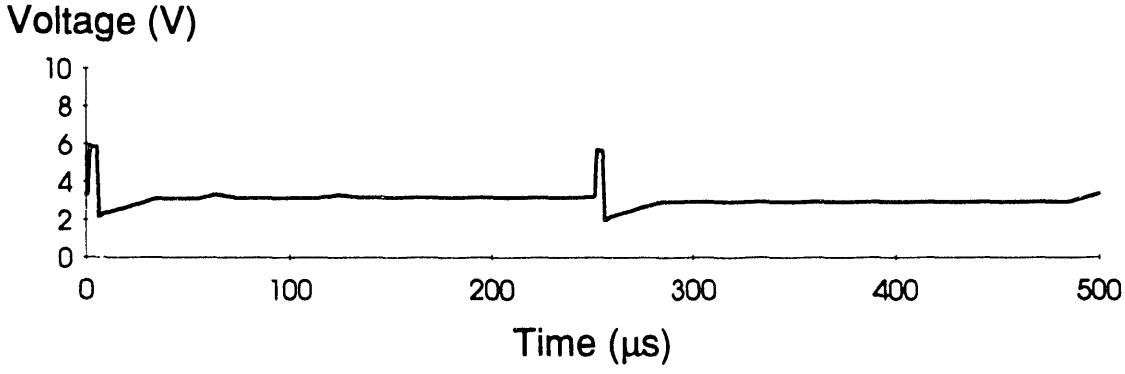

Figure 15. Simulation results of holding latch, node 5. This is the input node to the *p*-channel transistor of the output stage.

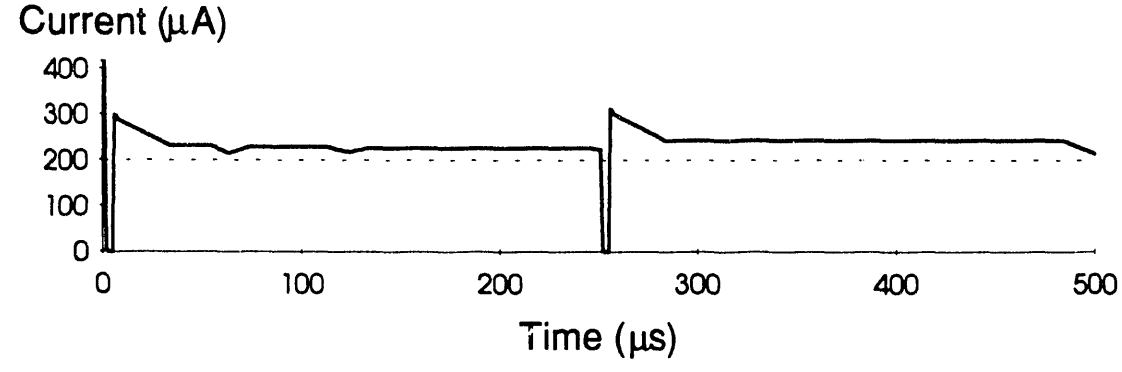

Figure 16. Simulated power supply current response of the latch circuitry. High current exists when both MP2 and MN2 are active.

2.0 Functional Failure (stuck-at-0 fault)

With the reduced power supply voltage (5 V), functional failures can be accounted for by the failure of the output stage of the latch circuit to hold the data line at a high logic state. During a read operation when the bit information is "1", the latch circuitry is designed to hold the pre-charge voltage until the bit is read and the next address is latched. For the "1" logic state on the data line, normal inverter operation would have the *n*-channel transistor biased into cutoff and the *p*-channel transistor biased into its linear region of operation. For the "0" logic state on the data line, the *p*-channel transistor would be biased in cutoff and the *n*-channel transistor would be biased in the linear region. During failure, the *p*-channel transistor in the output stage of the latch circuit was not biased properly due to the defective polysilicon interconnect. As a consequence, it was observed that the data bit line was not latched at the high logic state and a stuck-at-0 fault resulted.

By contrast, with the normal operating voltage of 10 V, there is sufficient tunneling current that occurs in the polysilicon gate to bias the defective *p*-channel transistor in the linear region. The increased potential permits the data latch to hold the pre-charge voltage and functional failures do not occur.

3.0 Polysilicon Gate Morphology

The voltage discontinuity and polysilicon gate morphology can be hypothetically explained by incorrect doping concentration of the *p*-channel transistor polysilicon interconnect/gate. The lack of grain boundary definition and non-vertical sidewalls of the anomalous polysilicon region can be attributed to less rapid etching of a lightly n-doped region, whereas the well defined grain boundaries and vertical sidewalls are more representative of the typical highly n-doped regions. It is well known that a highly n-doped region etches faster [3] and as the concentration of dopant atoms increases, grain growth is encouraged [6]. Therefore, it is likely that the lightly doped polysilicon grains are smaller. (Since the surface didn't etch well it's not possible to ascertain the exact grain size from the photomicrograph.) The varying widths of the defective interconnect are the patterning result of the two differently doped regions abutting each other.

Dopant (phosphorus) segregation at grain boundaries during the life test is believed to have caused the open-circuit type of failure. It is also believed that the segregation depleted the phosphorus from the region(s) immediately adjacent to the grain boundary and not from the bulk or interior of the grain. The thermodynamic driving force for the segregation is reduction of the grain boundary energy [7]. Not all dopants behave in this manner; it has been reported that arsenic and phosphorus segregate to grain boundaries in polysilicon, while boron does not [6]. Keep in mind that segregation occurs in all silicon grains doped with phosphorus. Typically, the dopant concentration is high enough that phosphorus segregation to the grain boundaries does not appreciably affect the conductivity. However, if the concentration of phosphorus is very low to start with, the polysilicon will stop conducting when enough phosphorus, primarily near the boundary, segregates to the grain boundaries. Once the dopant

atoms arrive at the grain boundary, the carriers normally donated are locally trapped and do not contribute to conduction since the grain boundary would provide an ideal site where a phosphorus atom could have all five valence bonds saturated.

Low temperature grain boundary diffusion data for phosphorus in polysilicon were not found in other publications. It is reasonable to expect grain boundary diffusion to be the dominant diffusion mechanism for temperatures of operation (~100 °C). Furthermore, it is believed that grain boundary diffusion can be six or more orders of magnitude greater than that in the bulk at these low temperatures [8].

Although the polysilicon doping apparently was abnormally low following fabrication, there was evidently sufficient conductivity to allow proper functioning of the affected transistor. An effect of the loss of carriers would be an increase in the barrier width of the boundaries. As the barrier width increases, a larger bias voltage is necessary to allow electrical conduction (by quantum mechanical tunneling) across the grain boundaries. This is consistent with the observation that the IC functioned at 10 V but not at 5 V.

CONCLUSIONS

Apparently, during the blanket phosphorus implant of the polysilicon prior to patterning, there was foreign matter on the surface which prevented adequate doping in the defective area. The implant masking resulted in a latent, random defect after patterning in the latch circuitry of the AD4 port cell. The time dependent failure is believed to be due to dopant segregation at grain boundaries in the area where the grain boundary density is high, that is, in the lightly doped area. Dopant segregation reduces the conductivity of the polysilicon gate by a net reduction of dopant atoms and the free carrier concentration near the grain boundaries. The lightly doped region appears markedly different from any other polysilicon on the die after deprocessing. The appearance of etching difficulties during the patterning process step, such as non-vertical sidewalls and varying width, are evident and can be explained by a lightly doped region abutting a heavily doped region. We consider this a random defect because careful inspection of the entire die revealed no other similar defects and no other failures of this nature have been encountered. The impact of this failure on the overall device reliability and similarly processed components (polysilicon gate technologies) is, thus, not significant.

To possibly screen components from this type of failure mode, this device should be tested at a lower operating voltage. The normal operating power supply potential is 10 volts, but when the power supply was reduced to 5 volts, the device failed functional and I_{DDQ} tests. Since electrical conduction in polysilicon thin films occurs by tunneling of charge carriers across grain boundaries, a lower operating voltage reduces the probability of carrier emission and provides a more sensitive screen for defects of the type found on this IC. There was no indication from the Sentry timing tests that a change occurred at the interim monitoring points of the life test. A test using a reduced power supply potential may detect such changes.

ACKNOWLEDGEMENTS

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