

Physics Division

**DESIGN AND DEVELOP  
SPEED/PRESSURE REGULATOR**

A. M. Hasanul Basher

Manuscript Completed—August 13, 1993  
Date Published—September 1993

**NOTICE** This document contains information of a preliminary nature.  
It is subject to revision or correction and therefore does not represent a  
final report.

Prepared for the  
Office of Energy Research  
KB 02 02 00 0

Prepared by the  
Oak Ridge National Laboratory  
Oak Ridge, Tennessee 37831-6285  
managed by  
MARTIN MARIETTA ENERGY SYSTEMS, INC.  
for the  
U.S. DEPARTMENT OF ENERGY  
under contract DE-AC05-84OR21400

**MASTER**

**DESIGN AND DEVELOP  
SPEED/PRESSURE REGULATOR\***

**A. M. Hasanul Basher<sup>1</sup>  
Physics Division  
Oak Ridge National Laboratory  
Oak Ridge, Tennessee 37831-6368**

**August 13, 1993**

---

**\* Operated by Martin Marietta Energy Systems, Inc. for the U.S. Department of Energy under contract No. DE-AC05-84OR21400 .**

**<sup>1</sup> Summer Faculty Research Participant, School of Engineering Technology, South Carolina State College, Orangeburg, South Carolina 29117.**

## Table of Contents

	<u>Page</u>
List of Figures	i
Acknowledgments	ii
1. Introduction	1
2. Implementation Strategy	2
3. Work Completed	3
Regulator Design	3
Power Supply Design	11
4. Circuit Build and Implement	13
Appendix	
List of Components	

## List of Figures

	<u>Page</u>
Figure 1 Regulator Block Diagram	6
Figure 2 Regulator Circuit	9
Figure 3 Regulator Simulation Results	10
Figure 4 Power Supply Circuit	12
Figure 5 Voltage Doubler Simulation Results	14

### **Acknowledgments**

This program was sponsored by Oak Ridge Associated Universities (ORAU) at Oak Ridge, Tennessee, and conducted under the supervision of Sigmund W. Mosko in the Physics Division at Oak Ridge National Laboratory. I greatly appreciate ORAU, especially Deborah D. McCleary, W. Mamie Johnson, and Richard E. Wieselhuegel for giving me an opportunity to work on this project. I wish to express my gratitude to my supervisor, Sigmund W. Mosko, for his invaluable suggestions and tremendous help in carrying out this project successfully. I must thank him again for proper guidance during the tenure of this project.

I greatly appreciate the help from Raymond C. Juras, Martha J. Meigs, and B. Alan Tatum, who provided advice, helpful discussions, and suggestions in preparing the report.

My thanks are due for help in the laboratory while building the circuit provided by Robert H. Brown, Raymond L. Glover, and Clarence R. Ketner, Jr. of the Instrument Shop.

I am surely indebted to Ms. Jeanette McBride for her assistance in arranging and editing the report.

## **DESIGN AND DEVELOP SPEED/PRESSURE REGULATOR**

### **1. INTRODUCTION**

The Physics Division at Oak Ridge National Laboratory has several recirculating water cooling systems. One of them supplies deionized water at 150 psi, which is mainly used for cooling magnet windings at the Oak Ridge Isochronous Cyclotron (ORIC). The system has three 125-hp water pumps, each of which is capable of supplying water at the rate of 1000 gpm. One of the major requirements of this water supply system is that the supply pressure must be kept constant. An adjustable-frequency speed controller was recently installed to control the speed of one of the pump motors. A servo-system was provided with the adjustable-frequency controller for regulating motor speed and, subsequently, the water pressure. After unsuccessful attempts to operate the servo, it was concluded that the regulator may not work for the existing system. Prior to installation of the variable-frequency controller, pressure regulation was accomplished with a pneumatically controlled load by-pass valve. To maintain constant pressure in the system, it is necessary to run always at full load, even if full load is not on the system. Hence, there is a waste of energy when full load is not connected to the system. So, designing and implementing one regulator that works at any load condition has become necessary.

The new regulator will be capable of maintaining constant speed and pressure at any load condition. Since the regulator circuit needs dc voltage supplies of both polarities, a power supply circuit will also be designed. The 12-V ac supply available on the existing system will be used as an input to the power

supply circuit. The dynamics of the existing system were completely unknown. So, it was necessary to study the system behavior.

Currently, one pump (125-hp) runs at 115% capacity to supply water at the rate of 1000 gpm at 130 psi of pressure. Normally, it runs for 300 days a year. The motor input power at 60 Hz is 120 kW. When it runs for 300 days a year and 24 hours a day, the pump motor operating cost, calculated at the rate of \$65 per MW hr, becomes \$56,000.00 per year. With the new regulator (controller), it will be possible to maintain the water pressure by reducing speed rather than bypassing water. This will reduce the water flow to 60% of the maximum most of the time and, hence, a saving of about \$22,400.00 per year.

In the following sections, we present the implementation strategy, work completed, design procedures, circuit diagrams, and computer simulation results. A list of components is presented in the appendix.

## **2. IMPLEMENTATION STRATEGY**

This project was carried out in the following phases:

**Phase I:** A study of the existing system behavior in terms of its response to different input conditions.

**Phase II:** Design of a regulator circuit that meets the required specifications.

**Phase III:** Design of power supply circuits to supply dc voltages to different sections of the regulator.

**Phase IV: Build the circuit in the laboratory and test it.**

### **3. WORK COMPLETED**

All the phases mentioned above are completed. The regulator circuit and the associated power supply circuit were designed from scratch, built in the laboratory, and tested on the water supply system. The performance of the regulator was found to be very satisfactory when tested for different load conditions. It is capable of maintaining motor speed and water pressure constant under various conditions. The following sections will give more specifics about the design criterion and the selection of components.

#### **REGULATOR DESIGN:**

Before we set our design criterion, we studied the system by observing its responses under different input conditions. During the study, it was noticed that the system reacts very slowly to any input changes and fast control actions may sometimes cause the system to oscillate. This suggests that the control signal generated to control the system should have a sufficiently long rise time.

The regulator (controller) provides the intelligence of the system. It has two inputs; one indicates the desired value and is called the Set Point (SP); the other input signal indicates the actual value (as measured by the sensor), and is called the process variable (PV). It is the purpose of the regulator to provide a signal that will cause the process to be modified in such a way as to keep the set point and the process variable equal. Any changes in the set point or the



loads on the process should cause a change in the controller's output, to assure that the PV tracks the SP.

All controllers must begin by generating the error signal

$$E = SP - PV$$

which is the difference between the set point and the actual value. This section is known as the Error Amplifier. To cause perfect steady-state tracking between the set point and the process variable, an integrator must be added to the controller. The integrator has an output whose rate of change is proportional to the error. As long as there is an error at all, the output of the integrator will continue to change. When the error has been driven to zero, the integrator's output no longer changes and it holds the output which is necessary to produce no error. When there is a large error, the integrator's output changes rapidly to correct the error. As the error gets smaller, the integrator's output changes more slowly. In many practical systems, this time-variant output alone is too slow and is usually coupled with a proportional controller in order to achieve rapid controller output changes. Because our system requires a slow rise control signal, a proportional controller is not needed.

To reduce the steady-state error to an acceptable level, sufficient gain for the controller is needed. A controller always has a block that provides gain.

A sensor is being used in the system which measures the process variable and converts that into the same form as that of the set point so that it can be compared with the set point to determine the error. If the output of the sensor is

not at the comparable level with the set point signal, a signal conditioner is needed.

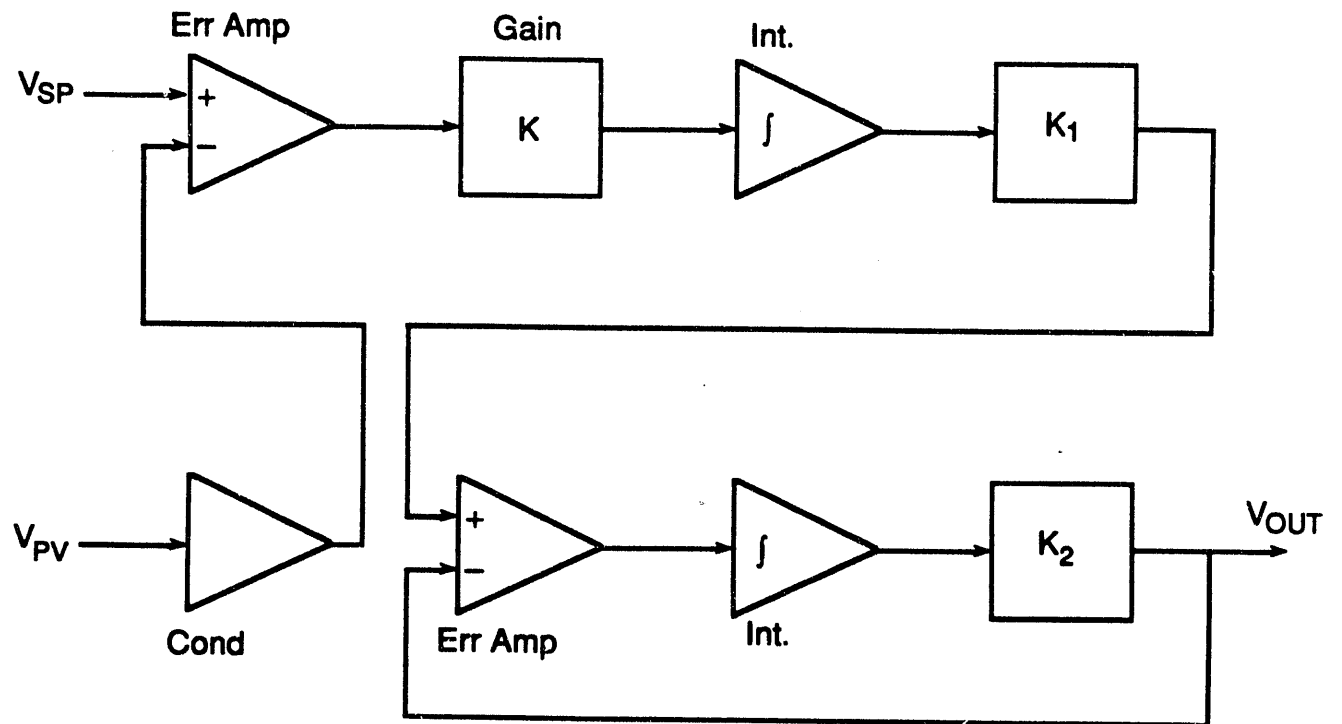
The design constraints can be summarized as follows:

- a. The control signal must have a long enough rise time so that the process can react properly to the changes.
- b. No overshoot in the control signal will be allowed (critically damped response is desired).
- c. Enough controller gain should be provided to reduce the steady state error to an acceptable limit.
- d. The reference (set point) voltage should range from 0 to 10 V dc.
- e. Output of the controller must not exceed 10 V dc.

The regulator is of the integral-type controller and the major blocks include Error Amplifier, Gain, Integrator, a block to generate a slow rise signal at the output, and a signal conditioner. The block diagram of the regulator is shown on page 6.

The transient and stability analysis of the regulator was done creating a feedback loop to itself by connecting its output to the signal conditioner block. Then the transient response was studied in order to determine the circuit

## Regulator Block Diagram



- $V_{SP}$  - Set point voltage
- $V_{PV}$  - Voltage from pressure sensor
- Int. - Integrator
- Cond - Signal conditioner
- $K$  - Controller gain
- $K_1, K_2$  - Integration constants

Figure 1

parameters of the regulator. The overall transfer function of the closed-loop system was found to be:

$$\frac{V_{OUT}}{V_{SP}} = \frac{K'}{S^2 + K_2S + K'}$$

where  $K' = KK_1K_2$ .

From the above transfer function, it can be shown that when

$$\frac{K_2}{KK_1} \geq 4$$

there will be no overshoot. Then,  $K$ ,  $K_1$ , and  $K_2$  can be adjusted to achieve sufficient controller gain and the control signal rise time. Two integrators are needed to have enough span (gain) for the controller and control over the rise time needed for the process to respond correctly.

The designed regulator circuit is shown on page 9 (Figure 2). Computer simulation results are obtained and shown on page 10 (Figure 3), with the output fed back to the input of the signal conditioner when the reference input is varied in steps over its range. The PSpice software package was used to obtain the simulation results.

General-purpose op-amps are used to generate error signal, to achieve controller gain, and for conditioning the sensor signal. The control signal rise time can be adjusted by selecting proper values for the resistors and capacitors in the integrator circuits. When the input (error signal) to the integrator is zero,

ideally, the capacitor can neither charge nor discharge. It should hold its voltage. If we use a general-purpose op-amp, the bias current is large enough to charge the capacitor, even with no error voltage. This causes the output to slowly rise when it is supposed to remain constant. A FET or CMOS op-amp has bias currents of the order of picoamperes or less. Using a FET or CMOS op-amp should cause no noticeable change in integrator output caused by bias currents. In our circuit, a FET (OP07) op-amp is used. The range of reference voltage and the controller gain that can be provided by the circuit are shown below.

Reference Voltage:  $0 \leq V_{SP} \leq 12.39 \text{ V}$

Controller Gain:  $0.4 \leq \text{Gain} \leq 20.4$

The gain range is sufficient for our system.

The sensor measures the pressure and produces an electrical signal over the range 0 to 10 V dc with some offset. A circuit is provided with the signal conditioner to overcome this offset.

## POWER SUPPLY DESIGN

As mentioned before, the  $\pm 15 \text{ V}$  dc needed for the op-amps in the regulator circuit is not available on the existing system, so it was necessary to design a new power supply. A 12-V ac signal is available on the existing system, which is used to generate  $\pm 15 \text{ V}$  dc. But this ac signal, when full-wave rectified and filtered by passing through a capacitor, fails to generate enough dc voltage to drive the voltage regulator, especially when all the loads will be connected. So,

# Regulator Circuit

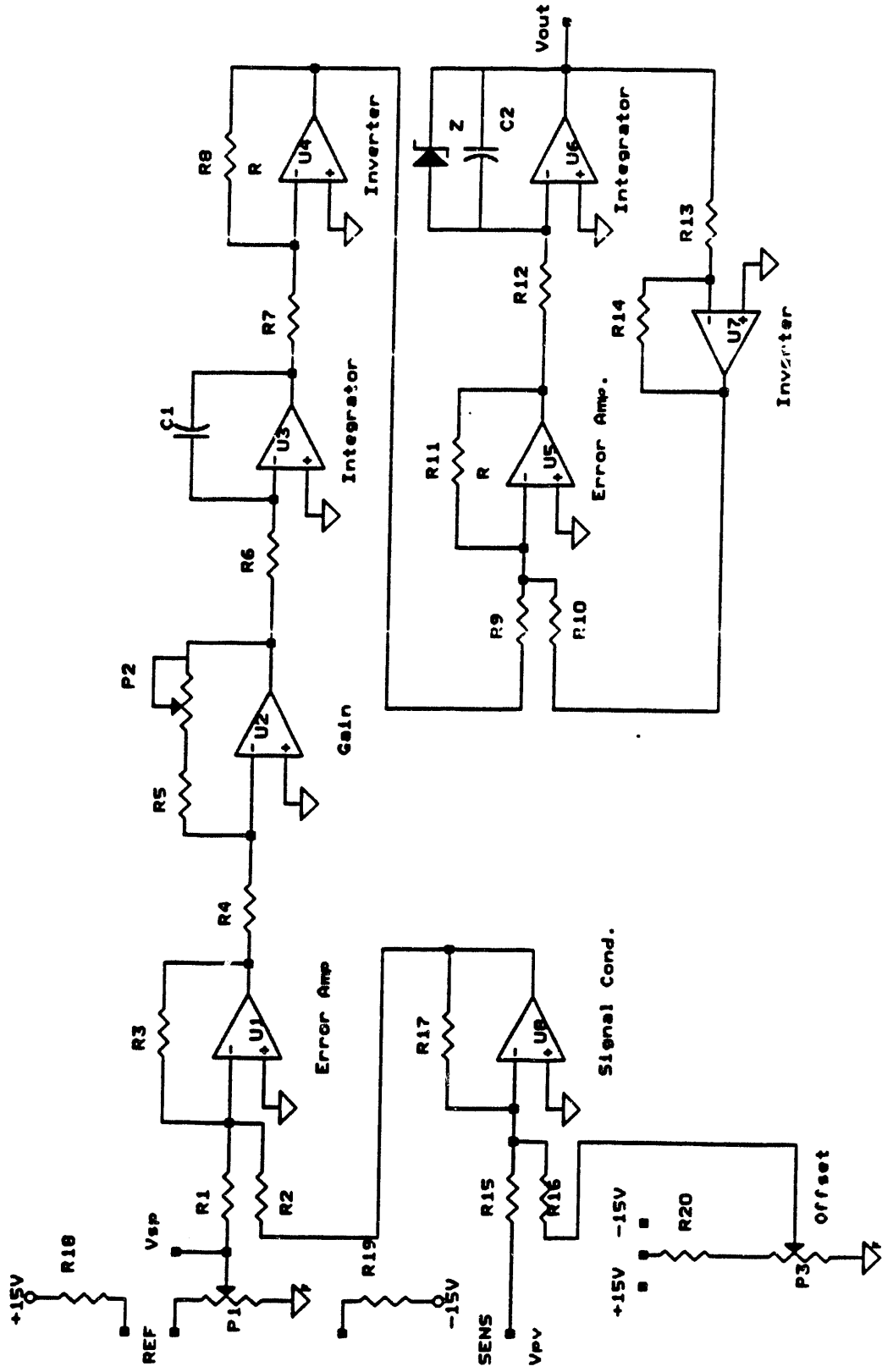


Figure 2

# Regulator Simulation Results

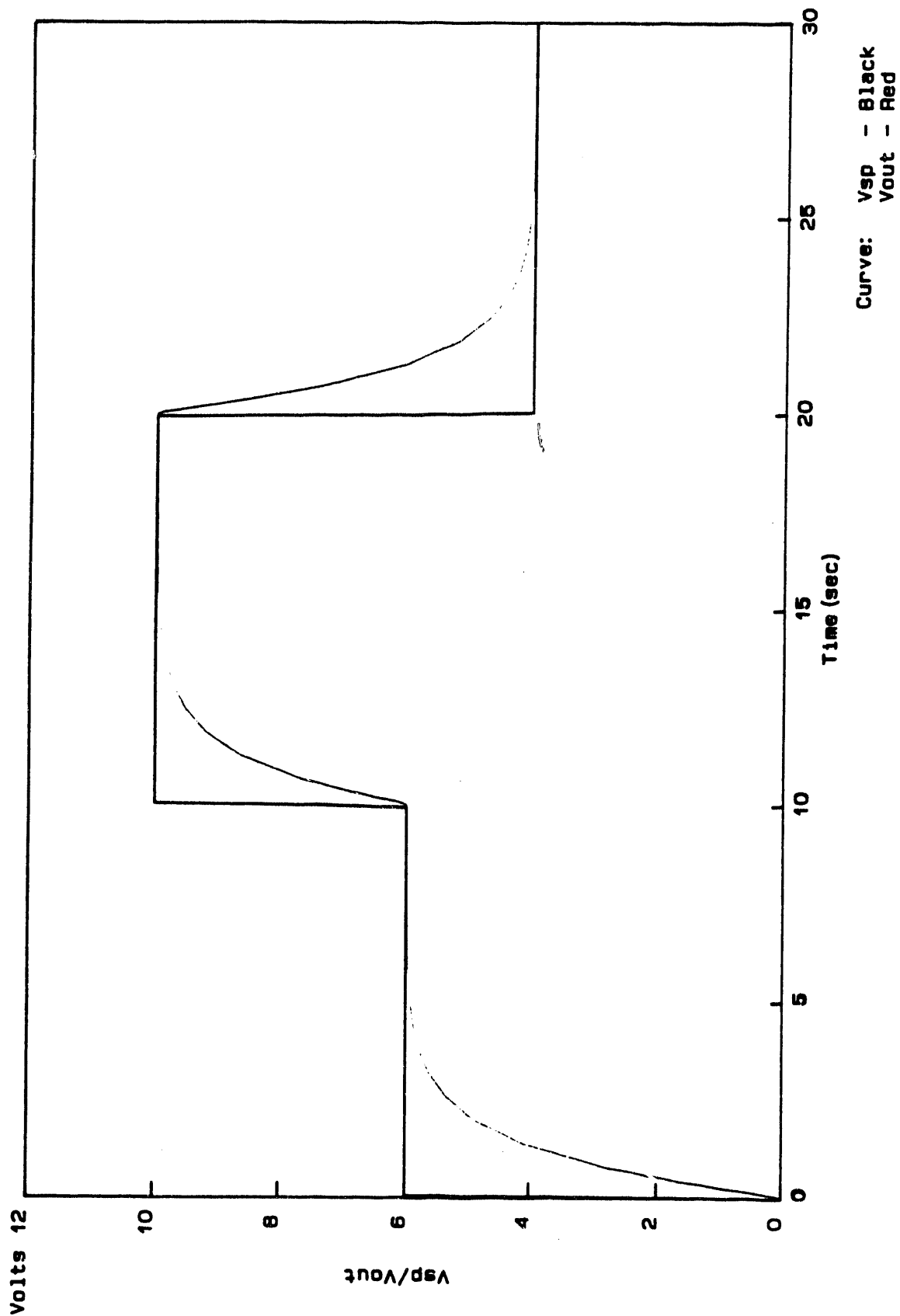


Figure 3

it was necessary to design a full-wave voltage doubler circuit. The designed power supply circuit has two major sections; a full-wave doubler and a voltage regulator circuit. The full-wave voltage doubler circuit produces dc voltages of opposite polarities with some ripple in each. These voltages become the inputs to the voltage regulator circuit. The complete power supply circuit is given on page 12 (Figure 4).

The MC1468L IC chip is selected for the voltage regulator, which requires a minimum of  $\pm 18$  V dc, but not exceeding  $\pm 30$  V dc, to produce  $\pm 15$  V dc at its outputs. The filter capacitors and the load resistors for the rectifier are selected to meet these input requirements. The peak inverse voltage (PIV) across each diode is 33.94 V, so accordingly, the diodes are chosen. The filter capacitors should be placed as close to the regulator IC chip as possible. Extra capacitors will be required from each input terminal of the regulator device to ground, if the device is located an appreciable distance from the rectifier filter capacitors. In our circuit, we have managed to place the filter capacitors very close to the device. Higher values for the output capacitors C7 and C8 are chosen to improve load transient response and to reduce the output noise voltage.



## Power Supply Circuit

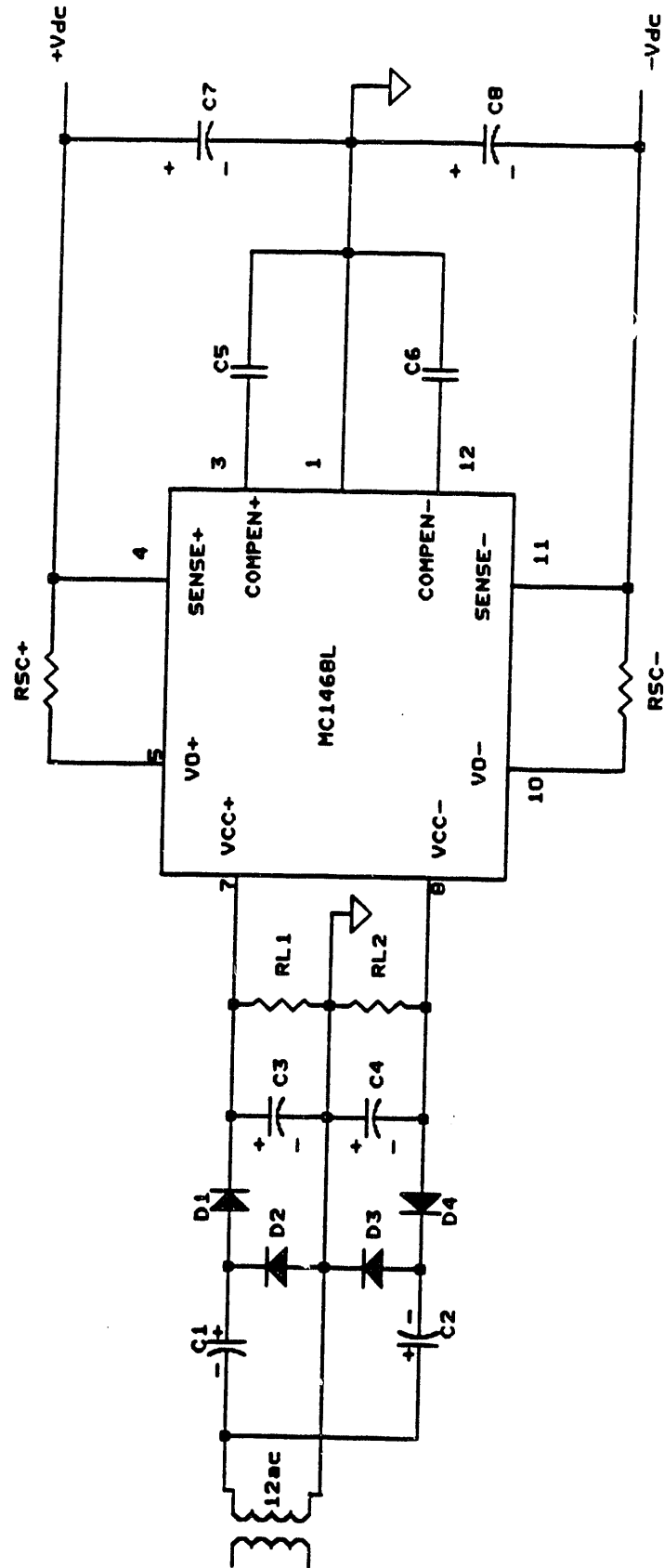


Figure 4

The following measurements are taken at different points in the power supply circuit:

**Voltage Doubler Output Terminals:**

**Vdc magnitude = 29.0 V**

**Ripple = 5%**

**Voltage Regulator Output:**

**+Vdc = +15.0 V**

**-Vdc = -15.1 V**

Computer simulation results of the full-wave voltage doubler circuit obtained using the PSpice software package are shown on page 14 (Figure 5).

#### **4. CIRCUIT BUILD AND IMPLEMENT**

The complete circuit was built in the laboratory. Both the regulator and the power supply circuits are on the same board. The regulator was tested with the main system. The performance of the regulator is very satisfactory and is tested for various load conditions.

The components connected to each op-amp are placed close to the chip itself with the components that go to the input terminals at the bottom and the components in the feedback path at the top of each op-amp. A few test points are also mounted, each of which is discussed later in this section. For offset adjustments, both positive and negative voltages are provided, which can be selected using a jumper. For reference input voltage, supply of both polarities is also provided in the circuit. Connectors are also mounted at the top right corner

# Voltage Doubler Simulation Results

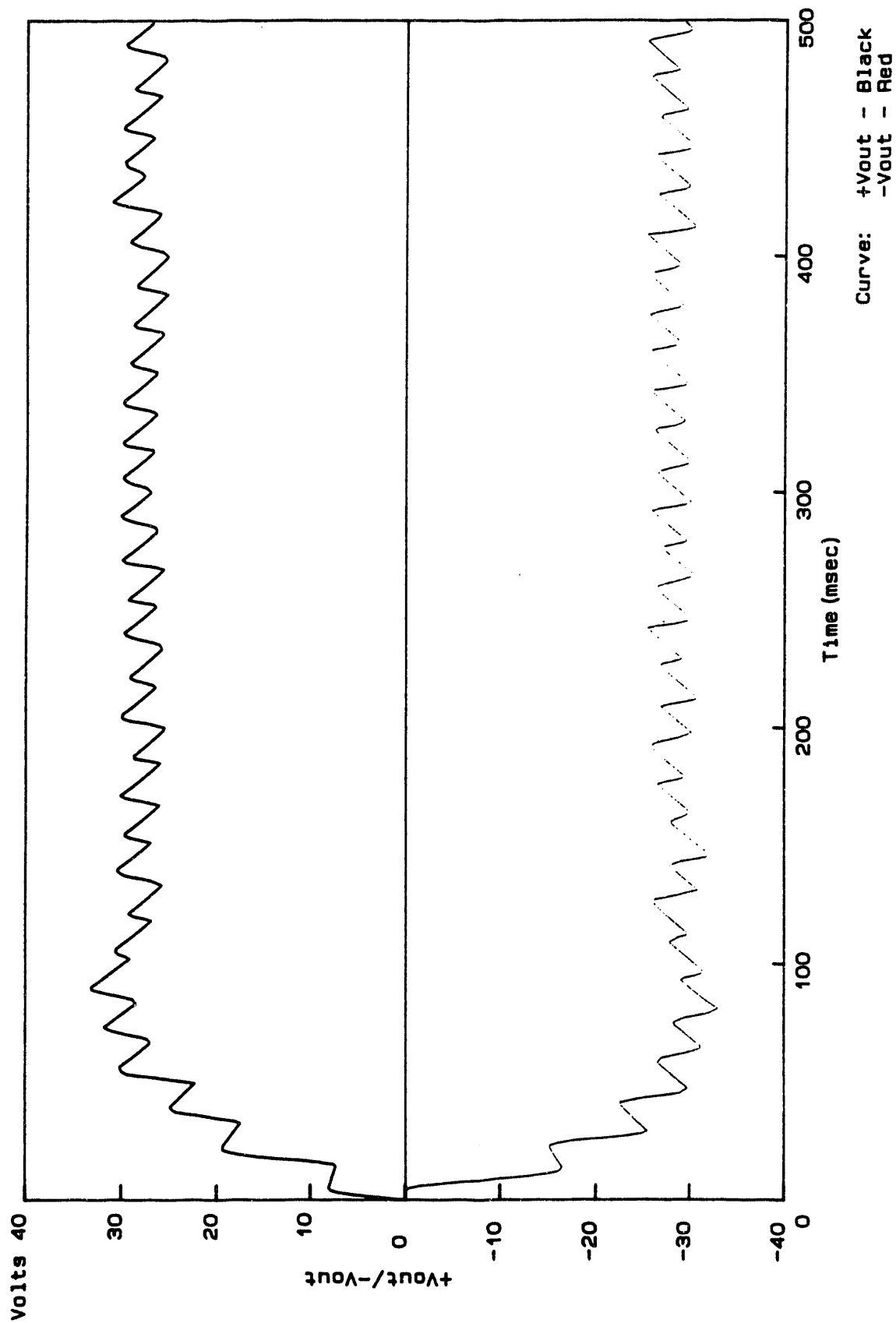


Figure 5

of the board for external connections, which are listed below. Wires of different colors are used for making connections of each section of the circuit which make tracing the circuit easier. Care is taken to avoid too many wire crossings. Physical location of the components is selected to avoid any use of unnecessarily long wire. The color convention that is used in building the circuit is indicated below. Some of the components and their functions are explained here.

**Color Convention:**

**Red - + 15 V dc or 12 V ac**

**Yellow - -15 V dc**

**White - Ground**

**Potentiometers:**

**P1 - adjust the set point voltage range**

**P2 - adjust the regulator gain**

**P3 - adjust the offset voltage**

**Test Points:**

**TP1 - check the set point voltage**

**TP2 - check the output of the first integrator**

**TP3 - check the sensor signal after being inverted**

**TP4 - +15 V dc supply (red)**

**TP5 - -15 V dc supply (yellow)**

**TP6 - Ground (white)**

**Connectors (counted from the top).**

- 1    - 12 V ac from the main board (from 23 of main board)**
- 2    - Ground (from 74 of main board)**
- 3    - +VE supply for reference voltage**
- 4    - -VE supply for reference voltage**
- 5    - Reference input**
- 6    - Ground**
- 7    - Sensor signal (from the pressure sensor +VE)**
- 8    - Ground**
- 9    - Output signal from the regulator (to 71 of main board)**
- 10   - Ground**

## APPENDIX

## LIST OF COMPONENTS

## Regulator Circuit:

Component Type and Number	Description
IC Chips	
U1, U2, U4, U6, U7, U8	Op-Amps, LM741CN
U3, U5	Op-Amps (FET), OP07
Resistors	
R1-R3, R15-R17, R20	11K, 1/4W
R4-R5, R7-R11, R13-R14	5K, 1/4W
R6	200K, 1/4W
R12	2K, 1/4W
R18-R19	1K, 1/4W
Potentiometers	
P1	50K, 1/4W
P2	100K, 1/4W
P3	50K, 1/4W
Capacitors	
C1	47UF, 50V (electrolytic)
C2	10UF, 50V (electrolytic)
Zener Diode	
Z	10V, 1N4740

**Power Supply Circuit:**

MC1468L	+15V Tracking Regulator
D1-D4	Diodes, 1N4005
C1-C4	47UF, 50V (electrolytic)
C5-C6	1620 Pf, ceramic
C7-C8	100UF, 50V (electrolytic)
RL1-RL2	5K, 1/2W
RSC+, RSC-	4.7 Ohms, 1/4W

## INTERNAL DISTRIBUTION

1. Central Research Library
2. Document Reference
- 3-4. Laboratory Records
5. Laboratory Records, R.C.
6. ORNL Patent Office
7. Y-12 Technical Library
8. G. D. Alton
9. J. B. Ball
10. F. E. Bertrand
11. D. T. Dowling
12. D. L. Haynes
13. C. M. Jones
14. R. C. Juras
15. S. N. Lane
16. M. J. Meigs
17. G. D. Mills
- 18-20. S. W. Mosko
21. D. K. Olsen
22. B. A. Tatum

## EXTERNAL DISTRIBUTION

23. Dr. A. M. Hasanul Basher, School of Engineering Technology, South Carolina State College, Orangeburg, SC 29117
24. J. T. Crockett, Jr., Director, Faculty and HBCU Programs, ORAU, Energy Bldg., Room OB-9, Oak Ridge, Tennessee 37831
25. Assistant Manager, Energy Research and Development, DOE/ORO
- 26-27. Office of Scientific and Technical Information, P. O. Box 62, Oak Ridge, TN 37831



**END**

**DATE  
FILMED**

*10 / 25 / 93*

