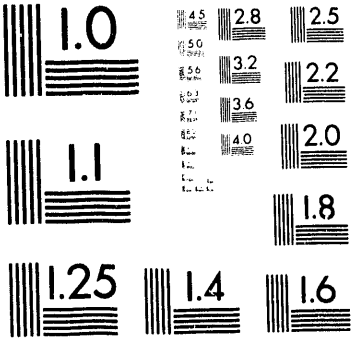
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Title: MULTIPORT SOLID-STATE IMAGER CHARACTERIZATION AT VARIABLE FIXEL RATES

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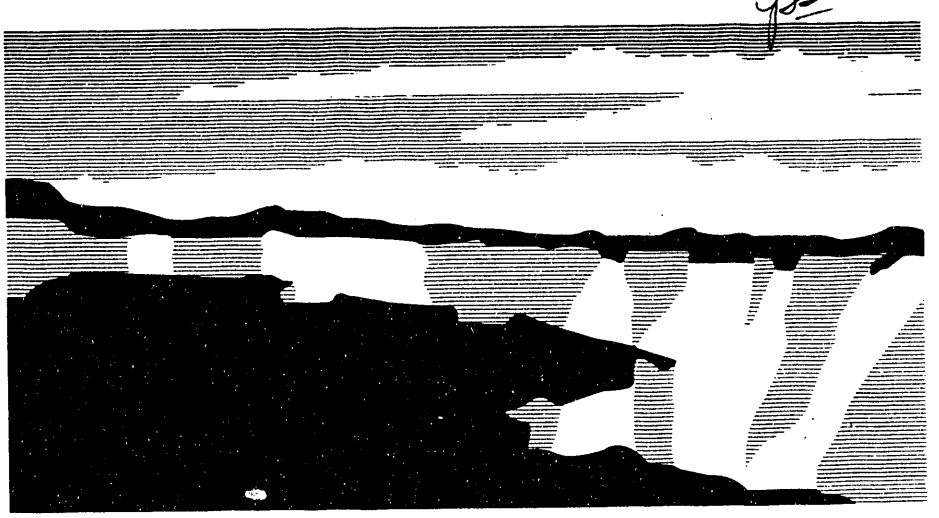

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Multiport solid-state imager characterization at variable pixel rates

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ABSTRACT

The imaging performance of an 8-port Full Frame Transfer Charge Coupled Device (FFT CCD) as a function of several parameters including pixel clock rate is presented. The device, model CCD-13, manufactured by English Electric Valve (EEV) is a 512 × 512 pixel array designed with four individual programmable bidirectional serial registers and eight output amplifiers permitting simultaneous readout of eight segments (128 horizontal × 256 vertical pixels) of the array. The imager was evaluated in Los Alamos National Laboratory's High-Speed Solid-State Imager Test Station at true pixel rates as high as 50 MHz for effective imager pixel rates approaching 400 MHz from multiporting. Key response characteristics measured include absolute responsivity, Charge-Transfer-Efficiency (CTE), dynamic range, resolution, signal-to-noise ratio, and electronic and optical crosstalk among the eight video channels. Preliminary test results and data obtained from the CCD-13 will be presented and the versatility/capabilities of the test station will be reviewed.

1. INTRODUCTION

A variety of solid-state imagers or Focal Plane Arrays (FPAs) designed to address high-speed imaging applications have recently been developed. Others are in design or R&D phases. Most designs feature multiple output video ports for parallel readout to achieve high-frame rates. The applications they will address include industrial, military, and medical imaging requirements that cannot be met using existing FPAs designed for conventional RS-170 rates or those scientific imagers designed for slow scan usage.

Testing and characterization of multiport imagers is desirable prior to fabrication of a TV camera for the devices. To meet that need, Los Alamos National Laboratory has designed and developed a high-speed solid-state test station[1] using commercially available PC/workstation based programmable waveform generators, digitizers, and display/analysis codes. Using commercially available hardware and software provides flexibility in the areas of portability and upgrades as improvements become available. The test station also requires specialized high-speed digital and analog circuitry, unique clock waveform software codes, and processing circuits, which are designed in-house at Los Alamos National Laboratory.

In this paper, the test station is discussed briefly and we report test results obtained using the station to operate the EEV CCD-13 , an 8-port FFT CCD.

2. TEST STATION

The station, because it uses a common set of drive and amplifier circuitry, permits direct comparison of important response data measured among various FPAs. This eliminates the requirement for exhaustive and sometimes inconclusive corrective normalizations to measured data as is currently required when FPAs are tested in their highly individualized camera systems as provided by the various manufacturers.

The programmable feature of the pattern generator provides variable clocking speeds to study rate effects on crucial FPA parameters such as responsivity, CTE, and resolution. Variable phasing among the multiple clock waveforms is also programmable to study duty cycle and overlap effects.

The test station can function as a PC-based "breadboard" for camera design engineers, thereby minimizing the number of actual prototype fabrication iterations required for optimization of camera/imager performance prior to finalization of designs. This utility of the test station facilitates development of special printed circuit "header" boards for any FPA providing optimum drive and acquisition circuitry, which is further enhanced using surface mount technology.

The test station block diagram is shown in Fig. 1. There are seven major components that comprise the station. These are (1) a programmable pattern generator and logic recorder for clock waveform generation and monitoring; (2) an imager header board that serves as a chip carrier mounting interface with clock level shifters to drive the FPA and video buffers/amplifiers to sample the FPA video outputs; (3) a high-speed digitizer for acquisition and storing video images from the FPA with subsequent downloading to PC/workstation using general purpose interface bus (GPIB) interface; (4) real-time display capability using a video multiplexer and x-y display for observation of one FPA video port at a time; (5) software for array reformatting and manipulation including translation, rotation, and analysis; (6)

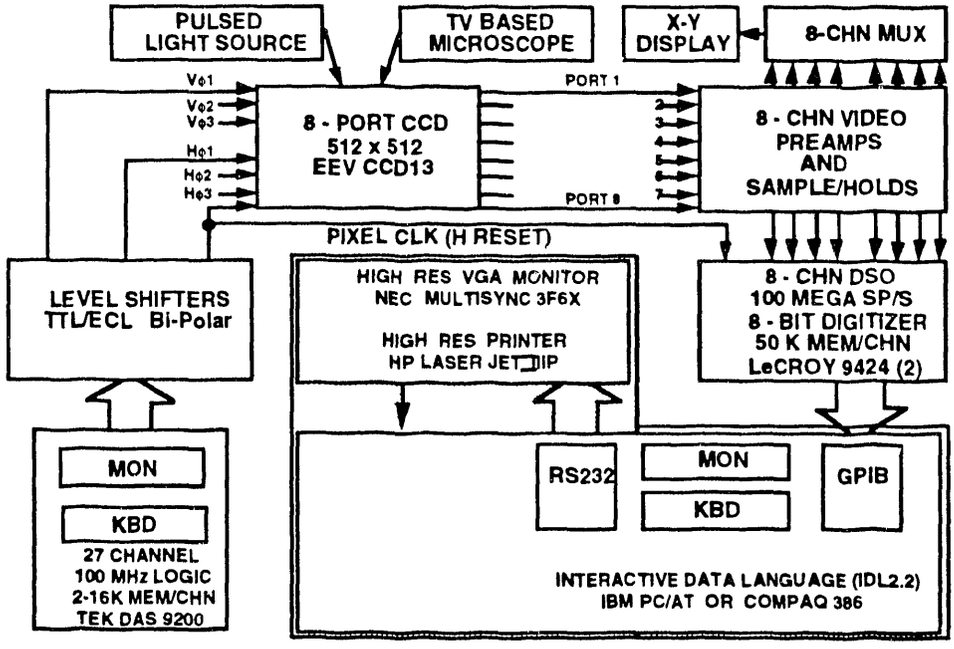


Figure 1. Programmable high-speed solid state imager test station block diagram. This configuration is for the EEV CCD13.

optical/electrooptic apparatus including precision mounts, various wavelength continuous wave (cw) and pulsed light sources, pinhole and conventional resolution patterns for optical stimulus to the FPA; and (7) a high-power TV microscope for chip inspection and for precise monitoring of location and positioning of pinhole illumination on strategic FPA pixel structures.

The programmable pattern generators are key components of a Tektronix PC-based multichannel waveform generator/recorder system, the Model 9200DAS (Digital Analysis System). They can be configured to provide either 54 channels capable of clock speeds up to 50 MHz or 27 channels for clock speeds between 50 and 100 MHz. The 54-channel version is comprised of two pattern generator boards, an 18-channel Model 92S16 and a 36-channel Model 92S32. The 27-channel version is accomplished by time-multiplexing half of the 92S16 channels for 9 channels and similarly half of the 92S32 channels for 18 channels. High-speed versions of the two generators, named 92SX109 and 92SX118, respectively, for the multiplexed 92S16 and 92S32 generators are for 50 to 100 MHz operation with the reduced number of channels.

The pattern generators are of different designs. One type (the 92S16 or 92SX109) provides algorithmic control over waveform generator sequences, allowing the operator to use familiar "FORTRAN-like" instructions. For repetitive waveforms, counters can be implemented by executing load and decrement/increment instructions based upon appropriate "decision-making" jump commands. Such "do-loops" can be nested to select the quantity of pixels per row followed by the quantity of rows per field for a given imager. The second pattern generator board (the 92S32 or 92SX118) can only be programmed for sequential execution of consecutive lines of output waveform vectors. Both generators are used to implement a replicated sequence of output waveform vectors. The 92S16 or 92SX109 functions as the "master" by controlling the number of times a given sequence is to be output while the 92S32 or 92SX118 functions as the "slave" outputting the desired waveform vectors during the sequence.

Each line of code is executed as the system clock is advanced. Depending on the code written for a given waveform, the system clock rate may or may not correspond to the FPA pixel clock rate. For the CCD-13, if time-phasing among each of the three horizontal phases is generated by three successive system clock pulses (all data presented are from this configuration), the effective pixel rate is one-third the system clock rate. If all three phases are generated by the same clock pulse and time-phasing is established internally (with 9200DAS phasing control) or externally using delay lines, then the pixel clock rate is the same as the system clock rate.

Output waveforms are generated for each channel by active line drivers at the probe tips of the pattern generator 10-conductor probe (Model 6464). They appear as static Boolean logic state variables corresponding to a given line of vector binary code, and change on a clock-by-clock basis as the program code is sequentially executed line-by-line. When the code is monitored on a continuous basis (by continuous clocking), the output waveforms are represented as real-time, time-varying transistor-transistor logic (TTL) or emitter-coupled logic (ECL) waveforms.

The header printed circuit board for the CCD-13 is shown in Fig. 2. The level shifters are high-speed, high-current switches that use MMBT 3960A NPN and MMBT 4216A PNP transistors in surface mount SOT-23 configurations. The switches operate as "charge pumps"[2] to quickly charge/discharge the CCD's vertical and horizontal clock line input capacitances and then remain quiescently idle for most of the actual clock pulse duration. This is accomplished by differentiating the square-wave clock pulses, thereby using primarily only leading and trailing edges for driving the switches. This approach reduces power dissipation significantly over that achieved by conventional full duty cycle "switching driver" technology

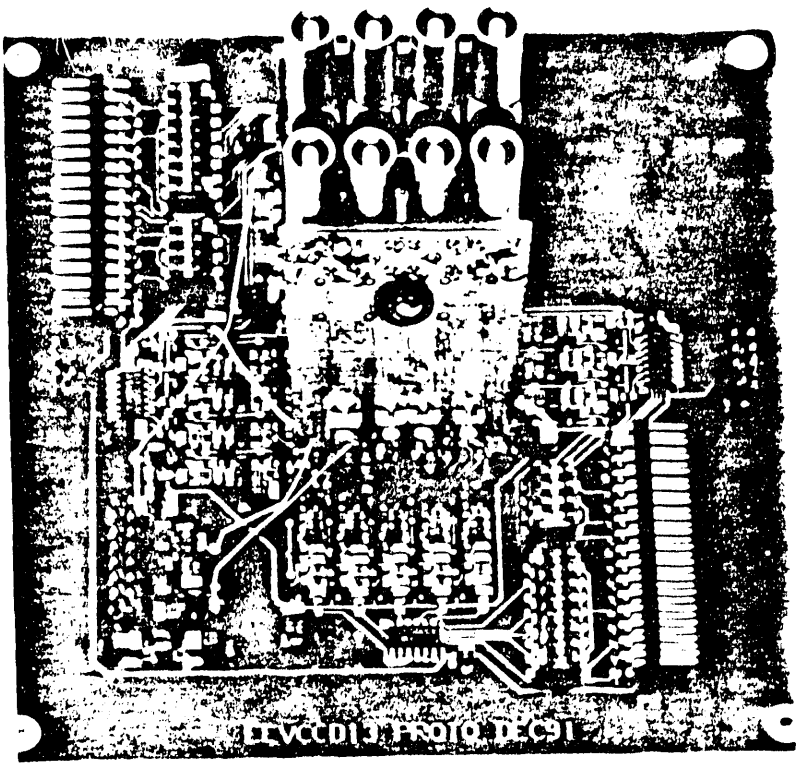


Figure 2. The surface mount printed circuit board for the CCD-13 imager showing high-speed level shifters and eight channel amplifier block (out of the plane of the board).

used by many designers. The high- and low-voltage levels between which the waveforms switch are jumper selectable. This high-level range is from +10 V to +20 V and the low-level range is from –5 V to +2 V.

The preamplifiers used in the CCD-13 header PC board are of nonlinear gain differential amplifier configuration using high bandwidth (–3 dB corner frequency of 200 MHz) Comlinear CLC400 DIP-8 integrated circuit operational amplifiers. Other preamplifier designs have been designed and prototyped for this imager to investigate various fixed pattern noise cancellation or minimization techniques. The data from those designs is currently under investigation but will not be available for this paper.

Self-clocking Sample and Hold circuitry was designed[3] using "constant fraction" techniques to follow the individual pixel peak charge amplitudes as functions of pixel clock rate and charge. This technique is essential to assure proper time-phased sampling of slew rate limited pixel charge where peak amplitudes vary with both input optical intensity and pixel readout frequency.

The digitizer system is comprised of two 4-channel high-speed digital sampling oscilloscopes (DSOs), LeCroy Model 9424 with internal 100 MHz sampling frequency or external clocking with system clock from the DAS9200. Each channel has a –3 dB at 350 MHz amplifier and an 8-bit flash analog to digital converter (ADC) capable of recording and storing up to 50 K samples. The video is stored in the DSO and can be analyzed using resident LeCroy waveform processing packages WP01 and WP02. The

WP01 option includes time domain signal averaging, integration, differentiation, square root, offset-dithering, log functions, absolute value, and extremal calculations. The WP02 option is a spectrum analysis package, which includes Fast Fourier Transform (FFT) and frequency domain functions.

The station digitizers are being expanded to include two additional 8-bit LeCroy 9314 DSOs that provide 1 megabyte of memory per channel. These new memories will provide storage for higher pixel density arrays than can be accommodated by the older 9424 DSOs. Data files can also be downloaded to a Compaq 386 PC using the GPIB port for further analysis with a variety of commercial software packages.

The current data analysis software package in use is Research System's Interactive Data Language (IDL) version 2.2. The capabilities include array matrix manipulations for reformatting the input data, gain contrast functions, vertical and horizontal profiling, and isometric and contouring routines. The choice of IDL was prompted by its capability to analyze nonstandard array formats by identifying quantity of lines (or rows) per field and quantity of pixels per line.

3. EEV CCD-13 DETAILS

High-speed operation of solid-state imagers is enhanced by providing multiple video output ports that permit parallel readout of several segments of the total array simultaneously. Additional increases in readout speed are accomplished using bidirectional clocking of pixel charge, both vertically and horizontally. Referring to Fig. 3 for the EEV CCD-13, this is accomplished by shifting rows (or lines) in the upper half of the array (Section A) upward into the top horizontal registers E and F, while simultaneously shifting rows in the lower half of the array (Section B) downward into the bottom horizontal registers C and D. Each row is composed of 512 pixels, 128 pixels from each of the four segments of one section. The first half of a row (pixels 1 to 256 corresponding to segments 1 and 2) are loaded into one horizontal register (register F for Section A, register C for Section B). Similarly, the second half of that row (pixels 257 to 512 corresponding to segments 3 and 4) is loaded into a different horizontal register (register E for Section A, register D for Section B). Each row is essentially truncated into two "half rows" by this device topology. Once a "half row" is loaded into its horizontal register, pixel charge within the "half row" is again simultaneously clocked (or shifted) left and right into output amplifiers located at each end of the register. For example, register F shifts pixels from TOP segment 1 bidirectionally, pixels 1 to 128 left into video Port 8, and pixels 129 to 256 right into Port 7. This highly parallel readout provides automatically at least an 8X improvement (over standard serial readout) in readout speed for a given pixel rate. In addition, the split array and split register readout scheme described earlier should provide additional increases at higher pixel rates where propagation times through the array or register dominate the response time.

The CCD-13 is designed to provide eight real output video ports (designated "OS") and eight dummy output ports (designated "DOS") as shown in Fig. 3. Two real ports read out each half of one of the four horizontal registers, hence the eight real outputs.

The dummy outputs are provided to allow fixed pattern noise subtraction in off-chip differential amplifiers. The dummy output is from an on-chip amplifier that is geometrically identical to the real output amplifier but has no light-generated image charge. Because it is located adjacent to its real output counterpart, the dummy output provides localized fixed pattern noise for proper background subtraction in the differential amplifier. Therefore, the header for this imager (shown earlier in Fig. 2) has eight 2-input preamplifier channels that are operated simultaneously in parallel configuration.

The characteristics of the CCD-13 (provided by EEV) are highlighted in Table 1.

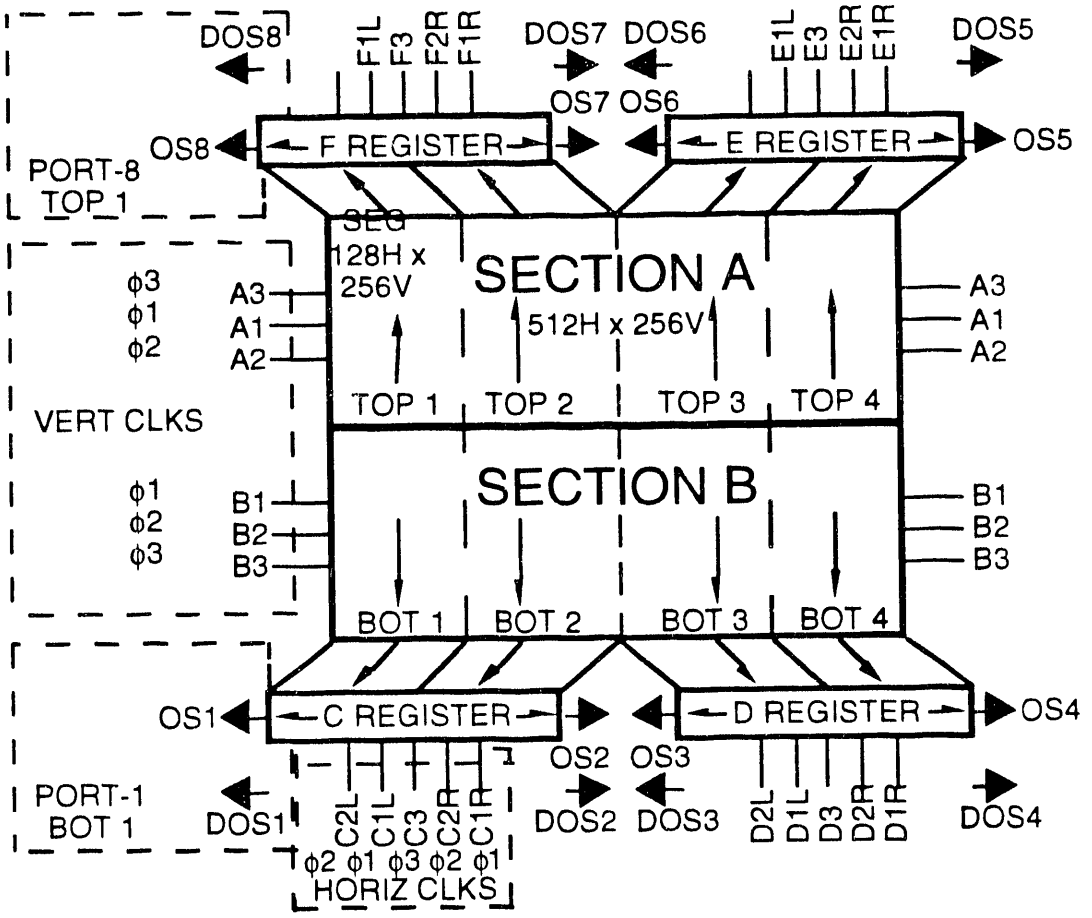


Figure 3. Functional schematic for the CCD-13 showing multiport bidirectional readout architecture.

4. MEASUREMENTS AND DATA

4.1. Experiment details

Light sources used for electrooptic characterization of the CCD-13 imager used the precision optics provided by TVO Optoliner Model K-4000 by Optical Instruments Corporation. A variety of calibrated pinhole arrays with diameter and pitch in the range of 5 to 75 microns were used to measure and estimate Point Spread Function (PSF) of the CCD-13 pixel structure. Standard Retma resolution patterns and PR-10 bar charts were used for Contrast-Transfer-Function (CTF) measurements. A variable diameter aperture was used to test amplifiers for area crosstalk, and sag or droop characteristics. Pulsed sources included a 532 nm frequency-doubled Nd·Yag laser and Xenon strobes. A COMPAQ 386 PC-based Optronic Model 740 spectrometer system was used for spectral and radiometric calibrations. The Nd·Yag laser, Spectra Physics Model 7000, a diode-pumped Q-switched laser, produced ≈ 10 μJ/pulse with ≈ 15 ns FWHM. The Xenon strobe, General Radio Model 538 produced much broader spectrum and longer pulses ≈ 10 μs FWHM, which were spectrally filtered to narrow bands ($\approx \pm 10$ nm) in the blue (400 nm) and green (520 nm). These three wavelengths represent the light spectra used in various LANL imaging experiments. The 532 nm is used in an underwater mine detection system. The 520 nm simulates the spectral emittance of P-20 phosphors used in image intensifiers that are coupled to LANL FPA cameras

Table 1. EEV CCD-13 FFT CCD specifications.

Architecture	
Image Area	10.75 mm × 10.75 mm
Horizontal pixels (active)	512
Vertical pixels (active)	512
Pixel size	21 μm × 21 μm
Number of output amplifiers	8
1 transitional, 7 dark reference, and 4 blank (or inactive) pixels are provided on either side of the image area for baseline restoration. Twenty-one nonimaging lines (or rows) are provided at top and bottom sections for buffering.	
Gated antiblooming drains are optional.	
Performance	
Number of output amplifiers	8
Maximum readout frequency	>20 MHz per amplifier
Total readout time	<2 ms
Responsivity	2.5 μV/electron
Peak signal	1000 mV
Peak charge storage	4.6×10^5 electrons
Dynamic range	5000:1
Binning capacity of output registers	4X
Saturation exposure (570 nm)	≈0.3 μJ/cm^2
Chip power dissipation	≤840 mW
Package	72 pin PGA

for high-speed shuttering and the 400 nm is the peak emission from Bicron BC430 or National Enterprises NE102 plastic scintillators when irradiated with ultraviolet or ionizing radiation sources.

The test station is designed with a precision mount for positioning of the solid-state imager header board with respect to calibration light sources. This mount and positioner, which is located on an optical bench for stability, provides micrometer resolution (1-10 μm) adjustments along both horizontal and vertical axes of the imager.

The experimental setup for measurements is shown in Fig. 4. The TVO Optoliner system forms the optical stimulus platform. It is used with its standard white light DC illumination source or by substituting one of the two pulsed light sources, i.e., the laser or xenon strobe. Referring to Fig. 4, when using the laser, an expansion lens is used to magnify the beam before it is directed to the diffuser. Both magnification and diffusion are required to produce a large area fairly uniform Lambertian source from the laser. For the xenon strobe source, the parabolic reflector helps with initial diffusion of the xenon lamp's filament structure. Both sources are fairly uniform over a disc of ≈1.5 to 2 inches diameter before relaying to the FPA sensors.

4.2. Optical crosstalk measurements

Initial optical crosstalk measurements were taken using the Nd·Yag laser. The beam spot of ≈2.5 mm diameter was imaged onto the center of TOP4 segment of the CCD-13 (refer to Fig. 3 for

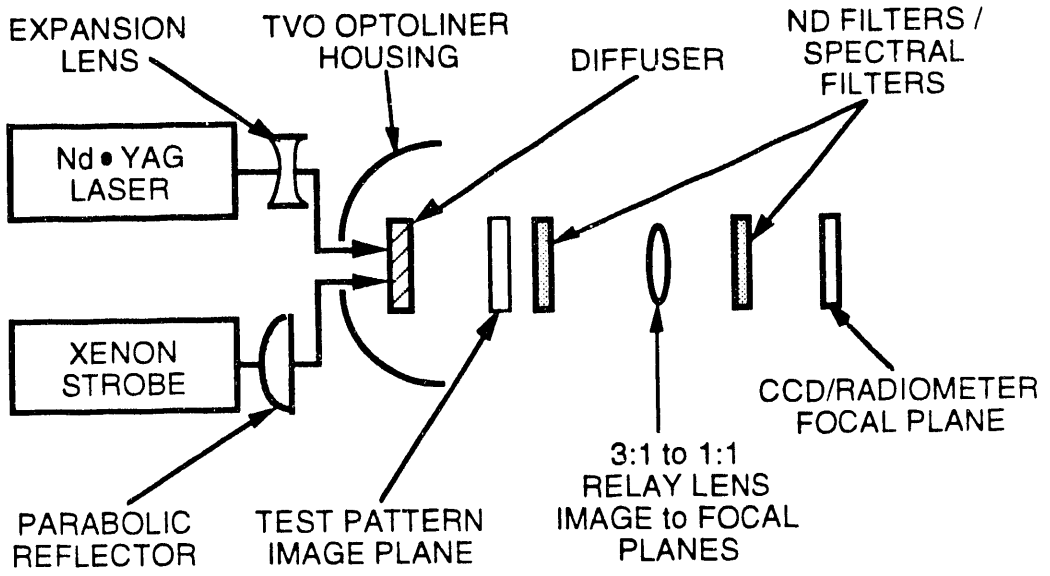


Figure 4. Experimental setup for pulsed light sources used in evaluation of the CCD-13 in the test station.

orientation). The imager without gated antiblooming drains was used and the laser irradiance was increased to approximately 5X saturation level for this test. The video peak amplitude corresponding to the centroid of the laser spot was measured from video port-5 (output for segment TOP4 as shown earlier in Fig. 3) and compared with spatially uncorrelated increases in video above quiescent unilluminated (dark) levels from the remaining seven ports. The test results are in Table 2. The noted increases in video from unilluminated segments are a measure of optical crosstalk and are probably due to a variety of light scattering mechanisms, including both internal and external reflections and refraction. The data show no obvious spatial correlation between illuminated areas and those unilluminated areas most strongly affected. Adjacent areas were not necessarily the most susceptible. No attempt was made to mask unilluminated segments or to repeat measurements at reduced irradiances because we felt the 5X saturation intensity represented the worst-case anticipated overexposure from most of our imaging applications, and masking is not feasible in "real" applications. The normalized values for the unilluminated segments at 1X

Table 2. CCD-13 Optical crosstalk from reference 5X saturation exposure in segment TOP4, which gave ~213 mV peak amplitude at centroid of illuminated area.

Segment	Video (mV)	Percentage of Reference (213 mV)	Percentage of Reference at 1X SAT
TOP1	2	0.9	0.18
TOP2	10	4.7	0.94
TOP3	4	1.8	0.36
BOT1	12	5.6	1.12
BOT2	8	3.8	0.76
BOT3	16	7.5	1.50
BOT4	12	5.6	1.12

saturation intensity in TOP4 segment are included in Table 2. At 5X saturation intensity, the data indicate ≈4.3% average crosstalk and ≈0.86% for the 1X saturation intensity. These crosstalk figures of merit were calculated using the following expression:

$$\text{crosstalk} = \frac{\text{observed signal - quiescent dark signal (Port - n)}}{\text{reference signal - quiescent dark signal (Port - 5)}} \quad .$$

To eliminate any infrared contributions from the Nd·Yag laser, the tests were repeated using the xenon strobe. A reference area just equal to the width of one segment was illuminated. The irradiance was set to just saturate the CCD-13. Segment BOT3 was illuminated and the video from two adjacent segments, TOP3 and BOT4 was digitized and analyzed using the DSO WP01 processing routines. Similar analysis under unilluminated conditions indicated increases in rms video values of ~2.2% for BOT4 and ~0.78% for TOP3. (The data are in Table 3.) These values are in good agreement with the previous data. They are somewhat higher, but are from larger area of illumination in the reference segment.

Table 3. CCD-13 optical crosstalk between a reference illuminated segment (BOT3) at 1X saturation and two unilluminated adjacent segments (TOP3 and BOT4). The illuminated reference signal was ~284 mV peak.

	TOP3		BOT4	
Signal Value	In Dark (mV)	BOT3 at SAT (mV)	In Dark (mV)	BOT3 at SAT (mV)
Maximum	26.2	26.2	22.1	22.1
Minimum	−9.7	−10.0	−8.0	−8.5
Mean	10.66	10.84	11.04	11.13
Standard deviation	3.86	4.10	3.46	3.50
rms	11.34	11.59	11.57	11.66

Another optical property of the CCD-13 was observed,[4] i.e., background buildup across a given partially illuminated segment when the other segments are fully illuminated. This varies with intensity as shown in Table 4. Reasons for the build-up were not identified. However, because the imager was essentially fully flooded with only a small area unilluminated, the build-up could be from smear leakage. This is a possible mode of operation so the background build-up characteristic could be a potential problem.

4.3. Electrical crosstalk

The primary electrical noise in the CCD-13 is fixed pattern noise associated with the pixel clock waveforms. The composite CCD pixel signal is a combination of clocking waveform components and light-induced charge. The CCD-13 architecture provides two on-chip source follower amplifiers for each segment as shown in Fig. 3. One amplifier ("real" output, labeled OS) receives light-induced pixel charge. The other ("dummy" output, labeled DOS) is identical to the OS amplifier except that it receives no charge. The "OS" notation is for the output source of the FET on-chip source follower amplifier. Because both OS and DOS amplifiers are spatially located adjacent to each other, they both have similar fixed pattern noise signatures. This provides camera designers with a quiescent dark reference signal from the DOS amplifier, which can be subtracted from the OS amplifier, leaving only the signal charge for off-chip

Table 4. CCD-13 signal and background build-up versus input light intensity from saturation to noise levels. A different imager/amplifier provided by EEV was used for this test.

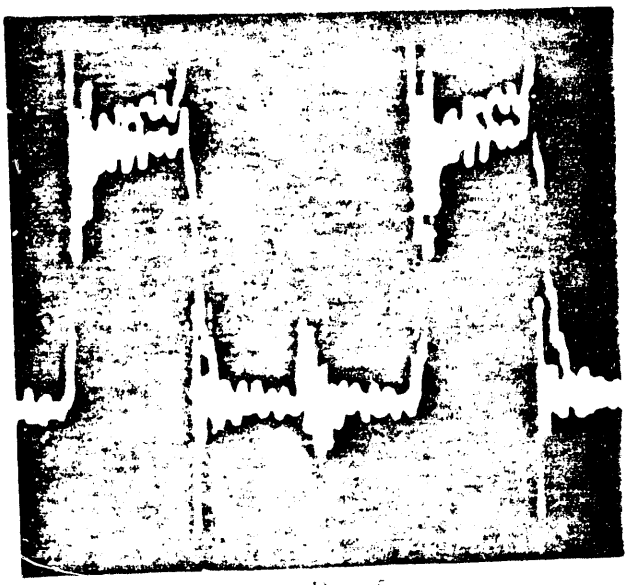
Input Light		Peak Signal (mV)			Background (mV)			Difference (mV)
Fstop	ND	Av	SDv	Var	Av	SDv	Var	
1.2	0	1023	0	0	47	3	9	976
1.4	0	831	0	0	42	2	6	789
2	0	428	0	0	29	2	4	399
2.8	0	228	0	0	21	1	2	207
4	0	122	1	2	17	1	2	105
5.6	0	66	1	3	13	1	2	53
8	0	36	1	1	12	1	2	24
11	0	23	1	1	9	1	1	14
16	0	16	1	1	10	1	2	6
16	0.3	13	1	1	9	1	2	4
16	0.6	12	1	1	9	1	1	3
16	0.9	11	1	1	9	1	1	2

amplification. This is accomplished by using conventional differential amplifiers. For this to work optimally, the ac gains and dc biases must be identical for both OS and DOS amplifiers.

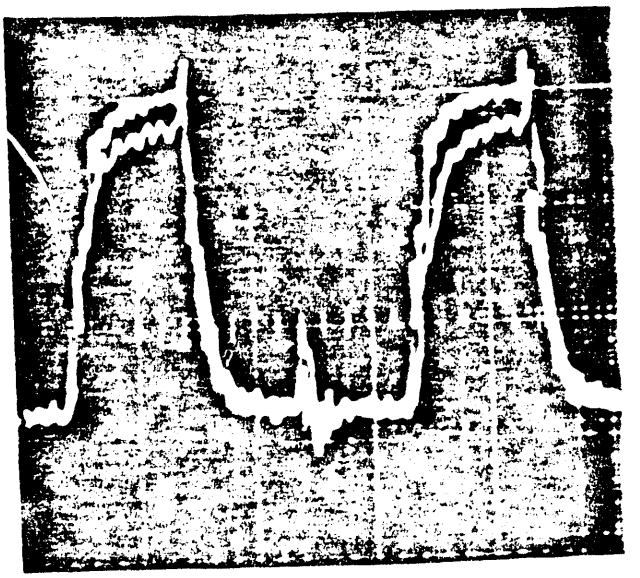
The quiescent drain-source bias currents in the OS and DOS amplifiers generate dc voltages across their respective external load resistors. The bias currents for the various OS ports were measured indirectly by measuring voltages [product of current (i) and resistance (r)] across their 3.9 kΩ load resistors. These varied slightly among ports. The average voltage was +8.76 V and the variance was ±0.02 V or ≈ ±0.23%. This corresponds to a nominal 2.25 mA. These differences among OS ports can be corrected by using different dc offsets in the test station digitizers to normalize all dc levels for equal dark reference. The DOS outputs have variable load resistors to allow adjusting of ir voltages to equal those at their OS counterpart outputs. However, this also affects gain because the source follower output impedance (1/gm) is finite (≈300 Ω) and is in series with the ≈3.9 kΩ source resistors. The net result is that corrections to normalize dc components may result in unequal ac components or vice versa.

The OS and DOS pixel waveforms from Ports 5 and 6 for the CCD-13 operated in a dark unilluminated condition are shown superimposed in Fig. 5. The differences in noise signatures between the two ports is obvious. This illustrates the value of the dummy amplifiers for canceling area or location "specific" rather than "average" or "typical" clock feedthrough fixed pattern noise components. [The normally narrow reset noise feedthrough component is not obvious on these waveforms because the reset and horizontal phase three (ϕ3) clocks were set at the same duration and phasing (for convenience) for this data set.] Similar waveforms were observed at all eight ports. Although most other ports showed better symmetry in their OS and DOS signatures, Ports 5 and 6 were selected to demonstrate potential problems with this noise cancellation technique.

Typical DOS fixed pattern noise signatures appear similar to their OS counterparts except for slightly lower amplitudes and slight time-phase differences. On the average, the DOS amplitudes are 225 mV whereas the OS amplitudes are 250 mV, or ≈ 10% higher. The differential output from the OS and DOS signals, also shown in Fig. 6, illustrates the incomplete cancellation. The differentiation on the

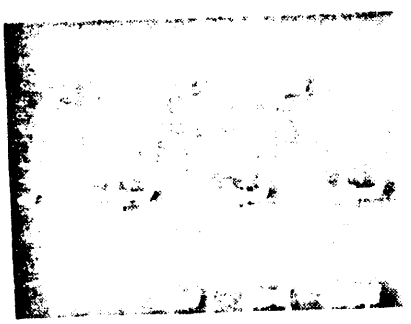


a. Port 5

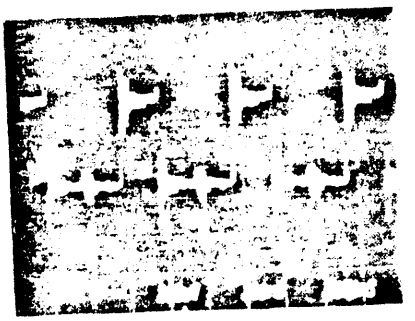


a. Port 6

Figure 8. The OS and DOS waveforms from ports 5(a) and 6(b) are shown superimposed to demonstrate differences in structure and amplitude between dummy (DOS) and real (OS) components and also between ports. The CCD 15 was operated in the dark for these waveforms.

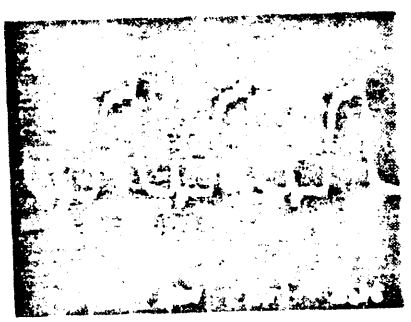


a. Port OS5, dark

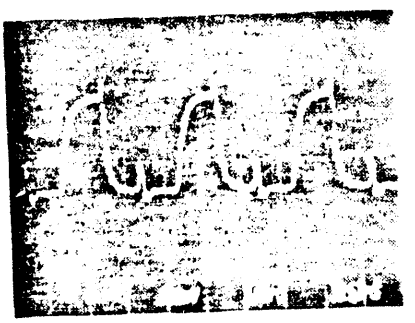


b. Port DOS5, dark

c. Output of differential amplifier



d. Port OS6, dark

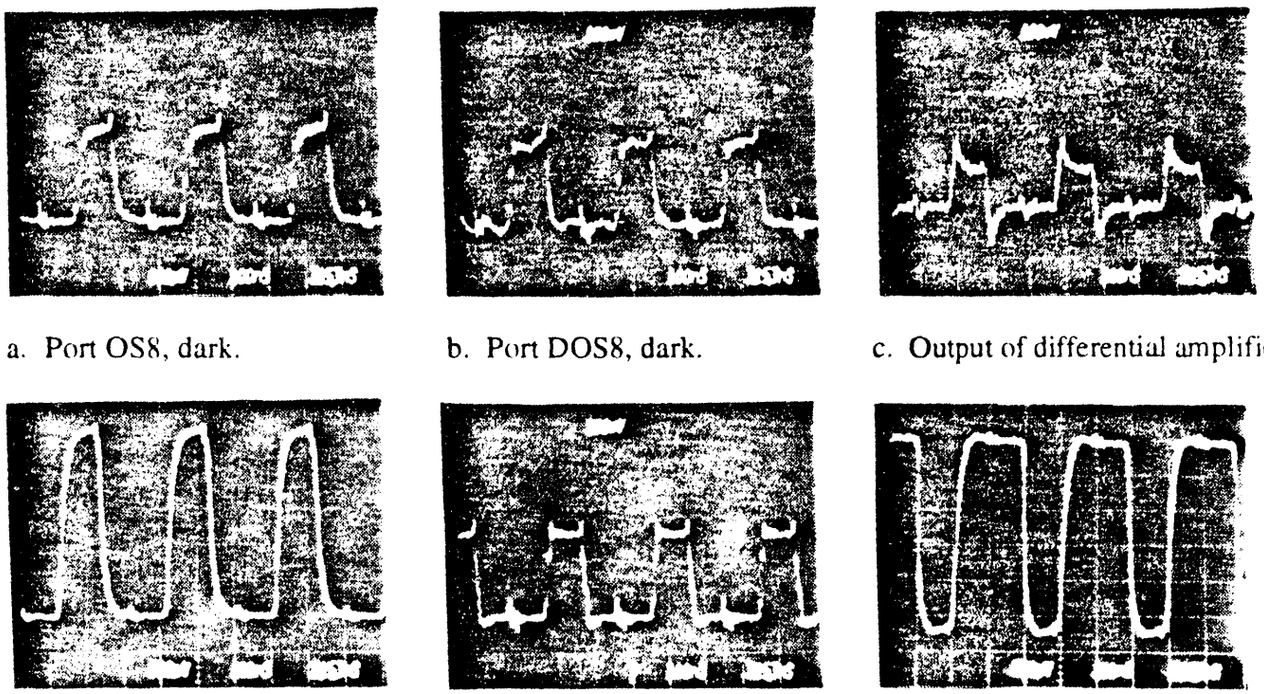


e. Port DOS6, dark

f. Output of differential amplifier

Figure 9. Noise signatures of OS and DOS amplifiers for Ports 5 and 6 when their segments (TOP5 and TOP6, respectively) are dark or unilluminated. These signatures are fixed pattern noise picked up by parallel clocking waveforms as they propagate through the CCD 15 clock electrodes.

leading and trailing edges is due to the time phase difference between the two signals. The slight negative signal is because the differential gain was 4 for the DOS input and 3 for the OS input, which intentionally negated absolute amplitude cancellation for easy identification of the two components. The differential amplifier was configured to accept OS signals at the inverting input and DOS signals at the noninverting input. Referring to Fig. 7, the OS and DOS signals for Port 8 and the differential amplifier's output (with



a. Port OS8, dark.

b. Port DOS8, dark.

c. Output of differential amplifier.

d. Port OS8, near saturation.

e. Port DOS8, with OS8 near saturation.

f. Output of differential amplifier.

Figure 7. Port 8 (segment TOP1) noise and signal signatures from DOS8 and OS8 amplifiers in dark and at saturation. The DOS signatures are very similar for the dark and illuminated conditions confirming their use for effective noise cancellation. Differences, however, are another indication of optical crosstalk.

50 Ω source and load resistances) in the dark and at saturation level illumination are illustrated. The expected and measured voltages under both conditions are in good agreement. For the dark condition, expected value [(−250 mV)(−3) + (−235 mV)(4)]/2 was ≈−95 mV and measured value was ≈−100 mV (Fig. 7c). For the saturated condition, expected value [(−1.05 V) (−3) + (−235 mV)(4)]/2 of ≈ 1.1 V and measured value (Fig. 7f) are approximately the same. These minor differences can be normalized with independent gain and phase controls for the OS and DOS signals prior to feeding the differential amplifier as shown in Fig. 8.

4.4. Dynamic range

The dynamic range of the CCD-13 was measured initially at 100 ns clock period using the Nd·Yag laser operated at 1 pulse per TV field. Segment BOT4 (Port 4) was used for these measurements. The peak signal/peak-to-peak noise was measured as ≈150:1. Using the nominal form factor of 3.3 to relate peak-to-peak and rms noise values gives dynamic range of >500 (Fig. 9).

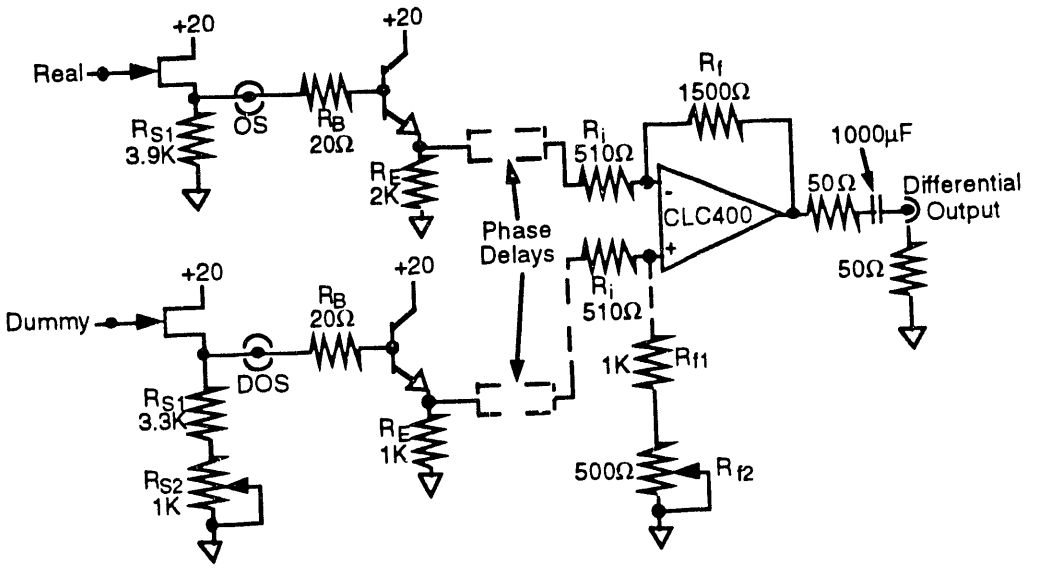


Figure 8. Differential amplifier for the CCD-13 featuring independent gain and phase controls for the OS and DOS amplifiers.

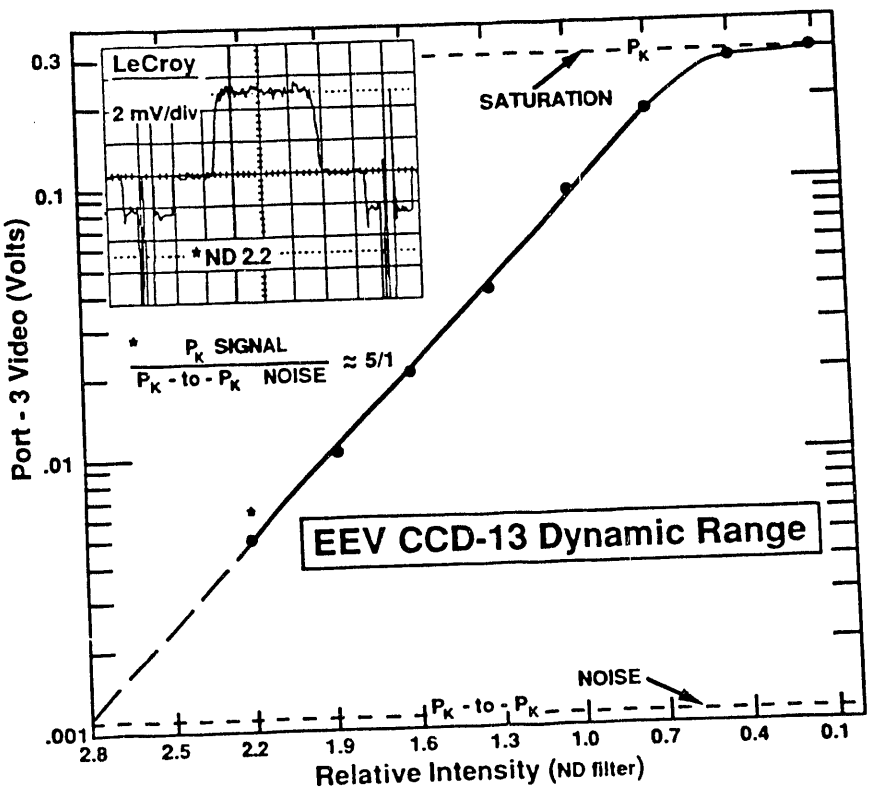
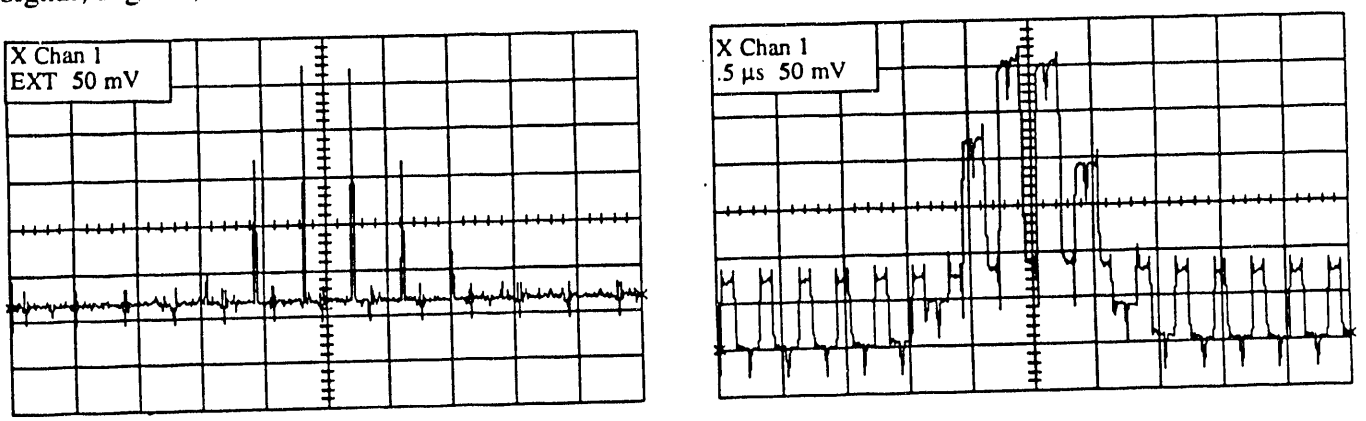


Figure 9. Dynamic range of the CCD-13. The inset in the figure shows a DSO scan line profile from which a single point on the transfer curve is derived. The asterisk indicates this amplitude profile corresponds to the ND2.2 point on the light axis with signal-to-noise ≈5:1.

The dynamic range of another segment (BOT3, Port 3) was measured using the xenon strobe with ~5 mm diameter aperture and plotting digitized values obtained directly from the processed DSO data. These data plotted in Fig. 9 indicate a somewhat larger dynamic range, ≈300:1 for peak signal to peak-to-peak noise or ≈1000:1 for peak signal to rms noise. This method of automatic data analysis using the DSO processing routines is probably more accurate than our older technique of measuring peak signals and "estimating" peak-to-peak noise levels. The processed data also give maxima, minima, and standard deviation values, which can also be used objectively for calculating dynamic range using these variables.

4.5. Resolution measurements

Using the xenon strobe and a 210 μm single pinhole with ≈2.7:1 demagnification ratio in the Optoliner produced an image spot of ≈78 μm diameter on the CCD-13. The resultant digitized video signal, Fig. 10, shows six rows (TOP) and six pixels (BOT) with charge. Along each axis the pinhole



a. Lines or rows illuminated.

b. Pixels illuminated.

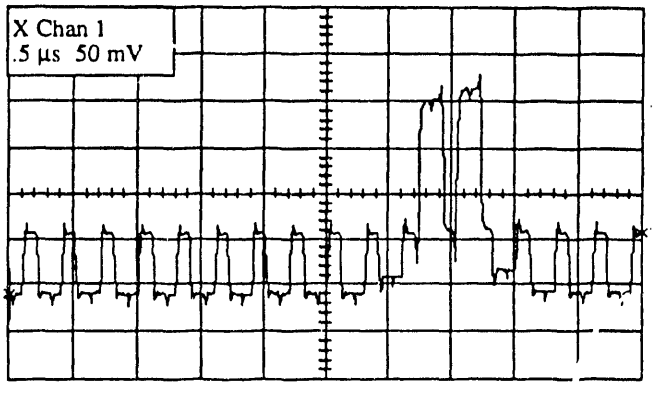
Figure 10. Single 210 mm diameter pinhole imaged demagnified ~2.7:1 onto the CCD-13.

image centroid shows a maximum (two pixels) and two slightly lower amplitude adjacent lobes (probably corresponding to the intensity distribution across the pinhole). There is also evidence of two much lower level side lobes, which we feel correspond to only partial illumination of pixels. The CCD-13's 21 μm^2 pixels indicate a centroid ≈84 × 84 μm from the imaged spot. Comparing the relative amplitudes of the centroid and side lobes indicates that, on the average, <10% of two additional pixels were illuminated along both axes. To a first approximation this adds ≈17 μm to the centroid diameter resulting in 88 μm for total pinhole diameter. Within experimental accuracy, this composite measured image is in good agreement with the projected image.

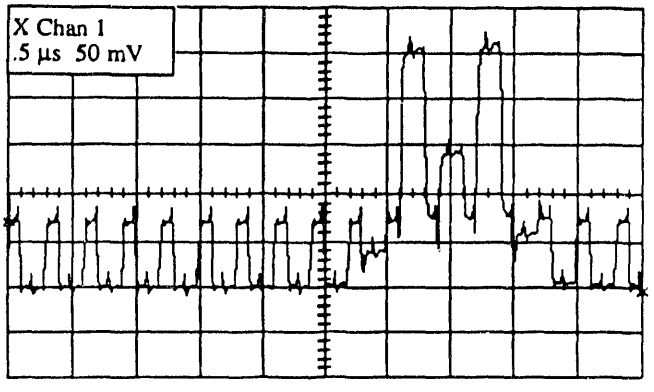
Next, PSF measurements were taken using the pinhole array patterns described earlier. The 25, 50, and 100 μm arrays were used with 2.7:1 demagnification providing 9.3, 18.5, and 37 μm diameter apertures with 16.7, 33.3, and 37 μm separation or spacing, respectively, at the CCD-13 focal plane. These apertures, their spacing, and the 21 μm^2 pixels of the CCD-13, when coupled with the spatial resolution (microns) of the test station translation positioning mounts, can result in several pixel illumination patterns. With care, the pinhole images can be strategically mapped onto the imager to preferentially illuminate individual pixels versus partial illumination of several pixels. The test station clock period was fixed at 100 ns for the first series of tests. The input intensity was varied to keep the CCD-13 out of saturation for the three pinhole arrays. The DSO was clocked internally to allow examination of individual pixels along a row (or line).

The data are shown in Fig. 11. The pixel data correspond to horizontal scans across the array. The scans show profiles corresponding to the optically transmissive pinholes (apertures) and the opaque area between pinholes. The resolving power of the CCD-13 is apparent from this data set. The 37 μm and 18.5 μm arrays are resolved with approximately the same valley-to-peak ratios (≈52%). The 9.3 μm array is not resolved. These two pinholes and their spacing project an array width of only 35 μm, which should occupy either two or three pixels depending upon image mapping between optics and the CCD-13. An array intermediate to the 18.5 and 9.3 μm arrays is necessary to ascertain the PSF accurately. In principal, this approach should provide amplitude/basewidth overlap data sufficient to measure PSF directly. The variable magnification of the TVO Optoliner optics and the various pinhole arrays available will allow this in later experiments.

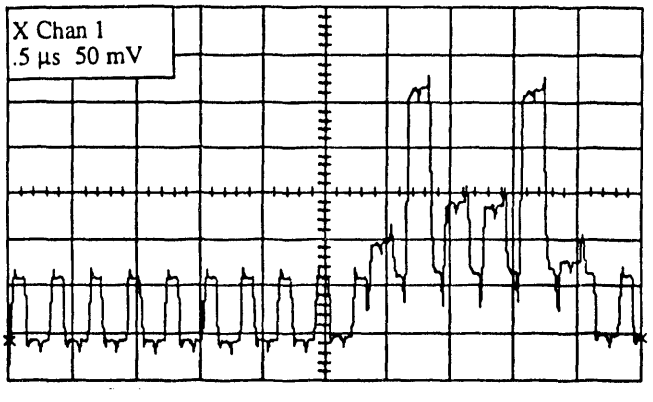
The CTF was measured using the conventional PR-10 resolution chart while operating the CCD-13 at 100 ns clock period. The 2.7:1 demagnification produces spatial frequencies of 6.2, 12.4, 18.5, and 24.6 lp/mm at the CCD-13 from the first, second, third, and fourth bar sets. The resolution limit of the CCD-13 using Nyquist criteria is 23.80 lp/mm. Therefore, only the first three bar sets can be resolved properly. The raw data from a DSO line scan are shown in Fig. 11d. The DSO was clocked externally for this data set. The CTF at 18.5 lp/mm is estimated at ≈33%.



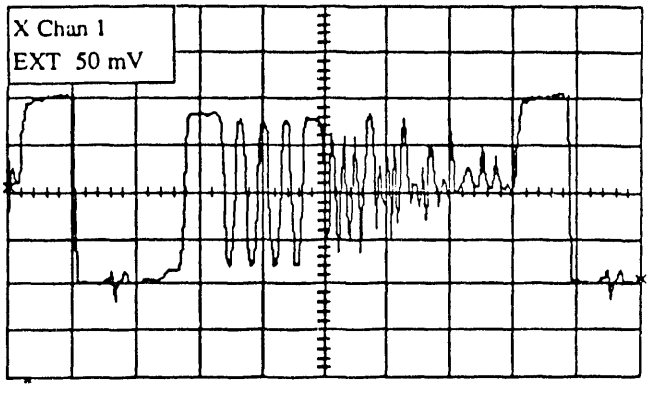
a. 9.3 μm diameter pinholes separated by 15.7 μm.



b. 18.5 μm diameters separated by 33.3 μm.



c. 37 μm diameter pinholes separated by 37 μm.



d. PR-10 bar sets demagnified 2.7X.

Figure 11. Pinhole array images (a, b, and c) and PR-10 resolution bar chart image (d). These data depict horizontal resolution of the CCD-13. For the pinhole data, the DSO was clocked internally (oversampling) to demonstrate the quantity of pixels involved. For the PR-10 data, the DSO was clocked externally to eliminate aliasing.

4.6 Rate effects

Using the dynamic range setup, the clock period was varied to periods of 20 ns, 50 ns, and 200 ns while keeping the input illumination constant. The CCD-13 video was measured for these three rates and compared with the 100 ns response at 50% saturation intensity to show rate effects. The ~5 mm diameter aperture used for these tests represent the low frequency response of the CCD-13. The imager's output is obviously rate sensitive, with lower responsivity at higher pixel clock rates as shown in Table 5. In theory, this effect could be due to either (or both) on-chip preamplifier bandwidth/slew-rate limiting or

Table 5. Responsivity and resolution as functions of pixel clock rate.

Clock Period (ns)	Responsivity (mV)	Valley-to-Peak(%)
20	10	33
50	50	62
100	70	57
200	110	60

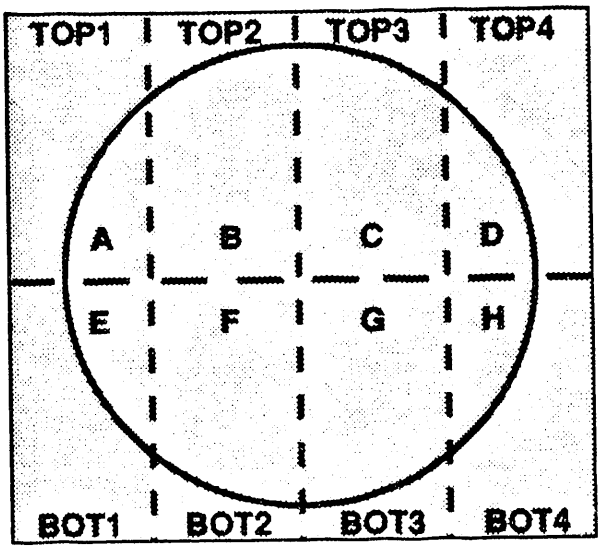
CTE. The effect was studied further in the resolution measurements discussed next, with no bandwidth problems identified. The dominant reason, therefore, appears to be related to CTE.

To distinguish bandwidth and CTE effects, the 18.5 μm array was selected for PSF measurements along both axes at different pixel clock rates. The periods selected were 20 ns, 50 ns, 100 ns, and 200 ns. The valley-to-peak ratios observed were fairly constant at all clock rates except the 50 MHz rate where the drive circuitry overlap criteria are not met. This indicates sufficient bandwidth for all spatial frequencies generated by this set up. (The discrete external phase delays required for proper overlap at the 50 MHz rate were unavailable for use in this test. These measurements will be refined later.) The pinhole valley and peak amplitudes are summarized in Table 5.

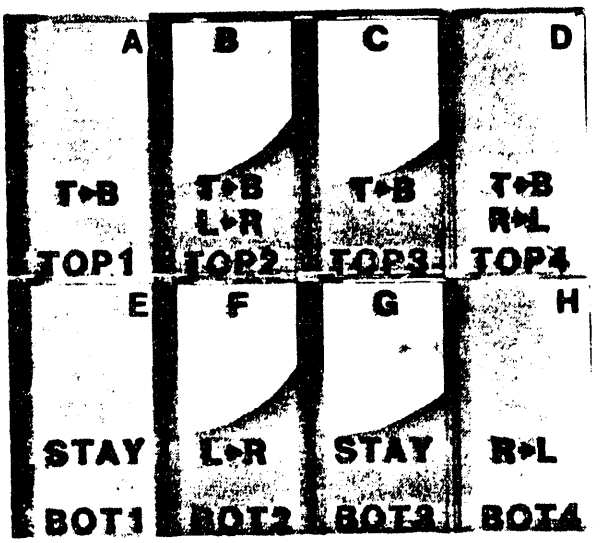
4.7. Data reconstruction

For some images, such as test images constrained to individual segments of the CCD-13, analysis can be performed using the DSO waveform processing package directly without involving a PC or workstation. However, for images involving the entire imager, because of the bidirectional scanning described in Fig. 3, the digitized image is spatially scrambled and must be reconstructed before analysis.

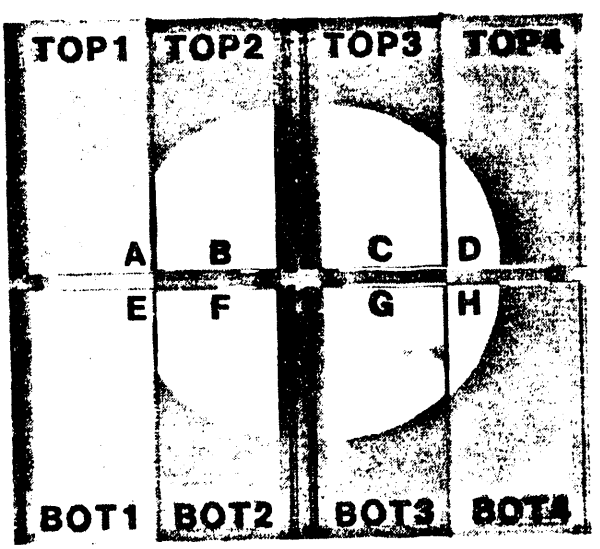
A circular aperture simultaneously illuminating portions of all eight segments as shown in Fig. 12a (top left) was imaged onto the CCD-13. The two DSOs simultaneously digitized the eight partial images in real time using the CCD-13 pixel clock for proper phasing of sampled data. The eight digitized image files were subsequently downloaded over GPIB to the Compaq 386. The IDL software resident on the Compaq 386 was used to display the raw scrambled image as shown in Fig. 12b (top right). The IDL translation and rotation routines were used to reformat and reconstruct the image. The individual segment scan directions and required reformatting functions are indicated in the Fig. 12b. Only segments BOT1 and BOT3 are scanned correctly during readout and are unaltered during reconstruction. They are used as orientation reference segments for the remaining segments. BOT2 and BOT4 required only horizontal translation, BOT2 left-to-right and BOT4 right-to-left. All TOP segments required vertical translation top-to-bottom. TOP1 and TOP3 (readout directionally like BOT1 and BOT3, respectively) required no horizontal translation. TOP2 (again, readout directionally like BOT2) required left-to-right translation. Similarly, TOP4 (reads out like BOT4) required right-to-left translation.



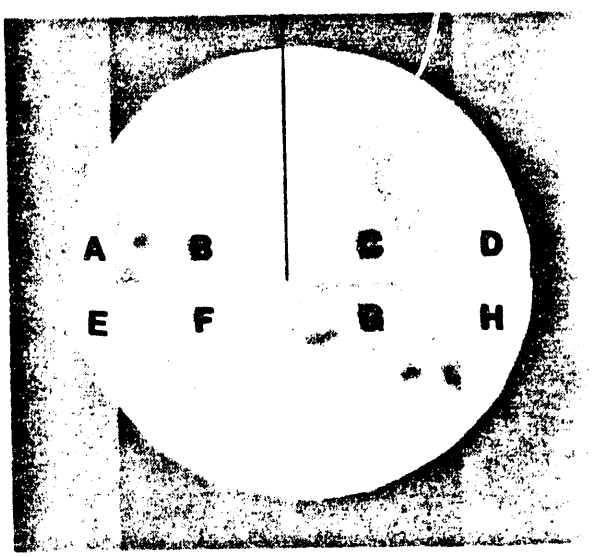
a. Illumination pattern.



b. Raw scrambled image.



c. Reconstructed image.



d. Merged image.

Figure 12. Image reconstruction using IDL. The CCD-13 was illuminated with a variable iris aperture projecting a circle of light covering portions of all eight segments as shown in (a). The scrambled image form bidirectional multiport readout is shown in (b), the reconstructed image in (c) and the merged image is (d). The differences in image size are from illustration reproduction processing, not from the CCD-13 or IDL. This figure is primarily for demonstration of scrambled data from the CCD-13 and reconstruction using IDL.

The reconstructed image is shown in Fig. 12c (bottom left) with the eight segments displaced for clear spatial identification of each.

The final step in reconstruction required merging of all segments as shown in Fig. 12d (bottom right). The slight variations in background among segments are obvious in the image. As indicated earlier, these are due to measured differences in quiescent OS drain/source currents. The dark spots in the otherwise white pattern are blemishes in the test pattern diffuser.

5. ACKNOWLEDGMENTS

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6. REFERENCES

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