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High-Efficiency Silicon Concentrator Cell Commercialization

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Contract 54-2191D

ABSTRACT

This report summarizes the first phase of a forty-one month program to develop a commercial, high-efficiency concentrator solar cell and facility for manufacturing it. The period covered is November 1, 1990 to December 31, 1991. This is a joint program between the Electric Power Research Institute (EPRI) and Sandia National Laboratories. (This report is also published by EPRI as EPRI report number TR-102035.) During the first year of the program, SunPower accomplished the following major objectives: 1) a new solar cell fabrication facility, which we call the Cell Pilot Line (CPL), 2) a baseline concentrator cell process has been developed, and 3) a cell testing facility has been completed. Initial cell efficiencies are about 23% for the baseline process. The long-range goal is to improve this efficiency to 27%.

Acknowledgements

We would like to acknowledge many of the people that did this work or made it possible. The technical team consists of Dr. Pierre Verlinden, Richard Crane, John Perkins, Karen Garrison, Jeff Basset and Charles Nickel.

The contract administration at SunPower is handled by Lori Adkins. Technical writing and layout of this report as well as monthly reports is done by Doug De Vries.

Bob Lorenzini, with Lori and Doug manage SunPower and provide the financial and administrative stability required to perform this cost-shared work.

Finally, we would like to thank Frank Goodman at EPRI and James Gee at Sandia for their technical and administrative oversight and assistance.

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SUMMARY

SunPower Corporation was formed to commercialize the high-efficiency concentrator cell technology developed at Stanford University under funding from the Electric Power Research Institute (EPRI) and the U. S. Department of Energy through Sandia National Laboratories. Sunpower's initial income is mainly from two research contracts, one with EPRI and the other with Sandia. These programs are coordinated into a complementary, forty-one month effort with joint project reviews, monthly reports, etc. The EPRI support is part of EPRI's High Concentration Photovoltaic Program and the Sandia portion is part of Sandia's Concentrator Initiative. This document is a report on the first year of activities.

The overall goal of the program is to transform previous laboratory-type cell designs into a highly-manufacturable, high-efficiency cell and to develop a process and production facility capable of cost-effectively supplying moderate quantities of these cells to companies which are developing concentrator systems. During the first year of the program, SunPower accomplished the following major objectives:

- A new solar cell fabrication facility, which we call the Cell Pilot Line (CPL), has been brought on line,
- A baseline concentrator cell process has been developed, and
- A cell testing facility has been completed.

As part of the coordinated program, individual tasks are assigned either to EPRI or Sandia. The status of each tasks is as follows.

Sandia Tasks

The Sandia portion of the program is divided into 12 month phases. These are the tasks for the first phase.

Task 1: Procure and Fabricate Necessary Cell Processing Equipment

This task pertains to the construction and qualification of SunPower's cell processing facility, the Cell Pilot Line (CPL). A major diversion from the process developed at Stanford University is the elimination of pyrophoric gasses. This decision followed cost studies which showed that that such a process will be much less costly, largely due to the vastly reduced requirements for safety equipment and code-mandated building improvements. This task is complete.

Task 2: Establish Baseline Cell Process

SunPower developed a new process based on liquid-source diffusions to replace gaseous diffusions and spun-on polyimide to replaced deposited silicon dioxide. This process was initially developed and proved out at Stanford University and then transferred to the CPL. This task is 50 percent complete. Current cells have a maximum efficiency of 23%.

Task 3: Improved manufacturability

This is an ongoing task aimed at improving the manufacturability of the cell.

Task 4: Deliver Cells

Starting in the fourth quarter of the program, SunPower must deliver 20 cells per month. These go to Sandia for testing, however, 10 belong to EPRI and 10 to Sandia. (Near the end of the program, SunPower will make a production run of 1000 cells to demonstrate yield and manufacturability)

Task 5: Long-Term Reliability

This task concerns qualification testing of SunPower's cells to determine long-term reliability. During Phase 1, efforts centered on solder fatigue tests which were performed at Sandia on SunPower cells.

Task 6: Develop Manufacturing Cost Model

No work in Phase 1.

Task 7: Reporting and Documentation

All reporting and documentation is done under this task. This includes monthly reports, annual reports (of which this is the first), and biannual project reviews.

EPRI Tasks

Task 1: Cell Modeling and Design

All cell design and mask procurement are performed under this task. The baseline process has been designed and implemented. No further activity on this task is expected until SunPower develops a second generation cell.

Task 2: Implement Process Characterization Capability

SunPower has implemented all process characterization capability needed for the high-yield, reliable production of cells. These include carrier lifetime, emitter saturation current and diffusion sheet resistance. Further activity will involve the implementation of a statistical process control system as the production volume warrants it.

Task 3: Fabricate and Deliver Baseline Cells

Cells fabricated as deliverables are manufactured under this task, which is ongoing throughout the contract. Initial deliveries began in June, 1991. This was two quarters early, as the contract called for deliveries to begin in the fourth quarter.

Task 4: Development and Implement Cell Testing Capability

SunPower has completed both an on-sun and an indoor flash testing facility for the rapid characterization of cells. This task is complete; however, up-grades and modifications to the facility are planned when production volume justifies it.

Task 5: Research on Methods for Improving Cell Performance

Initial processing work on this project involved transferring the baseline cell process developed at Stanford to SunPower. This process yielded cells in the 23 to 24% efficiency range. SunPower's long-range goal is to produce 27% efficient cells. This task has been at a low level while the facility and baseline process transfer are underway. It is expected that efforts on improving performance will pick up pace during 1992.

Task 6: Research on Passivation Layers with Improved Performance and Stability

As with Task 5, most of the activity on this task will begin in 1992. It was necessary, however, to develop new methods of diffusing the front layer because, as mentioned under Sandia Task 1, SunPower chose not to implement the capability to deposit CVD doped oxides. This development has been completed.

Task 7: Reporting and Documentation

Same as Sandia Task 7.

Task 8: Deliverables

Same as Sandia Task 4.

I. Introduction

This report covers phase one, November 1990 through December 1991, of a program in high-efficiency solar cell research and development at SunPower. This project is simultaneously supported by the Electric Power Research Institute, of Palo Alto, California and the Department of Energy through Sandia National Laboratories in Albuquerque, New Mexico. Through close cooperation, the two institutions have funded complementary areas in the research and development of high-efficiency solar cell design, fabrication, and manufacture.

The central goal of this project is to develop a manufacturing process for high-efficiency cost-effective concentrator solar cells. The strategy taken by SunPower and funded in large part by this program is to develop a process specifically designed for these concentrator solar cells. The original proof-of-concept for the high-efficiency solar cells that this program is based upon was achieved in the integrated circuit laboratory facility at Stanford University. The optimal manufacturing facility and process for fabricating these solar cells is similar to an integrated circuit facility, but in many ways is quite different. In order to achieve cost goals, it is required that full advantage be taken of these differences.

It is important to take full advantage of the manufacturing experience, technology, and support of the integrated circuits industry when it is appropriate. It is also very important to recognize the areas in which the concerns of integrated circuits demand far more sophistication and cost than is required for solar cells.

In the first year of this program, described in this report, three major goals have been achieved.

1) We have brought a new solar cell fabrication facility "on-line."

2) A baseline concentrator solar cell process has been developed.

3) We have designed, fabricated and qualified the equipment for a baseline cell characterization and test procedure.

The cell pilot line has been designed specifically to fabricate concentrator solar cells. This was achieved by purchasing used integrated circuit equipment, and rebuilding it when necessary, to meet the particular needs of an optimized solar cell process.

II. Chronology

In this section, we present a chronology of the work essentially culled from the monthly reports for the program. This chronology will establish a context for the topical discussions in the subsequent sections of the report.

In November and December of 1990, the work focused on design of the next generation of Fresnel cells. Some process optimization was done on new dopant sources, and the integration of optimized cell texture schemes into a concentrator solar cell process was investigated. A search for a new fabrication facility was underway, and equipment purchases of wet benches and photolithography equipment were completed. Prototypes of much of the proposed indoor cell testing equipment were built and tested. The first concentrator solar cells from SunPower were fabricated using the new dopant sources.

January and February of 1991 saw final approval of new electrode patterns for the EPRI Fresnel module solar cells in coordination with Cummings Engineering of Wilmington, Massachusetts. The laboratory work was directed at developing a new interlevel dielectric using an organic polymer, polyimide, as a replacement for the silicon dioxide that we had been using. After optimization of the polyimide layer itself, a subsequent step, the nickel and gold plating, had to be reoptimized to be process compatible with the polyimide layer.

The characterization of the new dopant sources continued. The cell designs were implemented using computer-aided design to lay out the mask sets necessary for the integrated-circuit process. The indoor test setup was semi-automated, to transfer the data directly into a computer. An final report for EPRI was finished summarizing seven years of work at Stanford.

The new mask set for the Fresnel cells became available in March. A lease for the cell pilot line was finalized for an existing clean-room in Sunnyvale. A used four-stack furnace was purchased to be rebuilt. The polyimide/plating compatibility problems were resolved. A chemical spreadsheet for chemical usage at all different wafer throughputs was put together to be used in planning for chemical permitting processes, storage, and cost projections. We finished the first Fresnel cells of the new design, but had not yet received mounts that were required for packaging and testing. These arrived in April. The entire process, including the newly developed polyimide and plating was applied to a run of solar cells. A good soldering yield for these devices was observed and we began x-ray studies of solder-void densities. In May SunPower transferred its administrative and testing operations into a new 11,000 square foot facility in Sunnyvale, located across the street from the cell pilot line.

A new mask set was designed on the computer-aided-design tool in order to fix shortcomings in the original layout. Two runs of solar cells were completed this

month. We began detailed investigations of single-sided etching techniques necessary to independently optimize the diffusions on each side of the wafer. The equipment in place in the new fab included the photoresist tracks, aligner, spin dryers, four-stack, wafer saw, and wet benches. It began to become apparent that the rate-limiting process to bringing the pilot line up would be obtaining the 16 permits required for operation.

By June, we were beginning to get Fresnel cells out from the new process sequences and cell designs. This processing was done at Stanford University. Initially, we had serious problems. The dopant-diffusion sequences that had been optimized individually were interacting in the actual cell process. Symptoms of the problems were high contact resistance and low output voltages. A diagnostics run was done with a simplified subset of the runsheet. This resulted in 200 good cells. Some were sent to Sandia National Laboratories for initial testing. Another 12 were sent to Cummings Engineering.

In the pilot line, the deionized water system became operational, the furnace stack was physically installed, and the quartzware for the tubes was specified and ordered. An outdoor tracker platform was installed at SunPower. This platform tracks continuously and is available for systems prototyping, outdoor cell testing, and long-term qualification and stability testing. An EPRI Mod-1 module was installed, with some cells, in order to begin some exposure tests.

Following good soldering results at Cummings Engineering in July, we sent 70 cells to Cummings Engineering that were subsequently used in prototypes of new module designs. We finished Run 13, which had much better characteristics than any previous run. Cells from this run were characterized in detail at our own facility, then sent to Sandia National Laboratories for further testing. These cells had very good characteristics, with efficiencies under concentration of greater than 20%. Additionally, the internal quantum efficiencies and spectral response looked good. They still had relatively large series resistance and suffered from a lack of an antireflection coating.

In August, we finished considerable work on the indoor testing facility. A lifetime tester was completed, with its associated software to extract lifetimes and emitter saturation current densities from our test wafers. We put it to immediate use to evaluate a matrix of dopant-diffusion experiments. Two collaborations with Sandia National Laboratories were initiated. The first, with Doug Ruby, was on the cell stability. We supplied numerous cells including cells from Stanford and cells from runs at SunPower up to Run 13 for Doug to expose under UV light. The second collaboration was to begin working with Tom Hund on solder bond and packaging issues.

With Runs 16 and 17 in September, we began to truly establish a baseline process. These cells were characterized with our indoor test apparatus. Unfortunately, we began to be plagued with problems in our solder-mounting. These were not fully

diagnosed until November, but essentially there was a defect in the mount materials from Cummings Engineering. The copper surfaces on the mounts were not flat, giving sporadic soldering results, and confusing our evaluations of the cells themselves. Some detailed comparisons of the two cell designs that we were using were made. Early results from Doug Ruby showed that our cells from Run 13 were essentially stable within the experimental uncertainties (they showed a 2% relative drop).

By October, we shifted the effort into bringing up the processing in the cell pilot line. The first process to be fully transferred was the wafer thinning operation. Following this qualification, the wafers for Runs 19 and 20 were thinned at the pilot line. Subsequent processing indicated that they were within specification for thickness, surface quality, and minority-carrier lifetime. Studies of the mounted cells from Run 17 were performed to debug the mounting difficulties observed in previous months. Matrix experiments on solder thickness, and weight during soldering were done. After these results were analyzed, and following discussions with Dick Cummings of Cummings Engineering, we concluded that the primary problem was in the mounts themselves.

To characterize these large numbers of cells, several improvements in the cell testing algorithm were made. We developed a system where the data from four strobe flashes was analyzed in the computer in order to determine the cell series resistance, and the fill factor and open-circuit voltages at two concentrations. A subsequent flash could then be used to find the sublinearity. This system, coupled with an outdoor test of one-sun responsivity, has become our baseline procedure for a complete cell-performance assessment.

Progress in November again focused upon the process development in the cell pilot line. The polyimide process and the Ni-Au plating were transferred. In addition to a simple transfer, the single-wafer process that had been used at Stanford was successfully converted to a batch process at SunPower. All wet-etching and photolithographic processing was fully qualified at the pilot line. As a consequence of this progress, all of the processing for Runs 19, 20 and 21 has been done at the cell pilot line with the exception of the high-temperature oxidation and dopant-diffusion steps. It is also significant that during the transfer to the cell pilot line, specifications for each process step were written and performed by a process engineer and process technician. All of these wafers were within specification.

During November and December, a metal sputtering machine was installed and the deposition characterized. Some of the wafers from Run 19 were deposited using this system. These wafers were subsequently sawed into individual die at SunPower. At this point, approximately 2/3 of all of the processing time expended on the wafers was at the cell pilot line. In the testing area, we purchased an automated IV curve tracer from Endecon of San Ramon, California. This system gathers data under steady state conditions up to 120 A. This will be used to characterize cells and systems in the outdoor test area. At the same time we specified and had fabricated

several precision apertures. Since the die size for our cells is larger than the active area to be illuminated, there are possible sources of ambiguity in the measurements and comparisons of measurements from the different laboratories. These apertures will define a precise area, will be used for all tests, and will reduce the possibilities for uncertainties in the measurements at Sandia and SunPower. Several cells were packaged on mounts with coverglasses and apertures to use in round-robin calibration tests between SunPower, Sandia National Laboratories, NREL, and other interested parties.

III. Cell Design

The first task in this project was to design a new Fresnel cell design. A consensus in the EPRI program was that a larger area cell was desirable. This would have several effects upon the performance. First, the lower concentration would allow the cell to operate closer to the incident concentration where it has maximum efficiency, around 100 to 200 suns. Second, a larger active area would reduce the cell temperature since the same heat (for a fixed lens size) would pass through a larger area at the alumina voltage isolator. The observed temperature drop across this voltage isolator, (about 10 C) could potentially be reduced to 2 - 3 C. This would also require a different electrode pattern in order to allow a more ideal heat spreading at the copper electrode level prior to the alumina. Another consideration was to minimize perimeter loss, which occurs when the sawcut edges are too near the active area. Last, it is important to minimize the die area for any given cell to reduce the cost by allowing the maximum number of cells from each wafer.

In choosing a process design and technology, several other issues came into play. For example, although thin solar cells are more efficient, thick wafers are easier to process and promise higher yield. A summary of modelled effects of various optimizations upon the cell performance is shown in Table 1. Physical dimensions for the particular cells modelled are shown in Figure 1.

EFFICIENCY CHANGES

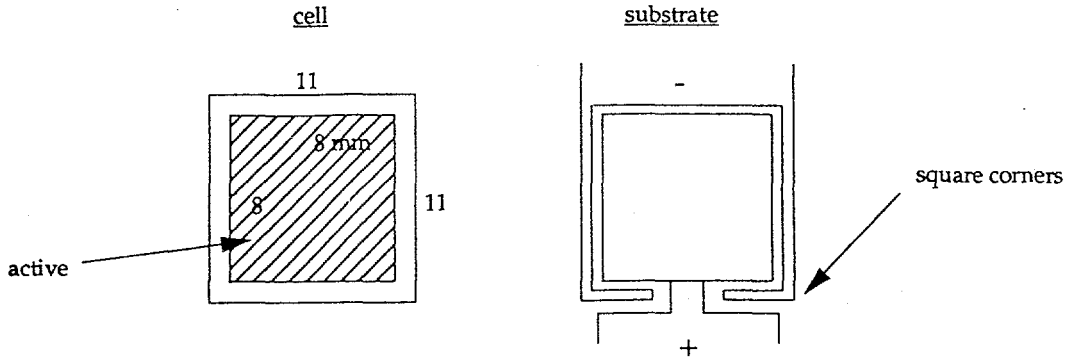
			Better Heat Dissipation	Perimeter	Lower Concentration		AR	Stability		Cost
1	Existing EPRI	1.1 cm	—	—	—	-6.9%	3%	6%	4%	—
2	Proposed	1.1 cm	1.2 to 2.0%	- 1 - 2%	1.6%	-3.6%	3%	6%	4%	—
3	Existing	1.2 cm	1.6 to 2.0%	- 3%	1.2%	-1.6%	3%	5%	5%	+ 20%
4		1.4 cm	1.9 to 2.0%	- 1.4%	1.6%	-1.2%	3%	6%	5%	+ 62%
					90µm	130µm		90µm	130µm	

Base Case: EPRI 1.1 cm 0.64 cm^2 active area

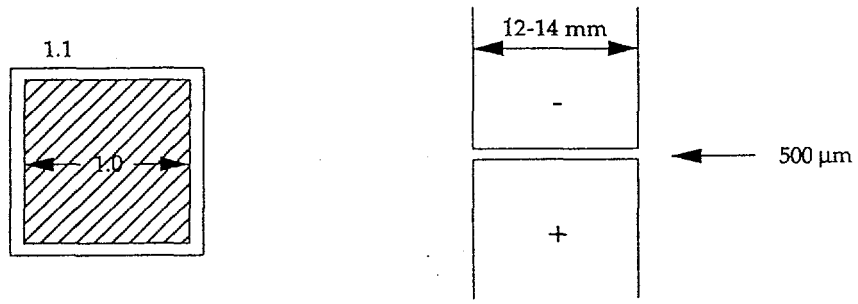
- 90-µm
- 1.4 Ω-cm
- Parameters as on delivered cells
- 23% measured efficiency [25.4 modelled efficiency]

Table 1: Summary of modelled effects of various optimizations upon the cell performance.

1) Existing EPRI 500 X cell (1.1 cm die)



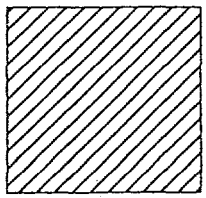
2) A proposed 320 X cell (1.1 cm die)

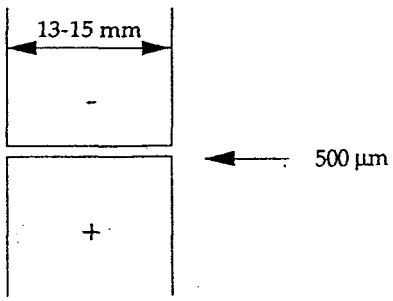


3) A proposed 260 X cell (1.2 cm die)

265 X

1.1 cm active area on 1.2 cm die





4) Same as (3), 1.25 cm active area on 1.4 cm die (205 X)

Figure 1: The cell and substrate design for one existing and two proposed cell designs.

The primary boundary condition on this optimization is that the lens size is seven inches. This fixes the cell current independent of the size of the cell chosen. This choice of size allows the cell to be compatible with both the EPRI modules, the Sandia Baseline III module, and other modules based upon these designs such as that from Solar Kinetics, Inc. of Dallas, Texas.

The first line shows the expected effects of several design and process changes upon the existing cells that had been fabricated at Stanford and demonstrated in outdoor tests in EPRI modules[1] and Sandia National Laboratories Concept 90 modules[2]. The Sandia Concept 90 module in particular had demonstrated a very high efficiency of 20.5% for a cell temperature of 25 C and 18.5% under operating temperatures. This was a 0.64 cm^2 cell on a 1.21 cm^2 die. The efficiency vs. concentration for this cell is shown in Figure 2.

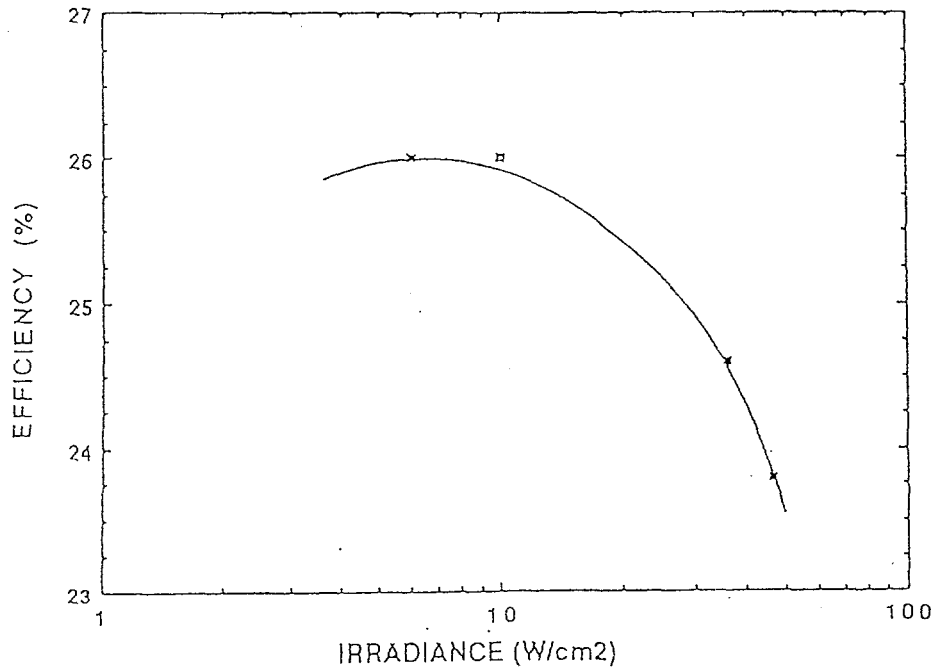


Figure 2: The efficiency vs. incident power density for cells of the type used in the EPRI module and the Sandia Concept-90 module. These were the 0.64 cm^2 cells shown in Fig. 1.

The optimization is for an operating condition of the EPRI module. Some results from such a module are shown in Figure 3. The module was roughly 18.5% efficient, based upon the lens areas and corrected to 25 C. This module was very nearly ideal, in the sense that measurement of the individual cells in the string showed that currents were matched within better than 2% and the power from each of twelve strings of four cells was matched to within 5% (best to worst). This data is courtesy of Cummings Engineering.

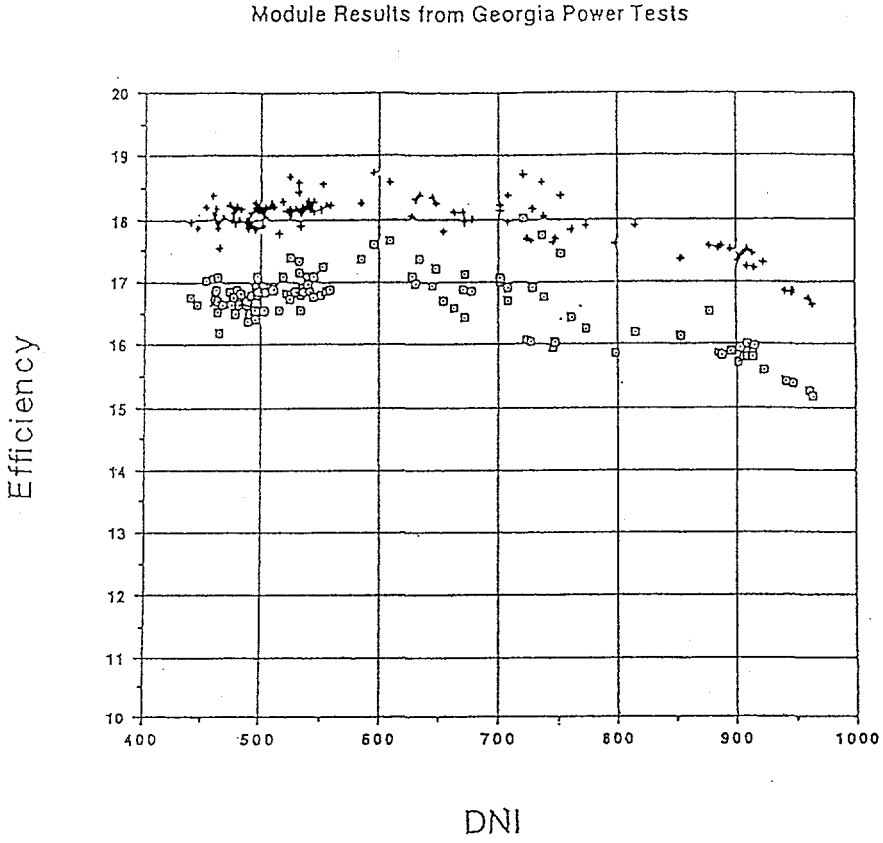


Figure 3: Results for an EPRI Mod-1 module. The upper data-set is corrected to 25 C. The lower data-set is at actual temperature. These efficiencies are based upon the total lens area.

Expected changes from the use of this cell in the EPRI Mod-1 module are shown in the Table 1. The first line shows the deviation from the performance of the existing cell that would be expected from changes in several parameters. If the cell were thicker, 130 micrometers rather than 90, the efficiency would drop by 6.8% (relative). An anti-reflection coating would give an expected improvement of about 3%. Stability improvements, based upon obtaining ideal front diffusions as investigated in[3], could be expected to improve the performance 6% for the thin cell and 4% for a thicker cell.

The second line in Table 1 indicates the results for a design that used the same die size, holding the cost constant, but had a larger active area (1.0 cm^2) within the die. The first effect is that the cell would run cooler, since the heat will pass through a

larger area of alumina voltage isolator. This gives an estimated 1-2% efficiency improvement. Some of this improvement is lost in perimeter recombination, the loss of current due to having the sawcut die edges near the active area. The lower concentration improves the cell efficiency by 1.6% if the cell is thin. The thicker cell, however, would still lose 3.6% in efficiency even at the lower concentration. Note that the efficiency improvements in going to larger cells in order to lower the concentration are not as large as might be expected from looking at the efficiency curve in Figure 2. This is because the measured efficiency in Figure 2 is not at constant current. The lower concentrations had less current, leading to less series resistance losses. This improvement would only be possible if the lens size were reduced in order to reach lower concentrations rather than just making larger cells. Note that the metalization series resistance of a cell, in Ohms, is constant independent of the size of the cell for a fixed metalization design. So for a fixed lens size, the metalization series resistance is fixed independent of the chosen cell size.

The third row in Table 1 shows a third option, a slightly larger die size with a larger active area as well. This is an 11-mm active area on a 12-mm die. The advantage of larger cells is that the area utilization of the die is better, and the concentration is lower. But the cost of the die is roughly proportional to the area so the cost is of course higher.

The last option is a much larger cell. This size was proposed by Dick Cummings in order to operate at the optimum cell concentration as shown in Figure 2, and also give bigger tolerances for cell and module alignments and tracking accuracy. This size of cell would be 62% more expensive than the baseline case based upon the die area alone.

Another important effect was not quantified here. This is the effect of non-uniform light distribution on the die. This impacts the series resistance losses, heating losses, and front-surface recombination losses. These effects generally favor the use of lower concentrations.

Based upon this analysis, we chose the design on the 1.2-cm^2 die. This cell costs only slightly more than the baseline case, but because of the lower operating concentration it is more tolerant of thicker substrates, hence promises benefits in manufacturability that could easily offset the increased cost of the larger die area.

The microscopic cell design of the diffusion geometries similar to that used at Stanford for the previous EPRI and Sandia cells[1,2] was chosen as a starting point for SunPower's cell designs. A cross section of this cell design is shown in Figure 4. A primary goal of SunPower is to achieve a low-cost, highly manufacturable, yet high-efficiency cell design. The design in Figure 4 has major advantages towards these goals. Importantly, it has the potential to be fabricated in an entirely self-aligned manner, reducing or eliminating the expensive photolithographic steps[4]. In the shorter term, when photolithographic masks are used, some of the same features have the effect of improving the yield. This can be described relative to

Figure 4. The metalization that contacts the n^+ diffusion only runs over n^+ diffusion area. Similarly for the p^+ metalization. Hence the danger of shorts between layers is essentially eliminated. Pinhole defects in the layer between the silicon and the metalization have little or no effect upon the cell performance. Also, the definition of the metalization at the step in the silicon improves the yield since this Al is the thinnest here, and is generally cracked across this step anyway.

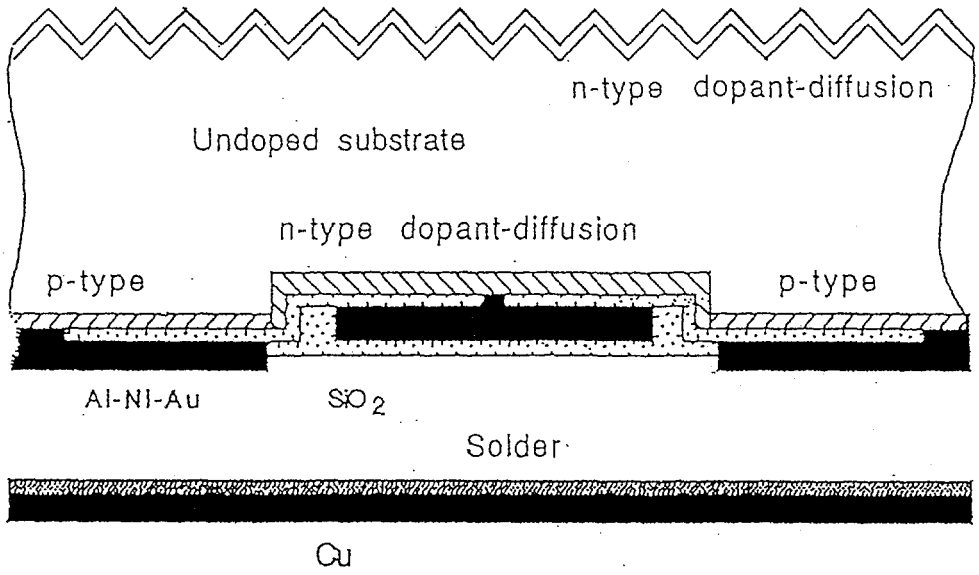


Figure 4: A cross-section indicating the previous 0.64 cm^2 cell design, the first in Figure 1.

An additional advantage of this design is that the cell performance is tolerant of very large features. The metalization lines can be quite wide before efficiency drops due to current crowding effects within the silicon[5] would become evident. This was an important consideration potentially impacting the manufacturing yield, cost, and performance. Large features allow the use of larger tolerances, for example in the photolithographic alignment and the wet-etch processing. This in turn allows the use of less expensive equipment, and promises very robust process sequences. Also, widely spaced diffusions allow wider Al busbars. This decreases the amount of via space between busbars, increasing the cell backside reflectivity and lowering the series resistance of the cell. These coarse patterns were also essential for our planned use of polyimide dielectrics to replace the deposited silicon dioxide layers in the cell as described in the section on process development. We chose a diffusion spacing that gave a modelled efficiency loss due to increased current crowding within the silicon of 0.5% in absolute efficiency, relative to the cells previously fabricated at Stanford. On the first mask sets, we laid out cells with larger diffusion spacings in order that we could confirm our modelled results for this important trend, essentially manufacturing tolerance vs. efficiency.

The proposed electrode pattern is shown in Figure 5. This pattern was designed especially for simplicity of soldering. There are only two pads, with a minimal border susceptible to shorting. With this single separation between pads, the unsoldered area under the cell is minimized, optimizing the heat transfer. Also, compared to the previous design, the heat spreading in the copper electrode is not impeded by the isolation (Figure 1). This should insure that the yield be even better than on the previous design. A plot of the yield for devices from a single wafer using the previous design is shown in Figure 6.

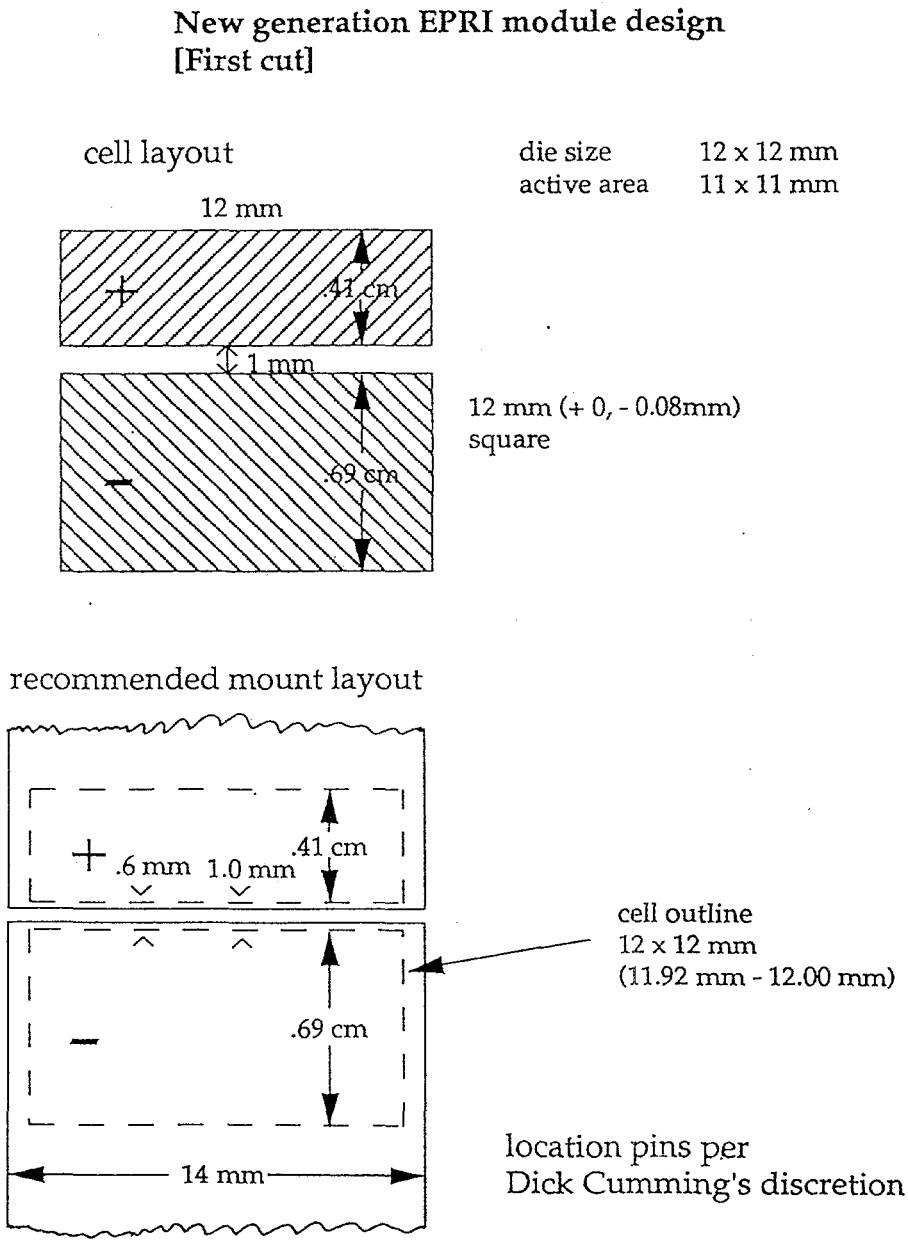


Figure 5: The proposed mount design. The key elements in this design were the desire for simplicity for high yield and good heat spreading.

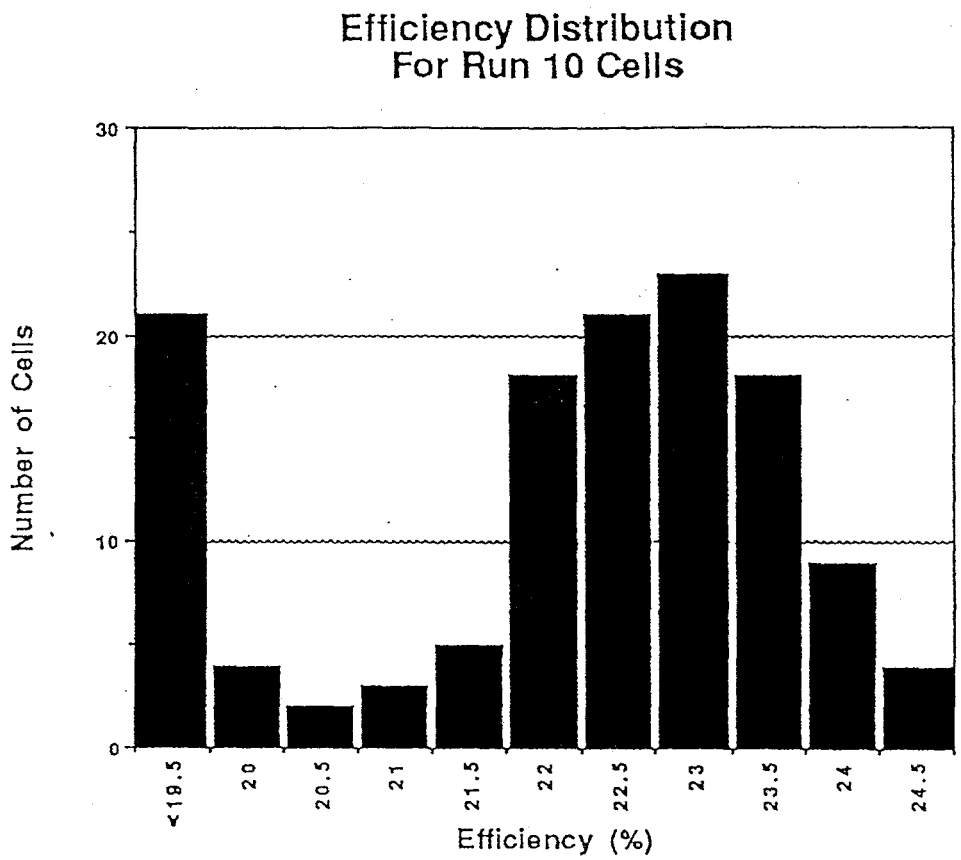


Figure 6: The efficiency of all of the cells soldered from one wafer, using the previous cell design. The lowest bin includes all cells lower than 19.5%.

IV. Process Development

The central goal of this research program is to develop a cost-effective, high-efficiency cell fabrication capability. Meeting the cost and efficiency goals required in the cell manufacture in order to meet the system cost goals requires a comprehensive program of optimization of the fabrication facility, the cell design, and the process design. The high concentration solar cells developed at Stanford University are more similar to integrated circuits than to conventional flat-plate solar cells. So an obvious first cut for an optimized facility would be an integrated circuit facility. Much of the research at Stanford was done in such an integrated circuit laboratory. However, these solar cells are actually quite different than most integrated circuits. They are significantly more demanding of the facility in many ways, especially with respect to materials purity and processing to maintain the high minority-carrier lifetimes in finished devices after high-temperature processing.

Equally as important though, these solar cells are significantly less demanding than current integrated circuits in many other areas. These include particulate contamination and minimum feature size. The technologies are in fact quite different. A demonstration of manufacture of these high-efficiency solar cells in a state-of-the-art VLSI facility is not sufficient. The additional requirement is to meet the cost goals.

Our strategy is to choose an appropriate technology optimized to make high-efficiency solar cells. We identified those areas where we could benefit from the manufacturing experience of the integrated circuit industry, yet specifically avoided machines and processes that were designed to meet difficult specifications that were not necessary for our solar cell fabrication. In this way, we have designed the most cost-effective process that we could.

As described in the previous section, the cell was designed specifically to achieve high manufacturing yields. This high yield is an absolute requirement in attaining low cost. Additionally, we designed a facility incorporating low-cost processing techniques.

One of the major process decisions was to eliminate the use of pyrophoric (self-igniting) gases in the fabrication process. Previously, we used silane, diborane, and phosphine in the wafer doping processes as well as for depositing oxides as dielectric layers needed in backside-contact solar cells. These gases are highly toxic and explosive. Their elimination allows a safer manufacturing facility, without the costs involved in engineering the necessary safeguards for minimizing the risks involved in the use of the pyrophorics.

To accomplish this goal, we have switched to BBr_3 and $POCl_3$ liquid-source dopants. This substitutes for the deposited oxides that we had previously used in the doping process. Additionally, we needed to replace the interlevel dielectric in

the metalization that had also been a doped oxide in the previous process. We did this by developing a process for the use of an organic polymer, polyimide, instead.

In order to achieve an even more general goal, each toxic material that we use in our process has been or is being assessed for possible substitutes in order that the process and facility that we develop is as ready for scaling up as possible.

Dopant-diffusion optimization

The characterization of the dopant diffusion processes has been one of the major efforts in 1991, and will continue to be an important area in 1992. Within the constraints of the cell design described in the last section, there are numerous diffusion parameters that must be optimized. First, each diffusion needs to meet the most basic criteria of maintaining the high lifetime in the substrate, having a low emitter saturation current density, requiring a sufficient surface concentration for contacts, and having the correct junction depth.

The next challenge is to integrate the dopant diffusion into the process. Our cell design requires three independent diffusions. The diffusion on the front side is ideally shallow, with a moderate surface concentration, while the phosphorus and boron diffusions on the backside need to be more heavily doped for contact resistance, and deeper for ideal emitter saturation current densities.

The difficulties come in integrating these diffusions into the process. The junction depths are determined by the total time at temperature that each diffusion sees. The total dose and lifetime parameters for each diffusion depend upon the detailed time, temperature, and ambient during the predeposition steps. Since the masking oxide is thermally grown, a careful optimization of masking thickness vs. dopant junction depth and surface concentration is required. The effectiveness of this mask against the predeposition of dopants depends upon the exact predeposition ambient, temperature, and time.

Additional difficulties arise in the silicon etch steps. The effectiveness of the mask against wet-etching depends upon the thickness and dopant content. Wet-chemical silicon etching depends upon the dopant type and concentration. Hence the texture and trench steps in the process depend critically upon the wafer processing up to the etch step. The last consideration in optimizing a dopant process sequence is to minimize the number of steps, especially photolithographic steps, that are required in order to achieve the desired structure. The way to do this is to use a logical sequence where oxides already existing in the process are used in subsequent masking steps.

Originally at Stanford, the structure shown in Figure 4 was implemented using doped oxides[4]. The advantage of the doped-oxide diffusion sources was that the single-sided processing of the wafer was automatic when the doped oxide source was an APCVD reactor depositing onto a platen. Furthermore, the masking oxide

thickness was independent of the junction depth since this masking oxide could be deposited to any thickness at low temperature. Our desire to eliminate pyrophorics from the process required that we abandon these advantages.

In more recent developments at Stanford, we optimized a hybrid process using boron deposited oxides in conjunction with a $POCl_3$ predeposition to achieve the three diffusions[5]. This process was especially elegant in its use of the characteristics of the dopant sources. The boron diffusion was first, and therefore deepest and single-sided since it came from a deposited oxide. The $POCl_3$ diffusion was shallow, being last, and could have the high surface concentration required for low contact resistance. Since $POCl_3$ deposits on both sides of the wafer, the result is that these two diffusion steps result in all three of the desired diffusions. About 40 large-area ($35cm^2$) one-sun cells were delivered to Sandia National Laboratories that were fabricated on this schedule. They were found to have very high performance and yield.

This process provided the starting point for this work at SunPower. Many extensions were required. First, the boron-doped deposited oxide needed to be replaced by a BBr_3 process, that could in some way accomplish the same single-sided doping with equivalent characteristics. Second, the dopant parameters needed to be reoptimized for concentrator applications. The backside dopant diffusions needed to be significantly heavier in order to meet the series-resistance and emitter saturation current density goals despite more metal-silicon contact area. The sunward-side diffusion has to be significantly more optimized for a concentrator cell than for a one-sun cell. Early work on this contract focused on finding the best compromise single n^+ diffusion that could be used simultaneously on the front and back of the cell. However, it was not found. We decided that this compromise costs too much in performance and therefore the n^+ diffusions on each side needed to be independently optimized.

Specifically, cells that were made with the same n^+ diffusion on both sides had an excessive sublinearity because the emitter saturation current density for the diffusion with the characteristics needed for the backside contact is too high for use as front-surface field under concentration.

We tried several proposed schemes. These each used one of several methods to achieve the three independent diffusions. The various methods tried are listed below --- some worked well and some did not.

1) Stack the wafers back-to-back in the boat during oxidation in order to obtain different masking oxide thickness on the front and back prior to doping.

2) Stack the wafers back-to-back during BBr_3 doping.

3) Dope the wafers back-to-back during $POCl_3$ doping.

4) Grow an oxide, coat one side with photoresist, etch the other side. Then during doping the wafer will be doped on only one side.

5) Do the doping predeposition, etch the doping oxide off of the wafer with a single-sided etching technique, then do an additional drive-in.

6) Do the doping predeposition, grow an oxide, etch the doping oxide off of one side, etch the silicon to remove the doped layer, then do a second predeposition.

7) Dope the wafer, grow an oxide, coat with resist, etch the oxide, do a second predeposition.

In each case, the critical parameters in the procedure were different for boron and phosphorus, and depended upon the previous history of the wafer. Each of these methods was tried and optimized to a certain extent before a preferred technique was chosen. By September, we had fixed this procedure and settled down to small deviations from a preferred runsheet schedule. As a result, the baseline process essentially became established at this time, with Run 17. Runs 18, 19, 20, and 21 (through December 1991) nominally used this baseline process schedule.

We have installed two four-stack furnace units at the cell pilot line. These furnaces will include oxidation, boron and phosphorus doping, and forming gas anneals. We will install the processes to mimic those that we have developed at Stanford University. In our own tubes, we will be able to further optimize the process to accommodate thin wafers. Furthermore, we will be able to more closely optimize the process parameters specifically to address the high-lifetime issues required to obtain the same high-quality emitter saturation current densities as we had previously achieved using the doped oxides. This is a tricky proposition, since the $POCl_3$ and BBr_3 are more commonly done under conditions of solid solubility that lead to supersaturation and defects that can propagate through the wafer.

Wafer thinning

At the beginning of this SunPower project, the wafer thinning was a well characterized process. Beginning in October, we transferred this process to the cell pilot line. All of the wafers (150) for Runs 19, 20, and 21 were thinned in the cell pilot line. Subsequent processing indicates they they are entirely within specification with respect to lifetime, surface quality, and wafer thickness.

Polyimide

In Figure 4, a silicon dioxide layer is used to define the areas to be directly solder-bonded to the header. Our desire to eliminate silane from the laboratory required that we eliminate the use of this oxide.

In previous processes, this oxide had several problems. The oxide was deposited at atmospheric pressure using silane and oxygen in nitrogen. This oxide typically has pinholes, and at the deposition temperature of 400 C the Al forms hillocks creating a topography that can crack the oxide or penetrate it. As a result, this process has yield problems.

The new process must address these problems. It must have high yield, high reliability, use non-pyrophoric sources, and preferably be environmentally safe. A spin-on organic polymer, polyimide, was chosen to meet these criteria. Polyimide is pinhole free. It is widely used in the integrated-circuits industry in applications similar to this one. It is spun on in a way similar to photoresist, and is cured at a relatively low temperature of 350 C. It can provide a thick layer, capable of good step coverage and planarization. Additional advantages are that it requires no special equipment, no pyrophorics, and can be patterned using relatively low-tech wet-etching techniques.

The drawbacks of polyimide are that it is relatively expensive and absorbs chemicals. This second point can (and did) cause problems in subsequent wafer processing. A variety of polyimides are available. The major criteria that we used to choose the appropriate one were cost, viscosity (to determine the layer thickness), thermal expansion matching to silicon, adhesion properties, and the possibility for wet processing. The more conventional (and more expensive) way to pattern polyimide is to use plasma etching.

This polyimide process was fully developed early in 1991, using the Stanford University facilities. The key milestones in this development were the choice and qualification of a polyimide with respect to stress, planarization, and adhesion, a demonstration of sufficient resolution in a wet-etch patterning technique, a high yield in the resulting devices, and finally a demonstration that the polyimide process, including the 350 C cure, caused no efficiency degradation in finished solar cells. This was accomplished by March. In November, the process was transferred to the cell pilot line. This was especially significant since it involved developing a batch process for the first time. At Stanford, we had a single-wafer process through the polyimide coat, expose, develop, and resist strip. After the polyimide cure, this was followed by another single-wafer process, the Ni and Au plating of the wafers. The equipment at the cell pilot line was designed with the proposed batch process in mind. This conversion went far more smoothly than we could have hoped.

These processes are now fully specified and performed by a process engineer or process technician in a batch mode. This full back-end process was first applied to Run 18 in December. This was closely followed by Runs 19 and 20 in January.

Ni and Au plating

The Ni and Au plating was a process that existed at Stanford as a single-wafer process used in the fabrication of the cells that were used in EPRI and Sandia Concept 90 modules.

The introduction of the polyimide dielectric in place of the silicon dioxide dielectric required significant additional development. The major problem is probably the absorption of chemicals into the polyimide. An additional problem is achieving an extremely clean surface after photoresist stripping subsequent to the polyimide patterning. Overly aggressive cleans at this stage prior to the polyimide cure will strip the polyimide. Any organic not cleaned from the wafer at this stage becomes baked on by the 350 C cure.

This problem required significant work in February and March of 1991, but was solved. No problems have been observed in the plating quality in runs processed since that time. As mentioned before, this process was successfully transferred as a batch process to the cell pilot line in December of 1991, and has been applied to wafers from three different runs to date.

Wafer texture

Our high-efficiency cells are designed to have a textured front surface. Early in this SunPower development program, we decided to use inverted pyramids instead of upright pyramids. The cells that we fabricated at Stanford in 1989 for the EPRI and Concept 90 modules had upright pyramids. However, in work on one-sun cells in 1990 we found that the inverted pyramids contribute an additional 0.5 mA/cm^2 of current compared to identically processed wafers with upright pyramids and offered superior process control[5]. This work followed that by other groups that had found similar results[6]. A photograph of the inverted texture pattern is shown in Figure 7.

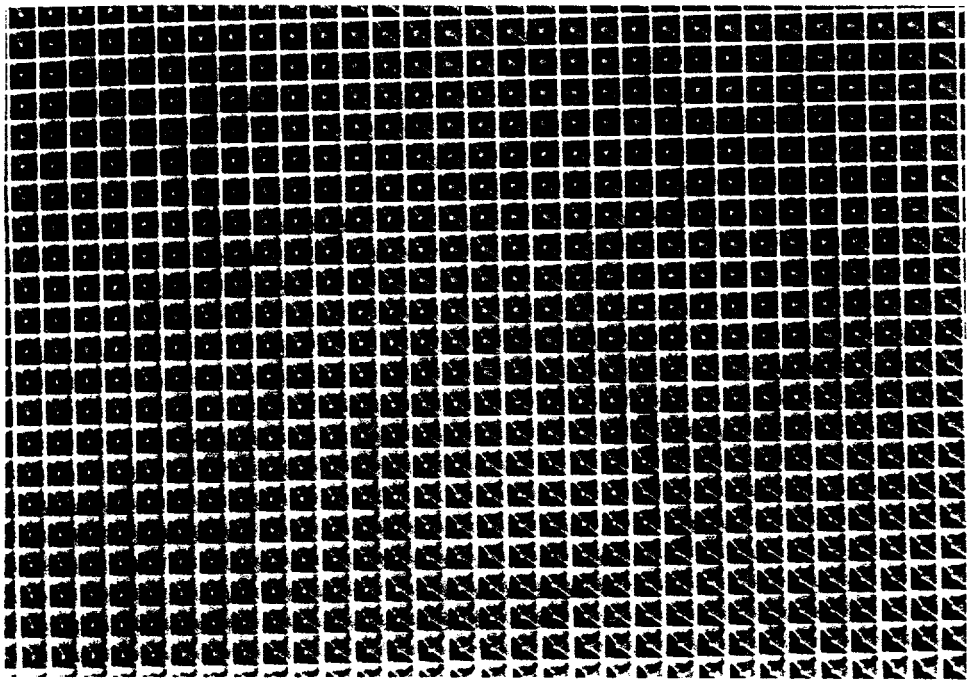


Figure 7: A photograph of the inverted texture pattern designed to maximize the transmission of light into the cell.

The investigations that we have performed during 1991 at SunPower primarily concern the integration of the texture into the process. This is largely a strategic question involving cost, complexity, and yield. The approach with the highest yield is probably to texture the wafers at the very beginning of the process. When this is done, the process through the middle, where the layers are aligned to each other, is the shortest. However, texturing at the beginning requires the growth and masking of an additional oxide to those that are necessary for the doping sequence.

A shorter overall sequence uses one of the oxides grown during an intermediate step as the mask for the texture etch. This strategy has some pitfalls. One is that masking and etching defects are then present in the doped layer, as mentioned above. Second, the etching behavior of the surface after doping is highly dopant dependent and has to be carefully characterized. A third concern is that this silicon

etch step thins the oxide mask which still has to be thick enough to be a barrier in subsequent dopant masking. In this way, the texture has an influence on the already-too-complex dopant sequence optimization.

We have optimized a procedure for this texture step. In December of 1991 this procedure was fully specified and transferred to the cell pilot line. Since then, 150 wafers from Runs 19, 20, and 21 have been processed by the personnel at our cell pilot line. Inspection and subsequent processing indicates that this texture process at the cell pilot line is very much more controlled than what we had developed at Stanford, primarily because the photolithography at the pilot line is superior to what we had previously used, and the process has now been more tightly specified.

Metal Sputtering Deposition

During the course of this work we have used metal sputtering deposition to metalize the cells. This has its own special difficulties with thin wafers. The metalization thickness that we use is sufficient to bow the wafers and make them incompatible with the automatic transports commonly integral in these sputtering machines. We have specified a machine and process at the cell pilot line that takes these problems fully into account. The machine was installed in December, and the first plasma achieved. Some depositions have now been completed using an existing target already in the machine. These wafers, a few from Run 19, have now been finished and have supplied working cells. A new target of the preferred composition has been ordered and will be installed in January, 1992. The sputtering machine that we have purchased has the capacity to do a full solderable metalization in-line without breaking vacuum. This is a future development topic that could provide a very appealing alternative to the Ni-Au plating procedure.

Wet processing

The wet processing stations have been installed and qualified. Beginning with Run 19, all wet processing can be performed at the cell pilot line. This includes the wafer thinning and texture as described above and also photoresist strips, Al etch, and oxide etch steps. The high-lifetime, final cleans remain to be characterized as the diffusion tube processes are brought up.

Photolithography

The photolithographic line was installed during the Fall of 1991. Beginning in December, all of our photolithography has been performed in the cell pilot line. We have fully specified the sequences that we need for the solar cell process, both positive resist processing and polyimide. All of the photolithography for the Runs 19, 20, and 21 has been performed in the pilot line. Optimization work continues on thin wafer transport through the wafer tracks and reducing the mean-time-to-failure for these robotic machines. We have also initiated work on the long term goals of reducing the volume of resist to minimize this very significant cost in the

wafer process. Happily, we have found that the photolithographic line that we have brought up at SunPower is superior to the one at Stanford, primarily due to the better condition of the aligner that we have.

Antireflection coatings

To date, our work on deposited antireflection coatings has been done through vendors. We have qualified a TiO_2 deposition that gave superior current from our wafers in March 1991.

These vendors were unable to supply this service in an ongoing manner. Currently, we are organizing a collaboration with Sandia National Laboratories to evaluate their vacuum evaporated antireflection coating. Additionally, we are installing an APCVD system to mimic the deposition process that we qualified from the vendors. It is anticipated that this machine will be operational as early as March, 1992.

Sawing

We have installed a wafer saw at the cell pilot line in order that we can separate our own die for mounting. This saw was installed during October and November, and fully specified in December. Since December, we have finished all of our devices with this saw, beginning with Run 18.

Soldering

Following the fabrication and sawing of the cells, they have been mounted onto electrode assemblies provided by Cummings Engineering of Wilmington, Massachusetts. The first of these mounts arrived in April, and we had very good success in attaining virtually 100% yield in the soldering operation. In September, we began to have trouble, in the form of increased void density. Eventually, this was traced to a quality control problem in the electrode mounts. A soft copper had been used rather than the usual alloy, and as a result the electrode surfaces where the cell was to be soldered were not flat to various degrees. That our problems were primarily due to this was not debugged until December. As a result, all of our cell results between September to December 31 are significantly confused by the variability in the solder-joint quality.

Several tests were performed in an effort to understand the soldering problems during this period. They involved different weights during soldering, and different solder thicknesses. The results were assessed by two measured parameters. The first was the void density as determined by x-rays, and the second was measurements of the series resistance. No real trends were observed relating the soldering techniques to these results. However, another interesting observation was made. The sublinearity was very well correlated with the series resistance. Devices with high series resistance also had large sublinearities. This means that a cell with a high void density will have a poor sublinearity as well as a high series resistance.

This is demonstrated in Figure 8. This figure suggests that without solder voids, the series resistance could be as low as 5 m-Ohm cm^2 and the sublinearity limited to 95%.

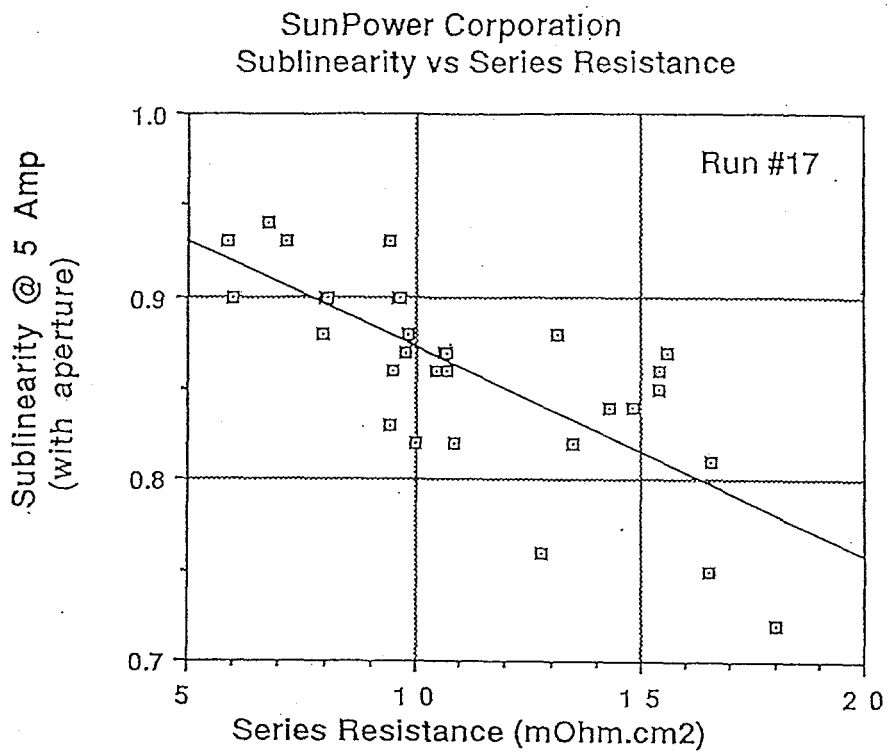


Figure 8: A plot illustrating the correlation between the sublinearity and the series resistance for a group of Run 17 cells. It is hypothesized that the common variable controlling both parameters is the solder-void density.

Several additional studies on the solder bond were done by Tom Hund at Sandia National Laboratories. He used thermal cycling to compare the package reliability of cells mounted at SunPower, Sandia, and Cummings Engineering. All of the cells substantially failed after the 250 cycles. The portion of the cell in which the interdigitated pattern allows less soldered area fails first. This may be a problem with the package and cell design. Further studies will address this problem. Possible solutions include the use of different solder. However, Tom recommends that the ultimate solution is a better thermal expansion match between the cell and the mount. Tom has experience with Cu-clad molybdenum for this application. SunPower has experience with silicon substrates. Both methods are now being pursued at SunPower in cooperation with Tom at Sandia.

In addition to these results, Tom recommended several process improvements including the use of biodegradable (non-CFC) flux removal methods and a different flux.

Summary: Status of Processing at the CPL

Much of this work has been described above and implied from the process run and machine status. Here is a simple summary of the process status:

Photolith	Up
Polyimide	Up
Wafer thinning	Up
Wafer texture	Up
BOE etch	Up
resist-strip	Up
Ni-Au plating	Up
Saw	Up
AR coat	Expected March 1992
Sputtering	Demonstrated, clean and new target in January
Diffusion/oxidation	Ready, except for jungles (planned February 1992)

The processes that are described as up have been fully transferred to the cell pilot line, fully described in a detailed specification document, and performed by a process engineer or process technician successfully on 50 or more wafers.

V. Cell Pilot Line

SunPower has a cell pilot line optimized for the production of high-efficiency concentrator solar cells. This is a 4000-ft^2 facility with 1700-ft^2 of Class 100 clean-room area.

At the initiation of this contract, we were searching for such a facility. The goal of this contracted work, as well as a central and necessary goal of SunPower is to develop a cost-effective source of high-efficiency solar cells. The solar cells that we have demonstrated in the past at Stanford University were fabricated in an integrated circuit facility. These cells are much more similar to an integrated circuit than to a conventional flat-plate one-sun solar cell. However, it is not sufficient for the long-term goal of producing competitive solar power to have a proof-of-concept, high-efficiency cell fabricated in an integrated circuit line. The solar cell has to be fabricated at a much lower cost per unit area than a typical integrated circuit.

There are many important differences between our solar cells and integrated circuits. In many ways, the solar cell is more demanding of the facility than an integrated circuit. Most notably, the solar cell demands extremely pure chemicals, gases, and wafer handling in order to maintain the long minority-carrier lifetime in the finished devices after the high-temperature processing. Just as important are

those aspects of state-of-the-art integrated circuit fabrication that are not required for solar cells. Some of these are extremely fine dimensions, low particle counts and defect densities, precision dopant quantities for threshold control, etc.

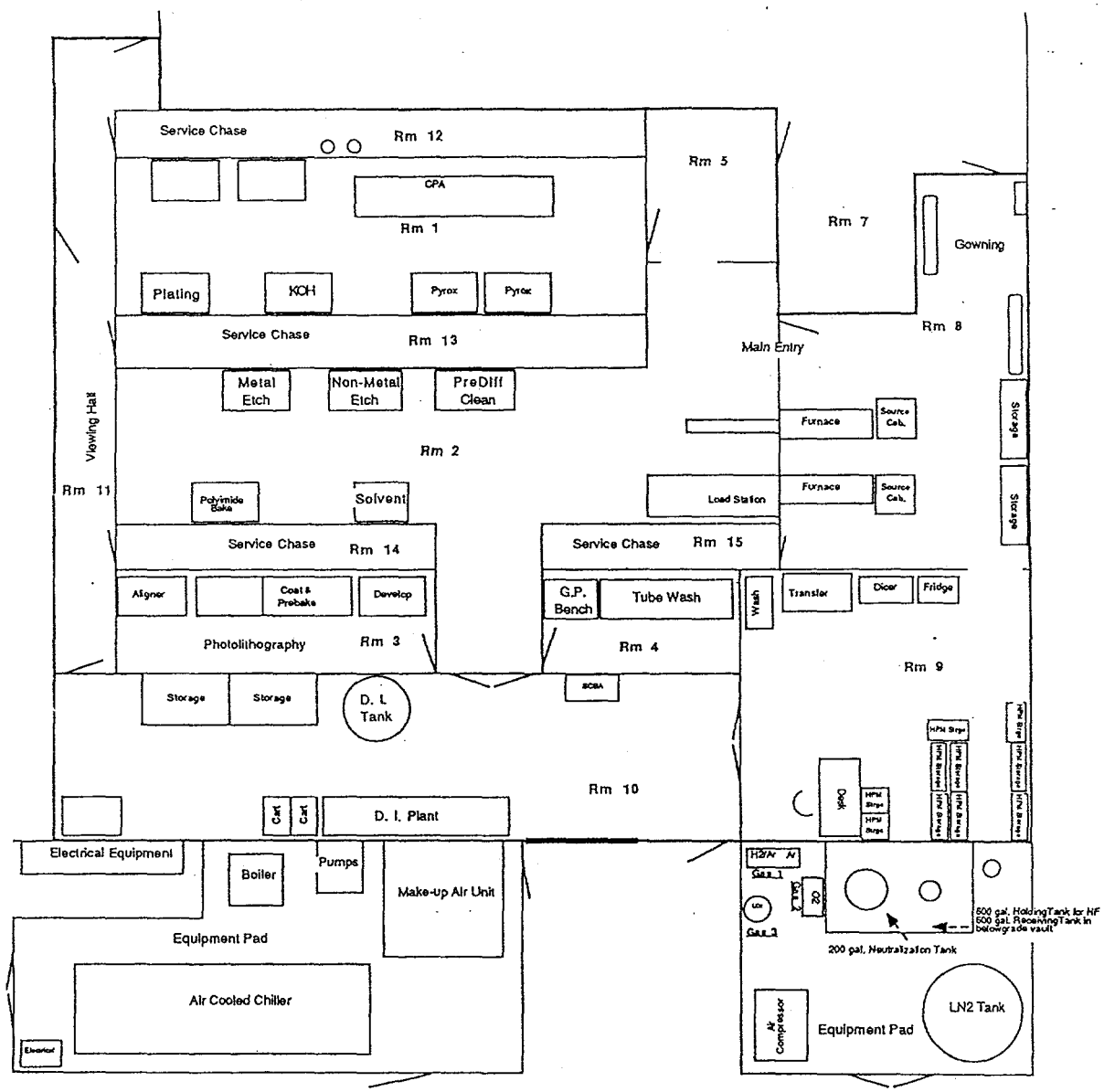
The challenge in developing a cost-effective solar cell fabrication line is to choose appropriate technology. It is important to take full advantage of the manufacturing, materials experience, and the vendor-service availability of the integrated circuit industry. It is also important to use the cheapest machines and processes that will meet the requirements of solar cell manufacture.

We found a small, abandoned fabrication facility, filled it with equipment selected specifically for its suitability for solar cell manufacture, and rebuilt and customized this equipment as necessary. A floor plan layout of this facility is shown in Figure 9.

We are bringing up a baseline process on this equipment and continue to optimize the facility, equipment, cell design and process in order to develop the best possible process.

The result is a facility and a process that is small, simple, but very complete. It has all of the necessary equipment to fabricate solar cells from the silicon all the way to a packaged solar cell. As such, it provides the opportunity to fully optimize a solar cell fabrication line vertically for the lowest possible cost. It is significant that this small lab, essentially with one of each necessary piece of equipment, would be capable when fully utilized of producing the solar cells for several megawatts of power per year.

We leased the space on April 1, 1991. Already, we had been purchasing equipment that we could move in. The facility needed several upgrades. This included the installation of a new exhaust system for the wet benches, modification of the existing air ducting, and rebuilding of the PVDF deionized water distribution system. Further projects included modification of the high-purity gas system to accept new process gases, and the creation of a new gowning area. Walls were moved and doors were installed.



CELL PILOT LINE

SunPower Corp.

November, 1991

clrm7.0/eq1.0

Figure 9: Floor plan for the Cell Pilot Line.

Following the facility improvements, all of the equipment was installed. Physically, this was largely completed by September 1991. Operationally, it continues to evolve, with about 3/4 of the solar cell process fully transferred to this facility at this time.

A significant fraction of the effort to bring up the facility was involved in obtaining the various permits. Figure 10 shows the basic structure of the tasks involved in coordinating various vendors, projects and consultants in order to obtain the occupancy permit that allows the use of this space as a fabrication facility. This was done during the course of the 9 months following obtaining the lease on April 1. The actual work in bringing up the facility was just the tip of the iceberg, with the permitting process contributing an incredible time sink and unpredictability to the planning and time-lines. Useful byproducts of the permitting process were that very detailed documentation of chemical usage, storage, disposal and facilities details were constructed that will benefit us in planning and costing the process, as well as designing for the least toxic chemicals and processes.

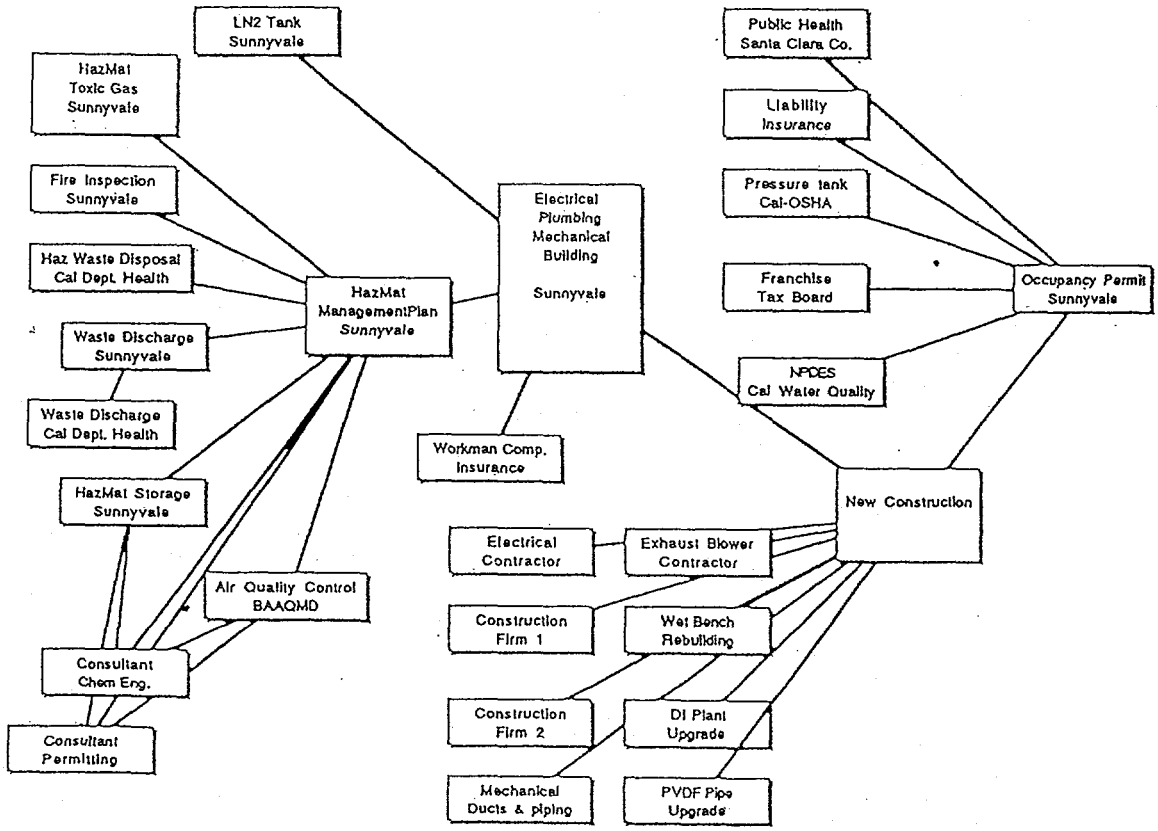


Figure 10: A flow chart indicating the coordination necessary to bring the Cell Pilot Line into operational status.

VI. Testing Capability

At SunPower, we have installed the capability to be self-sufficient in our ability to evaluate our solar cells for performance and degradation. In an indoor test facility, we have developed measurement techniques for obtaining the photoconductivity-decay lifetime and emitter saturation current density, sublinearity of the current density vs. concentration, short-circuit current vs. open-circuit voltage, open-circuit voltage decay, and sheet resistance. With the exception of the sheet resistance, these measurements have been automated using data acquisition directly into a computer for analysis.

We also have an outdoor tracker continuously tracking the sun. This tracker can be used for systems evaluation, and also for on-sun characterization of cells at one-sun and under concentrated sunlight. Measurements under concentration are done using an EPRI Mod-1 module. This module is also being used for long-term qualification of the cells, including the stability under concentrated sunlight. We also use this outdoor tracker to evaluate one-sun responsivities for our cells by comparison with a Sandia National Laboratories calibrated reference cell. We have purchased an automated data acquisition I-V curve tracer and load from Endecon of San Ramon, California in order to perform steady state measurements of our cells, modules, and systems. A photograph of the EPRI module on the tracker is shown in Figure 11. Sample I-V curves for several cells undergoing tests of stability are shown in Figure 12. The I-V curve as taken by the new Endecon load and data acquisition system is shown in Figure 13.

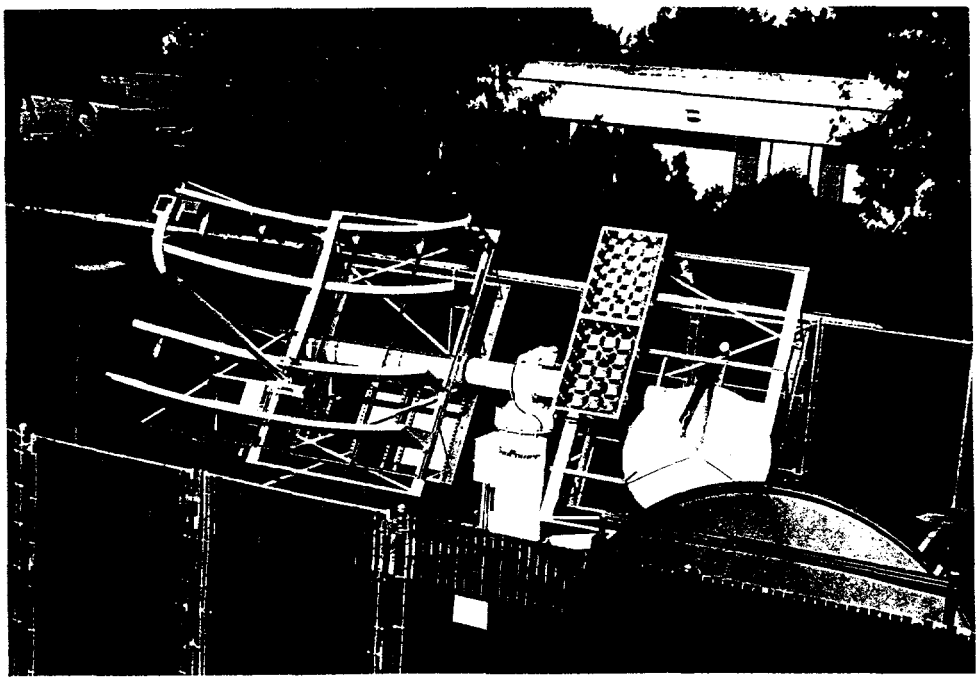


Figure 11: A photograph of the EPRI module on the outdoor tracker.

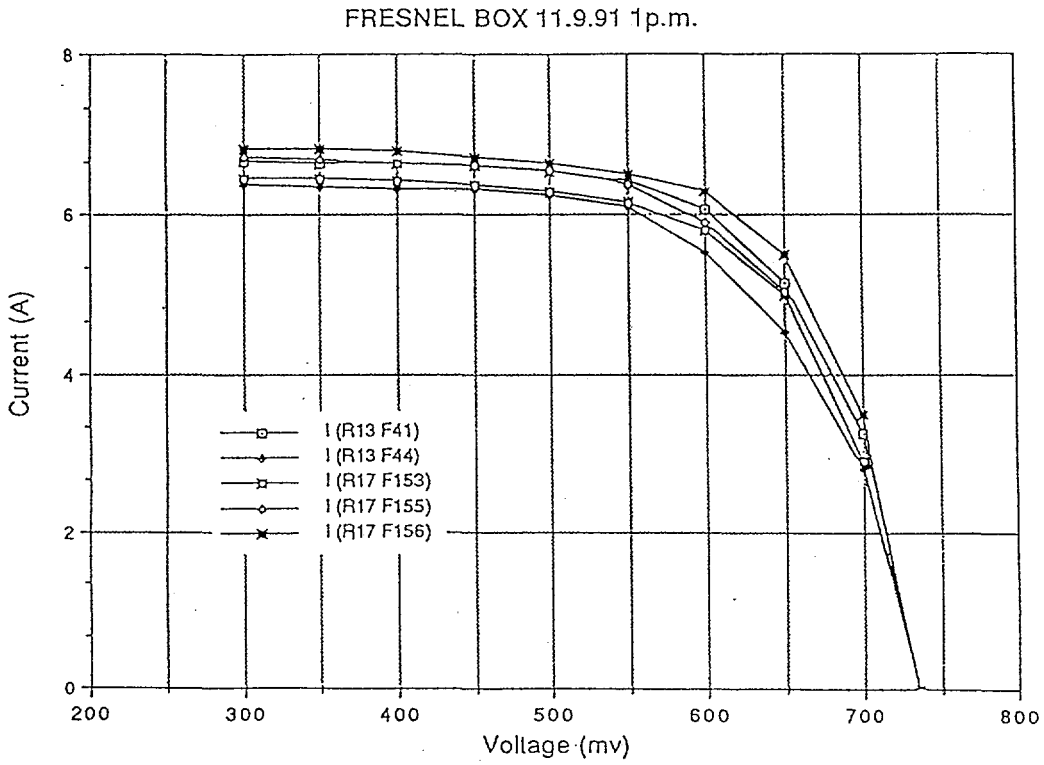


Figure 12: V curves for a group of cells undergoing stability tests in the tracker. The cells are measured individually in the EPRI module.

Endecon I-V curve tracer

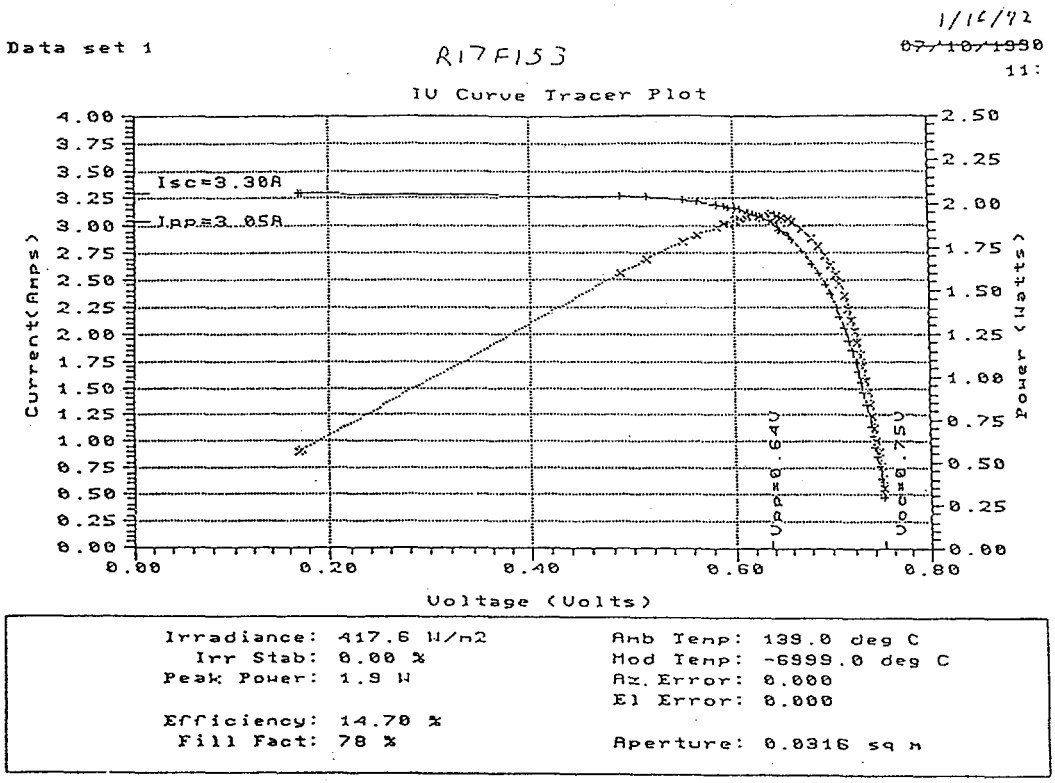


Figure 13: An example of the automatic data acquisition from the Endecon system. This is a cell in the EPRI module on a partially overcast day.

Most of this equipment and these techniques are rather standard and similar to those that we used at Stanford as well as elsewhere. Exceptions are the indoor tests for fill factor and series resistance and the sublinearity measurement. The major difference is that now we require the ability to screen large numbers of devices. Not only do we need detailed information on a few devices in order to evaluate the cell design and process, but we need the ability to do quality control, statistics, and qualification of batches of cells.

Towards this end, we have designed and fabricated an automated data acquisition system that can determine the fill-factor, open-circuit voltage vs. short-circuit current, maximum power voltage, and series resistance of a solar cell without a heat sink at any concentration of light up to 1000-2000 suns. In its current configuration, the cell drops into a mount, four flashes of a strobe are used, then the data is converted by the computer into the fill-factor and voltages at current densities

representative of 100 and 200 suns. The series resistance is also calculated. A block diagram of the actual test apparatus is shown in Figure 14.

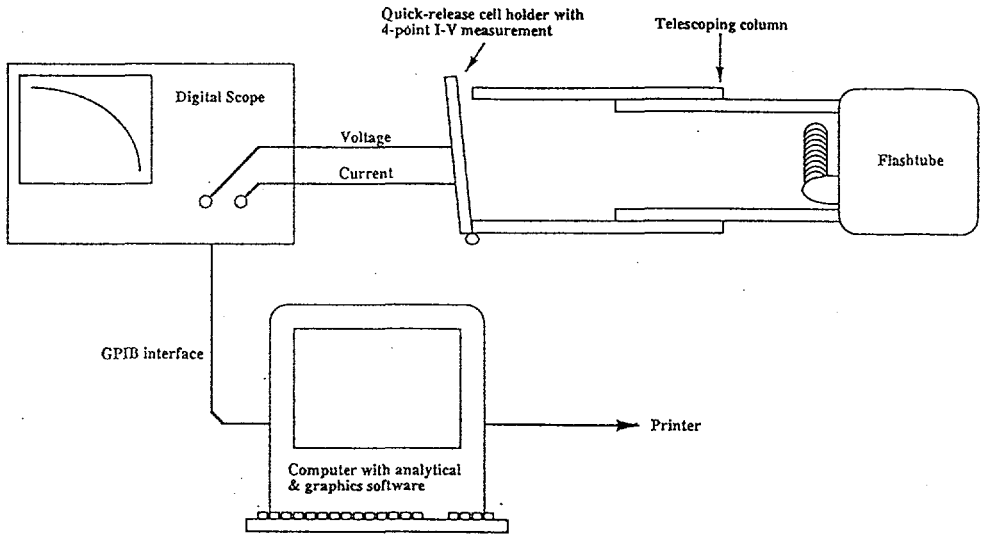


Figure 14: The indoor cell test jig. The cell is inserted into a jig that includes an integral four-point probe. The flashlamp built into the housing then is used as the light source for intensities up to 2000 suns.

An additional flash is then used to determine the sublinearity of current with respect to the incident power density for the solar cell at all concentrations.

An example of these measurements is shown for a cell from the archives, labelled H-157. This cell was fabricated at Stanford three years ago, and had a detailed characterization in our outdoor test facility at Stanford at that time. As such, the abbreviated indoor test sequence can be directly compared to outdoor test data. In this case, the outdoor test facility was a heliostat combined with a long focal length mirror that gave a very uniform beam over the width of the solar cell. The comparison is shown in Figure 15 and Table 2.

First, notice the tight distribution of the indoor test measurements. For example, in five measurements, the difference between the highest and lowest result for the fill factor at 8 amperes is less than 2%. The standard deviation over 5 measurements is 0.7%. Similarly, the scatter in the results for open-circuit and maximum power voltages are comparable or less than those typical from steady-state outdoor test measurements.

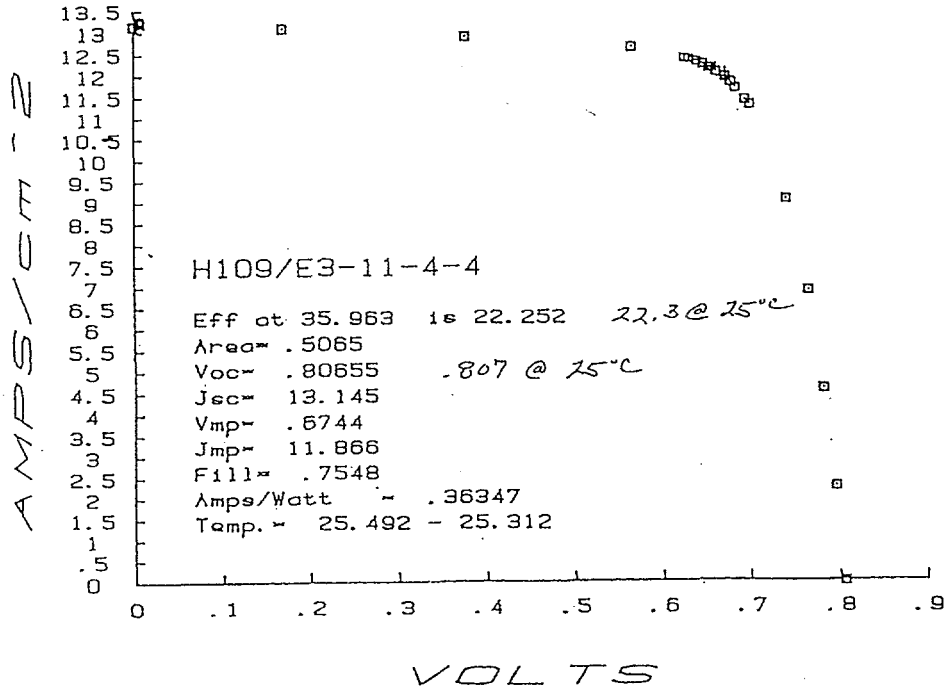


Figure 15: A measurement taken outdoors at Stanford University using a long focal length parabolic mirror to achieve the concentration.

EPRI III cell H-157

	8 Amperes			4.4 Amperes		
R_s(mΩ-cm)^2	FF	V_{oc}	V_{mp}	FF	V_{oc}	V_{mp}
4.6	76.4	811	662	79.1	791	678
4.7	76.4	812	675	79.3	792	675
4.4	75.7	812	666	79.3	792	667
4.0	77.1	811	671	79.6	797	674
3.9	76.3	812	676	78.8	798	664
4.3±0.4	76.4±0.5	811.6±0.5	670±6	79.2±0.3	794±3	672±5

Outdoor Test Results

8.2A				3.5A		
3.7	76.6	811	669	79.3	789	678

Table 2: Indoor and outdoor test results.

Because the indoor and outdoor test results shown here are at slightly different concentrations, the most comparable figure are the fill factors at the high and low concentrations. These are in absolute agreement, well within the uncertainty of either measurement.

A summary of the use of our test facilities shows our basic strategy towards process development and quality control. During the course of the fabrication process, we pull test wafers out at strategic points in order to track the run parameters for immediate decisions concerning the run as well as future correlation with results.

These tests are:

1) Wafer thickness after the wafer thinning.

2) Sheet resistance at boron predeposition.

3) Sheet resistance, lifetime, and emitter saturation current after the boron drive-in and oxidation.

4) Sheet resistance, lifetime, and emitter saturation current densities after the phosphorus diffusions.

5) All sheet resistances of a finished wafer without metal, as well as the lifetime and effective emitter saturation current densities.

Various other parameters are noted on each run or tracked as necessary. These include oxide thicknesses, trench depths, texture quality, metal thicknesses, and plating quality. Some examples of parameters tracked on Runs 17 - 21 are shown in Figures 16 and 17. These are the sheet resistances and emitter saturation current densities for wafers with the boron diffusion on both sides following the subsequent oxidation step.

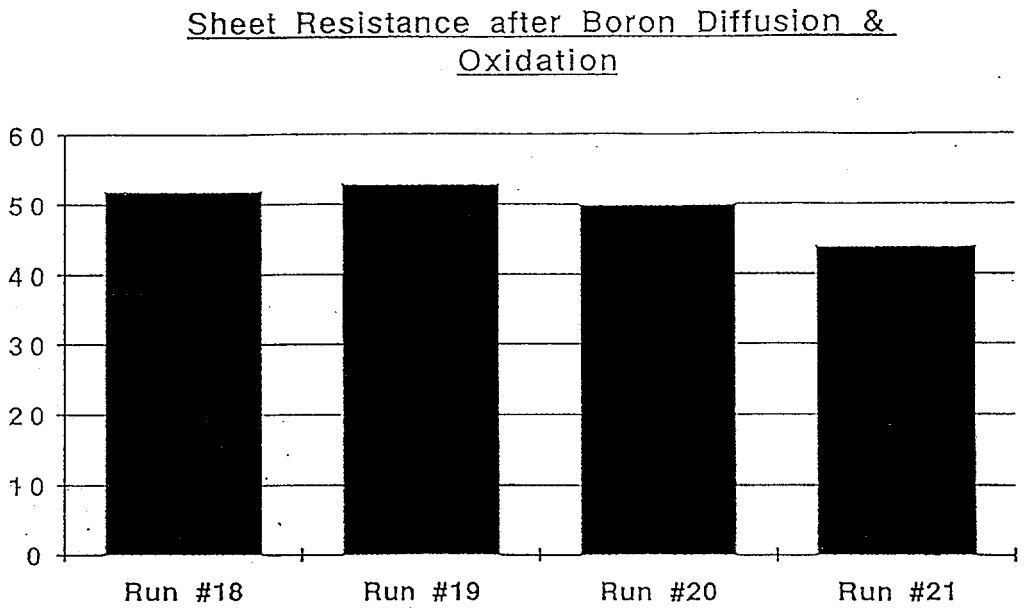


Figure 16: The sheet resistance of the boron diffusion after the boron predeposition and a subsequent oxidation. This figure compares the last four runs.

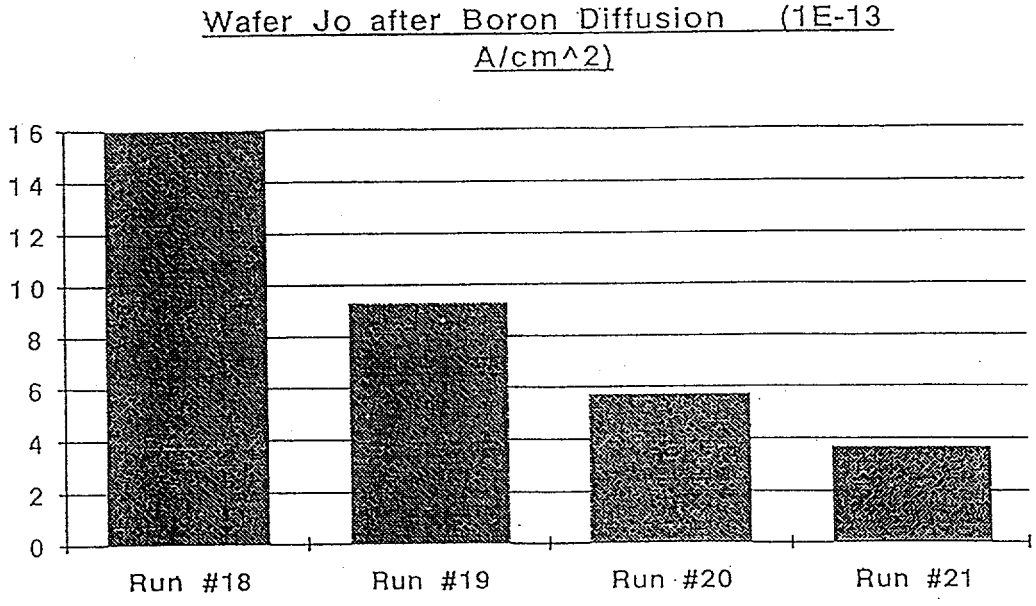


Figure 17: The emitter saturation current density for the last four runs at the same process step as in Figure 16.

Finished wafers are then soldered to the electrode mounts. Then the following tests are done:

Indoor

1) Series resistance, fill factor, and voltages at incident intensities corresponding to 100 and 200 suns.

2) Sublinearity vs. concentration.

Outdoor

1) One-sun responsivity relative to a Sandia calibrated standard cell.

These three measurements allow the calculation of the efficiency at 100 and 200 suns.

Following this, all cells are x-rayed, and for select cells, I-V curves are constructed and open-circuit voltage decays measured. Some cells are mounted into the EPRI module for on-sun steady-state measurements and qualification studies. These on-sun studies include stability.

These tests are complemented by the measurements available from Sandia National Laboratories. Typically, these include full one-sun measurements, and IV curves at current densities representing 100 suns. Select cells then are measured for full efficiency vs. concentration including sublinearity, spectral response, internal quantum efficiency, reflection vs. wavelength, soldering studies, and UV degradation studies.

VII. Solar Cell Results

During the course of this first year, 20 cell runs were processed. The purpose of the early runs was primarily to investigate the issues of optimization of the dopant diffusions, texture, and the integration of the discrete steps into a rational process. Most of these topics have been described in the sections on process development. In this section, we will present a summary of the key results in order to indicate the current performance of our baseline process, the key issues in the cell testing itself, and the trends and expectations for efficiency in the near future.

Runs 1 - 17 were processed at Stanford University under a research subcontract to use that facility. Run 18 was processed primarily at Stanford through the metal deposition, then the back-end, polyimide, plating, and sawing was done at the cell

pilot line during December of 1991. Runs 19-20 were done primarily at the cell pilot line with the exception of the high-temperature oxidations and dopant diffusions.

The first run incorporating a fully integrated process using liquid-source dopants and thin textured wafers was the Run 13, completed in July of 1991. Some results for this cell compared to previous runs are shown in Figures 18 and 19. Figure 18 shows a comparison of the I-V curves for the best cells from Runs 6, 12, and 13. The major improvements between these runs were in the open-circuit voltage and the series resistance. Both of these parameters are essentially improved because of improvements in the dopant-diffusion process.

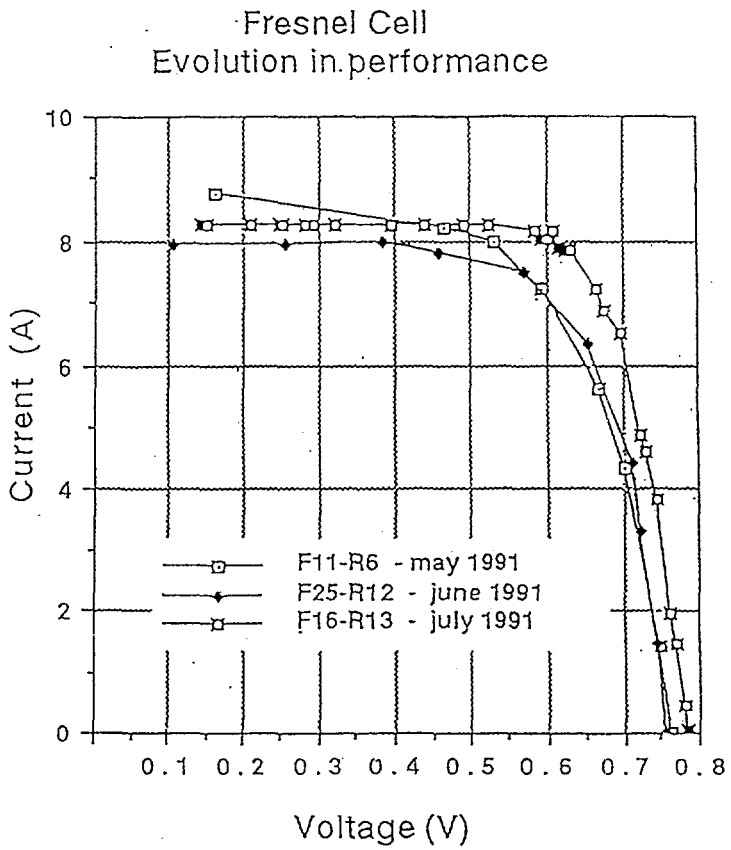


Figure 18: I-V curves indicating the improvements as the baseline process came under control.

Figure 19 shows the sublinearity characteristics for these same cells. Again, the improvement indicates improved dopant diffusions. In addition, this improvement was enhanced by the use of thin wafers in Run 13. The efficiency, as measured at Sandia National Laboratories is shown in Figure 20. The cell peaks at over 20% for a region between 2 and 60 suns, dropping to 18% by 200 suns. An I-V curve for one cell taken at SunPower is shown in Figure 21.

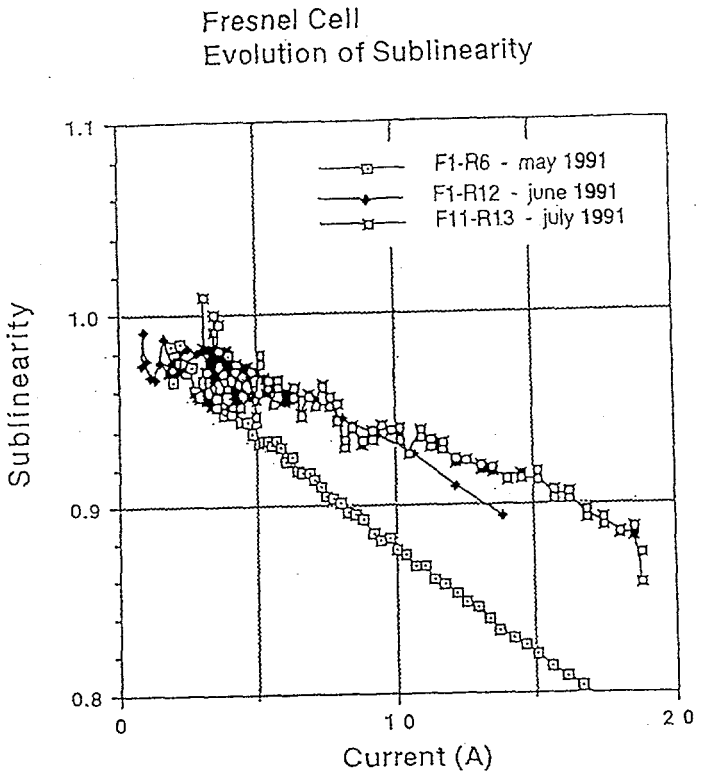


Figure 19: Improvement in the sublinearity of the devices as the process improved.

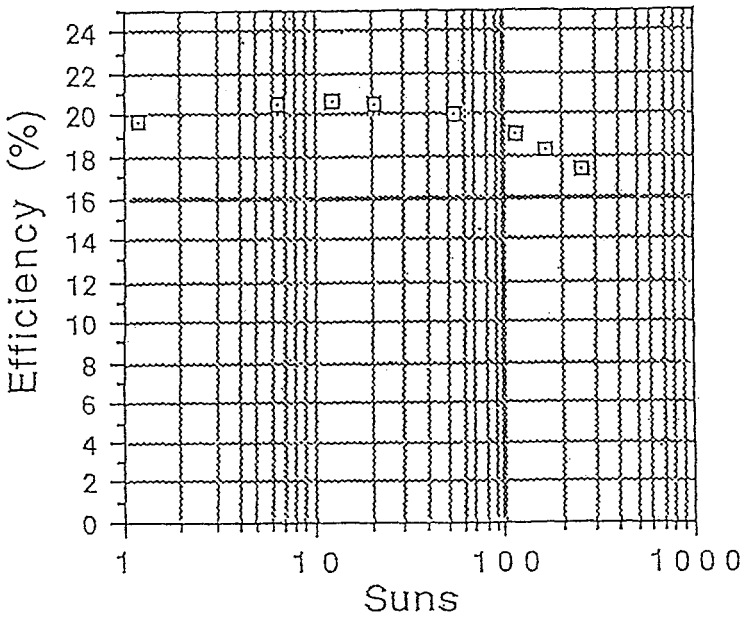


Figure 20: The efficiency vs. concentration for a Run 13 cell as measured at Sandia National Laboratories.

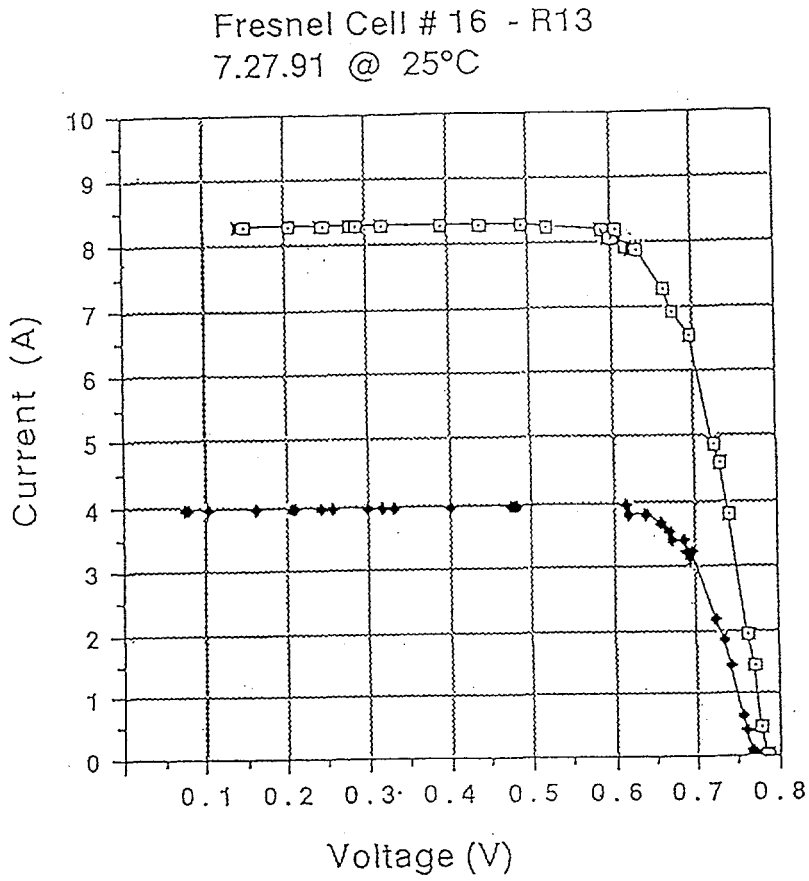


Figure 21: SunPower generated I-V curves for a Run 13 cell.

Other Sandia measurements frame the significance of the result. Figure 22 shows that the internal quantum efficiency of the cell was essentially unity. This indicates that the basic cell design and final lifetimes and surface parameters were very good. Figure 23 shows that the cell had a front side reflectance of about 8%. This is what we might expect to immediately improve upon the application of a double-layer antireflection coating, yielding an improvement in the efficiency to 22%.

Subsequent to this result, we continued to work on alternative process schedules for the n^+ dopant diffusions. The method of attaining the different n^+ surface concentrations on the front and the back of the cell was not satisfactory with respect to process control and flexibility. The problems with this process caused difficulties in the subsequent runs.

Beginning with Run 17, we had our current baseline process. This run has been characterized at Sandia National Laboratories. The efficiency was 22% at 100 suns dropping to 21.4% at 200 suns. The current density at one-sun for this cell was 38.64 mA/cm^2 with an open-circuit voltage of 773 mV at 100 suns and 789 mV at 200

suns. The sublinearity measured at SunPower was 95% at 100 suns and 90% at 200 suns.

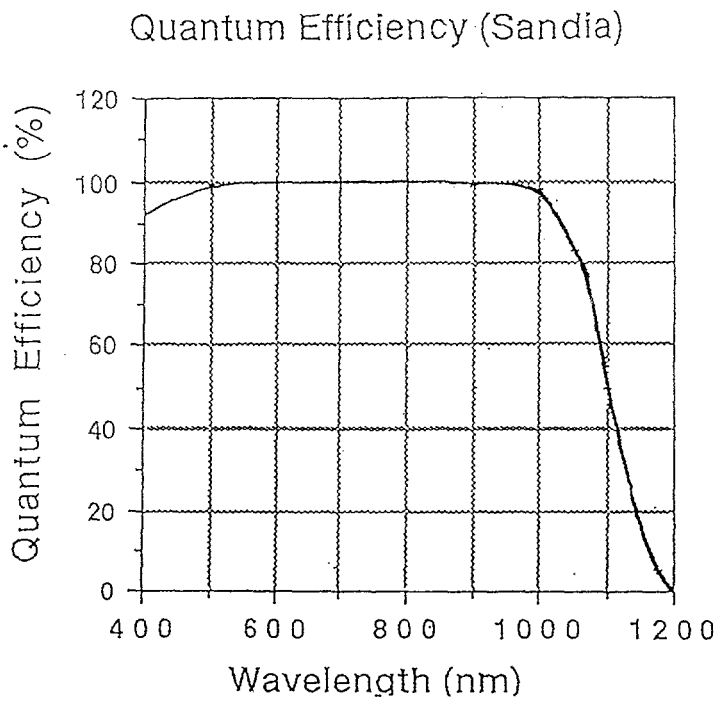


Figure 22: The internal quantum efficiency for the Run 13 cell.

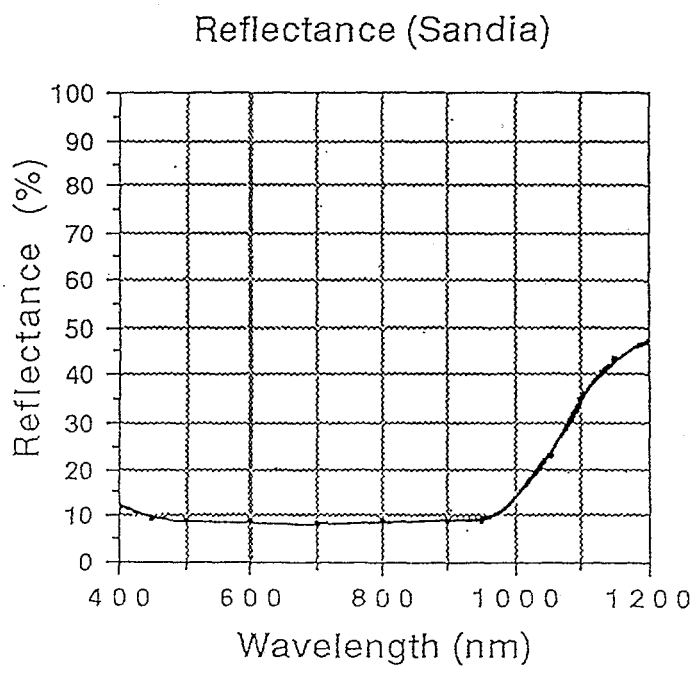


Figure 23: The front-surface reflectance from a Run 13 cell.

This Run 17 was also coincident with the establishment of our baseline testing regimen as described in the last section. Forty cells were measured at SunPower, then sent to Sandia. The agreement between the measurements at the two laboratories was quite good. Ratios of the key parameters illustrate this fact. The SunPower measurements divided by the Sandia measurements for each parameter show:

1)	V_{oc}	0.9992	
2)	FF	1.0076	
3)	J_{sc}1-sun	1.033	
4)	Sublinearity	1.01	(100 suns)
5)	Sublinearity	0.993	(200 suns)

These comparisons are shown graphically in Figures 24, 25, and 26.

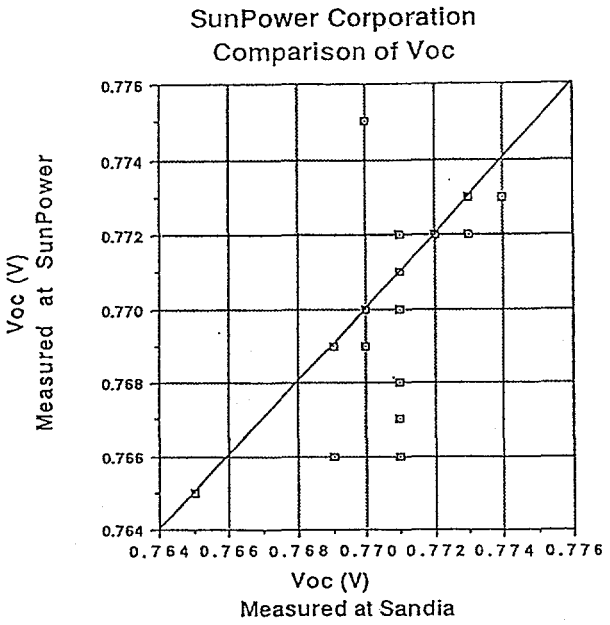


Figure 24: The correlation between SunPower and Sandia open circuit voltages. Note the scale. The scatter is less than 4 mV.

For sublinearity, we have compared the average of the full set of 20 cells measured at SunPower to the 4 measured at Sandia. The only parameter that is in significant disagreement is the one-sun responsivity. To address this problem, we have recently had fabricated precision apertures to define the active areas on our cells. These are used at SunPower and have been provided for use at Sandia. We have also prepared 8 cells from Run 17 with fixed apertures and coverglasses. These will be used as reference cells at SunPower and exchanged in a round robin between SunPower, Sandia, and NREL in order to have cross calibration on cells with the same spectral response as our cells under test.

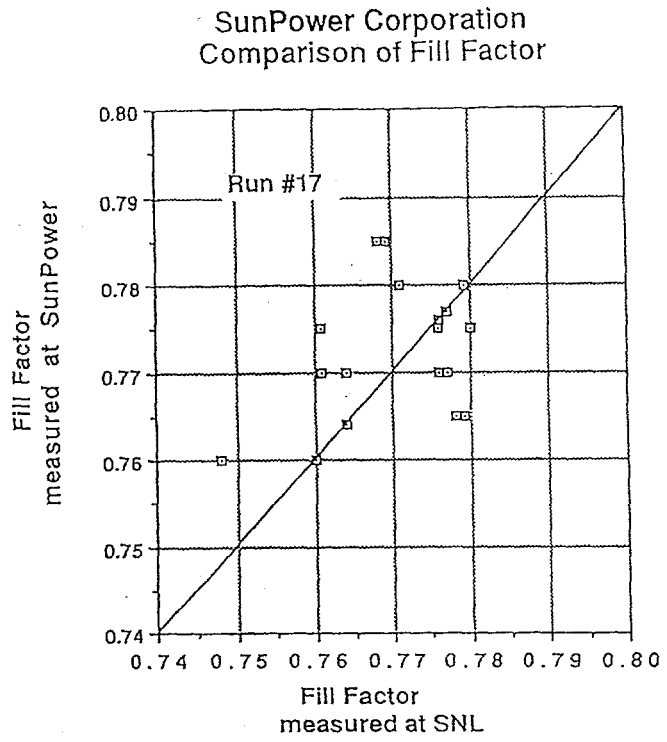


Figure 25: The correlation between fill factors measured at Sandia and SunPower.

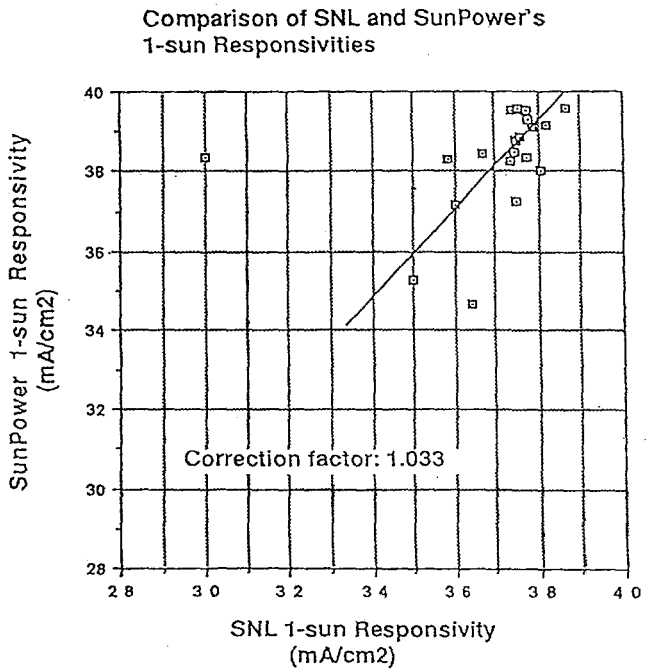


Figure 26: A comparison of responsivities at SunPower and Sandia. The line has a slope of 1.033.

A plot of the efficiency provided by Sandia National Laboratories, for 20 Run 17 cells, is shown in Figure 27. The efficiency at one sun was about 18% for these cells. At 100 suns, it was about 22%. However, these results were not corrected for the sublinearity or spectral response.

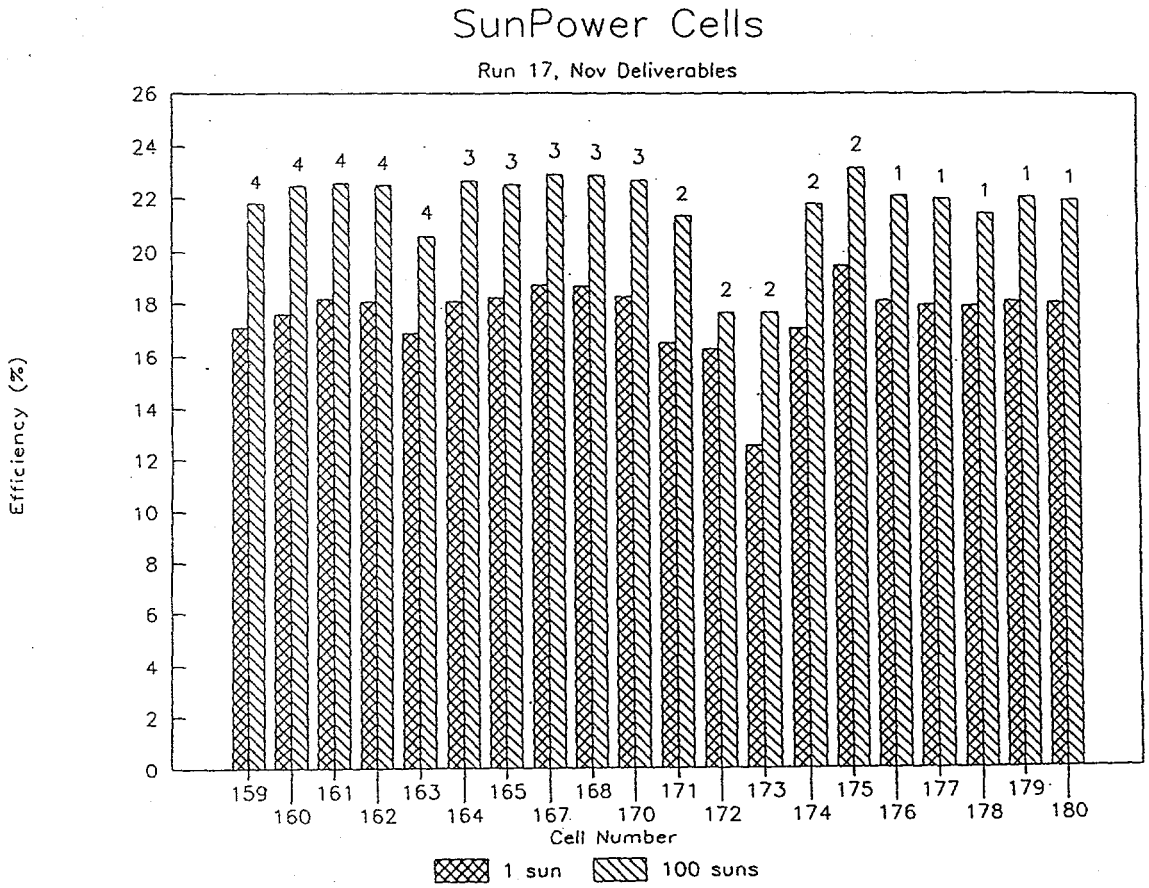


Figure 27: A bar chart from Sandia National Laboratories indicating the efficiencies of Run 17 cells at 1 and 100 suns. These efficiencies have not been corrected for sublinearity.

The latest run measured at SunPower was Run 18. The best cell had an efficiency of 22% at 100 suns and 21% at 200 suns. An I-V curve for this cell is shown in Figure 28.

Overall trends in cell performance as the year progressed are shown in Figures 29 and 30. As the year has progressed, improvements in the one-sun currents and the absolute efficiencies of the cells have continued.

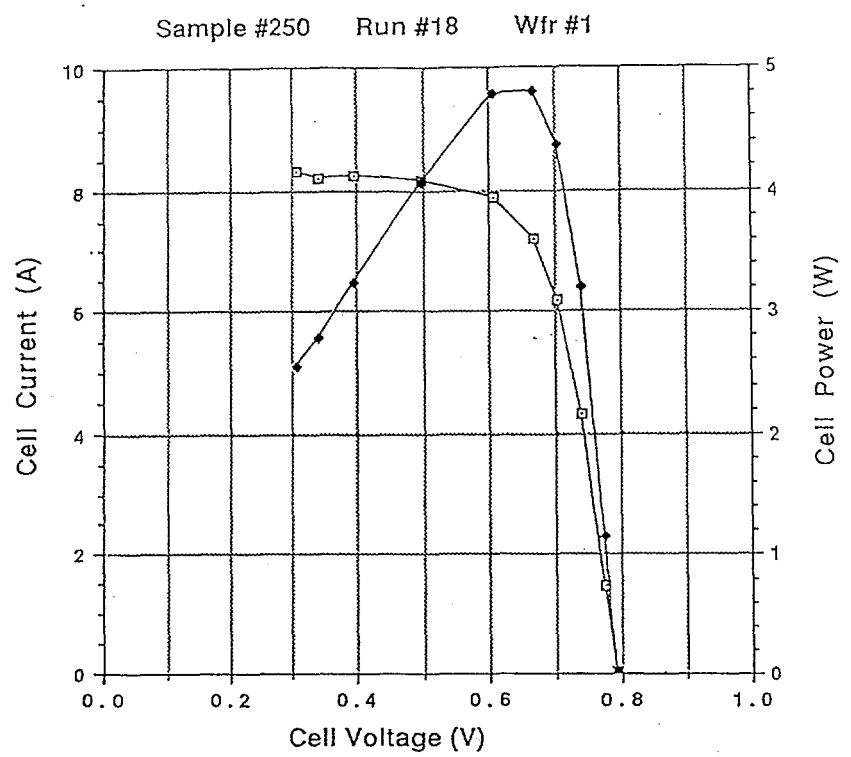


Figure 28: An I-V curve for a Run 18 cell.

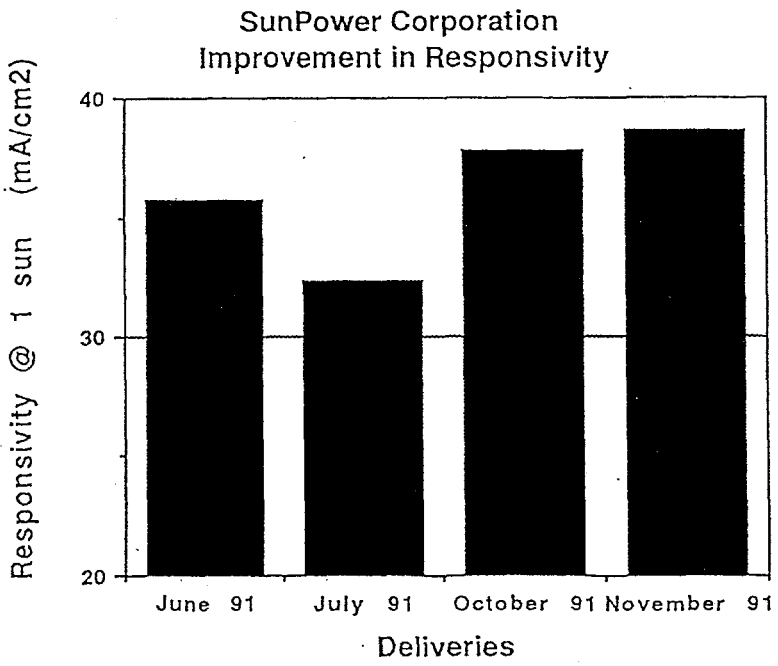


Figure 29: The improvement in responsivities for successive deliveries to Sandia.

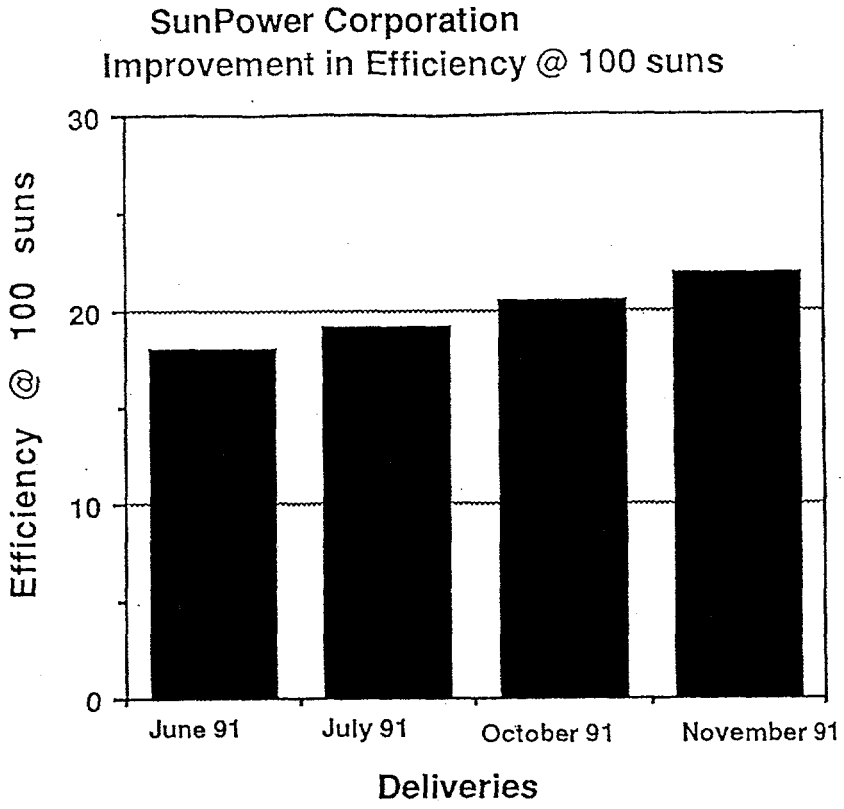


Figure 30: The improvement in efficiency for successive deliveries.

Another significant area of test results is for the initial stability studies on SunPower solar cells. We have begun stability studies in two ways. First, we have provided Doug Ruby at Sandia National Laboratories with sample cells from Run 13. Second, we have began exposing cells at 500 X in our own outdoor facility.

Some results from the Sandia study are shown in Figure 31. These results indicate that after 1500 sun hours of UV exposure, the change in efficiency at 100 X is less than 3%. Since this is nearly within the noise, it indicates that a large sample size needs to be used to investigate stability.

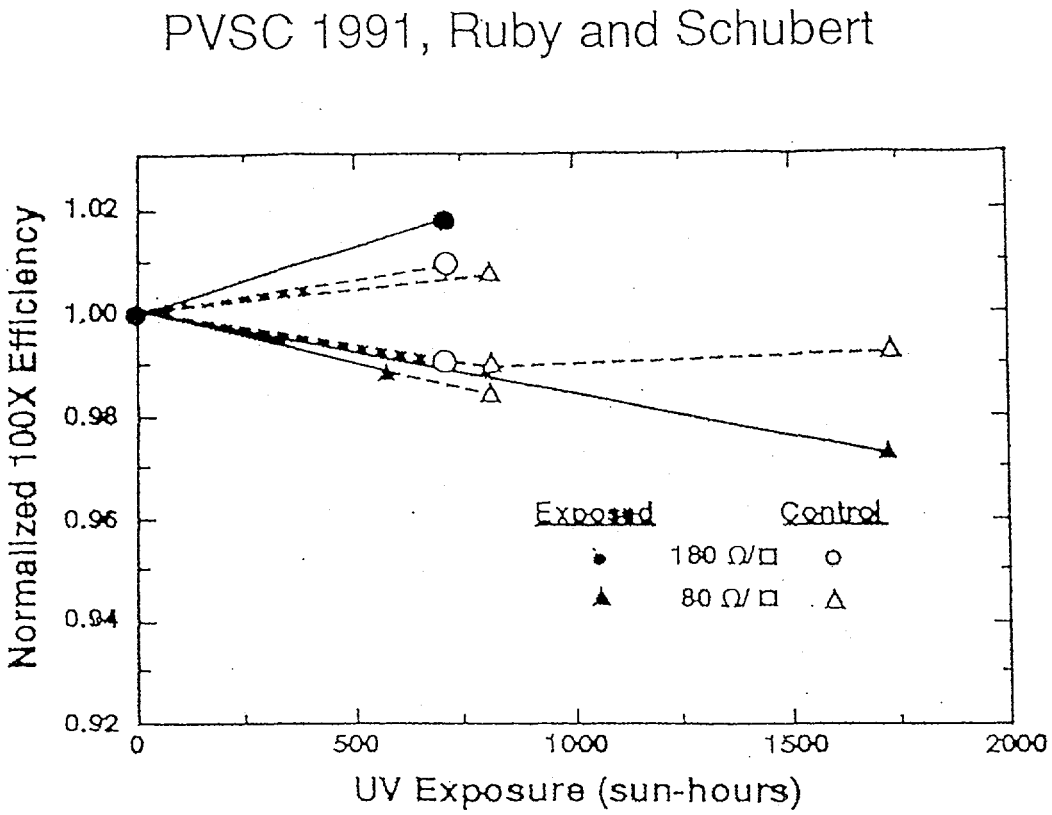


Figure 31: Measurements of the efficiency vs. UV exposure for SunPower cells exposed at Sandia.

The results from our own outdoor studies show similar results, and especially the need for large sample sizes for statistical significance. Two Run 13 cells showed a 3% drop in the current at 200 suns after 6 months of exposure, measured relative to controls. However, three Run 17 cells showed an improvement by 2% over a two month period preceding this report.

We have used our modelling and experimental results to analyze this baseline design to identify future improvements. The results of this analysis are shown graphically in Figure 32. Our near-term efficiency goal is 25% at 200 suns. Our current cells are about 21%. A detailed analysis identifies about 6 absolute percent in improvements. To reach the 25% goal, we need to eliminate 2/3 of these losses. Three losses account for most of the total. The first is the loss due to sublinearity, at 2%. This can be reduced by improving the front surface diffusion quality, the solder-void density, and by fabricating thinner cells. The second largest loss is the reflection loss, at 1 absolute percent. We plan to incorporate an antireflection coating into our cells to recover this efficiency. The third largest is a metalization series-resistance loss. This problem is most easily addressed by revising our metalization pattern.

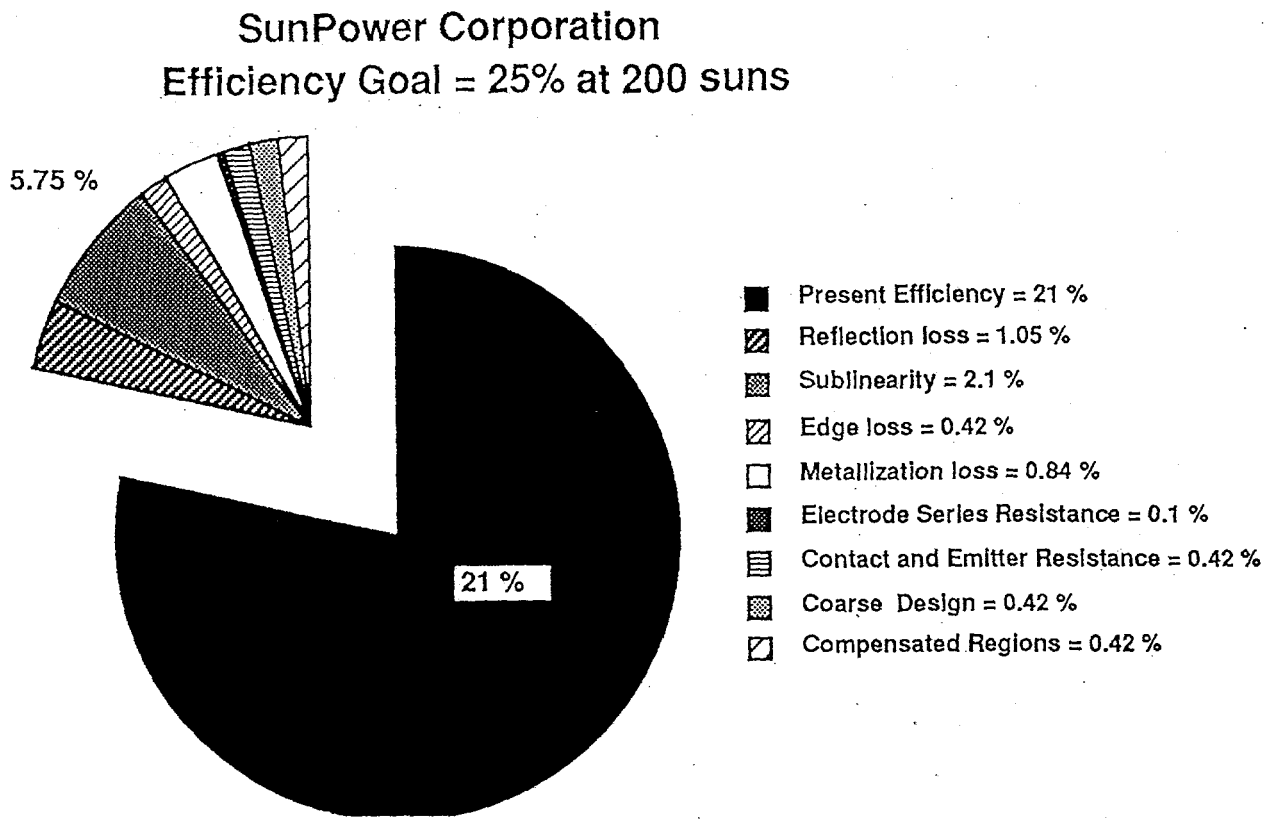


Figure 32: A graphic display indicating the current efficiency of 21%, and the various possibilities for improvement based upon modelling and experimental measurements of the various losses.

The contact resistance, emitter resistance, and the compensated region losses that together contribute 1% can be reduced by improvements in the dopant-diffusion optimization.

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6) M. A. Green, S. R. Wenham, J. Zhao, J. Zolper, and A. W. Blakers, "Recent Improvements in Silicon Solar Cell and Module Efficiency," 21st IEEE Photovoltaics Specialist Conference, Orlando, FL, pg. 207, May 1990.

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