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Circuit Description of Unipolar DC-to-DC Converters for APS Storage Ring Quadrupoles and Sextupoles

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ABSTRACT

This paper describes the control, interlock, and power circuits for 680 unipolar switch mode DC-to-DC converters used to regulate the Advanced Photon Source's (APS's) storage ring quadrupole and sextupole magnet currents. Quadrupole current stability is $\pm 6 \times 10^{-5}$ and the sextupole current stability is $\pm 3 \times 10^{-4}$. The stability is obtained with pulse width modulation, operating at a switching frequency of 20kHz with full current switching. The converters are housed in 200 cabinets located on top of the storage ring tunnel. Raw DC power is distributed from 80 AC-to-DC power supplies, four at each of 20 locations around the storage ring. Voltages, currents, and temperatures are computer monitored and logged for the converters and magnets. All converters and magnets are water cooled with the flow and pressure monitored at the inlet and outlet of groups. Water is interlocked with the raw power supplies and not the individual converters.

I. INTRODUCTION

All 680 unipolar switch mode DC-to-DC converters have the same circuit design and components with the exception of the current measuring device, the reference digital-to-analog converter (DAC), and the input capacitance. The quadrupole converters can operate at a DC output current of 0 to 460A and the sextupole converters from 0 to 200A. The output bus has a series damped low pass filter. There is also a 50Ω resistor across the magnet bus to parallel damp the cable used to connect a converter to the magnet. All converters are water cooled.

A total of up to four unipolar (quadrupole/sextupole) converters along with up to four bipolar correction magnet converters are housed in a 5ft x 3ft x7ft cabinet. Each cabinet also houses a microprocessor and interface cards to monitor and control the converters and magnets. A cabinet with converter chassis is shown in Fig. 1. This cabinet is used to power one magnet girder in the APS storage ring. There are 40 sectors with five magnet girders each (five converter cabinets) and one insertion device (ID) girder per sector. Each pair of sectors has four raw (not regulated) power supplies feeding the converters in the two sectors. The raw power supplies for two sectors also provide raw control power for the converter cabinets, ground protection, crowbar/shorting circuit for the DC-bus feeding the converter, and water flow interlock.

One of the 400 quadrupole DC-to-DC converters is shown in Fig. 2

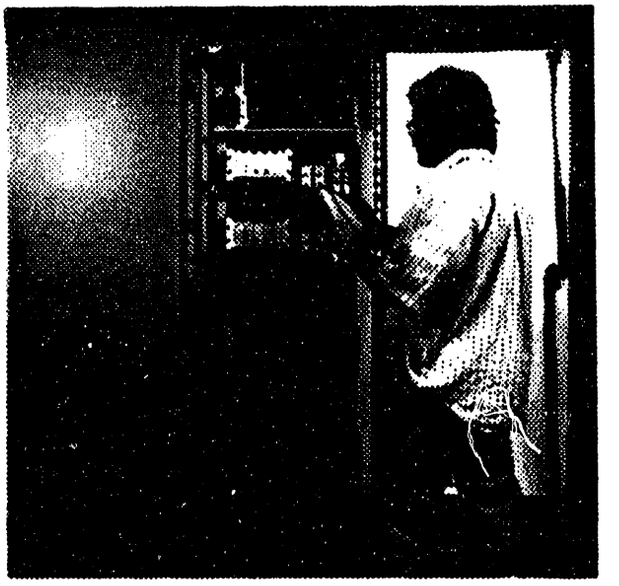

Fig. 1 One of the 200 storage ring converter cabinets.

Fig. 2 One of the 400 quadrupole DC-to-DC converters.

II. POWER CIRCUIT

The unipolar converter's power circuit is a buck converter operating into an inductive load, one of the storage ring quadrupole or sextupole magnets. This circuit is shown in Fig. 3. The charging voltage from the raw power supply was chosen to be ≥ 2 times the voltage drop of the magnet at 110% of full design current with a -10% low AC line. Two DC voltages are being used to supply all unipolar DC-to-DC converters.

Circuit Equations

The switching time for one cycle is $T_s = 50\mu s$ and the switching frequency is

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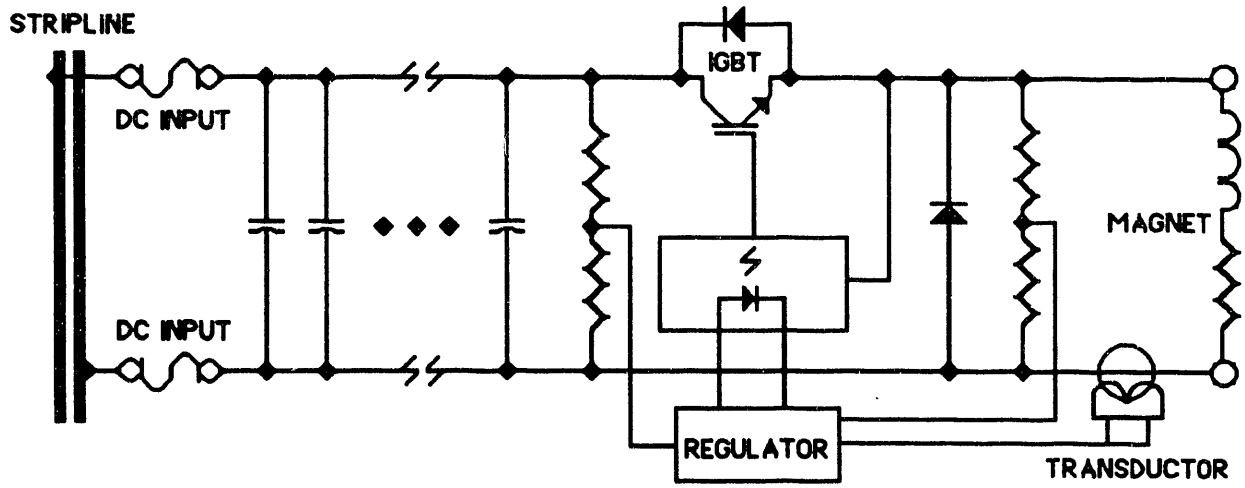

Fig. 3 A single line diagram of the DC-to-DC converter

$$F_s = \frac{1}{T_s} = 20kHz. \quad (1)$$

In this circuit the switching frequency is maintained constant at 20kHz and the switching element, insulated gate bipolar transistor's (IGBT) on time (t_1) is modulated to regulate the magnet current. The IGBT's duty cycle is

$$D = \frac{t_1}{T_s}. \quad (2)$$

The raw DC power supply voltage is given as V, the magnet inductance as L, and the circuit resistance as R. The normalized inductor time constant is

$$\tau_L = \frac{L}{R \times T_s}. \quad (3)$$

Minimum magnet current is

$$I_{L(min)} = \frac{V \times D}{R}\left[1 - \left(\frac{1-D}{2\tau_L}\right)\right], \quad (4)$$

maximum magnet current is

$$I_{L(max)} = \frac{V \times D}{R}\left[1 + \left(\frac{1-D}{2\tau_L}\right)\right], \quad (5)$$

and the peak-to-peak magnet current ripple is

$$\Delta i_L = I_{L(max)} - I_{L(min)}. \quad (6)$$

Magnet (D)	$I_{L(max)}$	$I_{L(min)}$	Δi	$\pm \frac{\Delta i}{I_{(Rated)}}$
0.8M Quad(0.33)	460.1250	460.0996	0.025340	2.754E-05
0.6M Quad(0.39)	460.4848	460.4614	0.023452	2.549E-05
0.5M Quad(0.34)	460.4159	460.3894	0.026449	2.875E-05
Sextupole (0.49)	200.8274	200.8135	0.013921	1.513E-05

Table 1. Magnet ripple current operating at rated current.

III. CONTROL

Control is divided into two parts. The first part is a hardwired clamp of the DAC that comes from the raw power supply. It is applied when the main contactor in the raw power supply is open and is removed a fixed time after it closes. The second part, performed by a computer using bit bus or RS232 communications, raises and lowers the reference DAC and resets the DC-to-DC converter and magnet interlocks. This reset (system normal) is required before the raw power supply interlocks can be made up and the main contactor closed; it is also hardwired.

Major components of the DC-to-DC converter's control circuits are:

1. An analog reference. Developed by an 18-bit DAC, it uses only the 16 most significant bits. This DAC is counted up or down 1 least significant bit at a time.
2. A direct current current transformer (DDCT) is used for the quadrupoles and a folded Zaran water-cooled shunt is used for the sextupoles. The DCCT has a bandwidth of 50 kHz, a ratio error of 50 ppm that changes 1 ppm/°K and/or 1 ppm/month. Its linearity error is < 20 ppm and offset error is < 10 ppm. The Zaran shunt has a temperature coefficient of resistance of ±3ppm/°K.
3. A high-gain, slow-current error amplifier. This amplifier with a 0.3 μV/°C max offset voltage drift, together with the current tranductor, allows the regulator to operate in the storage ring environment without temperature compensation (an oven).
4. A real-time, applied-voltage ramp circuit. Since the current's rate of change is slow compared to the 20kHz switching frequency, the ramp generator (integrator) is reset by the voltage across the freewheeling diode during the non-conducting period of the IGBT.
5. A very high gain comparator.
6. An IGBT gate driver circuit.
7. Switchmode control power supplies operating at ~100kHz. Since the total control power needed is <<150W (the upper limit for flyback configuration), and

the varied voltage outputs require transformer isolation, a switchmode flyback topology was selected.

VI. INTERLOCKS and MONITORING

There are three groups of interlocks: the raw DC power supply, the DC-to-DC converter, and the magnet interlocks. They are all hardwired. The dc-to-dc converter has eight binary interlocks and two magnet interlocks. The magnet's binary interlocks are two chains of temperature switches per magnet. The ten binary interlocks per DC-to-DC converter/magnet are ANDed into a single hardwired system normal and connected to the raw power supply. Anyone can shut off the raw power supply by opening the main contactor and clamping the DC-to-DC converter's reference DAC. When the raw power supply's main contactor is open, the output bus has a shorting (crowbar) switch across it. The raw power supply also has common interlocks for the DC-to-DC converters and magnets. These consist of magnet and power supply waterflow and ground circuit overcurrent.

Monitoring is accomplished by power supply control units (PSCUs). Each DC-to-DC converter is monitored by a PSCU combining ten binary interlocks to eight, selecting four of the five analog temperature signals and the precision analog-to-digital converter (ADC), and logging the data. Also, the PSCU used to monitor and control the raw power supplies in two sectors monitors water flow and pressure for both magnets and power supplies.

V. TEST SET UP AND RESULTS

Four unipolar DC-to-DC converters were installed in a converter cabinet with the outputs connected to magnets or dummy loads. A local computer connected to the PSCU controlled and logged the following 8-hour test run during preparation for large scale testing of converters. The test results of one of the quadrupole converter's output current transductor during this 8-hour run is shown in Fig. 4.

All of the APS storage ring power supplies will be test run in a temperature-controlled room with the temperature varing between 20°C and 50°C, even though the ambient temperature in the permanent location will be 24°C ± 1.5°C. A test run of the temperature-controlled room is shown in Fig. 5.

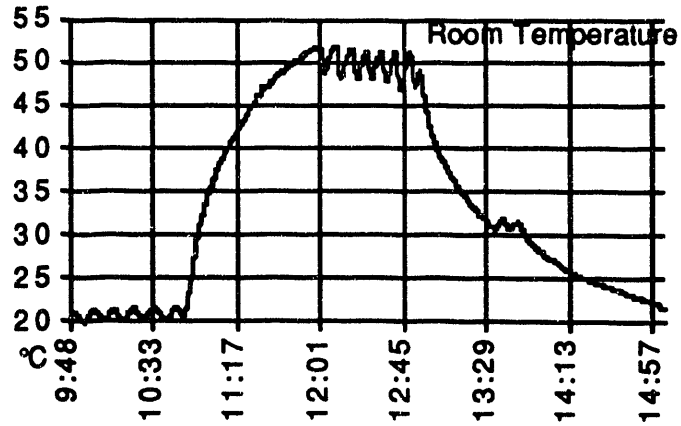

Fig. 5 Room temperature during a 5-hour test run.

The testing plan is to cycle each DC-to-DC converter to maximum and back to mimimum to verify proper operation. All converters are set to maximum design value and the temperature is raised to 50°C. It will be held at 50°C for one hour, then lowered back to 20°C and held there for one hour. The temperature is then cycled back to 50°C and held. The output currents of the DC-to-DC converters are randomly varied until we have run a minimum of eight hours. The unit data will be checked and, if acceptable, the converters will be installed. Failed converters will be repaired and retested.

V. REFERENCES

1. D. McGhee, "Status of Magnet Power Supply Development for the APS Storage Ring," 1989 IEEE Particle Accelerator Conference Proceedings, March 1989.
2. Rudolf P. Severns, and Gordon E. Bloom, "Modern DC-to-DC Switchmode Power Converter Circuits," Van Nostrand Reinhold Company, 1985.

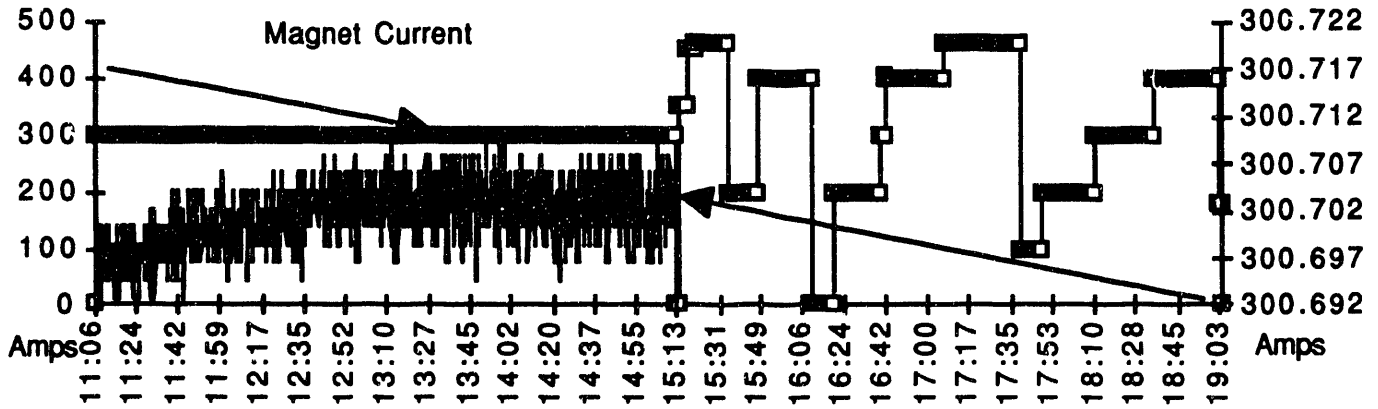

Fig. 4 The internal and external transductor signal for the full-current part of an 8 hour test run.

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