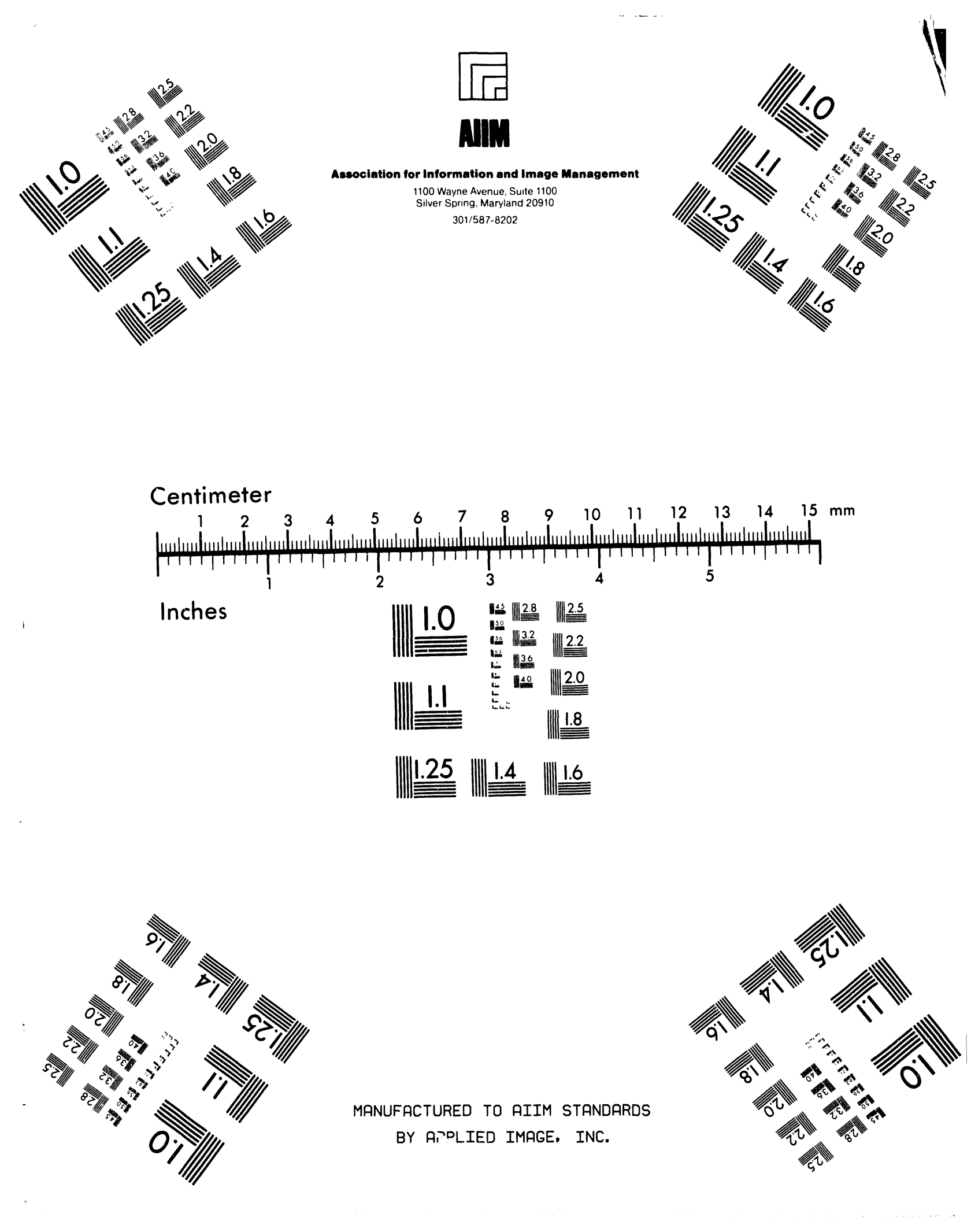

AIIM
Association for Information and Image Management
1100 Wayne Avenue, Suite 1100
Silver Spring, Maryland 20910
301/587-8202
Centimeter
Inches
MANUFACTURED TO AIIM STANDARDS
BY APPLIED IMAGE, INC.

1 of 1

EMBRITTLEMENT OF SURFACE MOUNT SOLDER JOINTS BY HOT SOLDER-DIPPED, GOLD-PLATED LEADS[1]

Paul T. Vianco
Center for Solder Science and Technology
Sandia National Laboratories
Albuquerque, NM 87185

ABSTRACT

The detachment of beam-leaded transistors from several surface mount circuit boards following modest thermal cycling was examined. Microstructural analysis of the package leads and bonding pads from the failed units indicated that gold embrittlement was responsible for a loss of solder joint mechanical integrity that caused detachment of transistors from the circuit boards. An analysis of the hot dipping process used to remove gold from the leads prior to assembly demonstrated that the gold, although dissolved from the lead, remained in the nearby solder and was subsequently retained in the coating formed on the lead upon withdrawal from the bath. This scenario allowed gold to enter the circuit board solder joints. It was hypothesized, and later confirmed by experimental trials, that increasing the number of dips prevented gold from entering the solder coatings.

INTRODUCTION

Copper is the material-of-choice for device leads, termination coatings, and circuit board pads. Copper tarnishes are readily removed by rosin-based (R) and mildly-activated, rosin-based (RMA) fluxes so as to permit wetting by electronic solders. However, copper does not always satisfy package construction requirements. For example, glass-to-metal seals that ensure the hermeticity of some ceramic packages must use one of the low expansion alloys as the lead material. Low expansion alloys, including Kovar™ (29Ni-17Co-0.2Mn-bal.Fe), Invar™ (36Ni-0.3Si-0.35Mn-bal.Fe), and Alloy 52™ (50.5 Ni-0.25Si-0.5Mn-bal.Fe)[1], are difficult to solder because of a tenacious oxide film formed on the surface. Only extremely aggressive flux chemistries, most of which are prohibited from use for the assembly of electronic packages, can promote solder wetting on the surfaces of these materials. Therefore, solderable coatings such as nickel and copper are

[1]This work was performed at Sandia National Laboratories and supported by the U.S. Dept. of Energy under contract DE-AC04-76DP00789.

deposited on the leads to provide a wettable surface, nickel being the predominantly used material. Recommended thickness of these coatings are specified in MIL-STD-1276D. In order to prevent contamination or excessive oxidation of the solderable surface, a protective finish is added on top of the solderable layer. The protective layer may be electroplated or hot-dipped pure tin or tin-lead solder as well as precious metal finishes such as gold, silver, palladium, or platinum. Gold is the preferred coating due to its protective capacity at limited thicknesses (1.3-3.8 μm), even when exposed to elevated temperatures such as those experienced in "burn-in" environments. In a soldering operation, the gold layer is quickly dissolved into the solder. The gold combines with the tin component of the solder to form one of two intermetallic line compounds: $AuSn_2$ or $AuSn_4$[2]. The latter intermetallic compound is the predominant composition. The capacity for gold to embrittle tin-lead solders is well documented[3,4,5]. Shown in Fig. 1 is the Izod impact toughness of tin-lead solder as a function of gold concentration[4]. From the data in Fig. 1, a maximum limit for gold content in tin-lead solder, above which embrittlement is likely, is approximately 3-4 wt%; however, some manufacturers maintain stricter guidelines or permit no gold, whatsoever, in their solder joints. Gold is typically removed from leads and leadless device terminations by dipping the lead or termination into a molten bath of solder. The gold quickly dissolves into the solder. The lead is left with a solder coating on the surface upon withdrawal from the solder. A dual-bath process is usually specified for the hot dipping procedure in order to prevent recontamination of the leads from gold build-up in the bath.

A case history is presented which describes the catastrophic failure of several beam-leaded transistors from their surface mount circuit boards. The gold-nickel plated Kovar™ leads were hot solder dipped in tin-lead alloy (dual-bath process) prior to assembly of the device onto the circuit board. The subsequent failure analysis demonstrated that gold embrittlement of the solder joints was responsible for the failure of the interconnects. Further theoretical and experimental analyses will identify the mechanism responsible for the embrittled solder joints.

CIRCUIT BOARD ASSEMBLY AND FAILURE HISTORY

The surface mount circuit board assembly was comprised of polyimide-quartz laminate 0.79 mm (0.031 in.) thick. The bonding pads were 1 oz. copper and solder coated by hot air leveling with 63Sn-37Pb (wt.%) followed by the hydrosqueege process to reduce the

solder coating thickness. The solder coating thickness was measured to be 0.15 mm (0.006 in.).

The configuration of the transistor is illustrated by the schematic diagram and photograph shown in Fig. 2. The emitter lead of the transistors measured 0.89 x 1.1 x 0.10 mm (0.035 x 0.043 x 0.004 in.). The lead material was Kovar™. Specifications called for the leads to be plated with 1.27-3.81 μm (50-150 microin.) of nickel as the solderable finish followed by a minimum of 2.2 μm (87 microin.) of gold (A maximum was not designated). Experimental measurement of the coating thicknesses showed them to be 3.3 μm (130 microin) and 3.8-4.3 μm (150-170 microin.), respectively. The thickness of the nickel layer complied with the transistor specification as well as the general MIL-STD-1276D. The gold thicknesses were somewhat higher than the values of 1.3-2.5 μm (50-100 microin.) specified by the military standard.

One transistor was located on each side of the board; they were denoted Q1 for that on the top side and Q2 for the unit located on the bottom side of the substrate. Prior to attachment of the transistors to the circuit board, each of the leads was hot solder dipped to replace the gold coating with a tin-lead solder finish. This practice was conducted in order to certify that gold was not introduced into the circuit board solder joints. The hot solder dipping procedure consisted of immersing each lead into a bath of molten 63Sn-37Pb solder held at 250°C for a period of 2 sec. The procedure was repeated a second time, using a different bath of molten solder to ensure that gold was not re-introduced onto the leads from its concentration build-up in the first bath. Briefly, the circuit board assembly process can be summarized in the following steps. (1) 63Sn-37Pb solder paste was stencil printed onto the *bottom* side of the circuit board. (2) The transistor (Q2) and other components were placed onto the solder paste deposits covering their respective bonding pads by an automated pick-and-place robotic system. (3) The circuit board was placed in the vapor phase reflow apparatus and subjected to the following heating schedule:

- preheat 95°C to 105°C within 7 min.
- reflow at 210-220°C for 30 sec.
- cool parts to 100°C within 7 min.

(4) The board was then turned over and the process repeated in order to attach components to the *top* side of the board (which included the Q1 transistor). Therefore, the solder joints of the parts installed on the bottom side were reflowed a second time. The surface tension of the liquid solder prevented the components from dropping off of

the inverted circuit board. (5) The circuit board assemblies were cleaned of flux residues (Freon TMF and isopropyl alcohol). The circuit board was then encapsulated in a protective foam.

Failure of the solder joints was discovered through the temperature dependent electrical performance of test units. The first failure was in a unit being held at 130°C; the circuit board had been at that temperature for less than one hour. The encapsulant was removed (chemically). It was observed that the Q2 transistor had separated from the board. A second test unit was being similarly tested for elevated temperature functionality when during its second excursion to 130°C, it also lost electrical performance. Removal of the foam encapsulant revealed that the Q1 transistor had separated from the board. A third circuit board was exposed to 130°C test temperature on two occasions. On the third ramp-up, the unit ceased to operate at 80°C. The foam encapsulant was removed and the Q1 transistor separated from the bonding pads. In each of the cited cases, the transistors had completely broken away from the circuit board at all three of the lead solder joints.

Shown in Fig. 3 are optical micrographs of (a) the transistor in place on the circuit board and (b) the bonding pads remaining after loss of the transistor. It was observed on each of the failed units that there were no apparent flux residues under the transistor packages to suggest poor cleaning efficiency and hence, the possibility of a corrosion mechanism being responsible for the failures. A scanning electron microscope (SEM), secondary electron image of the emitter lead bonding pad from one of the failed units is shown in Fig. 4. This micrograph is representative of the bonding pad failure morphologies observed on each of the defective units. Except for the missing solder pertaining to the footprint of the lead, the pad was otherwise undisturbed. High magnification SEM images of the bonding pad fracture surfaces showed a granular morphology without ductile tearing of the expectedly soft solder. These observations suggest that overload stresses (relative to the known strength of the solder) were not responsible for the catastrophic failures.

SEM micrographs of a failed lead are shown in Fig. 5. The transistor leads were not deformed so as to suggest the presence of excessive loading forces on the joints. Previous experience with the assembly processes, including encapsulation and depotting of the circuit boards, discounted those procedures as being directly responsible for the loss of the transistors. Moreover, an effort to remove intact Q1 and Q2 transistors on two other units was completely unsuccessful.

A solder layer measuring approximately 50 μm (0.002 in.) thick remained on the surface of the leads (Fig. 5b), indicating that the fracture path was within the solder. A schematic diagram that reconstructs the fracture path is shown in Fig. 6. The fracture path followed the contour of the lead, discounting the possibility that brittle copper-tin intermetallic layers at the solder/copper pad interface caused the failure. Clearly, a severe weakening of the *solder within the joint* had taken place.

Degradation of the solder's mechanical integrity was most likely caused by a change in the chemistry of the alloy. Therefore, backscattered electron imaging (SEM) was used to delineate possible composition variations of the solder in the failed joints. Shown in Fig. 7a is a magnified view of the remaining fillet on a failed solder joint. A combination of acicular and massive crystals were observed in the solder; these features are characteristic of the formation of gold-tin intermetallic compounds. Supporting evidence comes from the backscattered electron image in Fig. 7b. The contrast variations show the acicular and massive islands to be of a gray tone *between* the very light regions of the higher "Z" lead-rich phase (Z being the atomic number) and the very dark areas of relatively low "Z" tin-rich phase. The medium gray level intensity is expected for the gold-tin intermetallic since it is comprised of a mixture of both high "Z" gold and the low "Z" tin metals. A similar analysis was performed on the undisturbed surfaces of the leads from transistors which had separated from the circuit board. A morphology very similar to that exhibited in Fig. 7 was also observed on the leads.

An energy dispersive x-ray analysis (EDXA) was conducted on the fracture surface of a failed collector lead bonding pad (Fig. 8a). The EDXA spectra of the bonding pad fracture surface (Fig. 8b) indicated signals of tin and lead from the solder as well as those of gold and copper. The copper signal had two likely sources: (1) the copper bonding pad under the solder film or (2) the copper-tin intermetallic layer formed at the solder/pad interface and exposed by the fracture path located through that layer. Point (2) was discounted when a similar spectrum was acquired from the complimentary surface of the transistor lead (Fig. 8c). The copper signal was absent; however, the gold signal was still quite evident.

Examination of the fracture surfaces as well as the condition of the leads implied that the fracture was brittle in nature, with very little energy used to separate the transistor leads from the bonding pads. The qualitative chemical analyses by backscattered electron

imaging and EDXA, indicated that gold was present in the solder joints, despite measures to remove the gold plating from the leads prior to assembly. Therefore, gold embrittlement of the solder joints appeared as the likely source of the failures.

Prior to continuing the experimental studies, it was necessary to determine the feasibility of gold embrittlement, given the amount of gold available from the electroplated coating of the leads. The thickness of the gold measured on the leads was 3.8 - 4.3 μm (150-170 microin.); a value of 4.1 μm (160 microin.) being an acceptable mean. A summary of the calculation results is provided in Table 1. The "footprint" length describes the extent of the lead present on the bonding pad as measured from micrographs similar to that shown in Fig. 8a. The mass of gold present on each lead was calculated from the lead surface area and the average gold thickness. In order to determine the mass of solder present in each joint, it was noted that a solder paste thickness of 152 μm (0.006 in.) resulted in a solder thickness of 76-100 μm (0.003-0.004 in.); a value of 100 μm (0.004 in.) was selected for the computations. Hot solder dipping of the transistor leads added additional solder to the joint; albeit the amounts were variable both between leads as well as on the same lead. The latter condition is indicated by the cross sectional micrograph of hot a solder dipped lead shown in Fig. 9. An average solder thickness of 6.6 μm (0.0026 in.) was calculated from cross sectional micrographs similar to the example in Fig. 9. It is observed from the data in Table 1 that the gold content of the solder joints exceeded the 4 wt% limit. It must be noted that the gold concentrations could be much *higher*. For example, if the hot dipped solder layer was assumed to be nearly zero (a viable assumption given the image in Fig. 9), then the gold concentrations (Table 1) of the solder joints would increase to 6.1, 8.3, and 7.0 wt% for the collector, emitter, and base leads, respectively.

Therefore, it was apparent that the gold layers on the leads could *potentially* embrittle the solder joints. Moreover, because the calculated concentrations were in close proximity to the 4 wt% limit (and could be higher due to the variable quantity of solder involved), it became clear why in some instances, the transistor joints were embrittled while for other cases, the transistors were tightly bonded to the circuit board.

The next step in the failure analysis was a series of experiments to confirm that gold was being introduced into the circuit board solder joints. Then, the study will turn to identify the reason by which the particular hot solder dipping procedure was ineffective towards preventing gold embrittlement of surface mount solder joints.

EXPERIMENTAL INVESTIGATION

The objective of the first part of the experimental study was to examine transistor leads which were hot solder dipped in a manner similar to that used on the detached transistors. This approach was used to establish reproducibility of the gold contamination of the leads as well as to examine whether changes to the hot solder dipping parameters would alter the gold contamination process. Transistors were received from the supplier which had been hot solder dipped by the procedure outlined earlier in this report. Three leads were removed from as many transistors, mounted and metallographically cross sectioned along the length axis. A micrograph of those leads (Fig. 9) was presented earlier. It is evident that the solder layers resulting from the hot dipping process were extremely variable between the different leads. The gold plating layer was absent from a the lead surface/solder interface, except for sections that were very near to the transistor body where the solder coating significantly diminished to prevent package contact with the solder. The nickel layer was present with no excessive dissolution by the molten solder.

Visual examination of the solder layers did not reveal the acicular or blocky phases indicative of gold-tin intermetallic crystals. Under the premise that the gold was finely dissolved into the solder layer, an electron microprobe analysis (EMPA) was performed to detect its presence. X-ray dot maps were used as a semi-quantitative evaluation of the gold concentration. The regions of analysis were well away form the transistor body section of the leads. Shown in Fig. 10a is the SEM backscattered electron image a segment of interface from the lead in Fig. 9. Fig. 10b shows the gold x-ray dot map (L_α line) of the same region. Gold-rich areas were evident in the solder film, including a significant concentration remaining near the solder-nickel layer interface. A similar analysis was perform on a second lead; the associated SEM and x-ray dot maps are shown in Fig. 11. Substantial gold was observed in the solder film as well as near the solder-nickel interface.

In conclusion, these analyses demonstrated that the standard hot solder dipping process outlined in the second section did <u>not</u> completely eliminate gold from the transistor lead solder layer so that subsequent contamination of the circuit board solder joints was inevitable. Semi-quantitative analysis provided on the dot maps revealed gold concentrations well in excess of the 4 wt% limit shown to introduce solder embrittlement.

Next, a set of experiments was performed to determine whether the gold contamination of the hot solder dipped coatings could be reduced by altering the parameters of the dipping process (time and temperature of immersion). If this concept proved unsuccessful, then a fault intrinsic to the hot solder dipping practice, was present. The latter condition would require a thorough examination of the process itself. Because of the heat sensitivity of the devices, the option of using higher solder bath temperatures was prohibited.

It was hypothesized that in order to promote dissolution of the gold into the solder bath, a longer immersion time should be evaluated. Experiments by Bader[6] documented the dissolution rate of various metal wires in molten 63Sn-37Pb solder; that data is shown in Fig. 12. Clearly, the maximum 4.3 μm (170 microin.) thick gold film should be completely dissolved into the solder within the 2 sec. immersion time, even when account is taken for the difference in geometry between cylindrical wires (Fig. 12) and the beam leads of the transistor. Transistor leads were hot dipped using the same procedure as previously described, except that the immersion time was varied between 1, 2, 3, and 4 sec. One lead from each of two transistors was immersed for one of the time intervals. Outlined in Table 2 are the gold concentrations from electron microprobe analysis of the leads. The values in Table 2 are an average (and $\pm$ one standard deviation) of 20 data points which were taken per lead at steps of 100 μm (0.004 in.) along the lead length. The electron beam sampling area measured 30 μm (0.0012 in.) on a side. The gold content increased as the sample area approached the transistor body. The standard deviation values were caused by the variable distribution of gold throughout the films. Shown in Fig.13 are the SEM image and gold x-ray dot map of a lead hot dipped for 4 sec. Substantial gold is observed on the solder coating surface. A heavy gold concentration was also observed on leads immersed for 3 sec. Therefore, the extended immersion times did not improve the removal of gold from the solder film coating on the leads. Work by Vianco, et al.[7] on hot solder dipped, gold-nickel-plated Kovar coupons showed that in the vicinity of the solder film edge (a distance comparable to the length of the transistor leads), gold-tin intermetallic crystals were observed on the surface of the solder coatings. Those test coupons were immersed in the solder (260°C) for 20 sec.

In summary, it appeared that extending the immersion time was not a successful approach towards eliminating gold from the hot dipped coating. Therefore, the hot solder dipping technique was carefully analyzed to uncover some intrinsic "flaw" in the process which may be responsible for gold being retained in the solder coating and ultimately, embrittling the circuit board solder joints. This study appears in the following section.

ANALYSIS

The data by Bader (Fig. 12) demonstrated that gold should be completely dissolved into the molten solder. A close examination was made of the solder volume *geometry* present around the lead circumference during its immersion into the solder. An analysis was performed, the objective of which was to determine the gold content inside of the meniscus formed on the immersed lead. It will be assumed that the meniscus volume is stagnant and that gold transport parallel to the lead length dimension does not take place. Shown in Fig. 14 is the scale profile of the solder meniscus which forms on the lead upon contact with the molten solder. The profile of the solder meniscus was generated by equation (1) which describes the [x(y),y] coordinates of the meniscus surface[8]:

$$x(y) = A \left\{ (1/(2\sqrt{2})) \ln\left[(\sqrt{2} + q)/(\sqrt{2}-q)\right] - \right.$$
$$\left. - (1/(2\sqrt{2})) \ln\left[(\sqrt{2} + q_c)/(\sqrt{2}-q_c)\right] - q + q_c \right\} \qquad (1)$$

where:

$$A = \sqrt{\ } \left[2 \gamma_{LF} / g \rho\right] \qquad (1a)$$

$$q = \sqrt{\ } \left[2 - g \rho y^2 / (2 \gamma_{LF})\right] \qquad (1b)$$

$$q_c = \sqrt{\ } \left[2 - g \rho H^2 / (2 \gamma_{LF})\right] \qquad (1c)$$

The parameters of equation (1) are: ρ is the solder density (8.49 g/cm^3); g is the acceleration due to gravity (980 cm/sec^2); H is the meniscus rise height (0.265 cm)[6]; and γ_{LF} is the solder-flux interfacial tension (360 dyne/cm with a rosin-based, mildly activated flux)[6]. The lead is several millimeters long when immersed into the solder; however, only a length of approximately 1.5 mm (0.060 in.) nearest to the transistor body is used in the circuit board joint. It is apparent that the volume of solder available into which the gold can dissolve is very limited.

A calculation was performed to determine the gold concentration in the meniscus which forms on the lead during the hot solder dipping process. As shown in the scale drawing in Fig. 15, the solder meniscus profile was divided into five segments. The area of the segments (which represent the meniscus volume with a depth dimension of unity) was

calculated by integrating the function x(y) from equation (1) between the boundaries "a" and "b" as shown in equation (2):

$$A[a,b] = \int x(y)\, dy \qquad (2)$$

The computation was done numerically. Next, the gold present in each of the segments was computed from the coating thickness (4.1 μm) available on the lead between the boundaries "a" and "b". It was assumed that there was negligible lateral diffusion of gold between the segments. The gold concentrations (wt%) appear next to each of the segments. The results demonstrate that local gold concentrations exceed the 4 wt% limit.

Verification of the existence of a concentration gradient due to the geometry of the meniscus was determined by means of the following sessile drop experiment. A preform of tin-lead solder was placed on top of each of two Kovar™ coupons which had been electroplated with nickel and gold. The gold thickness was measured to be 2.7 μm (106 microin.). A thermocouple had been spot welded to each of the coupons. Next, each coupon plus preform was placed atop a hot plate (260°C). The solder preform on the first coupon formed a lenticular sessile drop and was promptly removed from the hot plate (Fig. 16a). In the case of the second specimen, the coupon was removed from the hot plate with the sessile drop having a bulbous geometry (Fig. 16b). The two configurations in Figs. 16a and 16b represent the confined and open geometries, respectively, at the solder film edge. The geometry in Fig. 16a was similar to that of the solder meniscus formed on an immersed lead (Fig. 14). The sessile drops were cross sectioned and the surface prepared metallographically. Then, electron probe micro- analysis was performed along a line trace parallel to the interface. The traces were run at distances of 5, 10, and 25 μm (200, 400, and 1000 microin.) from the interface. The gold concentration along the line trace at 5 μm (200 microin.) is shown in Fig. 17a for the lenticular drop (Fig. 16a) and Fig. 17b for the bulbous drop geometry (Fig. 16b).

In the case of the lenticular drop, the gold concentration increases from the center of the drop towards the edge. Although the data is somewhat scattered, it is observed that the gold concentrations are similar to those computed in Fig. 15; that is, the gold concentrations range from about 20 wt% at the very edge to a approximately constant value of 1-2 wt% at a distance 1500 μm (0.059 in.) from the leading edge. For the traces further out from the interface, the peak concentration diminished to about 15 wt.% at the edge of the solder film and similar values to those in Fig. 17a at the drop interior. The

effect of the bulbous configuration on the gold concentration is illustrated by Fig. 17b. In the open configuration of the bulbous joint, the gold concentration is relatively constant along the entire interface at a value of 2-3 wt%; there is no appreciable build-up of gold at the edges of the solder film. The same concentration profile was repeated for traces taken at 10 μm (400 microin.) and 25 μm (1000 microin.) from the interface.

In summary, a hypothetical analysis showed that the gold concentration in the molten solder meniscus could be substantial, particularly near the lead interface. Experimental analysis of sessile drops confirmed that for confined configurations like the volume of the meniscus, the gold would become highly concentrated. More open geometries such as the bulbous drop allowed the gold to diffuse into the bulk material. The solder contained in the meniscus is used to form the hot dipped coating which remains on the lead(s) upon withdrawal from the bath. Therefore, these analyses demonstrate the following scenario: Immersion of the gold-plated lead into the molten solder dissolves the coating from the substrate surface (in agreement with Bader's experiments). However, it appears that the gold does not readily diffuse away from the solder meniscus. Therefore, the hot dipped coating developed on the lead upon withdrawal transports the gold to the circuit board solder joints.

Finally, a scenario was developed to explain the *embrittlement* of the solder joint, based upon the physical metallurgy of gold in tin-lead solders. Shown in Fig. 18 is the pseudo-binary phase diagram for gold (0-20wt%) and 63Sn-37Pb solder (under equilibrium)[9]. To begin, the hot dipping process is performed at a solder bath temperature of 250°C. In the solder meniscus formed on the lead, the gold concentration was observed to range largely between 1 wt% and 10 wt%, except for the region near the very edge of the meniscus (Fig. 15). Therefore, the gold will be in solution ("L" or liquid phase field) at that temperature. Upon withdrawal of the lead from the bath, the solder solidifies, forming a two phase composite of 63Sn-37Pb matrix and $AuSn_4$ intermetallic compound. Some of the gold may remain in a super saturated solid solution in the solder due to the rapidity with which the solder coating solidified. This latter expectation was confirmed by optical micrographs and x-ray dot maps of contaminated leads presented earlier.

The next processing step is for the device to be mounted onto the circuit board. In this case, the vapor phase (or condensation) process was used; reflow took place at a temperature of 215 - 220°C and lasted 30 sec. Referring again to the phase diagram in Fig. 18, the gold will largely re-dissolve into the molten solder. Upon the slow cooling

rate inherent in the vapor phase equipment, the gold comes out of solution as the solder solidifies, combining with the tin to form the $AuSn_4$ intermetallic compound which subsequently embrittles the joints. Nucleation and growth of the intermetallic crystals *within* the circuit board solder joints increases the chances of the intermetallic for having an orientation favorable for the development of a continuous fracture path surrounding each transistor lead (Fig. 6).

In summary, the scenario by which the gold coating on the transistor leads causes embrittlement of the circuit board solder joints has been illustrated. The gold layer is dissolved from the lead during the hot dipping process. However, the gold is confined to the meniscus that has formed on the lead, and is subsequently picked up again by the remainder of the lead upon withdrawal from the bath. During the cooling step of the vapor phase reflow cycle used to assemble the transistor to the circuit board, the gold precipitated as gold-tin intermetallic crystals which subsequently embrittled the solder joints.

REMEDIATION OF THE EMBRITTLEMENT MECHANISM

Once the root cause of the gold embrittlement of the circuit board solder joints was identified, appropriate action was sought to correct the problem. It was observed earlier in the investigation that prolonging the immersion time had no significant effect on the degree of gold contamination in the solder film. Also, although increasing the bath temperature was not an option due to the temperature sensitivity of the devices, this action, much like prolonging the immersion time, would not be expected to have an appreciable effect in light of the above analysis. After all, the gold was readily dissolved from the lead surface; it simply remained in the meniscus solder volume which later contributed to the hot dipped coating on the lead. Potentially corrective actions included the following approaches: (1) removal of the meniscus configuration characterizing the immersion process, (2) use of agitation to assist the diffusion of gold away from the meniscus, into the bulk solder bath, or (3) the use of multiple immersion steps so that each time the lead is hot dipped, the meniscus solder volume (and therefore, the solder coating on the lead) becomes increasingly more dilute of gold.

Point (1) would seek to remove the solder meniscus, altogether. However, the meniscus geometry is an intrinsic property of solder wetting phenomena. Therefore, it is unlikely that this approach has a significant potential for success.

Agitation of the solder bath appeared to be a viable recourse for the removal of gold from the hot dipped film. However, attempts at physical agitation of the bath by stirring or nitrogen gas blow-through proved unfeasible due to the small size of the device and the requirement for restricted solder contact with the package housing.

Finally, the third approach was examined. The basis for increasing the *number* of immersions, is described as follows: When the lead is initially immersed into the solder, the gold plating is dissolved into the solder meniscus volume as described earlier. However, the entire meniscus volume is *not* retained on the lead. Rather, only a fraction of the meniscus solder coats the lead. Assuming that the gold diffuses throughout the meniscus volume, then "only a fraction" of the dissolved gold is taken up in the solder coating upon withdrawal of the lead. Therefore, re-immersion of the lead a second time dissolves the solder coating (plus gold) into the new meniscus volume, thereby further diluting its concentration. If the entire meniscus volume were retained by the lead, then there would be no opportunity for the dilution process to take place. The meniscus provides a much more limited volume of solder than was assumed to be the case for the entire bath.

The thickness of the solder coating formed upon withdrawal of the lead can be approximated through the use of steady state fluid mechanics. By the action of a fluid (molten solder) moving past a solid interface (the lead), a boundary layer is developed in the fluid near the substrate in which the liquid velocity gradually slows down to match that of the substrate (i.e., zero if the substrate is at rest). This concept is shown schematically in Fig. 19 in which the velocity of fluid, u(x,y), is a function of position along the plate, x; the distance, y, from the surface; and the far field velocity of the fluid, U. Conversely, if the substrate is moving and the fluid is still, a boundary layer of fluid develops near the substrate with a velocity field similar to that in Fig. 19. This latter case describes the withdrawal of a lead from the solder bath. Time-dependent start-up effects are assumed to be insignificant. If it is assumed that the fluid layers near the substrate with a velocity greater than 0.9 of the substrate velocity remain "intact" on the substrate, then the calculation of that layer thickness will approximate the quantity of solder coating the lead.

The development of the boundary layer on the lead withdrawn from the solder is assumed to be laminar (as opposed to turbulent). In order to verify this assumption, a calculation

of the Reynolds number was necessary. The Reynolds number, N_R, is determined from the following expression:

$$N_R = U L / \nu \tag{3}$$

where U is the substrate velocity, L is the characteristic length dimension of the "system" (in this case, the full length of the lead), and ν is the kinematic viscosity of the molten solder. The value of N_R must be less than 500,000 for laminar flow conditions to be present[10]. Assuming a withdrawal velocity of 1.3 cm/sec, a characteristic length of 0.632 cm (for the uncut lead), and a kinematic viscosity of 0.00263 cm^2/sec (calculated from the values for tin and lead, combined by the mixing rule)[11], the Reynolds number is 312. It is apparent that the precise values of U, L, and ν were not critical in the computation since, a posteriori, the value of N_R is more than three orders of magnitude less than the criterion; therefore, laminar boundary layer theory was applicable to these circumstances.

The velocity of the fluid at any point, x, along the length of the lead (x=0 is point "A" in Fig. 19) and at a distance, y, from the substrate surface, is given by the expression:

$$u(x,y) = U (2\eta - \eta^2) \tag{4}$$

where η is:

$$\eta = y / \delta(x) \tag{5}$$

The term, $\delta(x)$, is the boundary layer thickness and is given by the expression:

$$\delta(x) = [(2\beta / \alpha)^{1/2}] [x / (N_{R,x})^{1/2}] \tag{6}$$

where β and α are numerical constants (1.63 and 0.35, respectively[10]) and $N_{R,x}$ is the local Reynolds number, xU/ν. The boundary layer of molten solder with a velocity (u) of greater than 0.9 of the lead withdrawal speed, U, is shown to scale with the meniscus geometry and the lead in Fig. 20. It is apparent that only a fraction of the meniscus volume remains on the lead upon its removal. Therefore, the *amount* of gold retained is a corresponding fraction of the amount in the meniscus. As a consequence, further immersions of the lead into the molten solder should cause the gold concentration in

subsequent solder menisci to be further diluted which should diminish the gold content of the solder coating upon lead withdrawal.

A calculation of the dilution effect will be made in order to determine the number of immersions required to reduce the gold concentration in the solder meniscus. In order to simplify the computation, an average gold content was calculated for the entire volume of the meniscus. Next, it is assumed that the boundary layer developed at the lead surface (which will become the solder coating thickness after withdrawal) is 0.0025cm over the entire length. Therefore, the boundary layer (to be solder coating) removes approximately 0.00019 g of gold from the meniscus formed by the initial immersion. Re-immersion of the lead into the solder bath will cause a mean gold concentration in that meniscus to be 0.5 wt%. Therefore, two immersions *should* be adequate to dilute the gold content so as to produce acceptable joint ductility.

The fact that the two-immersion process did *not* successfully prevent gold from entering the circuit board solder joints suggests that the gold plating which dissolved from the lead during the first immersion, did not fully diffuse away from the boundary layer region. The requirement of *dissolution of the gold electroplating* as part of the first immersion may have caused the poor distribution within the solder meniscus. As a consequence, most of the gold was retained in the solder film and thereby contaminated the meniscus of the second immersion. The second immersion, which involved *melting of the solder coating* , may have better represented the model conditions through a more complete dissolution of gold within the meniscus volume, and became effectively, the "first" immersion step. A greater number of immersions would appear necessary in order to compensate for the ineffectiveness of the first immersion process.

An experiment was conducted in which the leads were exposed to *three* immersions. An SEM image (back scattered electron) and gold map from a representative sample are shown in Fig. 21. Only a few isolated patches of gold are observed; the remaining signal is simply background emissions from the solder. Therefore, it appeared that by providing an additional immersion step, the gold was largely removed from the subsequent hot dipped coating. The second and third immersions, which were characterized by the melting of a contaminated solder film, more closely approximated the dilution process (and gold diffusion across the meniscus) portrayed by the model described above.

SUMMARY

(1) The failure of beam-leaded transistor from surface mount circuit boards after modest thermal cycling was analyzed.
(2) Microstructural analysis of the failed units determined that gold embrittlement was responsible for the loss of solder joint mechanical integrity. The sole source of the gold was the electroplated finish on the leads. The leads were hot solder dipped (twice) in a bath of 63Sn-37Pb solder prior to installation on the board.
(3) Analysis and supporting experiments demonstrated that although the hot dipping procedure was probably effective at removing the gold coating from the lead, the gold remained in the solder meniscus and was subsequently retained by the lead upon withdrawal from the bath, thus allowing the gold to enter the circuit board solder joints.
(4) Considering the volume of the solder meniscus formed on the lead during hot dipping as the actual "solder pot" into which the gold is dissolved, it was determined that increasing the frequency of dips was the effective means of removing gold from the solder coatings (although *theoretically*, the two step immersion should have been adequate). Experimental data later confirmed this hypothesis. Three immersion steps were found adequate to prevent gold contamination of the circuit boards solder joints.

ACKNOWLEDGMENTS

The author wishes to thank Paul Hlava who performed the electron probe microanalysis; Jim Reif for the scanning electron micrographs and energy dispersive x-ray analysis; and Alice Kilgo for the sample metallography.

REFERENCES

[1] "Kovar", "Invar", and "Alloy 52" are registered trademarks of Carpenter Technologies.

[2] Binary Alloy Phase Diagrams. Vol. 1, ed. T. Massalski (ASM, Inter., Materials Park, OH; 1986) p. 316.

[3] F. Foster, "Embrittlement of Solder by Gold from Plated Surfaces", ASTM-STP 319, (1962), p. 13.

[4] M. Bester, "Metallurgical Aspects of Soldering Gold and Gold Plating", Proc. InterNEPCON, (1968), p. 211.

[5] R. Duckett and M. Ackroyd, "The Influence of Solder Composition on the Embrittlement of Soft-Soldered Joints on Gold Coatings", Electroplating and Metal Finishing, May 1976, p. 13.

[6] W. Bader, "Dissolution of Au, Ag, Pt, Cu, and Ni in a Molten Tin-Lead Solder", Welding Jour., Res. Suppl., 48, p. 551s (1969).

[7] P. Vianco, F. Hosking, and J. Rejent, "Solderability Testing of Kovar with 60Sn-40Pb Solder and Organic Fluxes", Welding Jour., Res. Suppl. 69, p. 230s (1990).

[8] A. Mayhew and K. Monger, "Solderability by Meniscometry", Proc. InterNEPCON, 1972, p. 53.

[9] M. Karnowsky and A. Rosenzweig, "The Gold-Tin-Lead Alloys- The Gold-Tin-Lead System", Trans. AIME 242, (1968) p. 2257.

[10] R. Daugherty and J. Franzini, Fluid Mechanics with Engineering Applications, (McGraw-Hill, New York, NY; 1977) pp. 282-284.

[11] G. Carter, Principles of Physical and Chemical Metallurgy, (ASM, Metals Park, OH; 1979), p. 102.

Figure Captions

Fig. 1 Izod impact toughness of tin-lead solder as a function of gold content[4].

Fig. 2 (a) Schematic diagram and (b) photograph of the beam-lead transistor that is the subject of this case study.

Fig. 3 Optical micrographs of (a) the transistor in place on the circuit board and (b) a similar area from which a transistor had fallen from the substrate.

Fig. 4 Scanning electron micrograph (secondary emission) of the emitter lead bonding pad from a failed transistor solder joint.

Fig. 5 Scanning electron micrographs (secondary emission) of a failed lead at two magnifications. A thin, uniform solder layer remained on the lead surfaces.

Fig. 6 Schematic diagram depicting the geometrical relationships between the lost lead and the bonding pad.

Fig. 7 Scanning electron image (a) secondary emission and (b) backscattered emission of the fillet area of a failed solder joint.

Fig. 8 (a) Scanning electron micrograph of the collector lead bonding pad of a lost transistor. (b) Energy dispersive x-ray analysis (EDXA) spectrum of the bonding pad fracture surface. (c) EDXA spectrum of the complimentary fracture surface on the transistor lead.

Fig. 9 Optical micrograph of the longitudinal cross sections of a lead hot solder dipped by the process outlined in the text.

Fig. 10 (a) SEM backscattered electron image of a segment of solder interface from the lead in Fig. 9 that was hot solder dipped by standard practice. (b) The gold x-ray dot map of the region shown in (a).

Fig. 11 (a) SEM backscattered electron image of a segment of solder interface from a second lead that was hot solder dipped by the standard practice. (b) The gold x-ray dot map of the region shown in (a).

Fig. 12 Dissolution rate of metal wires (change in wire radius) in molten 63Sn-37Pb solder (Ref. 6).

Fig. 13 (a) SEM backscattered electron image of the surface of the solder coating of the solder lead hot solder dipped per the standard procedure except that the time interval was increased to 4 sec. (b) Gold x-ray dot map of the same region in (a).

Fig. 14 Scale diagram of the solder meniscus which forms on the transistor lead by immersion into the molten solder during the hot dipping process. The form of the meniscus is shown for the 1.5 mm length of the lead closest to the transistor body which is used on the circuit board solder joint.

Fig. 15 Computed gold concentrations in the solder meniscus formed on the transistor lead immersed into the solder. The gold thickness was assumed to be 4.1 μm (160 microin.)

Fig. 16 Schematic diagram of the two sessile drop configurations obtained from tin-lead solder on gold-nickel-plated Kovar™ coupon: (a) lenticular geometry and (b) bulbous geometry.

Fig. 17 (a) Electron probe micro-analysis (EMPA) gold concentration trace along the solder-substrate interface (5 μm distant) of the lenticular sessile drop geometry (Fig. 16a). (b) The EMPA gold trace for the bulbous sessile drop geometry (Fig. 16b).

Fig. 18 Pseudo-phase diagram of gold/63Sn-37Pb couple for a gold concentration of up to 20wt%.

Fig. 19 Boundary layer development of a fluid layer moving past a stationary substrate. Point "A" is the origin of the x-coordinate along the length of the lead; the y-coordinate is the distance away from the lead surface with its origin at the lead surface. u(x,y) coordinate-dependent velocity and U, the far-field (uniform) velocity.

Fig. 20 Schematic drawing (to scale) of the boundary layer of fluid developed near the lead surface upon its withdrawal from the solder bath.

Fig. 21 SEM (backscattered electron) and gold dot map of solder film on a transistor lead immersed three times in a solder bath held at 255°C.

Table Titles

Table 1 Summary of Gold Content Calculation for Hot Solder Dipped Coatings on the Transistor Leads.

Table 2 Gold Concentration by Electron Microprobe Analysis versus Immersion Time.

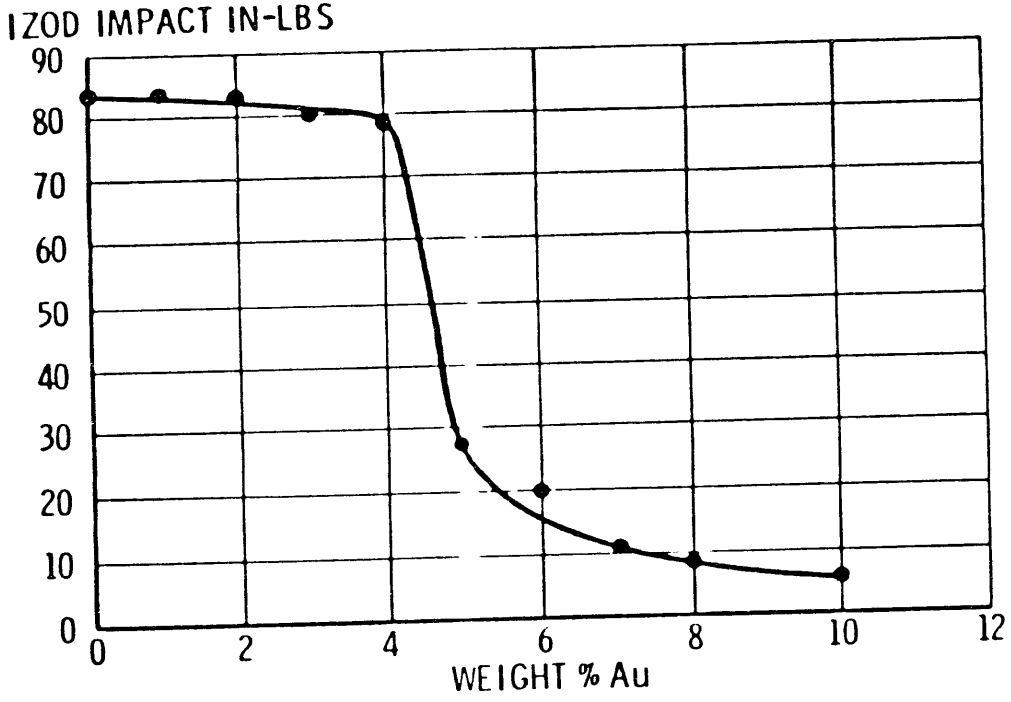
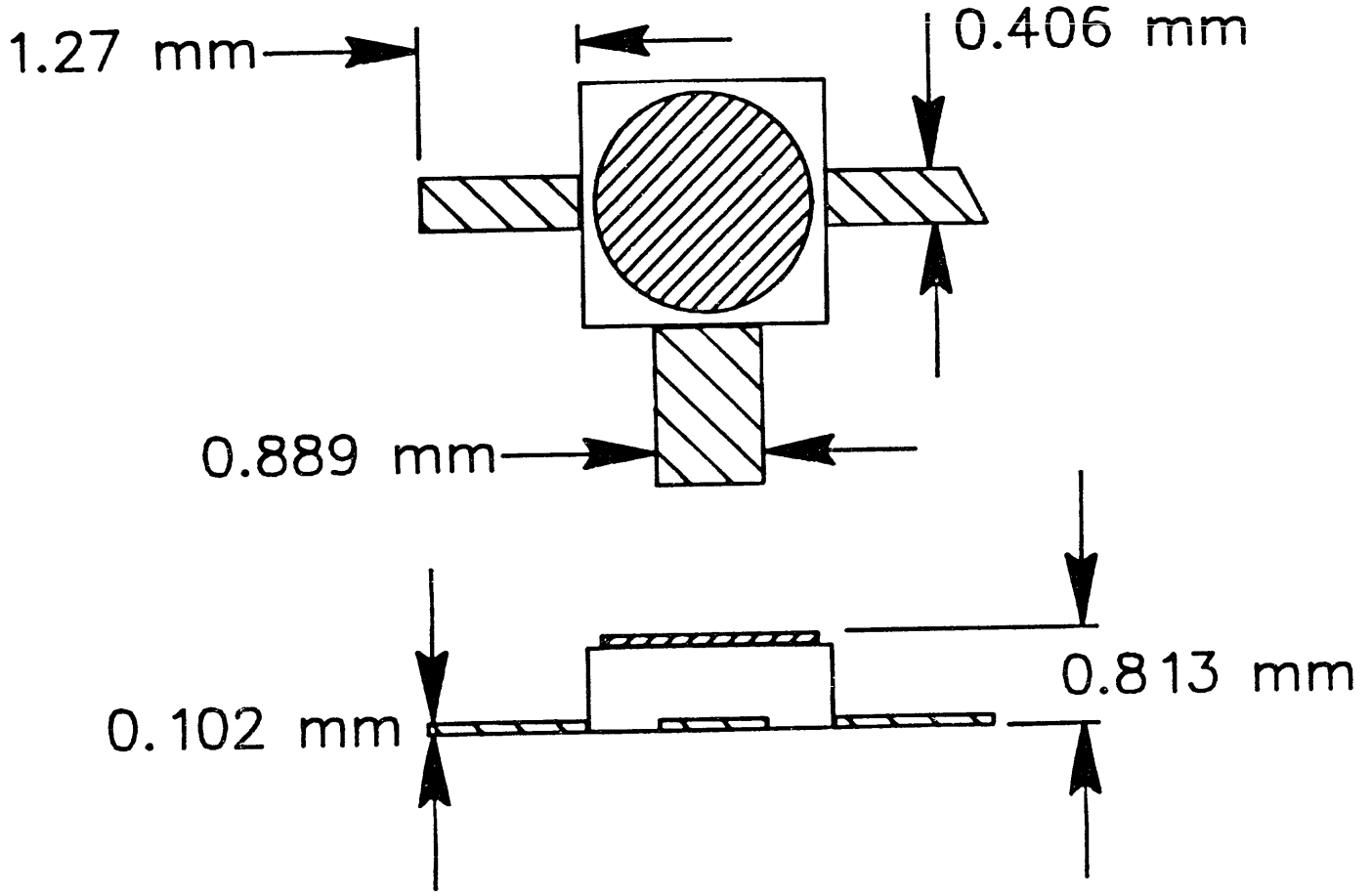
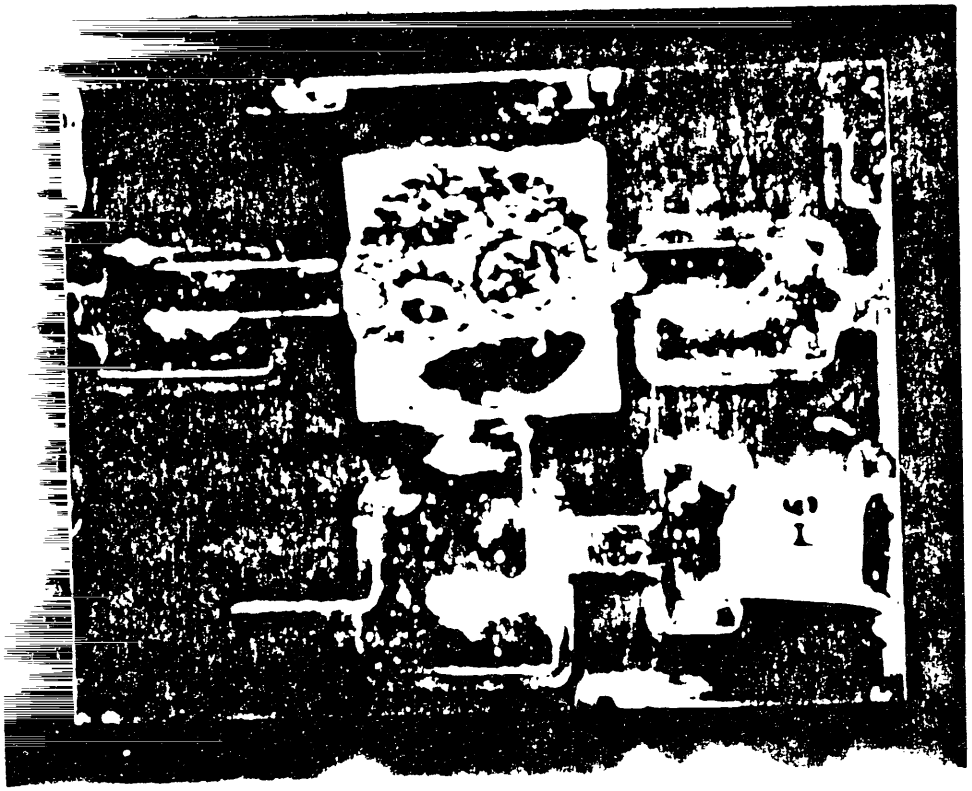

IZOD IMPACT IN-LBS
90
80
70
60
50
40
30
20
10
0
0
2
4
6
8
10
12
WEIGHT % Au

Fig. 1



sm193a_1

FIG. 2b



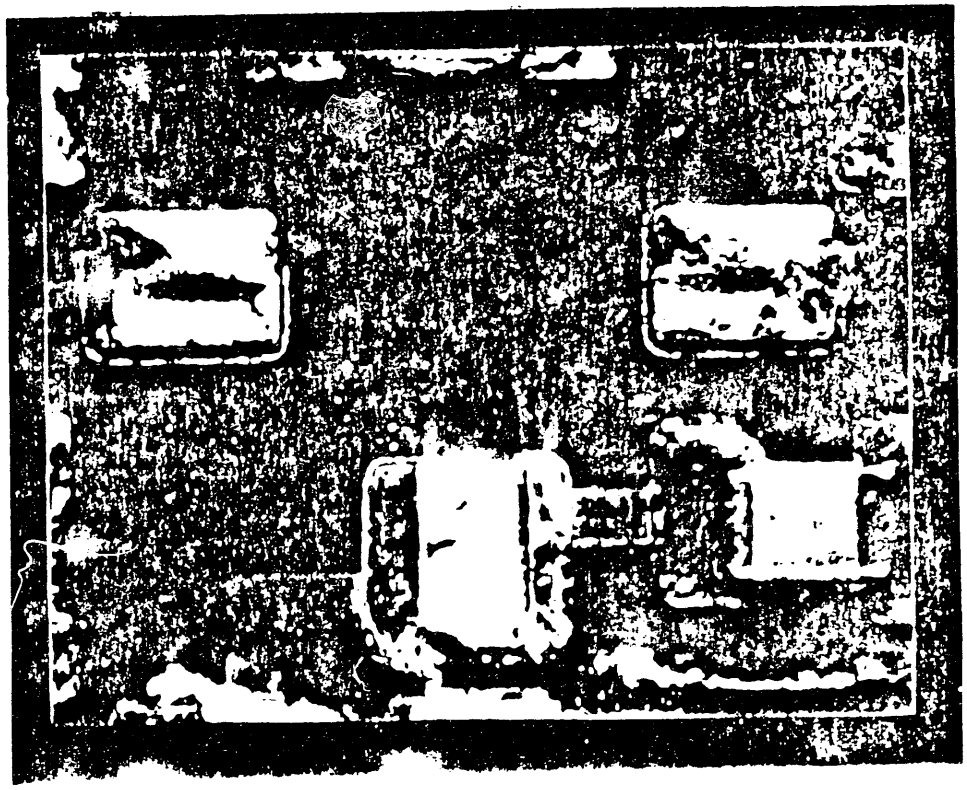
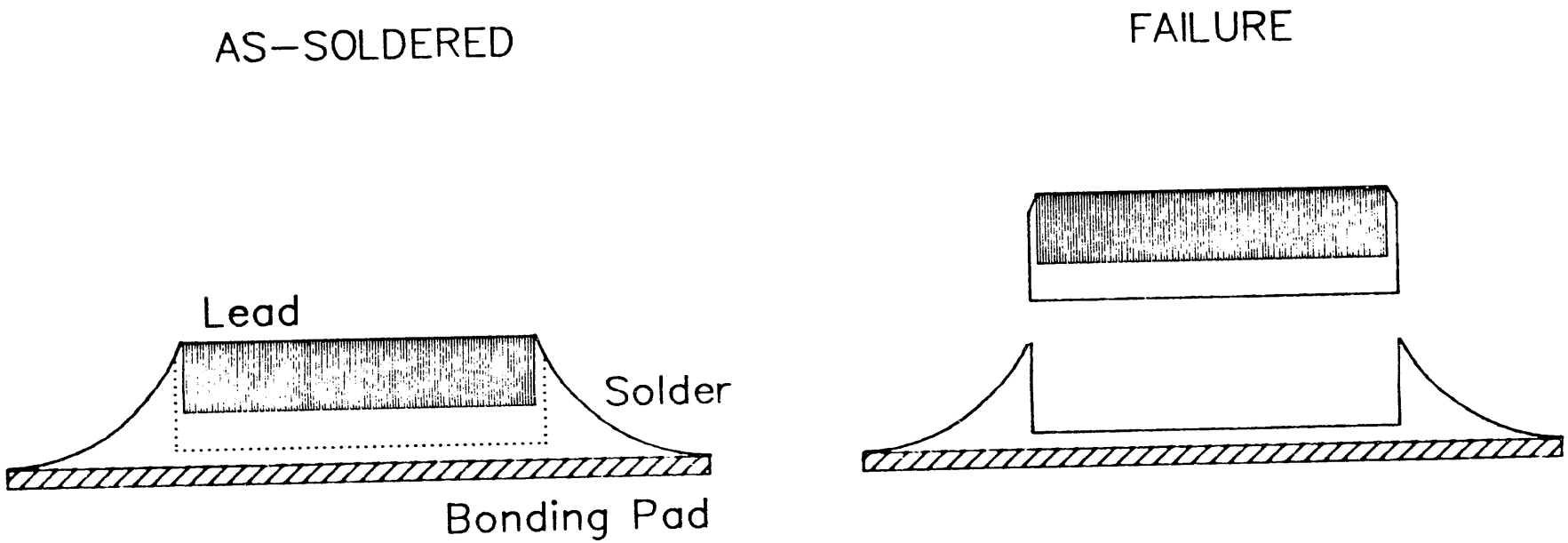


Fig. 2

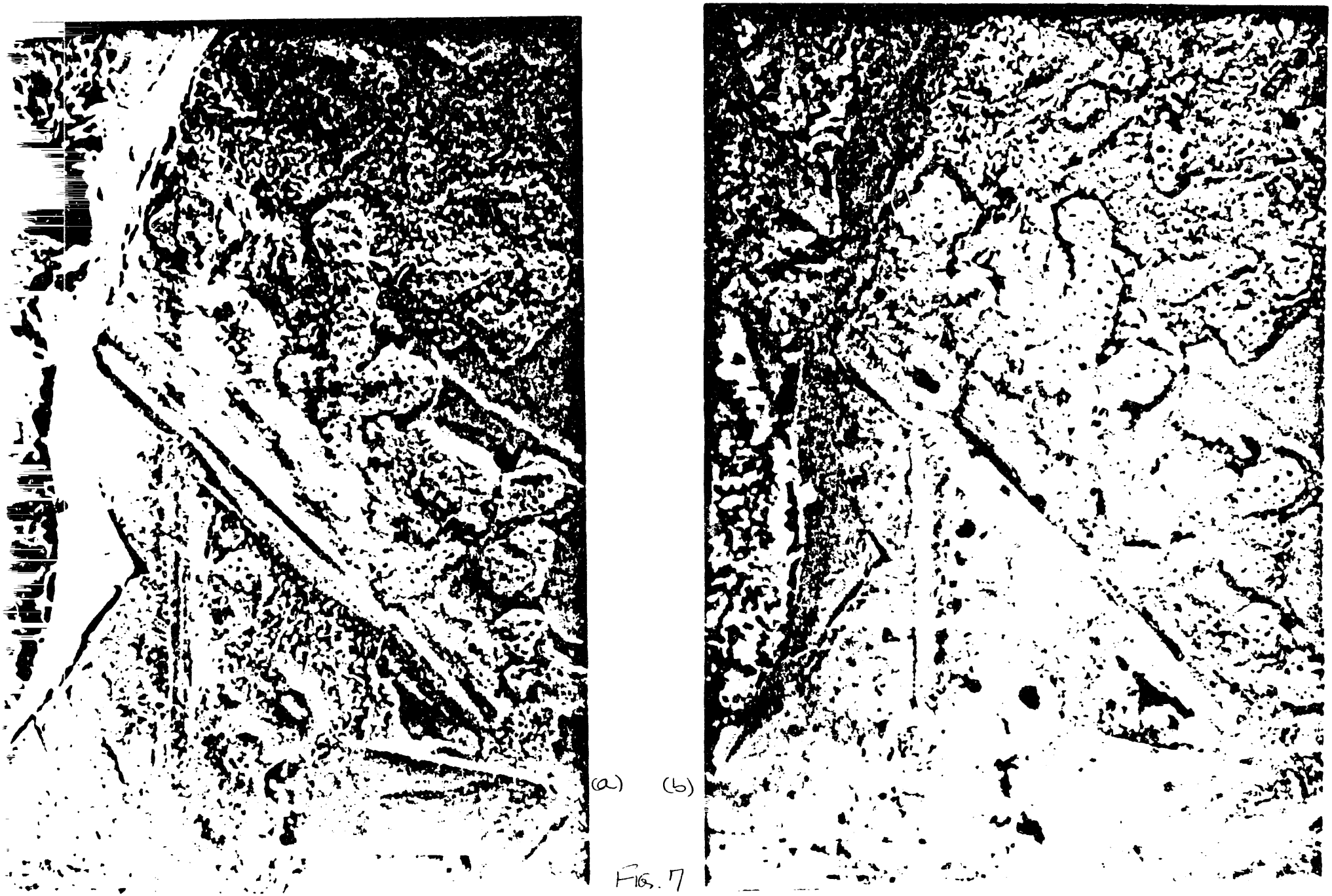
FIG. 4

FIG. 5



Failure Geometry of the Q1 and Q2 Transistor Leads

Fig. 6



(a) (b)

Fig. 7

POLY PG. 5x7
prinz STOCK # 210-81

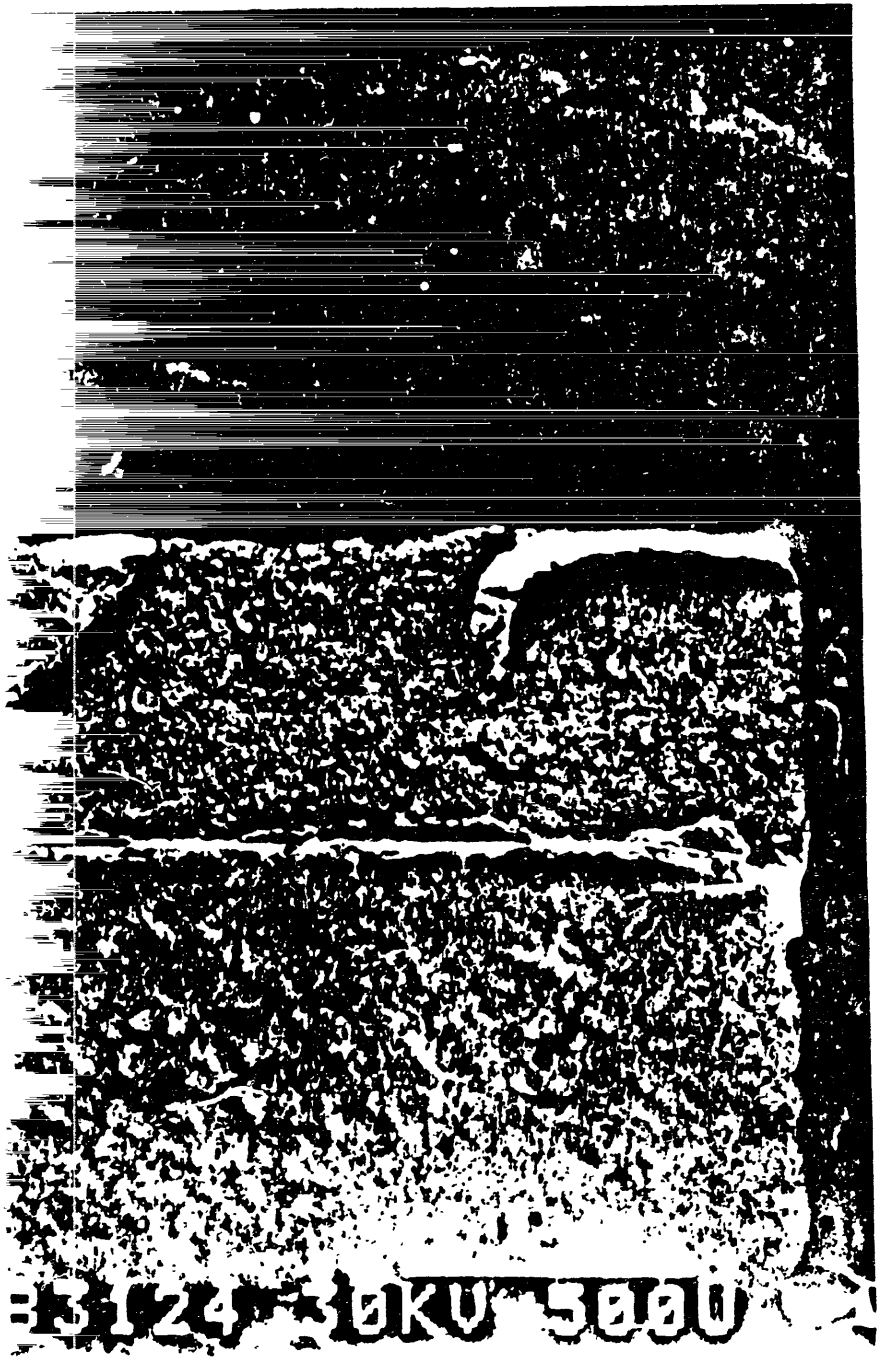
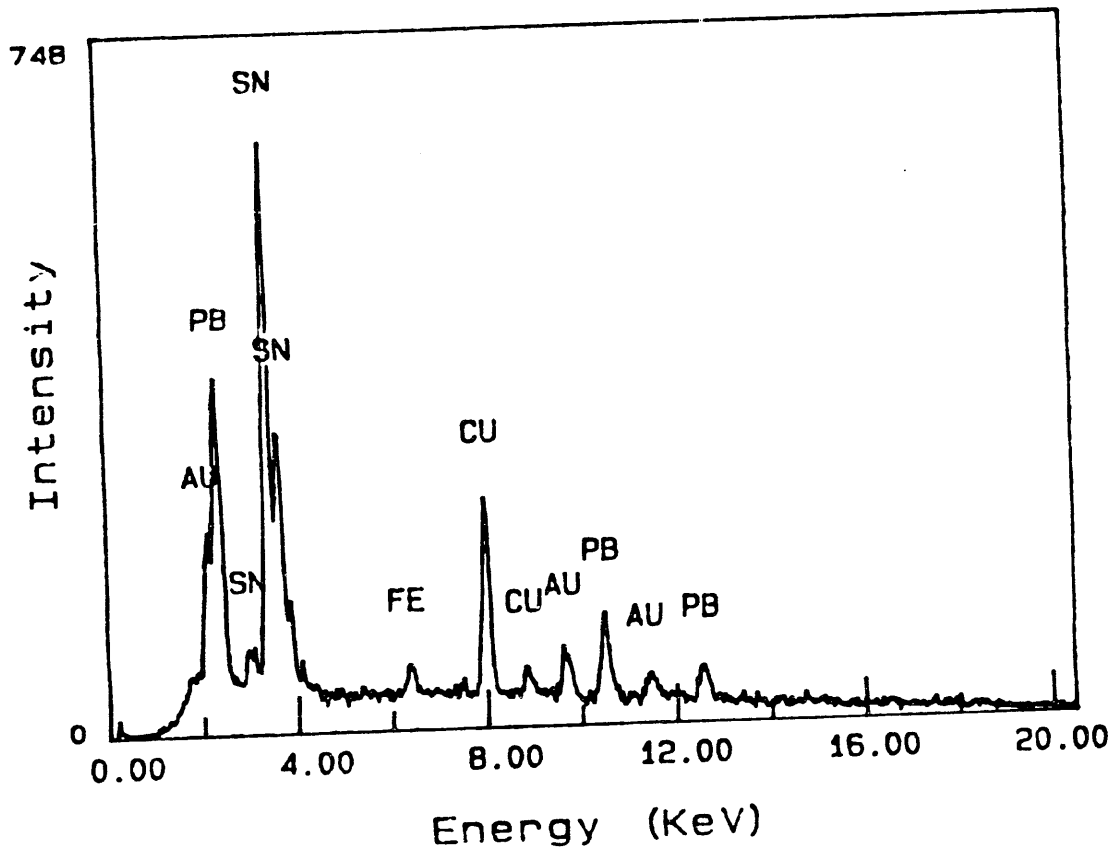
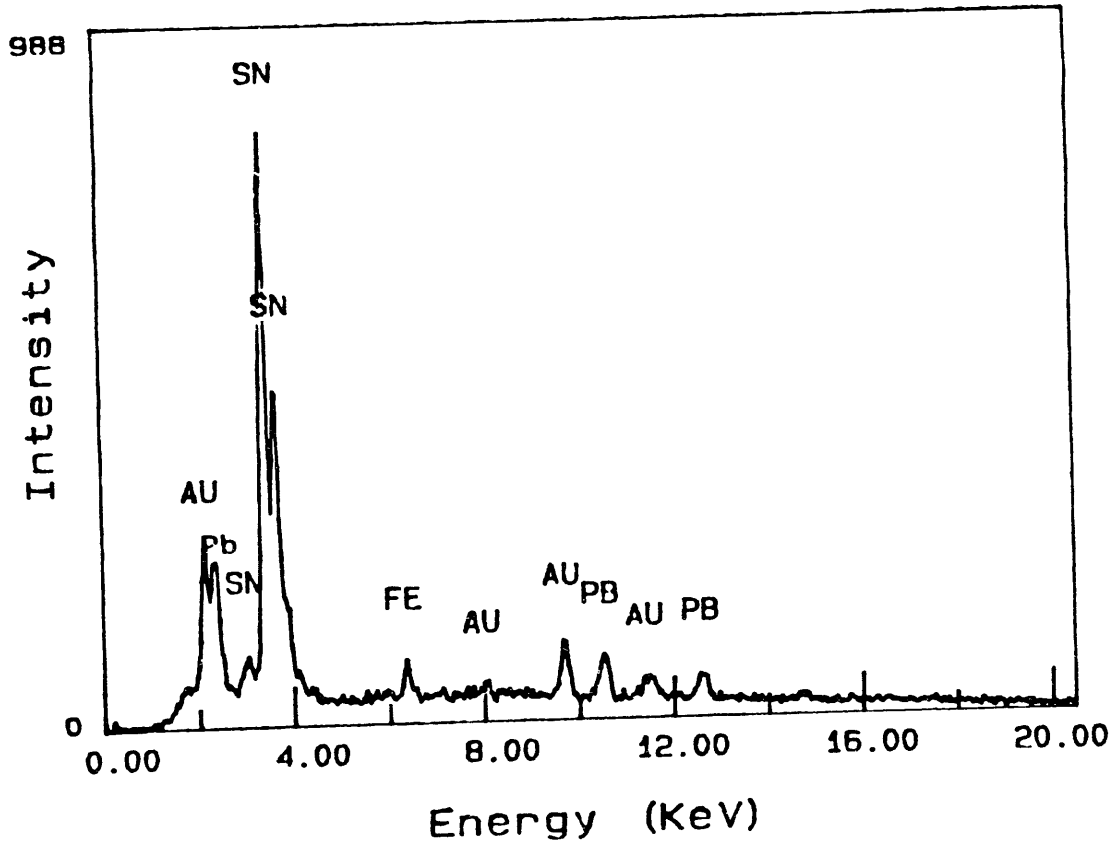


Fig. 9a


748
SN
PB
SN
AU
SN
CU
FE
CU
AU
PB
AU
PB
Intensity
0
0.00
4.00
8.00
12.00
16.00
20.00
Energy (KeV)

(b)

FIGURE 8


988
SN
SN
AU
Pb
SN
FE
AU
AU PB
AU PB
0
Intensity
0.00
4.00
8.00
12.00
16.00
20.00
Energy (KeV)

(c)

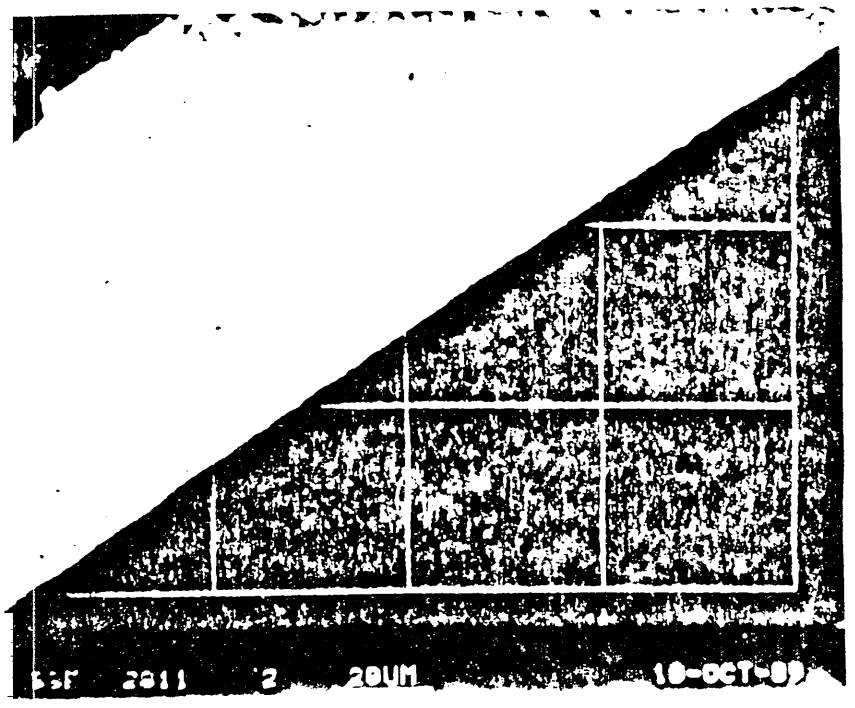
FIGURE 8

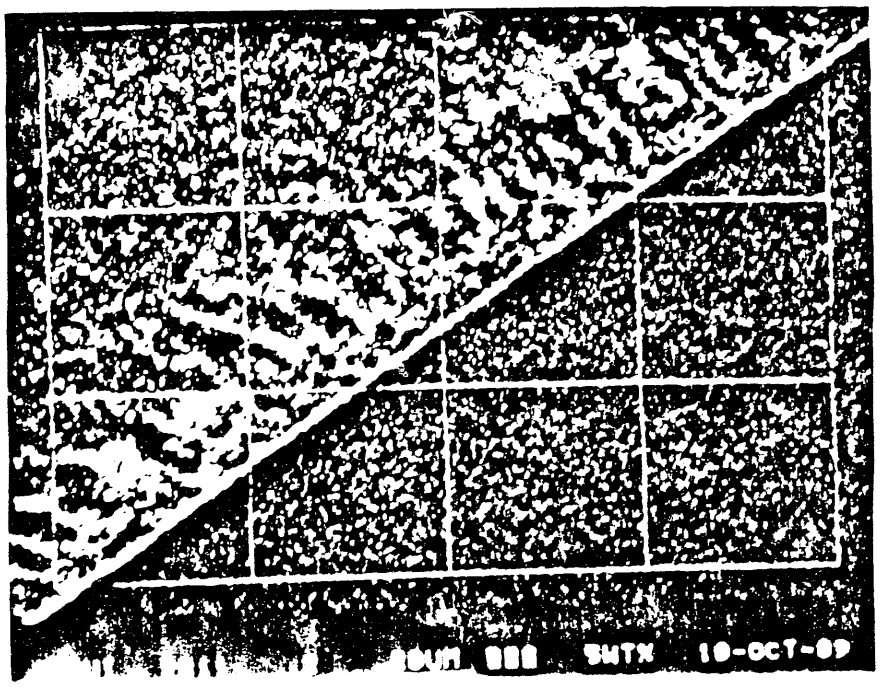
Fig. 9A

(a)

FIG 10

(b)


2811 2 20UM 10-OCT-89


SMTX 10-OCT-89

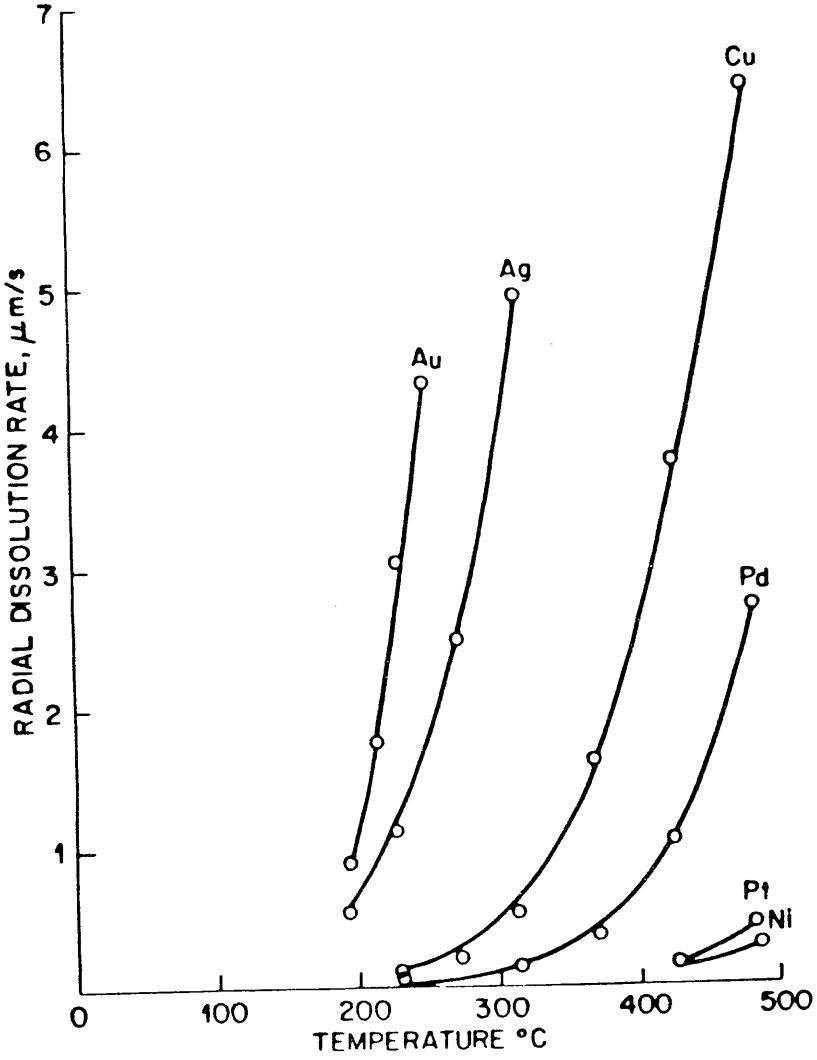
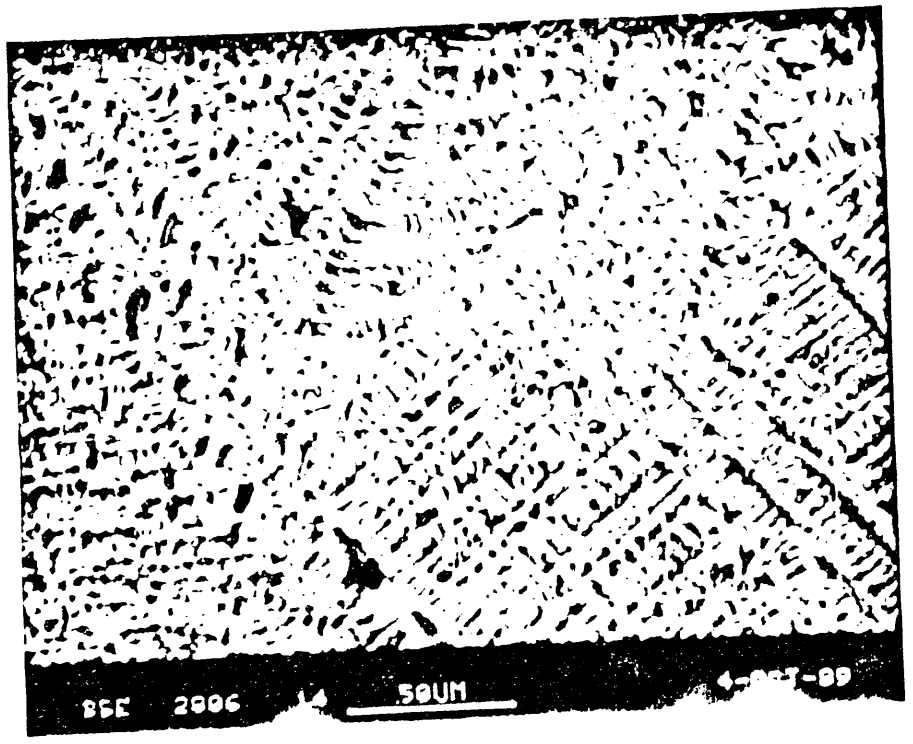

RADIAL DISSOLUTION RATE, μm/s
TEMPERATURE °C
0
100
200
300
400
500
1
2
3
4
5
6
7
Cu
Ag
Au
Pd
Pt
Ni

FIG. 12



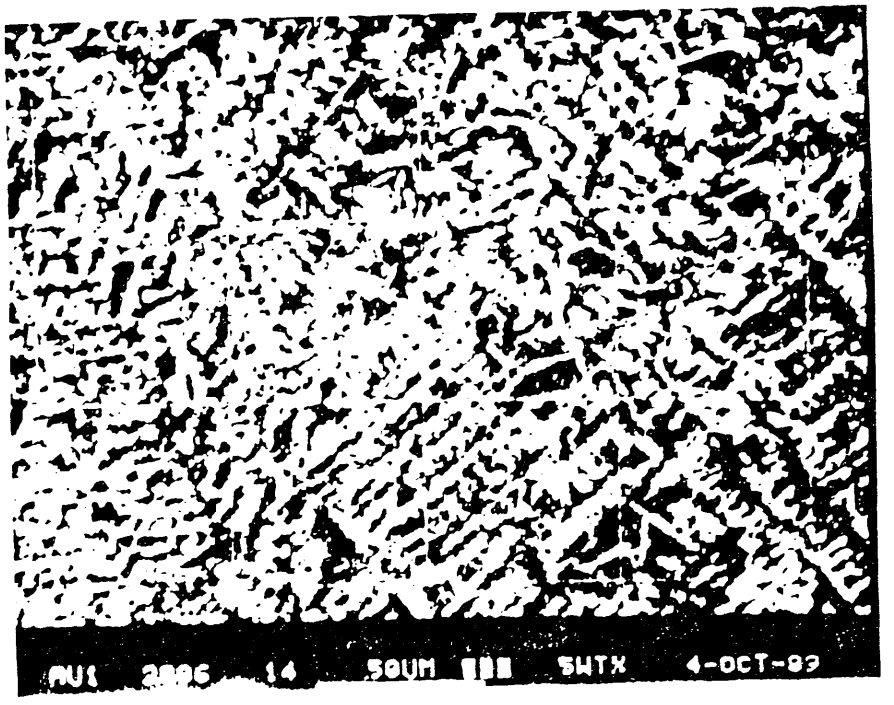
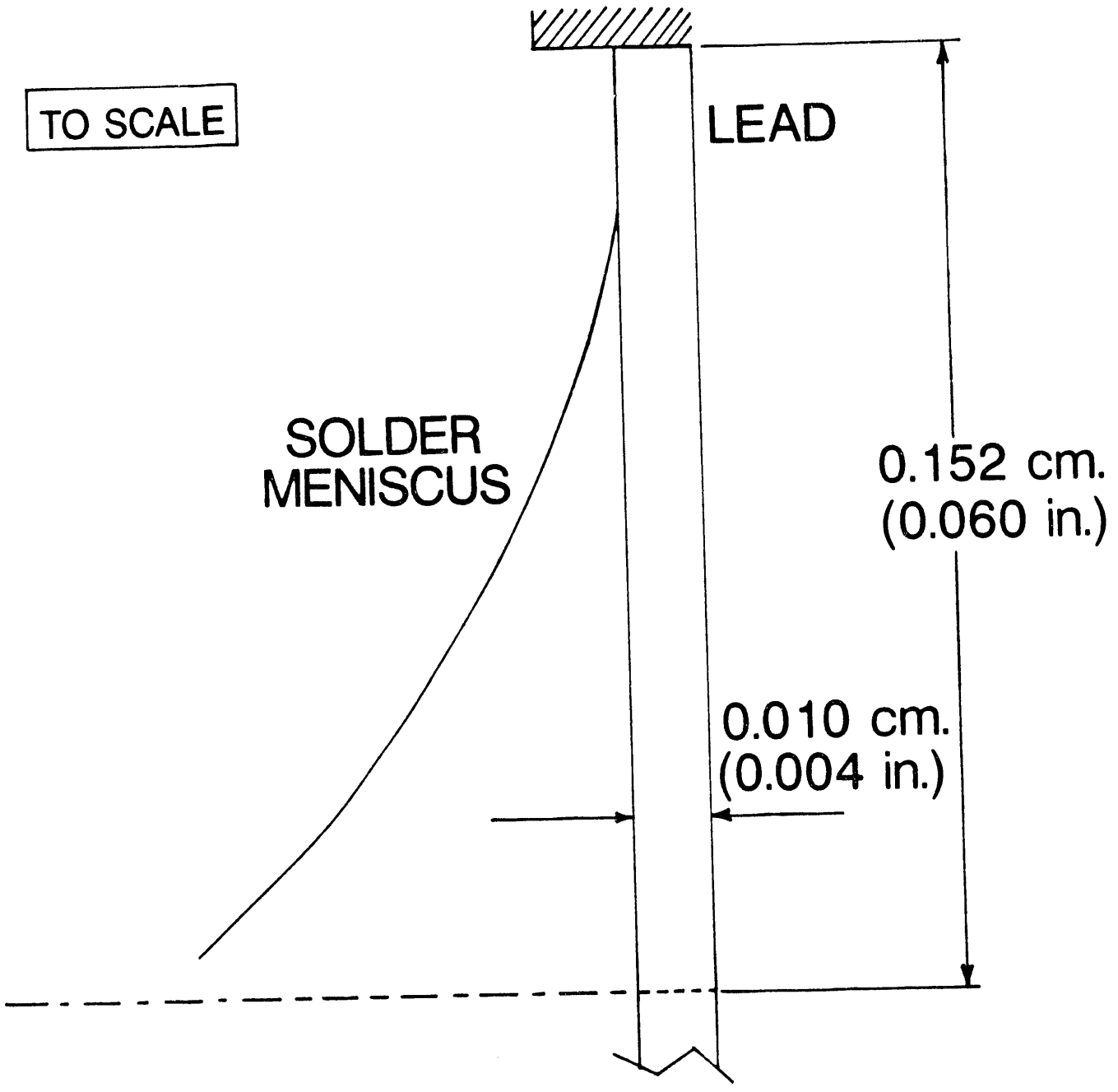


FIG. 13


TO SCALE
LEAD
SOLDER
MENISCUS
0.152 cm.
(0.060 in.)
0.010 cm.
(0.004 in.)

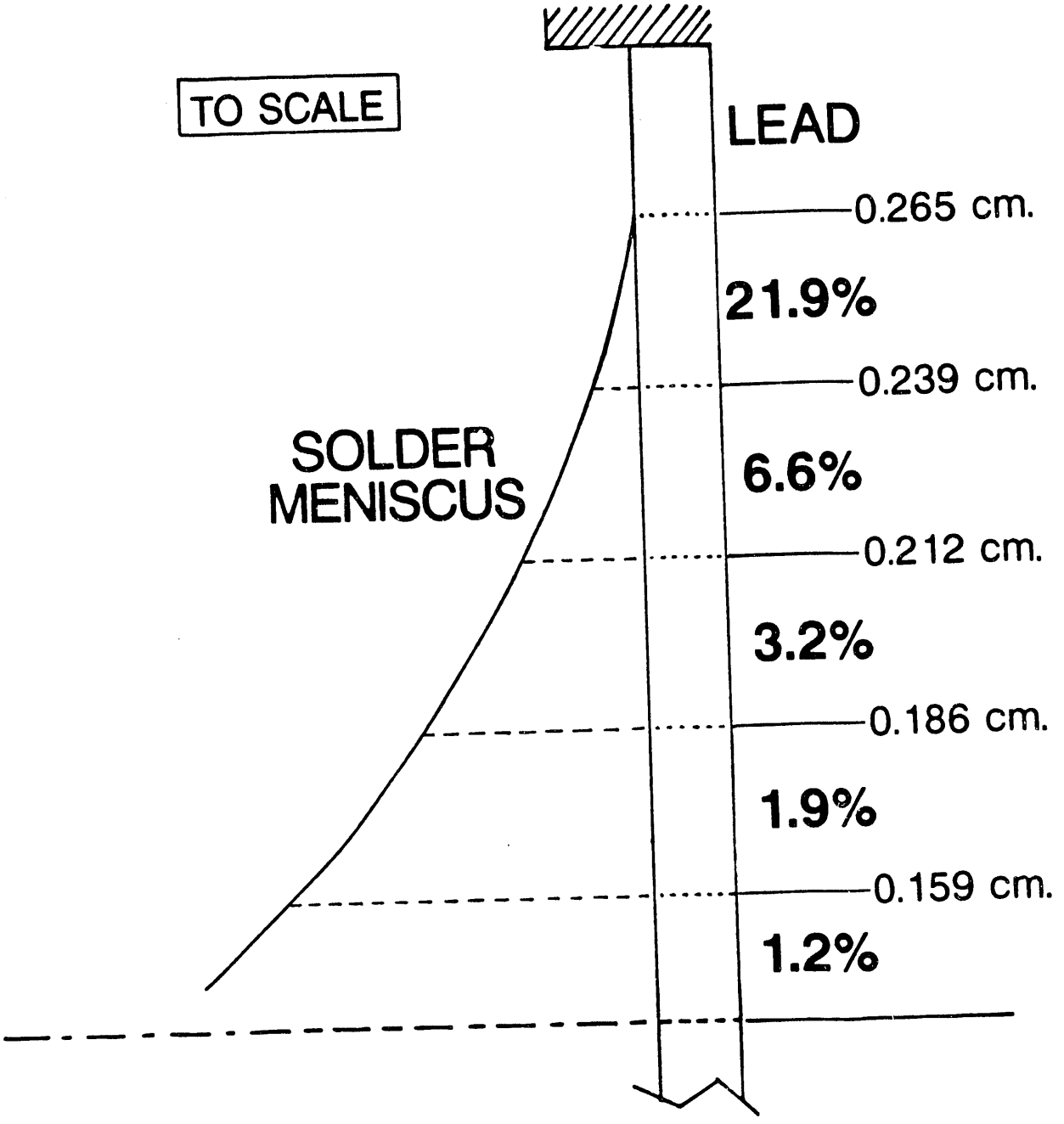
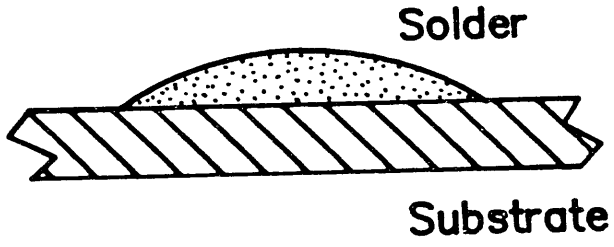
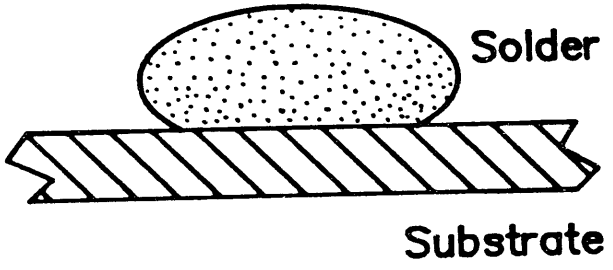

TO SCALE
LEAD
0.265 cm.
21.9%
0.239 cm.
SOLDER
MENISCUS
6.6%
0.212 cm.
3.2%
0.186 cm.
1.9%
0.159 cm.
1.2%

FIG. 15



(a)



(b)

sms93A_2

FIG. 16

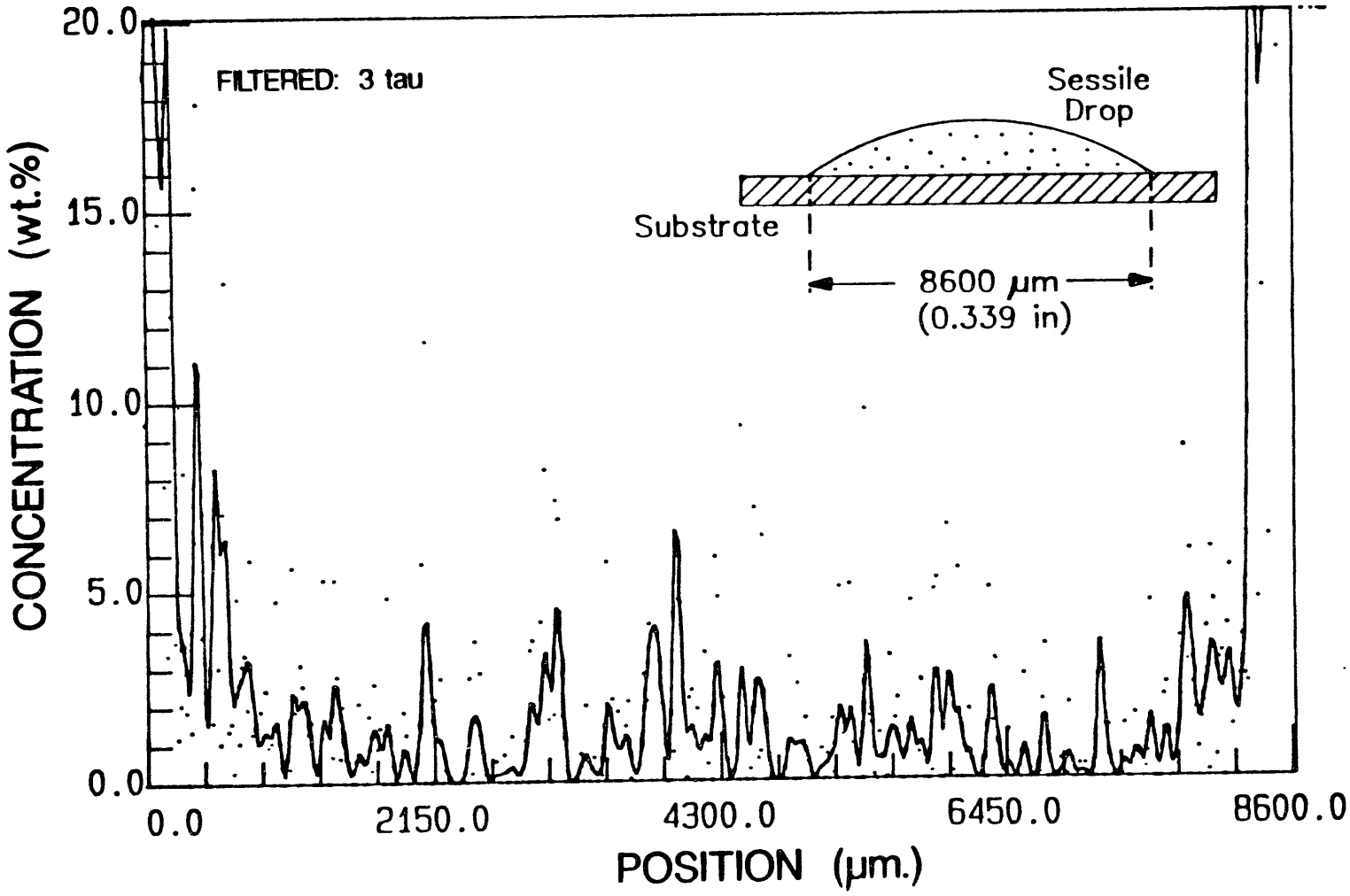

FILTERED: 3 tau
Sessile
Drop
Substrate
8600 μm
(0.339 in)
CONCENTRATION (wt.%)
20.0
15.0
10.0
5.0
0.0
0.0
2150.0
4300.0
6450.0
8600.0
POSITION (μm.)

FIG. 17.c

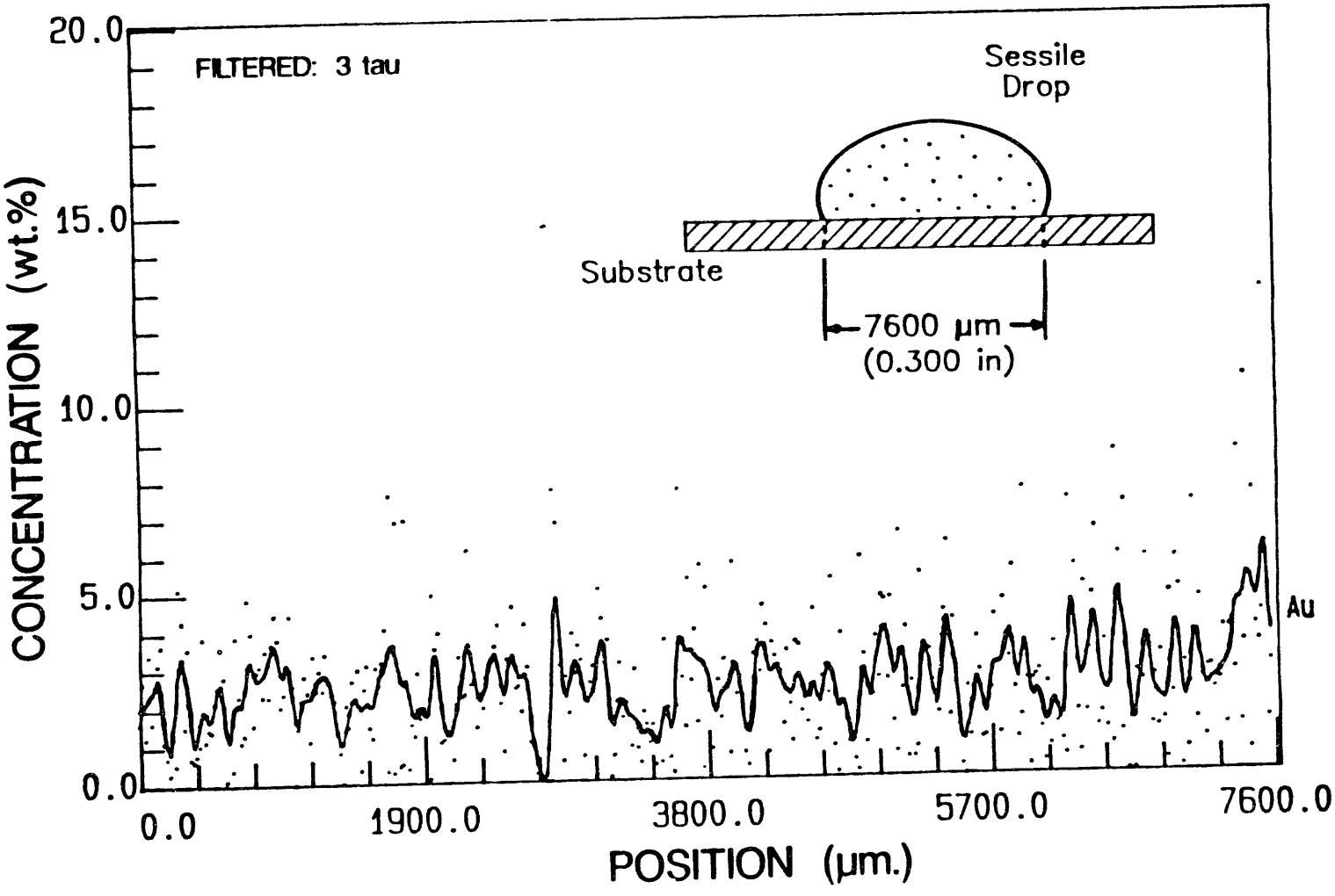
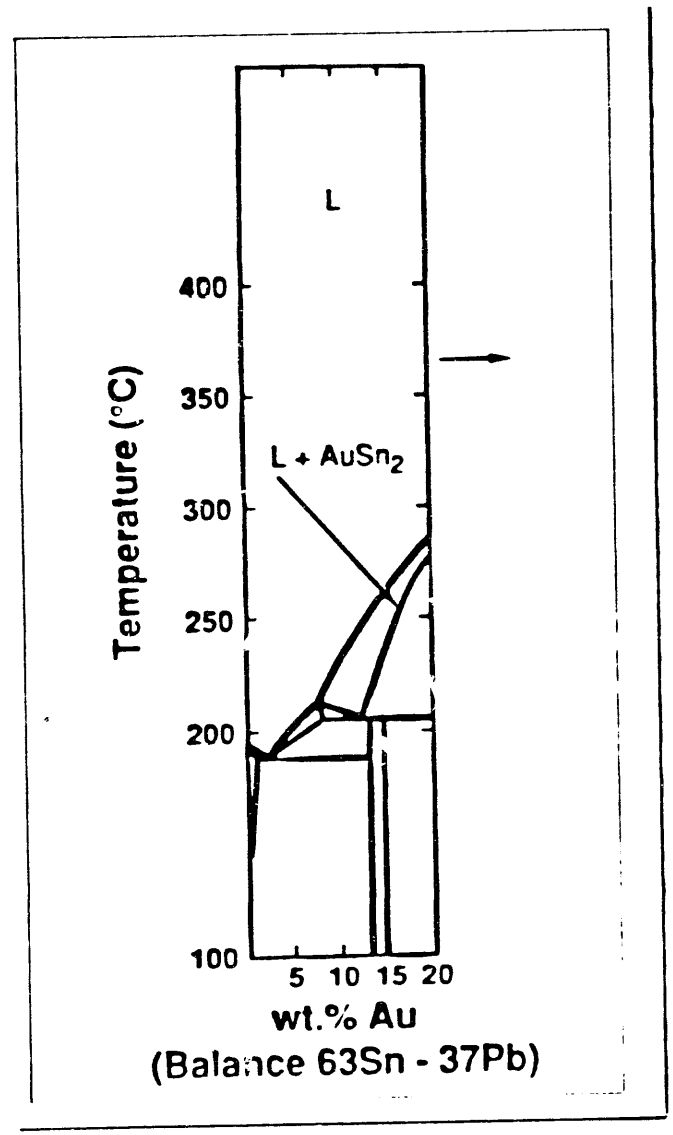
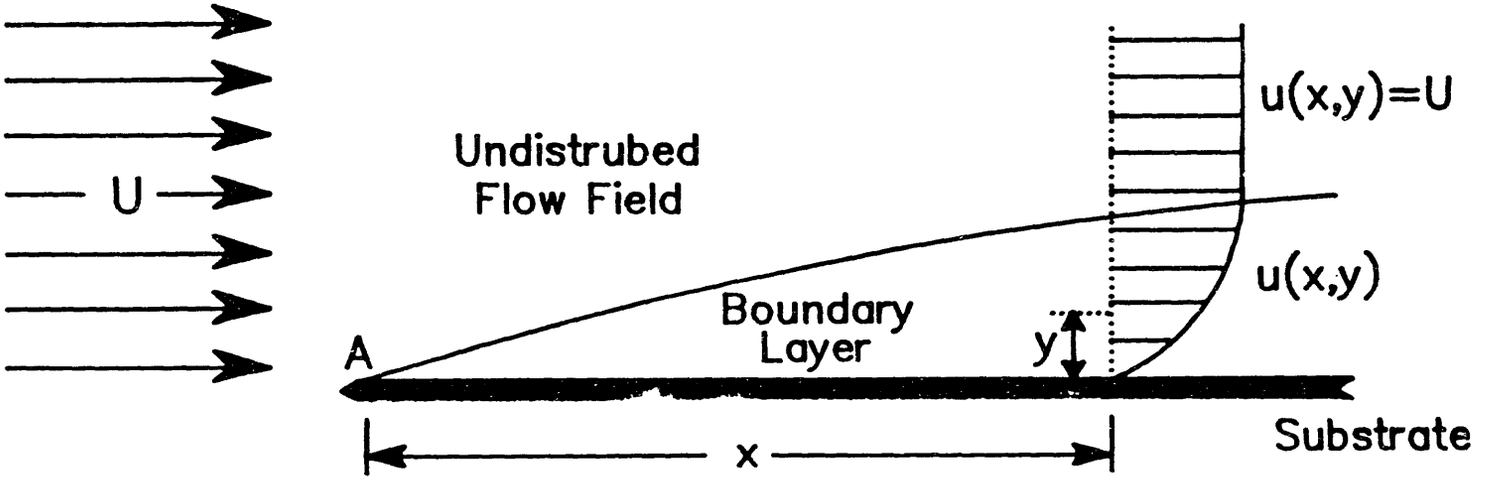

FILTERED: 3 tau
Sessile
Drop
Substrate
7600 µm
(0.300 in)
20.0
15.0
10.0
5.0
0.0
CONCENTRATION (wt.%)
Au
0.0
1900.0
3800.0
5700.0
7600.0
POSITION (µm.)

Fig. 17b



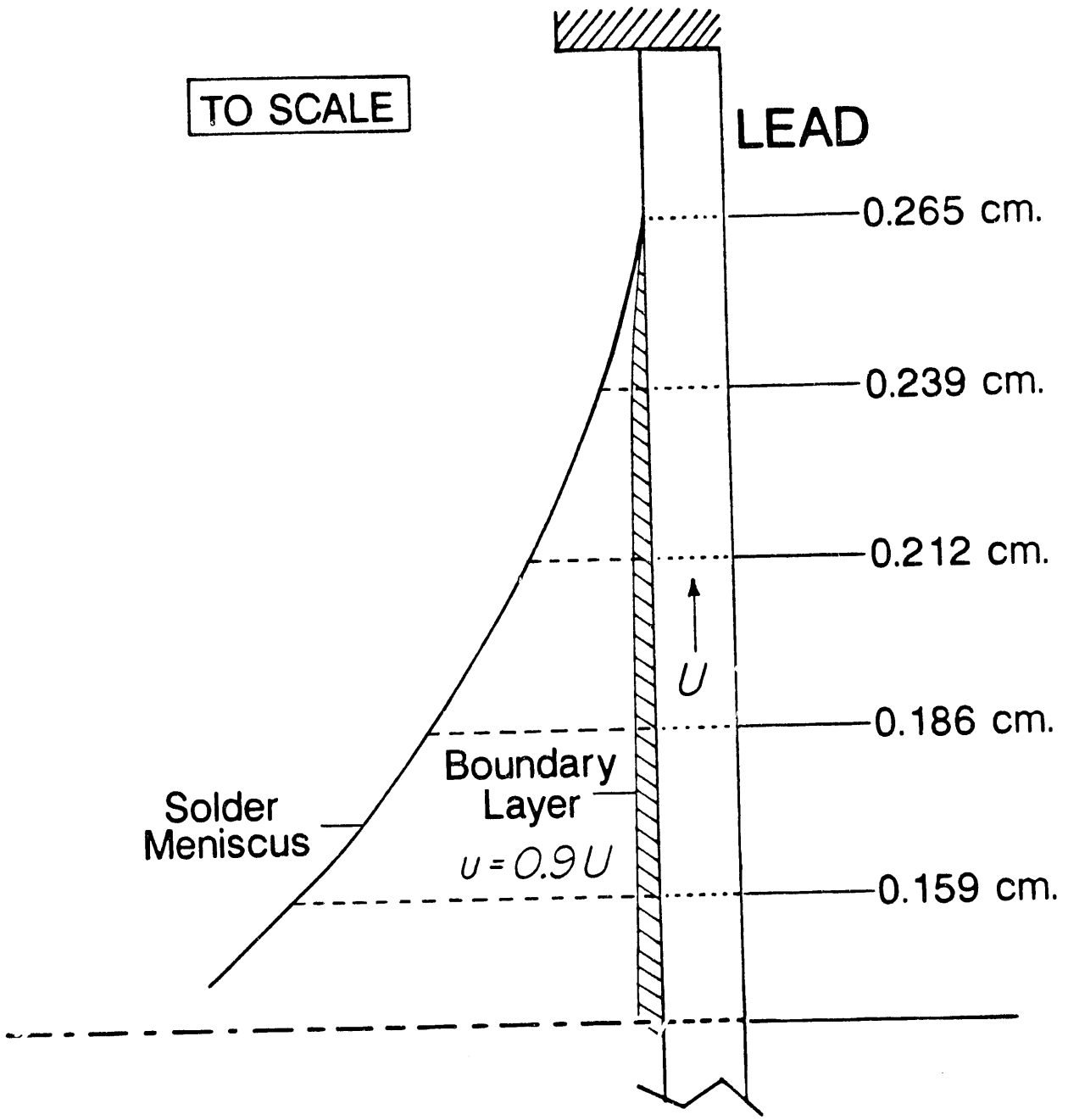
aws9.1b.19

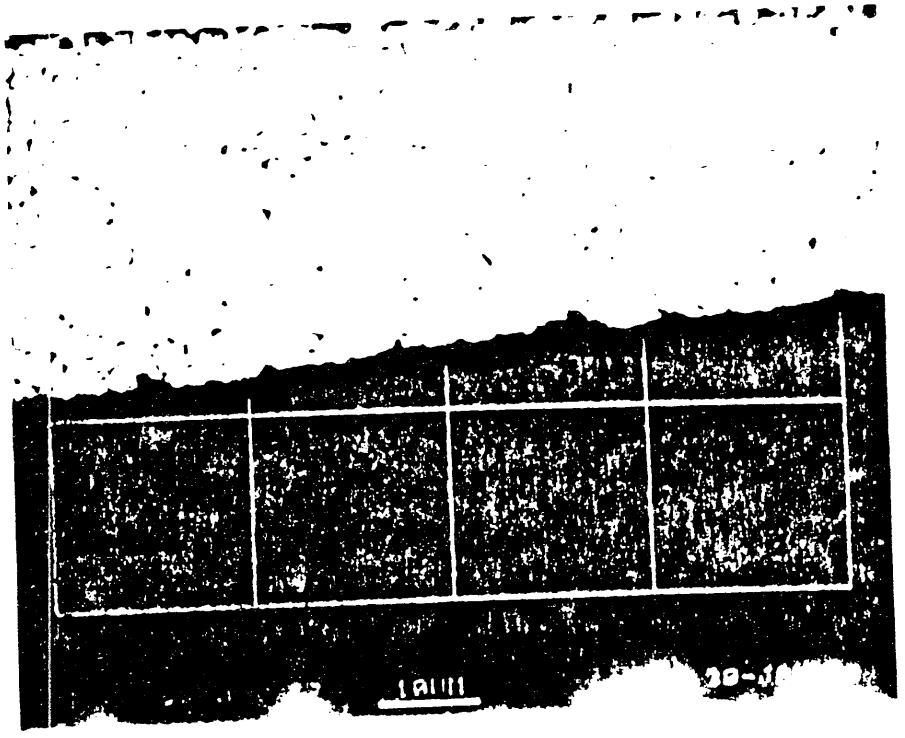
Fig IV

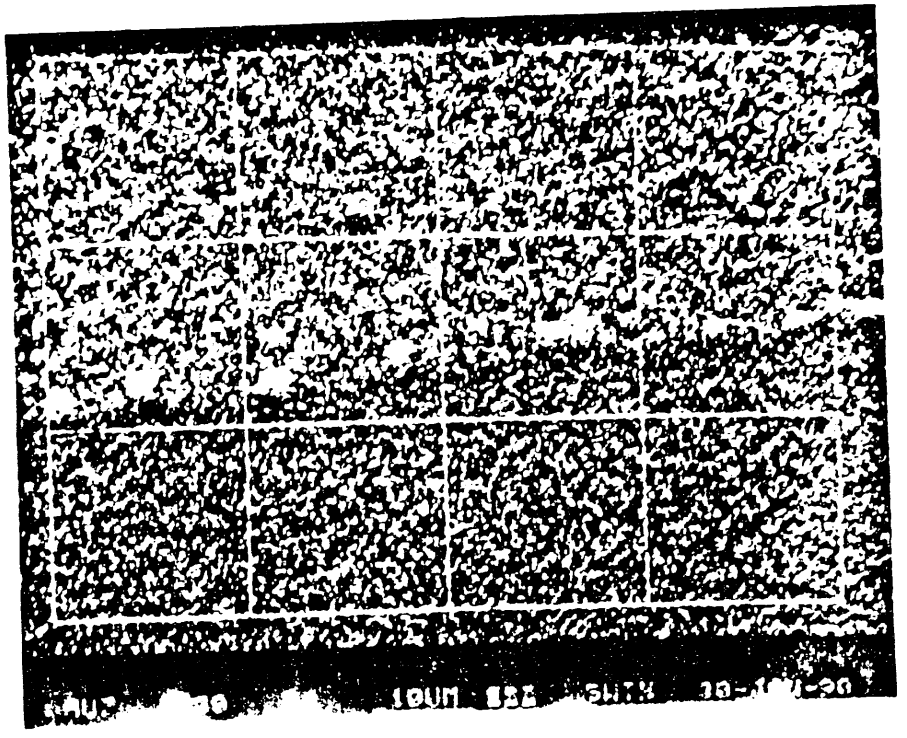


sm93a_3

FIG. 19


TO SCALE
LEAD
0.265 cm.
0.239 cm.
0.212 cm.
U
0.186 cm.
Boundary
Layer
u = 0.9 U
Solder
Meniscus
0.159 cm.


10um


10UM

Lead	Thickness (in.)	Width (in.)	Footprint[1] Length (in.)	Weight Gold ($\times 10^{-7}$ lb.)	Weight[2] Solder ($\times 10^{-7}$ lb.)	wt.%[3] Gold (%)
collector	0.004	0.020	0.050	2.69	60.6	4.3
emitter	0.004	0.039	0.059	5.68	103	5.2
base	0.004	0.020	0.054	2.91	59.5	4.7

(1) Length of the lead on the bonding pad.

(2) Bonding pad solder plus the pretinning solder layer.

(3) $$\frac{\text{mass (Au)}}{\text{mass (Au) + mass (solder)}} \times 100$$

Table 1

Depencence of Transistor Lead Gold Content on Pretinning Time

Lead	Immersion Time (sec.)	Gold Conc. (wt.%)
1	1	3.6±1.9
2	2	5.4±1.7
3	3	2.9±2.6
4	4	2.1±1.6

DATE
FILMED
9/14/93
END