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Title: CHARACTERIZATION OF MULTIPORT SOLID STATE IMAGERS AT MEGAHERTZ DATA RATES

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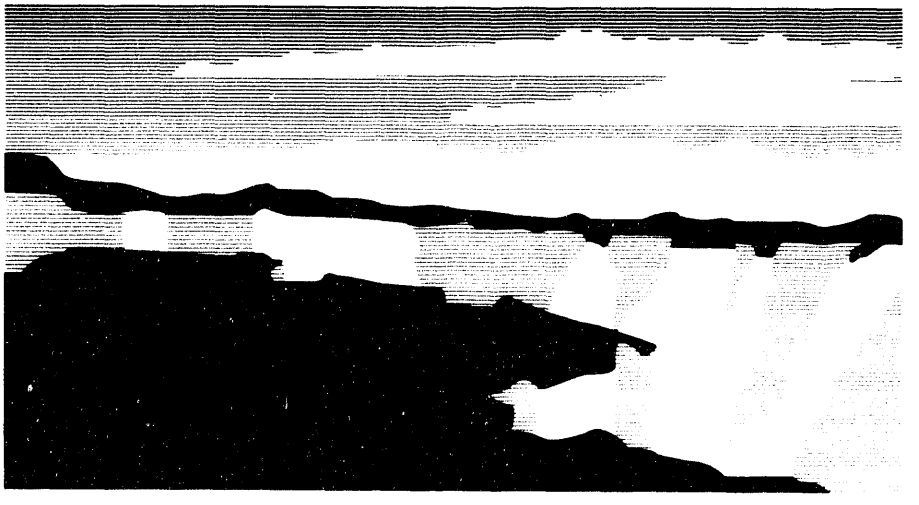

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Characterization of multiport solid state imagers at megahertz data rates

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ABSTRACT

Test results obtained from two recently developed multiport Charge-Coupled Devices (CCDs) operated at pixel rates in the 10-to-100 MHz range will be presented. The CCDs were evaluated in Los Alamos National Laboratory's High Speed Solid State Imager Test Station (HSTS) which features PC-based programmable clock waveform generation (Tektronix DAS 9200) and synchronously clocked Digital Sampling Oscilloscopes (DSOs) (LeCroy 9424/9314 series) for CCD pixel data acquisition, analysis, and storage. The HSTS also provided special designed optical pinhole array test patterns in the 5-to-50 micron diameter range for use with Xenon Strobe and pulsed laser light sources to simultaneously provide multiple single-pixel illumination patterns to study CCD point-spread-function (PSF) and pixel smear characteristics. The two CCDs tested, EEV model CCD-13 and EG&G Reticon model HSO512J are both 512x512 pixel arrays with eight (8) and sixteen (16) video output ports respectively. Both devices are generically Frame Transfer CCDs (FT CCDs) designed for parallel bi-directional vertical readout to augment their multiport design for increased pixel rates over common single port serial readout architecture. Although both CCDs were tested similarly, differences in their designs precluded normalization or any direct comparisons of test results. Rate dependent parameters investigated include S/N, PSF, and MTF. The performance observed for the two imagers at various pixel rates from selected typical output ports is discussed.

Keywords: Solid State Imager Test Station ((HSTS), Multiport Imagers, Pixel Rate effects.

INTRODUCTION

Los Alamos National Laboratory has designed and implemented a High Speed Solid State Imager Test Facility (HSTS) which has been used to characterize a number of newly developed imagers. The HSTS is a PC/work station-based optical stimulus system for operating and testing Focal Plane Arrays (FPAs) at variable pixel, line, and frame rates to identify rate effects for imagers designed specifically for high speed readout. Data were also taken using a programmable logic system at Lawrence Berkeley Laboratory. Modern state-of-the-art FPA designs gain speed by parallel readout of segments of the array using multiple output video ports. In this paper we report on two such FPAs, the EEV CCD-13 Full Frame Transfer 8-port CCD and the Reticon Frame Transfer 16-port CCD.

1. TEST STATION (HSTS)

The complete HSTS, described in detail elsewhere[1,2,3], is comprised of several major components or sections. In fig. 1. an engineer is shown using the Tektronix 9200 DAS programmable waveform generator to write binary codes to implement the required clock waveforms for the EEV-CCD-13 and Reticon HS0512J CCDs. Distribution of these waveforms to the actual CCD clock lines requires proper phase alignment to study overlap effects among horizontal and vertical phases. Internal phase adjustments from the DAS are augmented by selectable high bandwidth passive delay lines as shown in fig. 2 and 3. The distribution design of, routes DAS waveforms to the CCD under test, and fans the signal to the DAS logic acquisition probes for software simulation of waveforms derived from binary code. The distribution also allows high impedance monitoring of the waveforms, delayed and undelayed, to examine and adjust phasing.

The printed circuit carrier cards for the CCD under test are mounted in an X,Y,Z tracking platform (fig. 4.) for alignment of the array with precision optical pinhole patterns in the TVO Optoliner Optical relay system. The tracking platform, Polytec PI Model M-353 is controlled by an IBM PC and allows one-inch travel in all three axis with sub-micron resolution and repeatability. The software allows the user to generate a matrix of X,Y coordinates for registration or assignment of a given pixel to a pair of coordinates. In this way, a pixel map can be stored in the PC and individual pixels can be interrogated repeatedly.

Figure 1. An engineering student (co-author, Pena) is shown writing software codes on the HSTS Tektronix 9200 DAS for implementation of clock waveforms for EEV CCD-13 CCD.

Figure 2. Distribution system for clock waveforms from Tektronix 9200 DAS. Shown are the DAS state tables and software generated waveforms (visible on the PC screen), and the pattern generator and acquisition probes.

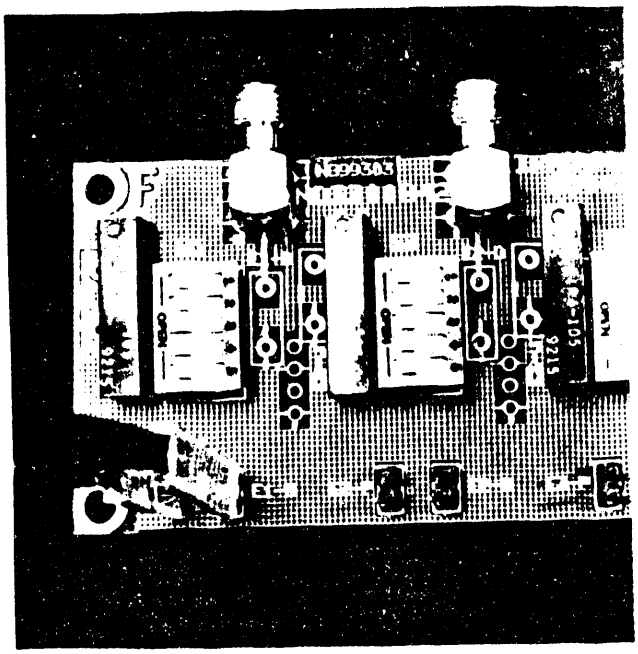


Figure 3. Enlarged view of clock distribution showing input from DAS active probe (bottom left), fanout to DAS logic acquisition probe (next) and passive delay modules and selection switches (middle) prior to exporting to CCD via coax connector (top).

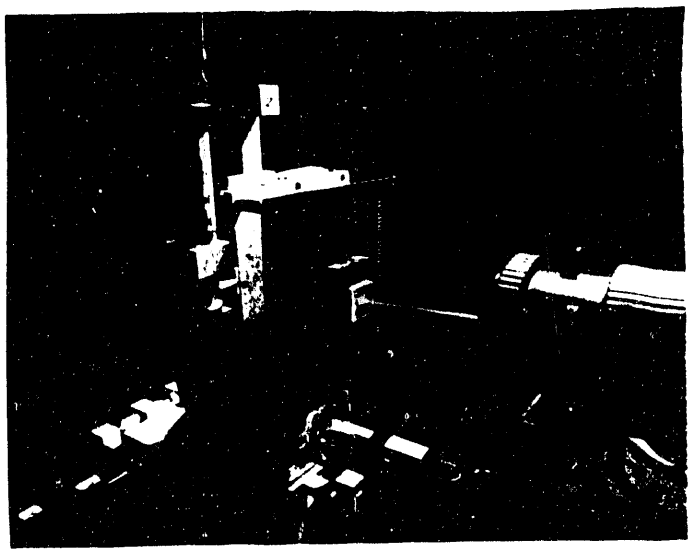
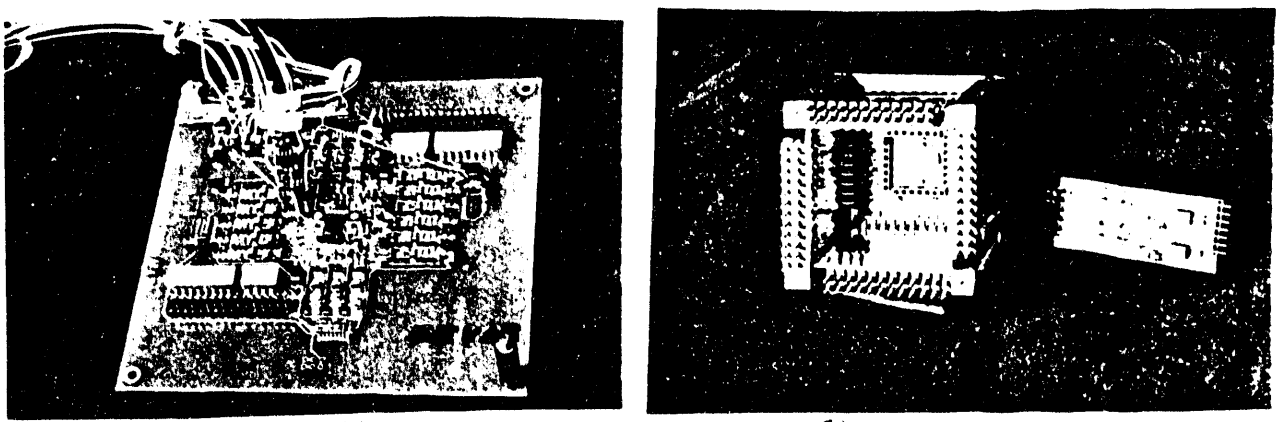


Figure 4. Tracking platform for three axis positioning of FPA under test (EEV CCD-13) with respect to laser pinhole illumination patterns from TVO Optoliner optical platform.

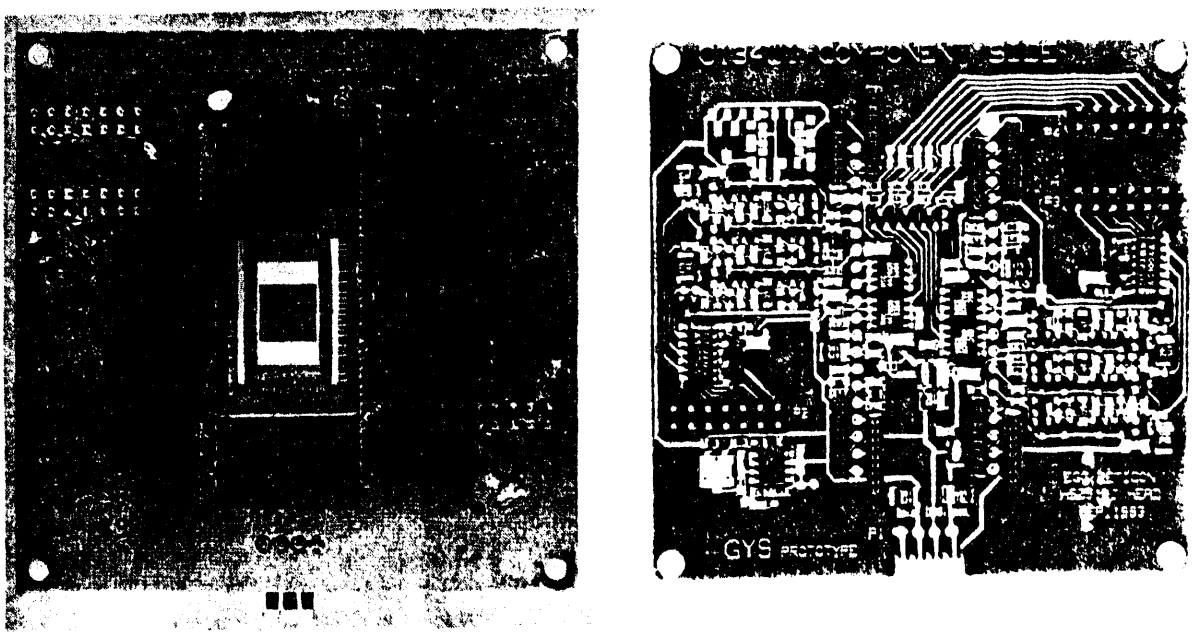
2. CCD HEADER PC BOARDS AND DIAGRAMS

A special header board is designed for each CCD to be evaluated in the HSTS. The boards have a minimum of circuitry, allowing for off-board flexibility in analog signal processing and freedom in generation of clock waveform characteristics and rates. The boards have high speed clock drivers/translators to generate the appropriate horizontal and vertical voltage amplitude waveforms and quiescent DC bias levels required to operate the solid state imager under test. The boards also have high bandwidth, high slew rate video amplifiers for buffering the imager's on-chip amplifiers for line driving capability for relaying video to remote processing and acquisition circuitry which comprise the HSTS. The CCD-13 header board is shown in fig. 5. and the Reticon HS0512J in fig. 6.



(a) (b)

Figure 5. Two EEV CCD-13 header boards. In (a), our original board is shown with single-channel amplifier plugged into one CCD output port. A reduced version for use in small camera head is shown in (b), with amplifier module to the right.



(a) (b)

Figure 6. Reticon HS0512J header board showing front view (with CCD in place) in (a) and rear view (b) showing clock level shifting circuitry. The single channel amplifier used for the EEV CCD-13 (fig. 5.) is plugged into the video ports individually when testing.

Both CCDs are designed for high speed readout by simultaneous bi-directional vertical clocking of upper and lower sections of the array as illustrated in fig. 7 and 8. Here the similarities diverge. The EEV CCD-13 is a Full Frame CCD, with no on-chip storage. The Reticon HS0512J is a Split Frame Transfer CCD, with upper and lower section storage areas adjacent to their respective image sections. Both use three phase vertical clocks for bi-directional readout. The EEV CCD-13 has four horizontal registers (two at bottom, two at top of array) which have output video ports at opposite ends of each register. They are clocked bidirectionally to increase clocking speed a factor of two by employing three phase horizontal clocks. Their architecture provides 8 output video ports. Each port has a "real" and "dummy" amplifier which are identical and located in same region of array. The "real" amplifier receives CCD video where as the "dummy" receives none. The "dummy" signal is used for background subtraction from the "real" signal, to eliminate common-mode fixed pattern noise. The Reticon HS0512J, by contrast, has two horizontal registers, one at top and one at bottom of the array. Each register is truncated to accept eight segments from each vertical storage section. This design doesn't provide bi-directional horizontal clocking, but has similar inherent speed to the EEV-CCD because each segment is 64 pixels horizontally as opposed to 128 pixels for the EEV-CCD. Two phase complementary clocks (180 degree phasing) are used with inherently higher speed capabilities when compared with the unipolar three-phase (120 degree phasing) design of the EEV-CCD.

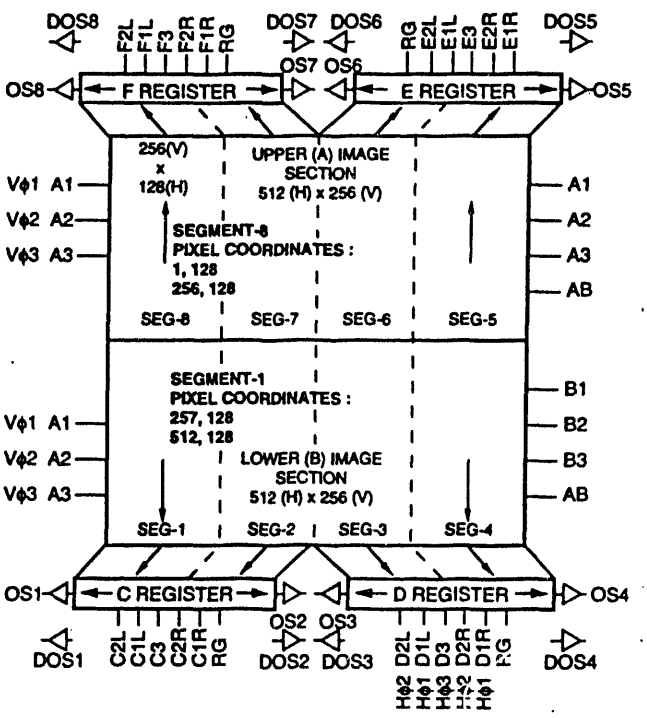


Figure 7. Readout diagram for EEV CCD-13.

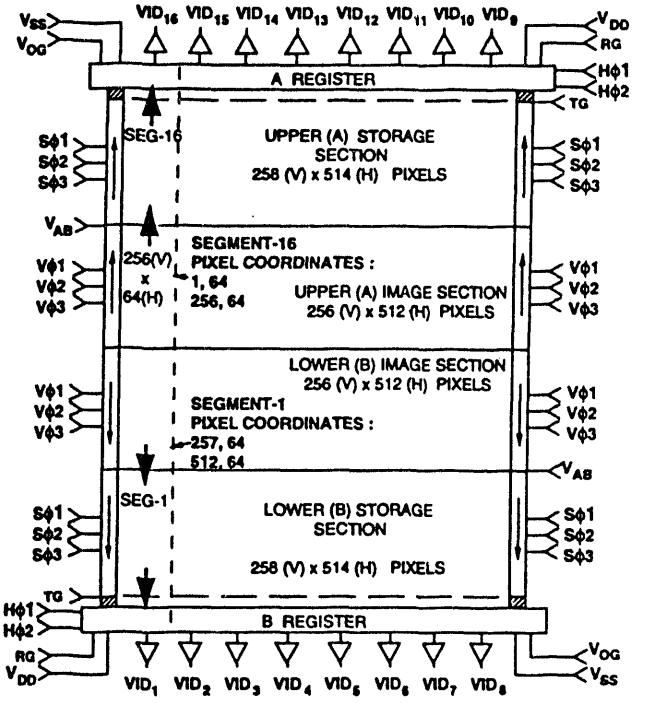


Figure 8. Readout diagram for Reticon HS0512J.

3. HSTS CODES FOR CCD CLOCK WAVEFORM GENERATION

Programming CCD clock waveforms on the HSTS involves writing binary or hexadecimal, octal, etc., codes to develop logic state tables which are converted to ECL or TTL time-varying waveforms by the Tektronix 9200 DAS clock. The lines of code in the state tables are executed sequentially by the DAS clock, which can operate up to 50 MHz in conventional mode or up to 100 MHz in multiplexed mode. The DAS has several output Pods which are essentially 8 parallel channels each. Two channels, when combined by a DAS MUX will have their respective binary codes executed once per each clock cycle, sampling first channels from one Pod, then channels from the other. The EEV code using the multiplexed mode for generation of its clocks is shown in fig. 9. Software waveforms from DAS acquisition logic are at top in fig. 9. The Reticon code and waveforms are shown in fig. 10. The feedback loops for both codes are illustrated for ease in following code execution.

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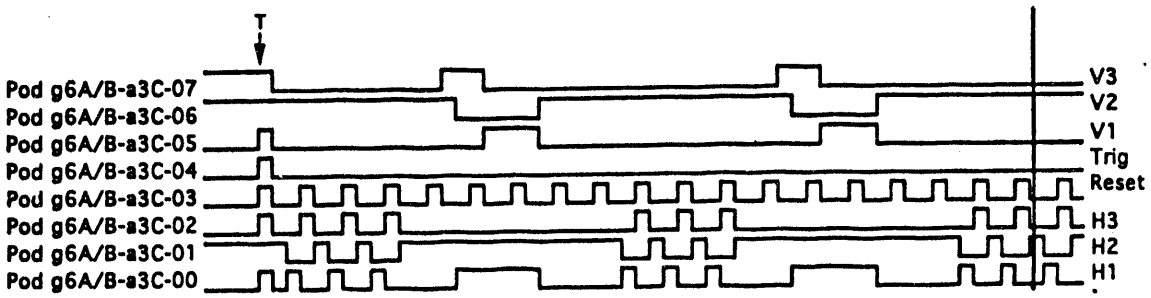

Seq	Label	Instruction		Dec	Pg5_1 Dec	Pod 6B Pod 6A
					0	7------07------0 CHANNEL
9					0	1111111111111111 Trigger Line
10	start				2	0100001001000001
11	cont3	Load	B	2	1	0100000101011100
12	cont4	Load	A	1	0	0100110001000010
13					0	0100001001000001
14	cont1				0	0100000101001100
15					0	0100110001000010
16					0	0100001001000001
17					0	0100000101001100
18		Decr	A		0	0100110001000010 A=0
19		If A=0	Jump	cont2	0	0100001001000001 A≠0
20		Jump		cont1	0	0100001001000000
21	cont2				0	0100001001001010
22					0	0100101001000010
23					0	1100001001000010
24					0	1000001110001011
25					0	1000101110000011
26					0	0010001110100011
27					0	0010001100101011
28					0	0010101100100011
29					0	0010001100100011
30					0	0100001000101010
31					0	0100101001000010
32					0	0100001001000010
33					0	0100001001001010
34		Decr	B		0	0100101001000010 B=0
35		If B=0	Jump	cont3	0	0100001001000010 B≠0
36		Jump		cont4	0	0000000000000000
37		Halt			0	0000000000000000
38					0	0000000000000000
39					0	0000000000000000
40					0	0000000000000000
41					0	0000000000000000
42					0	0000000000000000
43					0	0000000000000000
44					0	0000000000000000
45					0	0000000000000000
46					0	0000000000000000
47					0	0000000000000000

Figure 9. DAS program for generation of EEV CCD-13 code (bot), waveforms (top).

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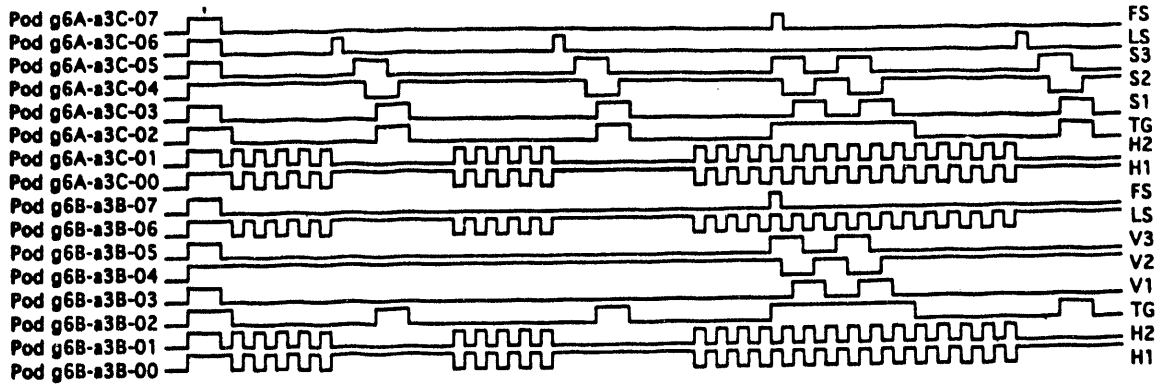

Seq	Label	Instruction			Pod 6B	Pod 6A	
			Dec		7------0	7------0	CHANNEL
9					11111111	11111111	Trigger Line
10	start	Hold	Out		11111111	11111111	
11					11111111	11111111	
12					01010101	00010101	
13	cont5	Load	B	2	00010010	00010010	
14	cont3	Load	A	2	01010001	00010001	
15					00010010	00010010	
16	cont1				01010001	00010001	A=0
17	H loop	Decr	A		00010010	00010010	A≠0
18		If A=0	Jump	cont2	01010001	00010001	
19		Jump		cont1	01010001	01010001	
20	cont2				01010001	00010001	
21	INTG				01010001	00110001	
22					01010001	00100001	
23					01010101	00101101	
24					01010101	00001101	
25					01010101	00011101	
26					01010001	00010001	
27		Decr	B		01010001	00010001	B=0
28		If B=0	Jump	LNCLR	01010001	00010001	
29					01010001	00010001	B≠0
30		Jump		cont3	01010001	00010001	
31					01000001	00000001	
32					01000001	00000001	
33					01000001	00000001	
34					01000001	00000001	
35					01010001	00010001	
36	LNCLR	Load	B	2	01010001	00010001	
37					01010001	00010001	
38					01010001	00010001	
39					00010010	00010010	
40	RPT				01010001	00010001	B=0
41		Decr	B		00010010	00010010	B≠0
42		If B=0	Jump	cont4	01010001	00010001	
43		Jump		RPT	11110101	10110101	
44	cont4	Load	A	2	00100110	00100110	
45	cont6				01101101	00101101	
46	F XFR				00001110	00001110	
47		Decr	A		01011101	00011101	A=0
48					00010110	00010110	
49		If A=0	Jump	cont5	01110101	00110101	A≠0
50		Jump		cont6	00000000	00000000	
51		Halt					

Figure 10. DAS program for Reticon HS0512J CCD (bot), waveform (top).

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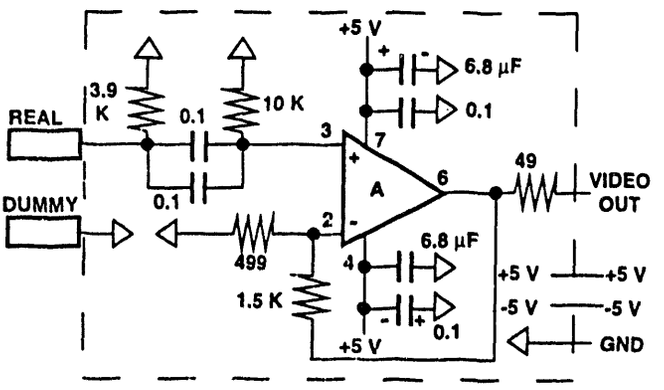
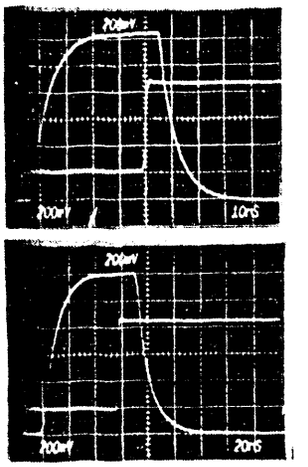
4. ANALOG PROCESSING OF CCD VIDEO

For comparison of individual video port signals, a single amplifier is used first to eliminate differences that might occur from variations among the multiple amplifiers required for multiport imagers. Two versions of the same amplifier fig. 11(a).with different frequency response to accommodate various pixel data rates were designed using Comlinear CLC-400 and Analog Devices AD811 monolithic integrated circuits in Surface Mount packages. The response for each amplifier is shown in fig. 11(b) and 11(c)., for impulse input of 5 ns rise time. The amplifiers plug into the imager's individual video output ports. The amplifier's output is then connected to our high speed analog peak sensing and stretching circuitry (fig. 12.) which processes the video on the pixel-by-pixel basis. The circuitry[3,4] also extracts properly phased clock signals to strobe the Sample and Hold amplifier which follows in the video chain. The raw CCD video at two amplitudes (small in a', large in a) is shown to reach peak values at different times t_1 and t_2 respectively. With peak sensing, obtained by first detecting raw (a) and integrated (b) video crossover, then stretched by a Sample and Hold amplifier. This flat portion of signal for the two amplitudes allows sampling either accurately at t_3. This video processor module is shown in fig. 13.



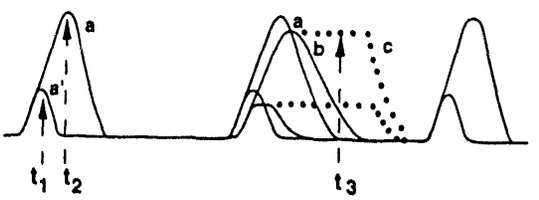
(a)



(b)

(c)

Figure 11. Buffer amplifier used for single-channel analysis of individual output video ports, circuitry (a), Comlinear CLC-400 response in (b), Analog Devices AD811 response in (c).



t_1 = peak for small amplitude a'
t_2 = peak for large amplitude a
t_3 = peak for either amplitude
a = raw pixel video
b = integrated video
c = peak sample & hold video

Figure 12. Video processing circuitry depicting slew rate limited CCD pixel signals (a and a'), pulse peak sensing (b) and Sample and Hold waveforms (c).

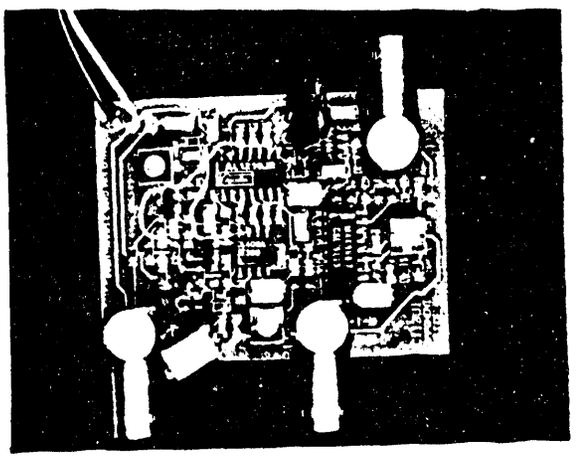


Figure 13. Printed circuit board of Video Processor module. The circuit is designed using surface mount technology for high speed performance.

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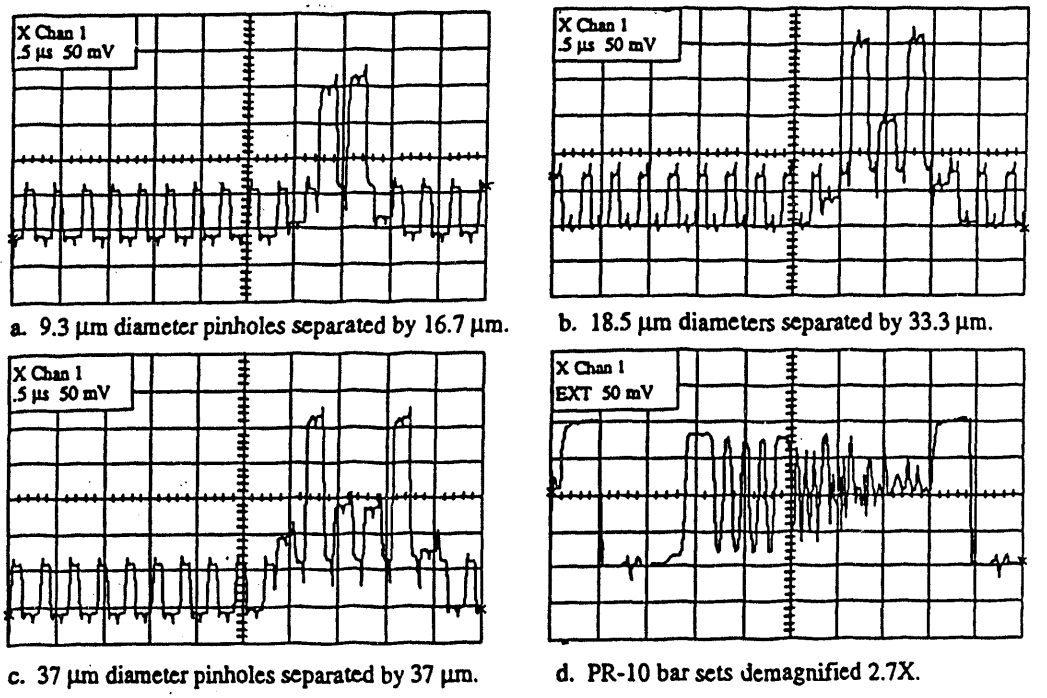
The output from the video processor is fed to high speed digitizers, LeCroy model 9314 Digital Sampling Oscilloscope (DSO). The pixel data are stored and analyzed directly with the DSO, using math/engineering waveform processing software (WP01, time domain functions and WP02, frequency domain operations). The DSO provides hard copy using RS232 printer. The data are also down loaded to an IBM PC via GPIB for permanent storage and further processing using IDL software. The IBM PC files are also transferred via floppy disc to Macintosh PC for analysis using public domain image processing software (NIH IMAGE) from National Institute of Health. The HSTS system is currently being upgraded to work station compatibility for networking of it's several personal computers via Ethernet.

5. DATA

The resolution measurements for the CCD-13 were taken using the HSTS Optoliner optics and pinhole array PSF and PR-10 CTF patterns. This provided ~2.7:1 demagnification at the CCD focal plane. For the CCD-13, Nyquist limit establishes resolving power of ~23.8 lp/mm (from 21 micron pixel pitch). The pixel clock frequency was 10 MHz for this initial measurements. The PSF data correspond to consecutive pixels across the array. The profiles correspond to the optically transmissive pinholes (apertures) and the opaque area between pinholes. The 37μm and 18.5μm arrays are resolved with approximately the same valley-to-peak ratios (~52%). The 9.3μm array is not resolved. These two pinholes and their spacing project an array width of only 35μm, which should occupy either two or three pixels depending upon image mapping between optics and the CCD-13. (These data show two pixels with charge.) An array intermediate to the 18.5 and 9.3μm arrays was unavailable to measure the PSF accurately. In principal, this approach (illustrated in fig. 15.) should provide amplitude/basewidth overlap data sufficient to measure PSF directly. The 2.7:1 demagnification produces spatial frequencies of 6.2, 12.4, 18.5, and 24.6 lp/mm at the CCD-13 from the first, second, third, and fourth bar sets. Therefore, only the first three bar sets can be resolved properly. The raw data from a DSO line scan are shown in fig. 14d.



a. 9.3 μm diameter pinholes separated by 16.7 μm.

b. 18.5 μm diameters separated by 33.3 μm.

c. 37 μm diameter pinholes separated by 37 μm.

d. PR-10 bar sets demagnified 2.7X.

Figure 14. Pinhole array images (a, b, and c) and PR-10 resolution bar chart image (d). These data depict horizontal resolution of the CCD-13. For the pinhole data, the DSO was clocked internally (oversampling) to demonstrate the quantity of pixels involved. For the PR-10 data, the DSO was clocked externally to eliminate aliasing.

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6. COMPARISON OF ARCHITECTURES

Each CCD architecture has its individual merits and limits. Interline Transfer (ILT) CCDs are capable of fastest electronic shuttering (~1-3μs), but at the expense of "fill factor", and some question as to potential smearing from vertical registers[5]. Their active photosensitive area for light collecting varies from 10% to <50%. Frame Transfer (FT) and Full Frame (FF) CCDs have essentially contiguous pixels with "fill factors" approaching 100%, but both require external shutters for light pulses in the microsecond range. The FT CCDs are vulnerable to smearing during frame transfer phase (~100-400μs) and the FF CCDs are susceptible during their entire read-out phase. For recording consecutive images, the ILT CCD can record a second image after transferring the first image from its photosite section to its vertical storage/transport section (again ~1-3μs). The FT CCD is ready for a second image only after its image section data has been transferred to its storage section (again ~100-400μs). The FF CCD can accept a second image only after complete readout of the entire array (~1-10 ms).

Much U.S. government supported R&D in fast readout (single field or high frame rates) CCD development involves parallel readout using multiport technology. To our knowledge, most multiport CCDs are generically FT devices. Therefore with regard to recording of shuttered images followed by fast readout, the FF CCD dominates for single-field applications because immediate readout occurs without any time requirement for transfer of images to storage, but the FT CCD dominates for consecutive field recording.

ACKNOWLEDGMENTS

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