Paper to be Presented at
IEEE Nuclear Science Symposium

BNL-49016

FABRICATION OF LARGE AREA Si CYLINDRIC DRIFT DETECTORS*

W. Chen, H. W. Kraner, Z. Li, P. Rehak
Brookhaven National Laboratory, Upton, NY 11973 USA

F. Hess
Phy. Dept. of Heidelberg University, Germany

April 1993

*This research was supported by the U.S. Department of Energy:
Contract No. DE-AC02-76CH00016.

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Advanced Si drift detector, a large area cylindrical drift detector (CDD), processing steps, with the exception of the ion implantation, were carried out in the BNL class 100 cleanroom. The double-side planer process technique was developed for the fabrication of CDD. Important improvements of the double-side planer process in this fabrication are the introduction of A1 implantation protection mask and the remaining of a 1000 Angstroms oxide layer in the p-window during the implantation.

Another important design of the CDD is the structure called "river," which allows the current generated on Si-SiO_2 interface to "flow" into the guard anode, and thus can minimize the leakage current at the signal anode. The test result showed that most of the signal anodes have the leakage current about 0.3 nA/cm^2 for the best detector.

Wei Chen
Brookhaven National Laboratory
Instrumentation Division
Building 535B
Upton, New York 11973
(516) 282-4213
FAX: (516) 282-5773
E-mail: Weichen@bnlcl1

SUMMARY

The silicon drift detector is based on the principle that a semi-conductor wafer with rectifying junctions implanted on both sides can be fully depleted through a small anode contact. The depletion field confines the electrons generated by the ionizing particle in buried potential channels. parallel to the surface. An electrostatic field parallel to the surface can be superimposed independently by rectifying junctions at different potentials on both sides of the wafer. This field transports the electrons along the buried potential channel toward a collecting electrode (anode), as shown in Fig. 1. The drift time of the electrons inside the channel measures the distance of an incident particle from the anode since the field (E) and therefore the drift velocity ($V_d=\mu E$) is known. The shape of the junctions as well as the applied potential on each of them may vary to achieve different drift geometries[1-5].

The advantages of the silicon drift detectors are not only that they provide very precise position measurements and only use one-dimensional readout for two-dimensional information and also require a much lower bias to achieve fully depletion of the silicon bulk compared with the standard p-n-diodes, but also that their anode capacitance is much lower than that of standard p-n-diodes detectors of the same dimensions. Therefore the amplifier noise can be reduced to a much lower level, and as a result we obtain an excellent position resolution.

The design of the CDD fulfilled the need of the NA45 experiment at CERN SPS(Super Proton Synchrotron). Two hundred forty one concentric rings of rectifying junction were designed on both side of the 3 inch diameter wafer with 140 micrometer pitch radially. To be precise, these "rings" were not circular, but had the shape of a 120 sides polygon. The width of each rectifying junction ring was three times that of the silicon dioxide ring. Electrons produced by ionization particles, drifted radially inside the silicon towards the outside circle of the detector where the 360 anodes with an anode pitch of 500 micrometer were located. The drift time measured the radial coordinate of the particle's hit and the charge sharing between anodes measured the angular coordinate. The active area was practically the entire 3 inch diameter of the silicon wafer with a small hole in the center to allow the non-interacting particle beam to pass. There were 240 resistors of voltage dividers integrated on each side of the wafer. The arrangement of the resistors was such that the voltage difference between the neighbor rings was constant. Another important design of the CDD is the structure called "river", which allows the current generated on Si-SiO_2 interface to "flow" into the guard anode, and thus can minimize the leakage current at the signal anode. The detector provided certain pairs of the polar coordinates for events with multiplicities up to several hundreds. The position resolution was 20 micrometers in each direction, equivalent to two million two-dimensional pixel elements [6].

Based on the charge transport principle of the CDD, the distribution of impurities in silicon must be uniform in order to get a uniform electrical field. The most uniform n-type silicon to date is the neutron transmutation doped (NTD) silicon, and therefore double side polished NTD n-type (111) 3-inch-diameter Wacker silicon wafers were used. The resistivity of each wafer is 5k ohm-cm and the thickness is 250 microns. The minority carrier lifetime after oxidation process is about 3 msec, the interface states density is $1.3x10^{10}/cm^2$ and the oxide charge density is $2.1x10^{11}/cm^2$.

All detector processing steps, with the exception of the ion implantation, were carried out in the BNL class 100 cleanroom. The photoresist used was KTI the 825 positive resist. The photoresist was applied on double side of the wafer by a photo resist spinner system (Headway Research, Inc. Model MD-EC101D-CB15). The double side lithography was realized with the use of a mask aligner that had an infrared light source and an infrared viewer. The photoresist developer we used was KTI the 809. Al masks and final metallization were sputtered in a dc sputtering system which has a Al source containing 2% silicon. Sintering was done by the Rapid Thermal Processing unit which is a PPC (Process Products Corp.) Model PTM-2016-M-2F-FC.

Fig. 2. shows the major processing flow chart of the double-side planer process technique developed for the fabrication of CDD [7]. Oxide passivation was achieved by thermal oxidation in three steps called oxide C with a mixture of dry oxygen and TCA (trichloroethane). The resulting thickness of silicon dioxide was about 4500 Angstroms. The oxide C is the best among all different oxidation conditions, see Table I. It had the highest minority carrier generation lifetime compared with others and had relative lower flat band voltage and small stretch-out with relative thicker oxide. It was believed that the intrinsic gettering had happened in the oxide C process, resulting in a defect free zone beneath the surface [8].

The photolithography step was done by the infrared mask aligner which enabled the double side lithograph step for opening of the windows in the oxide. In order to protect the wafer from possible contamination and damage due to high energy ion bombardment, a thin oxide layer of about 1000 Angstroms was left in the ion implantation window. The comparison of leakage currents between the diodes made by implanting through the thin oxide layer and the ones made by implanting directly through silicon (control samples) are listed on Table II. We can see that there is much less leakage current in the ones made by implanting through the thin oxide layer than those implanted directly into silicon. In the table the average leakage current referred is for 350 micron meter thickness of the wafer. Another advantage of having such a thin layer of oxide is to prevent a short circuit which could be produced by the contamination during the implantation process. Fig. 3. demonstrates how this thin layer of

oxide can prevent a short circuit effect. There were three groups of CDD fabricated. In the first group there was no 1000 Angstroms oxide layer for protection, while in the second the protective oxide layer was introduced and the third group followed the same processes as the second group.

Since both the anode and the p-ring were built on the one side of the wafer usually called the n-side, two extra protection masks were needed on the n-side to implant the boron and the phosphorus separately. Therefore on the n-side two additional steps were required to make the 2500 Angstroms thick Al protection masks before each boron and phosphorus ion implantation. The first group produced six detectors, but testing result showed the existence of the problem as shown in Fig. 4(a). It showed a lot of peaks in the leakage current curve which indicated the defects on the detector. The implantation mask used in this group was a positive photoresist mask (instead of Al) which may introduce pinholes and contaminations. In the second and third group of fabrication the Al implantation mask were used. The overall improvement of the detector performance can be seen in Fig. 4(b), which shows a good leakage current performance compared to Fig. 4.(a). This proves that the pinhole free Al mask production is an important step in the two sided detector fabrication.

After opening the windows on the oxide and making the Al protection mask, the wafers were ready to be sent out for implantation. Boron ion implantation was used for the p-type junction at an energy of 60 keV, and a dose of 0.75×10^{13} atoms/cm^2, which was derived by the requirement that the voltage divider resistors were 7k ohm/square. The boron activation plot is shown on Fig. 5, on which the 600 c and 800 c curves are illustrated. In order to get a 700 c annealing temperature as the following paragraph demonstrates, the 0.75×10^{13} atoms/cm^2 was chosen to obtain a 7k ohm/square sheet resistance. The anode was also implanted using phosphorus at an energy of 50 keV and a dose of 1×10^{14} atoms/cm^2.

Post implantation annealing was done in thermal furnace at 700 degrees c for 30 min in a dry nitrogen atmosphere. From Fig. 6 we can see that 700 degrees c is the lowest temperature that yields a stabilized the sheet resistance. The higher the temperature the more the risk of activating other ions produced by contamination, and so we chose the lowest possible temperature in the stabilized zone.

After post implantation anneal, an additional cut of 1000 Angstroms oxide was performed in both sides with diluted (10:1) Buffered HF solution. In the first group fabrication we used pure buffered HF solution for oxide cut. In the second group we changed to a 10:1 diluted Buffered HF for oxide cut. The results are also shown in Fig. 4. Diluted HF used during oxide etching step is another factor of improving the overall performance of the CDD, since it gives inclined cutting edge of oxide which can prevent spiking in a later stage of the fabrication. The spiking is most likely to happen near the oxide cutting edge. Fig. 7 shows the

cross section of the oxide cut in different etching solutions as seen through an electron microscope. Fig. 7 a) shows the steep cutting edge from the pure buffered HF etching and Fig. 7 b) shows the inclined cutting edge from the diluted HF etching.

Metallization was done by sputtering Al which contained 2% Si and followed with a rapid thermal process (RTP) sintering step to avoid spiking [9]. Since silicon diffusion into Al polycrystalline film is the mechanism of the spiking [10], first, the saturation of the silicon in thin film alloy can eliminate the silicon diffuse into aluminum; second, the shorter the annealing time the shorter the diffusion distance for silicon traveling into the aluminum ; (since the distance silicon travels inside Al $d=\sqrt{Dt_a}$, where D is the diffusion coefficient of silicon and t_a is the anneal time) therefore the smaller the spiking problem.

Important improvement of the double-side planar process in this CDD fabrication are the introduction of aluminum implantation mask and the remaining of a 1000 Angstroms oxide layer in the p-window during the implantation, which is expected to protect the window area from the damage and contamination during the high energy ion bombardment. This oxide layer should be thick enough to prevent 50 KeV phosphorus ions (anode implantation) from being implanted through this thin oxide to the p-type junctions even when there are pinholes on the Al protection mask. Therefore this thin oxide layer actually reduces the probability of the formation of pinholes which can only happen in the case that both the pinholes on the Al mask and the ones on the thin oxide layer are aligned. A graphic demonstration is shown in Fig. 8. The energy of the phosphorus ions should be such that they would not penetrate through the depth of existing p-type junctions even when the pinholes on the Al protection mask are aligned up with the ones on the thin oxide.

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Fig. 1

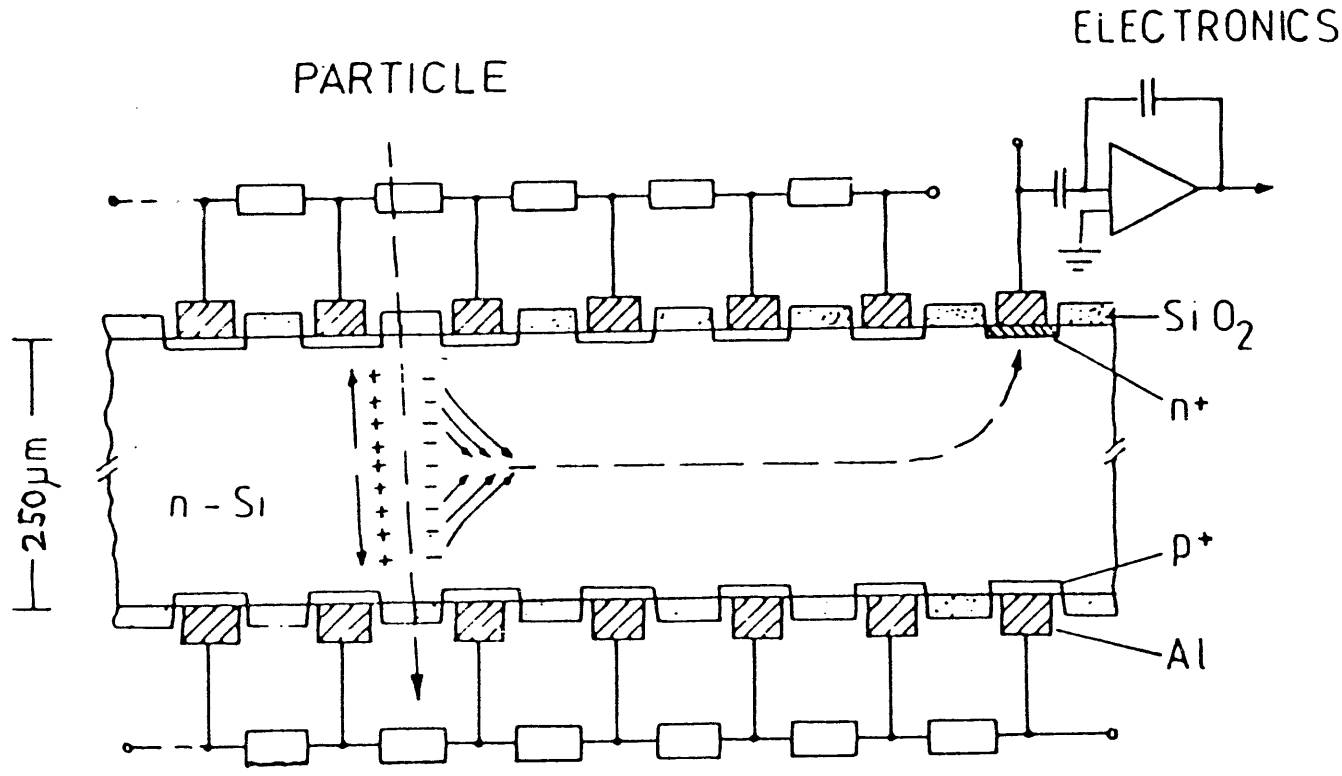


Fig. 2

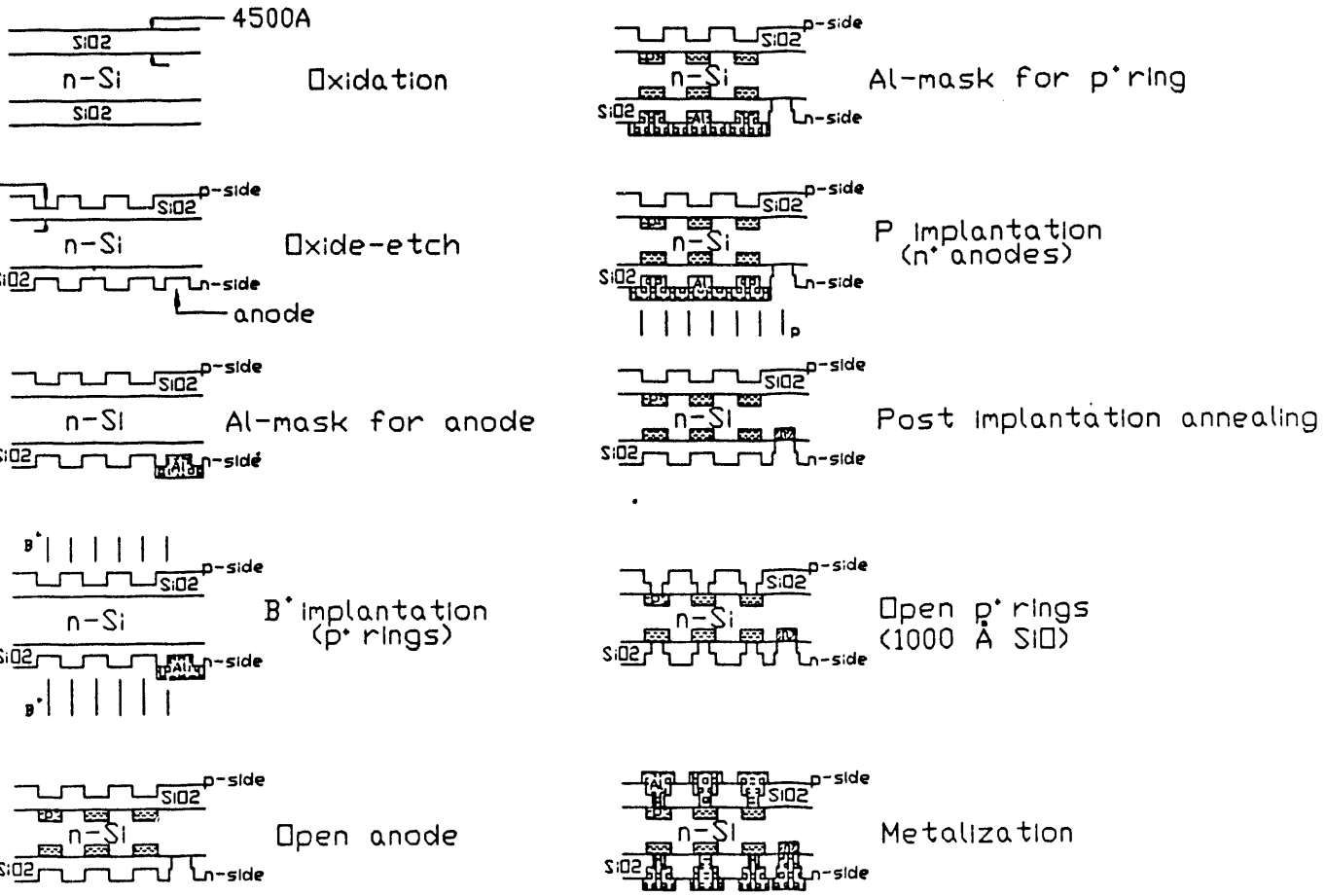

4500A
SiO2
n-Si
SiO2
Oxidation
1000A
p-side
SiO2
n-Si
SiO2
n-side
anode
Oxide-etch
p-side
SiO2
n-Si
SiO2
Al
n-side
Al-mask for anode
B+
p-side
SiO2
n-Si
SiO2
Al
n-side
B+
B+ implantation
(p+ rings)
p-side
SiO2
n-Si
SiO2
n-side
Open anode
p-side
SiO2
n-Si
SiO2
Al
n-side
Al-mask for p+ ring
p-side
SiO2
n-Si
SiO2
Al
n-side
P
P implantation
(n+ anodes)
p-side
SiO2
n-Si
SiO2
Al
n-side
Post implantation annealing
p-side
SiO2
n-Si
SiO2
n-side
Open p+ rings
(1000 Å SiO)
Al
p-side
SiO2
n-Si
SiO2
Al
n-side
Metalization

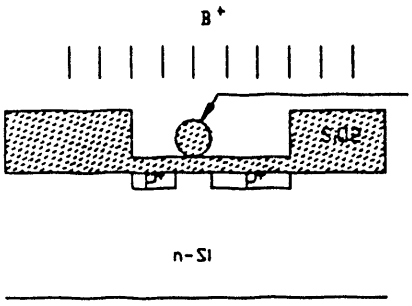
TABLE I

Oxide	Condition	V_{Fb} (V)	δV_{Fb} (V)	N_{ox} (Cm^{-2})	N_{it} (cm^{-2})	τ (ms)	Oxide Thickness (Å)
A	975°c, 18hrs O_2 975°c, 2hrs N_2	-8.40	0.70	5.43×10^{11}	4.53×10^{10}	1.10	3350
C	1100°c, 6hrs O_2+TCA 700°c, 16hrs O_2+TCA 1000°c, 5hrs O_2+TCA 1000°c, 2hrs N_2	-3.10	0.23	1.39×10^{11}	0.89×10^{10}	4.92	4573
B	1030°c, 4hrs O_2+TCA 1000°c, 1hr N_2	-2.60	0.30	2.46×10^{11}	2.84×10^{10}	1.57	2043
Ā	1200°c, 20hrs O_2 1000°c, 2hrs N_2	-8.60	0.90	1.95×10^{11}	2.04×10^{10}	0.92	9340

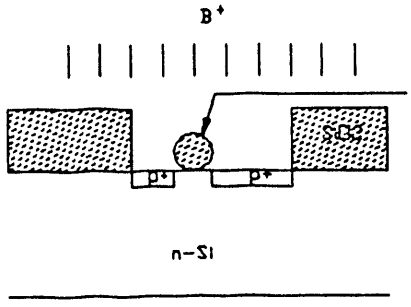
TABLE II

#	B^+ implant through	Sheet Resistance	Average Leakage Current I at 100V (nA/cm^2)	$\frac{I}{I_c}$
		B(Ω/□)	$0.25cm^2$dot	
1000	control	1.15K	$115.onA/cm^2$	13.9%
	400Å	1.65K	$16.onA/cm^2$	
1001	control	1.2K	$145.onA/cm^2$	9.9%
	500Å	1.85K	$14.4nA/cm^2$	
1002	control	1.4K	$88.onA/cm^2$	12.6%
	600Å	2.45K	$11.1nA/cm^2$	
1003	control	1.52K	$150.onA/cm^2$	14.0%
	700Å	2.86K	$21.onA/cm^2$	

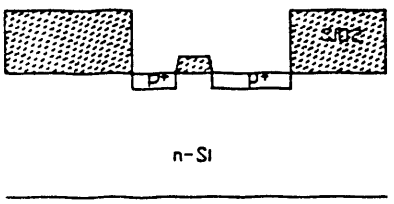
Fig.3



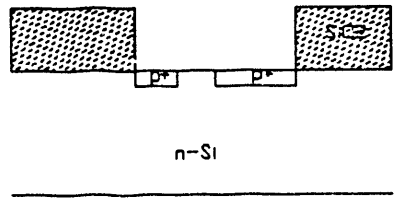
B+ implant through thin oxide layer



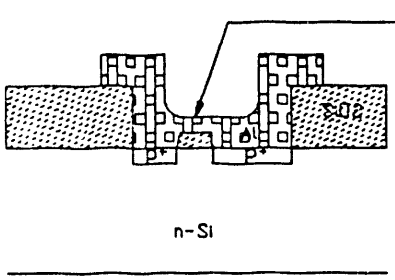
B+ implant



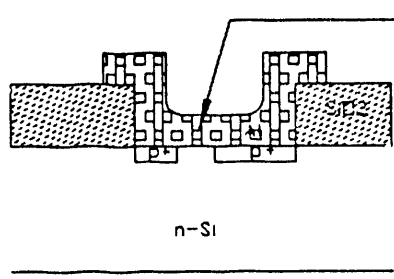
Thin oxide cut



Cleaning

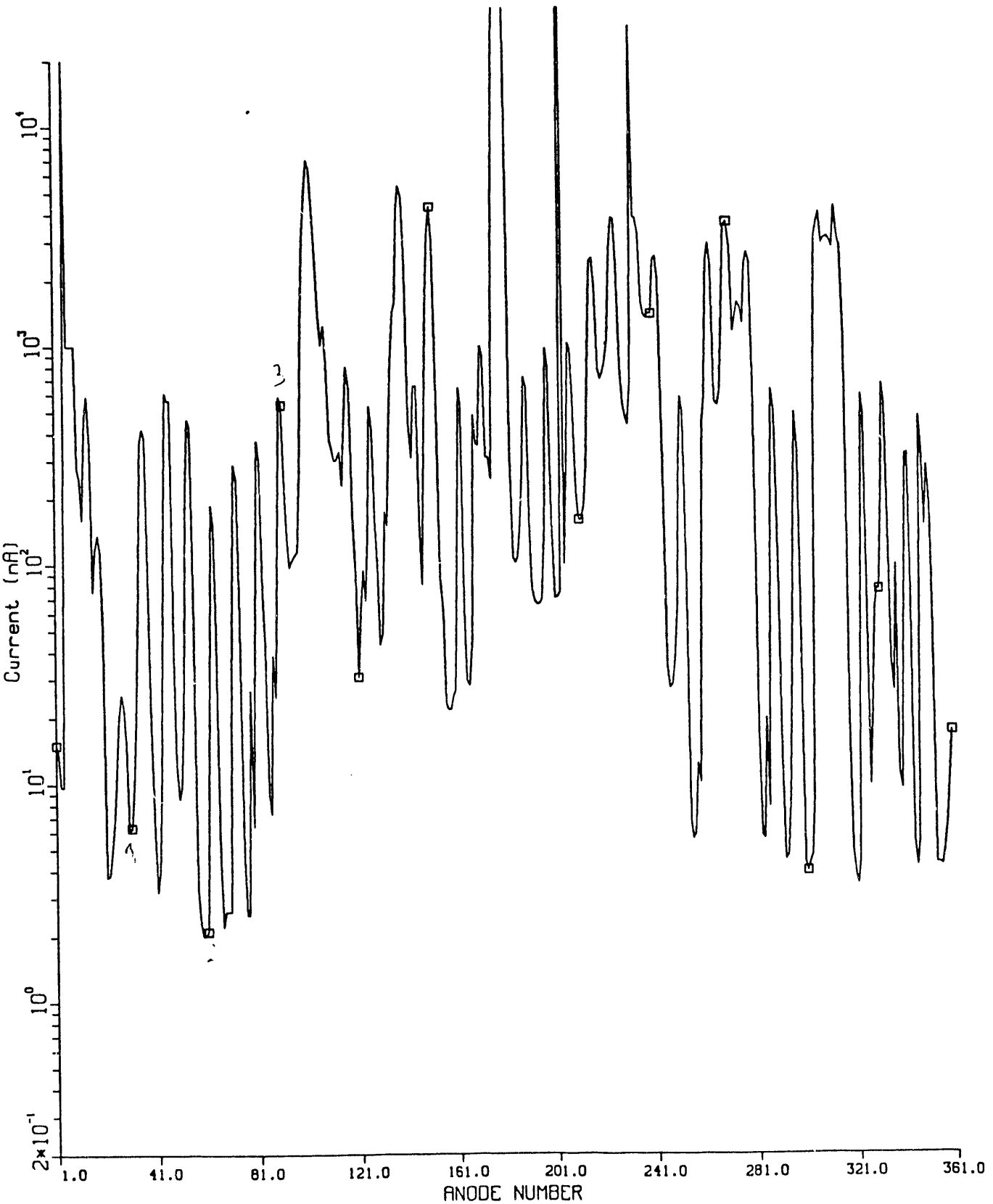


Metalization



Metalization

B6 individual anodes for -130.0 V at ring #37



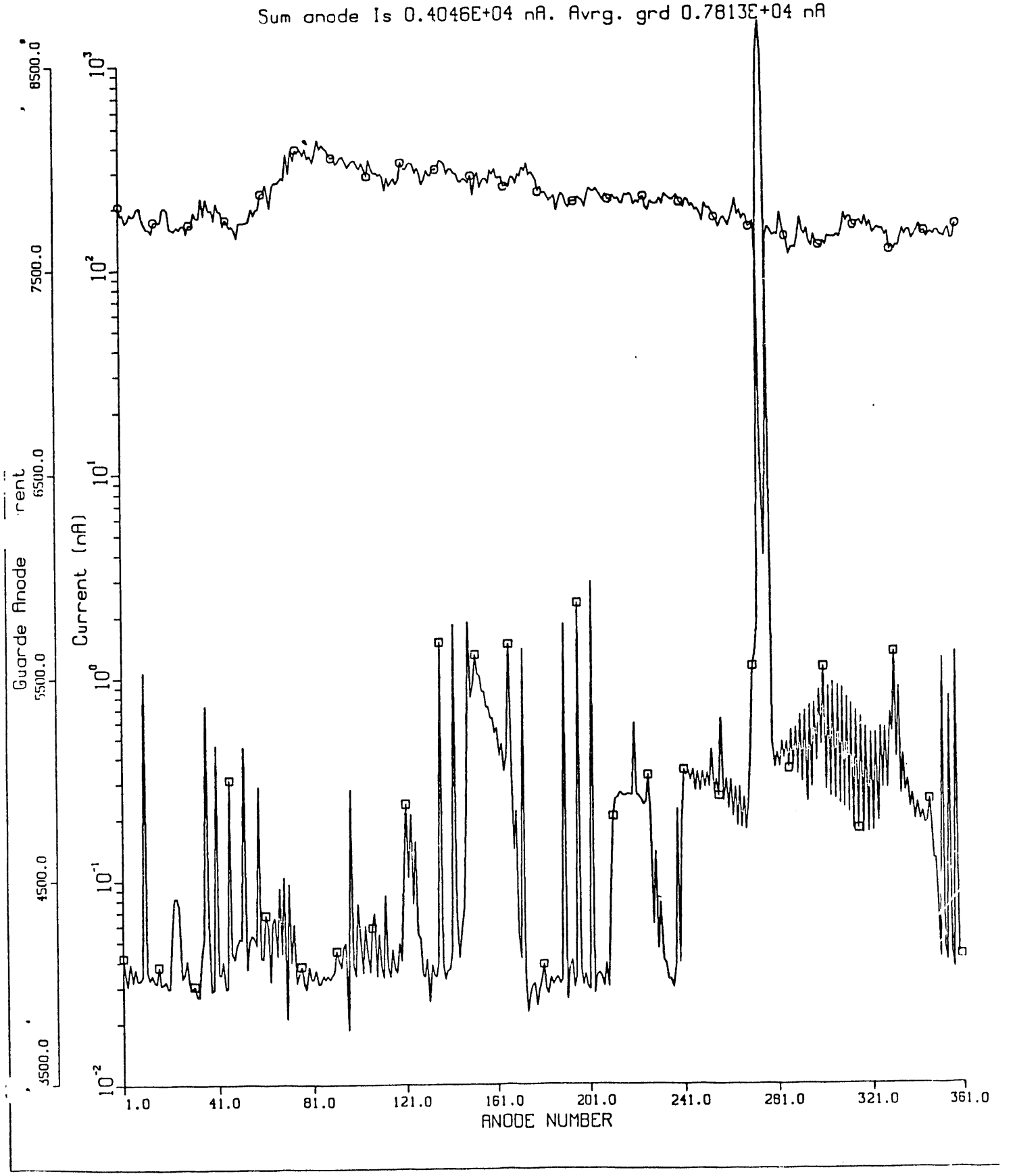

B18. -1000V at rg 193. 60V drop into inj4
03-27-1992
Sum anode Is 0.4046E+04 nA. Avrg. grd 0.7813E+04 nA
Current (nA)
ANODE NUMBER
1.0
41.0
81.0
121.0
161.0
201.0
241.0
281.0
321.0
361.0
Guarde Anode
8500.0
7500.0
6500.0
5500.0
4500.0
3500.0

Fig. 5

Boron Activation Plot

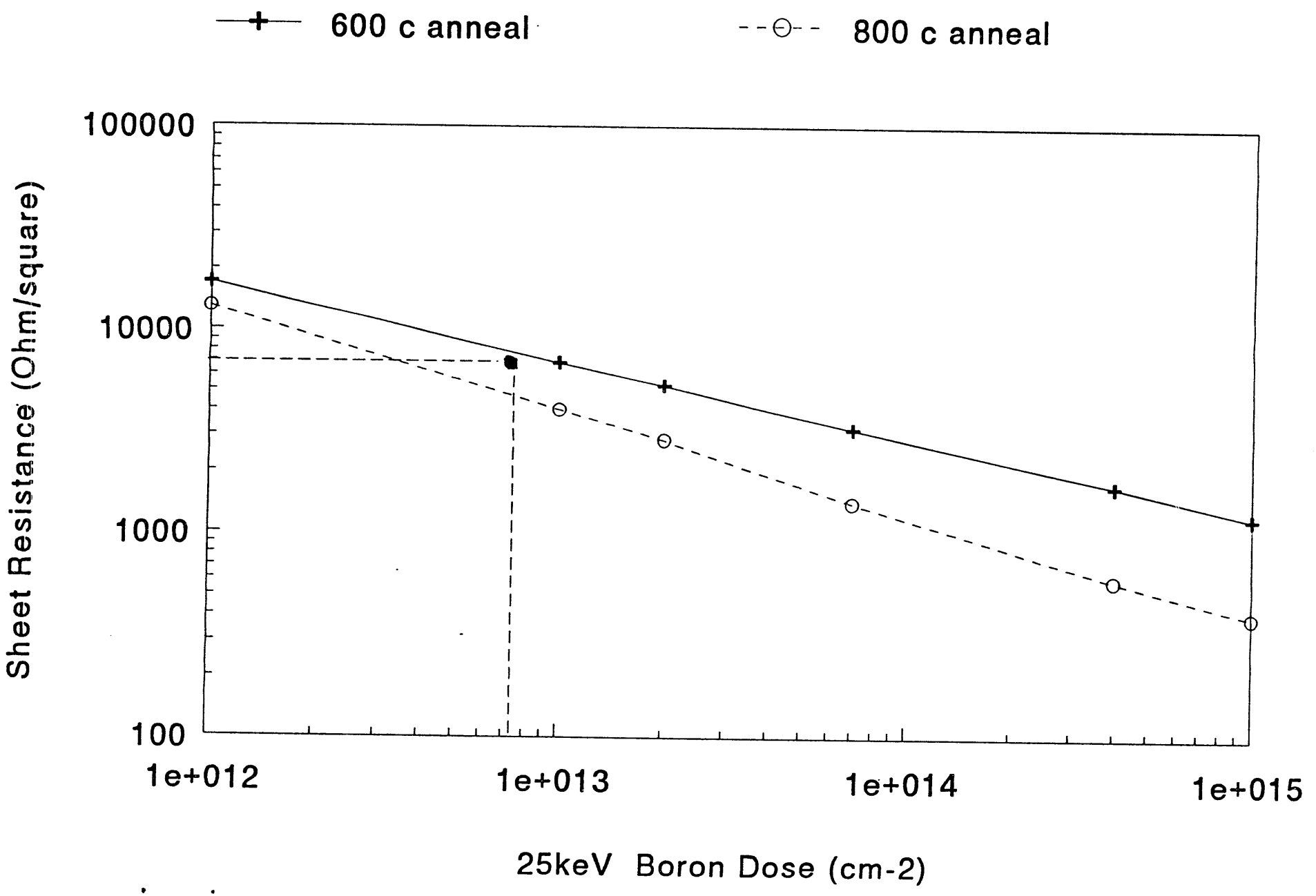


Fig 6

BORON ACTIVATION PLOT

25 KcV, 7E13/cm2

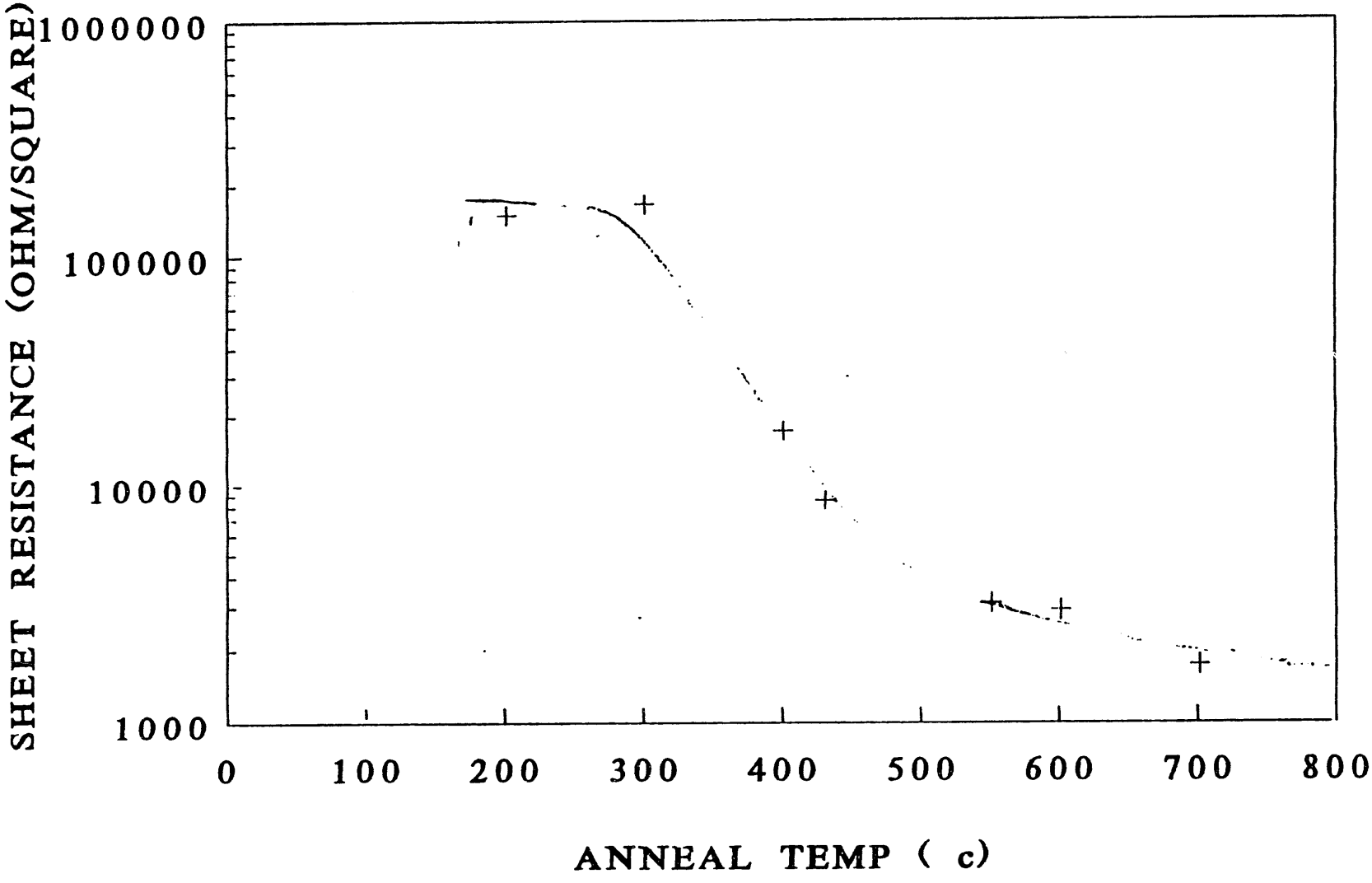
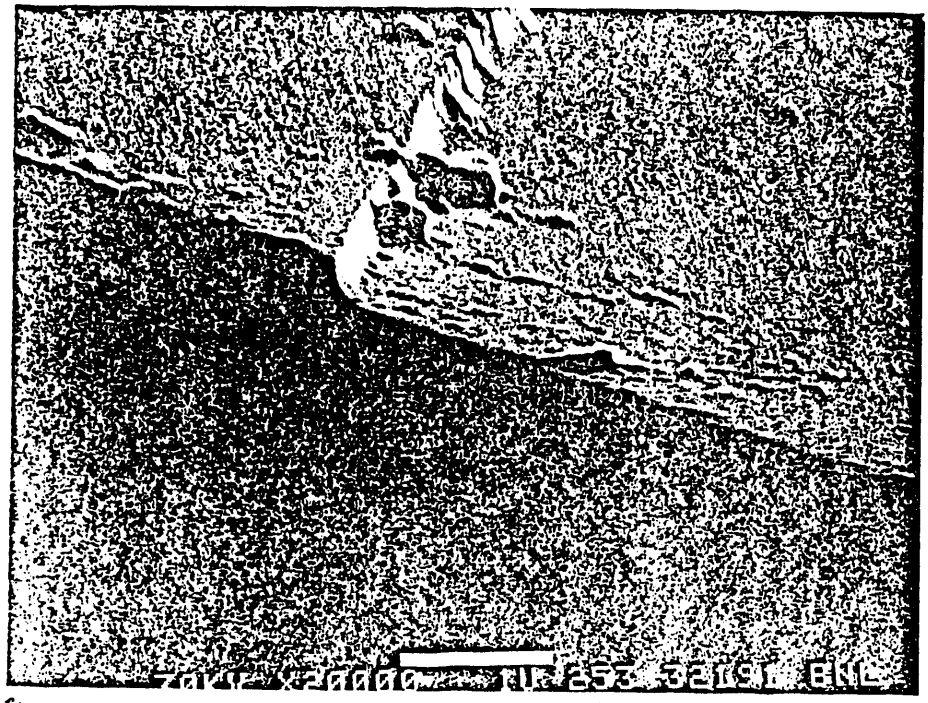


Fig 7

(a)

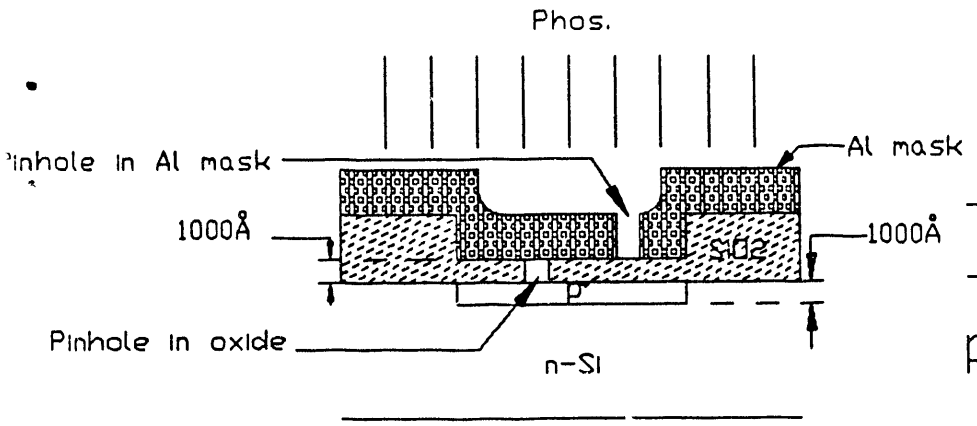


8 1-HF , No Resist

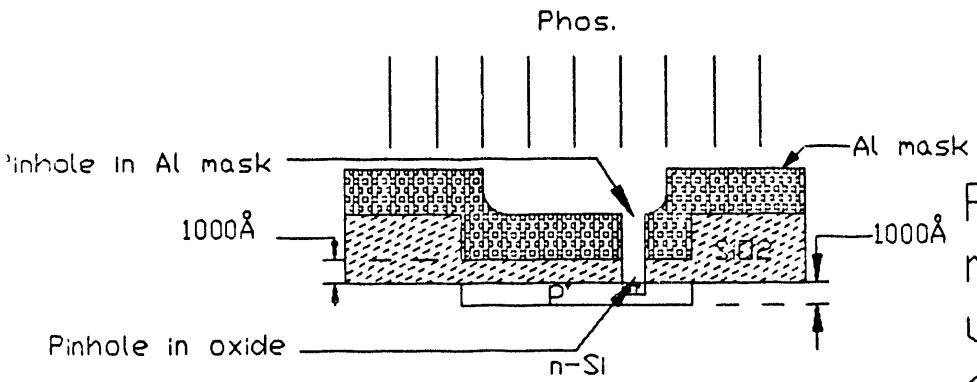
(b)

4 10:1 HF No resist (DN)

Fig.8



Thin oxide reduces the probability of pinhole



Pinhole on Al mask is aglined up with pinhole on thin oxide

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