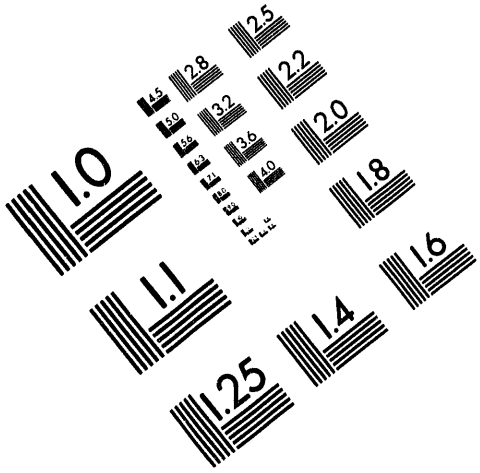

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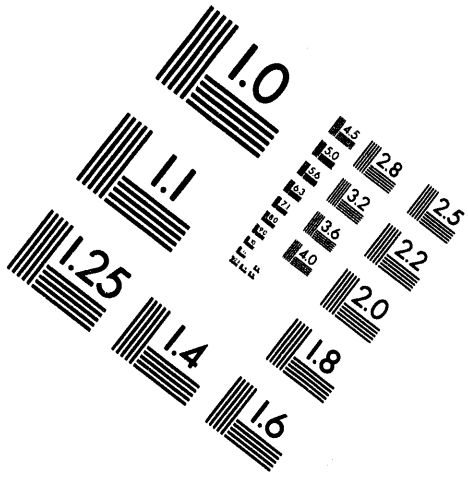

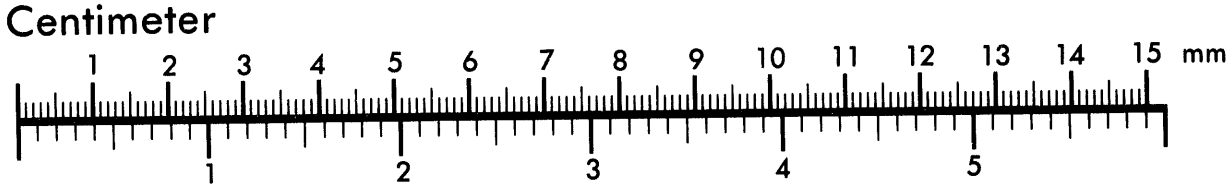

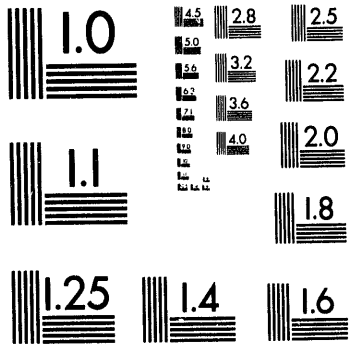

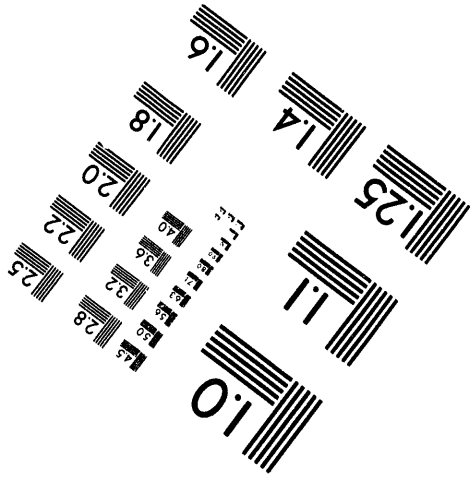

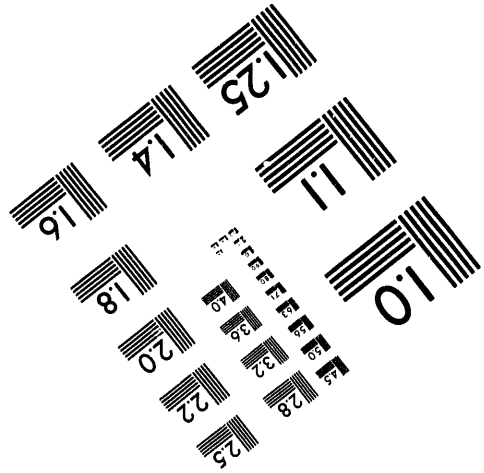

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I_{DDQ} Testing for Ultimate Low Power Design Verification and Defect Detection

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Abstract

I_{DDQ} testing is mandatory to ensure that low power CMOS ICs meet their design intent. I_{DDQ} testing is both a design verifier for low quiescent current and a sensitive production test for defects. Quiescent power reduction is particularly important for products such as cardiac pacemakers, laptop computers, and cellular telephones.

Introduction

CMOS VLSI ICs typically have dc power supply background currents below 50 nA when care is taken in the design to avoid unnecessary elevation of the quiescent current (I_{DDQ}). This low I_{DDQ} property has two important uses: (1) it is a design verifier for the low power intent of the product, and (2) it is a production test for large classes of CMOS IC defects. No other measurement assures designers that the product is truly low power in its quiescent state. Low power design practices also have significant, positive impact on CMOS IC quality. Recent manufacturing data show that I_{DDQ} testing is necessary to ensure that low power products have low test defect levels, higher reliability, and more accurate diagnostics [1,2].

What is I_{DDQ} Testing? I_{DDQ} is the quiescent power supply current into the chip V_{DD} pin and I_{DDQ} testing is performed by measuring this current for multiple test vectors (it is more than a simple power down test) [1,2]. Fig. 1 shows the I/O voltages and I_{DDQ} for a generalized CMOS IC with and without a defect in the internal logic. Most CMOS defects elevate I_{DDQ} by 3-7 orders of magnitude. Typical I_{DDQ} pass/fail limits for defects lie in the 1 μA to 500 μA range, with some companies using limits below 1 μA. Lower I_{DDQ} limits detect more defects. Similarly, elevated I_{DDQ} can indicate design or mask errors if all ICs show logic state dependent I_{DDQ} elevations. Typical CMOS IC designs can achieve < 1 μA levels. For example, ICs with about 2 million transistors have been shown to have I_{DDQ} below 50 nA for all logic states.

I_{DDQ} testing was performed by RCA in the 1960's on their CD4000 series SSI CMOS ICs. Philips in Europe, Sandia Labs in the United States, and NEC in Japan began using I_{DDQ} testing in the 1970's. Historically, I_{DDQ} testing developed from intuitive reasoning. Static CMOS ICs designed with fully complementary transistors had low nA quiescent current, therefore elevated current indicated abnormalities (defects). Recent excitement stems from data linking CMOS IC defects and elevated current, and data from several comparative studies showing increased defect coverage when I_{DDQ} is used in addition to the normal Boolean tests (functional or stuck-at fault) [1,2]. IC defect levels measured as production test escapes dropped by factors ranging from ten to over a hundred when I_{DDQ} testing was added.

Is I_{DDQ} Testing a Demonstrated Verification Tool for Low Power Designs? Yes - Sandia Labs, Philips, and other companies use I_{DDQ} testing for both low current designs and for defect testing. I_{DDQ} testing has detected many incidences of high leakage paths caused by design errors. Many of these design violations arise from subtle oversights, such as bus contentions, mask level open circuits, mask-error-induced power to ground shorts that did not interfere with circuit function, and connectivity errors.

What is the Link Between I_{DDQ} Testing and IC Reliability? An experiment by Ford Microelectronics Corp. on 59,000 CMOS ICs showed that 8.3% of the die that functioned, but had high I_{DDQ} values, functionally failed a 1000 hour life test [2]. Sandia Labs showed that I_{DDQ} testing must be used for gate oxide short detection [1]. Fig. 2 shows a gate oxide short readily detected with I_{DDQ} testing. High current states due to design reduce the ability to detect design errors, layout problems, and manufacturing defects.

DISCLAIMER

What is the Diagnostic Technique that Uses I_{DDQ} Responses? When only certain vectors elevate I_{DDQ}, then defect localization is possible. Sandia Labs failure analysis has used this tool for many years. Aitken described a precise technique using both I_{DDQ} and Boolean test results to isolate defect locations in CMOS ICs [3]. Information from SEM images and I_{DDQ} testing can be used to identify logic nodes associated with high current [4].

What Design Rules are Important for Low Quiescent currents? Low quiescent background currents are not technically difficult to achieve. Designs should avoid dynamic nodes, pullup resistors (these may be gated out for an I_{DDQ} test mode), floating buses, transmission gates that allow high impedance states, and contention between transistors. Dynamic nodes do not prevent I_{DDQ} testing, but may restrict the clock frequency used for the test and may limit the choice of I_{DDQ} test instrumentation. Other techniques for low power design are also effective [5]. Sandia Labs has practiced design for I_{DDQ} testability for over 15 years. Josephson of Hewlett Packard demonstrated I_{DDQ} test design rules in the HP PA-RISC design that operates at 100 MHz and has about one million transistors [6].

Is Transient Current Reduction Important in I_{DDQ} Testing? Yes - I_{DDQ} measurement rates are often limited by transient current settling time. Shorter settling times allow faster I_{DDQ} test rates. Also, I_{DDQ} instruments must be protected from large transient current peaks with bypass circuitry. Lower peak currents ease this problem.

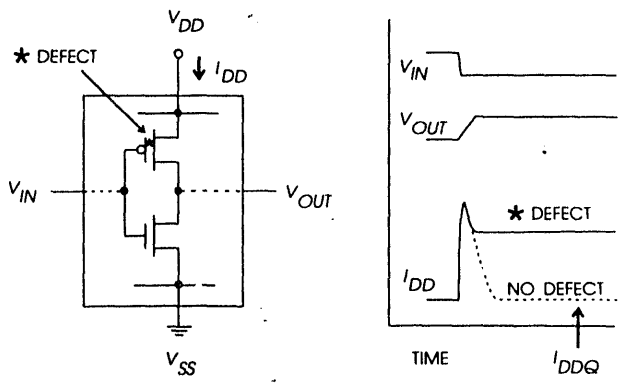

Fig. 1. I/O voltages and $i_{DD}(t)$ for a generalized CMOS IC with and without a defective gate in the internal logic.

Conclusion

Low power CMOS IC design requires I_{DDQ} testing for low power design verification and for achieving low test defect levels and improved reliability.

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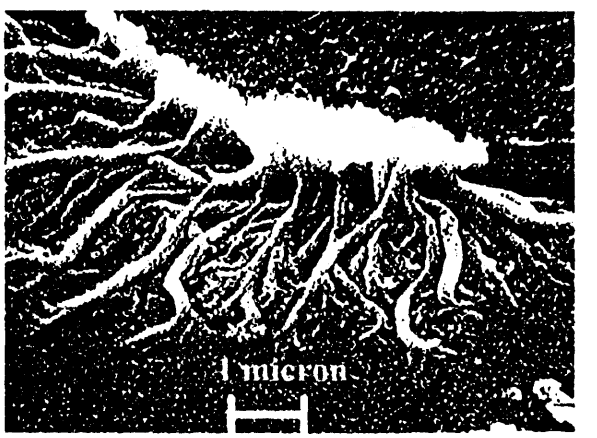

Fig. 2. SEM image of a gate oxide short in a CMOS IC. These types of defects often can only be detected with I_{DDQ} testing.

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