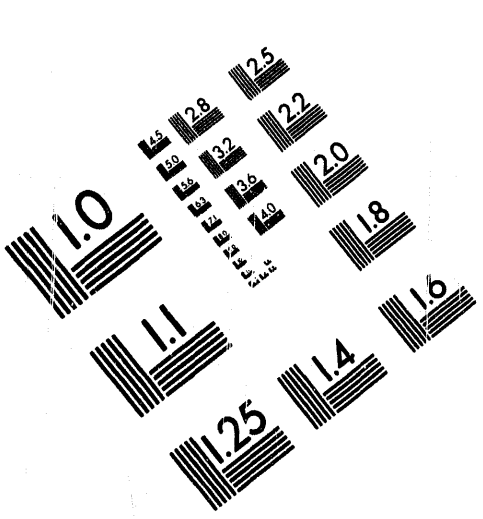

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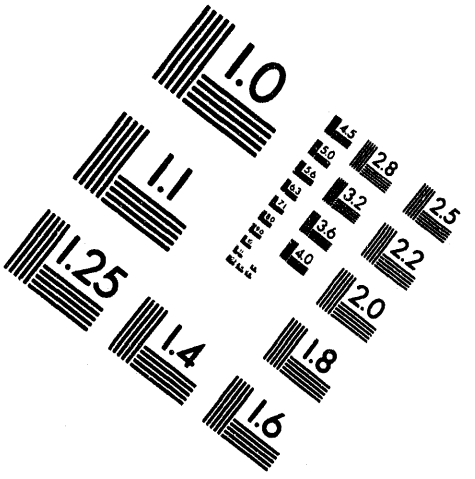

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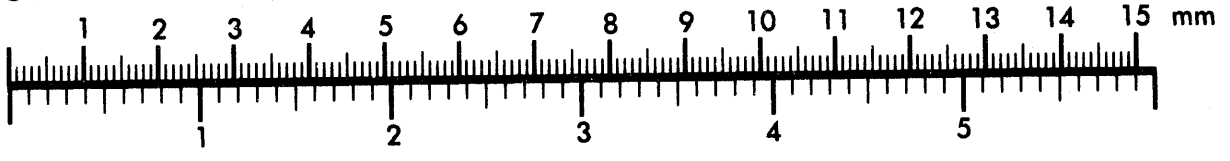

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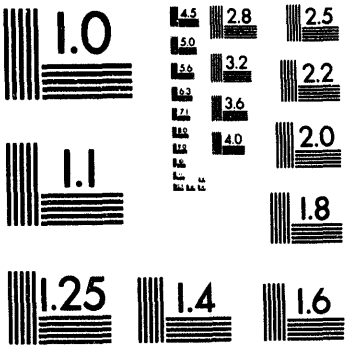

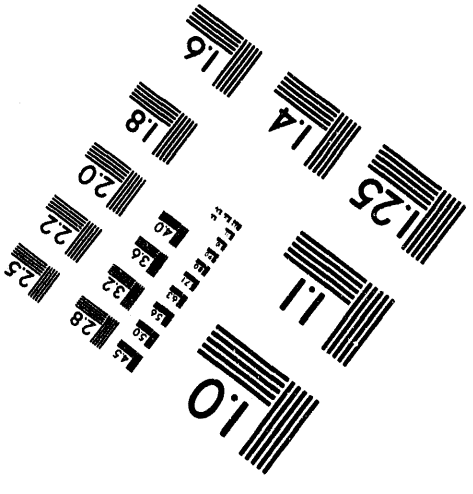

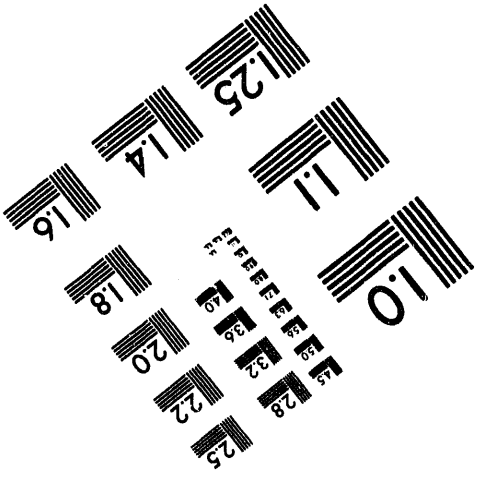

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Presented at the IEEE Nuclear Science Symposium
Oct. 31- Nov. 6, 1993

BNL-49016
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Fabrication of Large Area Si Cylindric Drift Detectors*

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April 1994

DISCLAIMER

*This research was supported by the U.S. Department of Energy:
Contract No. DE-AC02-76CH00016.

Fabrication of Large Area Si Cylindrical Drift Detectors*

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Abstract

The processing of an advanced silicon detector, a large area cylindrical drift detector (CDD), was carried out in the BNL Instrumentation Division Fabrication Facility. The double-sided planar process technique was developed for the fabrication of the CDD. Important improvements of the double-sided planar process in this fabrication include the introduction of an Al implantation protection mask and implantation of boron through an 1000 angstrom oxide layer in the step of opening the p-window.

Another important aspect of the design of the CDD is the structure called "river," which allows the current generated on the Si-SiO_2 interface to "flow" into the guard anode, and thus minimize the leakage current at the signal anode. The test result showed that for the best detector most of the signal anodes have leakage currents of about 0.3 nA/cm^2.

I. INTRODUCTION AND HISTORY

A new charge transport method in a fully depleted silicon detector, to be called the semiconductor drift chamber, was first proposed by E. Gatti and P. Rehak in 1984[1]. Since then, a great deal of effort has been directed into the analytical and numerical modeling and the simulations of silicon drift detectors. Up to now only linear geometry and cylindrical geometry with the drift of electrons toward the center have been realized[2-3]. The first linear drift detector produced was at the Lawrence Berkeley Laboratory (LBL) in 1983[4]. Several other drift detectors were produced at the Technical University. of Munchen later in 1984[5]. The active area of each early detector was about one square centimeter.

A detector with a large active area was required for high energy physics experiments. The cylindrical geometry is the ideal design for many of the fixed target experiments[6].

In this paper, we will mainly report the fabrication aspects of a large area cylindrical drift detector (CDD). The paper consists of five sections. The second section briefly states the principle of the drift detector and the structure of the CDD. The third section describes the parameters of the material, the equipment and the cleanroom facilities used in the fabrication of the CDD. In the fourth section we give details of the flow of the fabrication steps and discuss some critical processes. In the last section we present some laboratory test results and the effect of critical processing steps on the detector performance.

II. PRINCIPLE OF DRIFT DETECTOR AND STRUCTURE OF THE CDD

The silicon drift detector is based on the principle that a semiconductor wafer with rectifying junctions implanted on both sides can be fully depleted from each of the opposite wafer faces with respect to a small anode on the one side of the wafer. The depletion field confines the electrons generated by the ionizing particle in buried potential channels parallel to the surface. An electrostatic field parallel to the surface can be superimposed independently by rectifying junctions at different potentials on both sides of the wafer. This field transports the electrons along the buried potential channel toward a collecting electrode (anode), as shown in Fig. 1. The drift time of the electrons inside the channel measures the

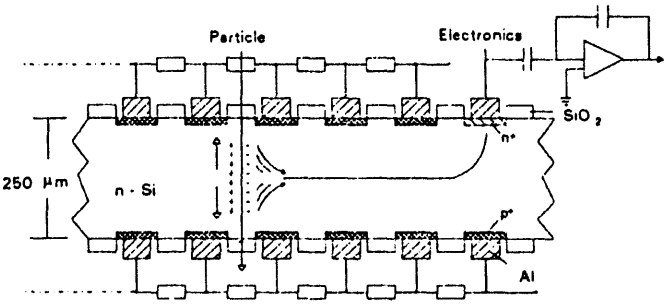


Fig. 1. Schematics for the operation of a drift detector.

distance of an incident particle from the anode since the field (E) and the drift velocity ($v_{dr}=\mu E$) are known. The shape of the junctions, as well as the applied potential on each of them, can be varied to achieve different drift geometry.

The advantages of the silicon drift detectors are not only that they provide very precise position measurements and require a much lower bias to achieve full depletion of the

*This research was supported by the U.S. Department of Energy: Contract No. DE-AC02-76CH00016.

silicon bulk compared with the standard p-n-diodes, but also that the anode capacitance is much lower than that of standard junction detectors of the same dimensions. Therefore the electronic system noise can be reduced to a much lower level (generally dominated by the first amplifier stage, $G_m C_m$), to obtain excellent position resolution.

The design of the CDD fulfilled the need of the NA45 experiment at the CERN Super Proton Synchrotron[6]. A sketch of the design is shown in Fig. 2. Two hundred forty

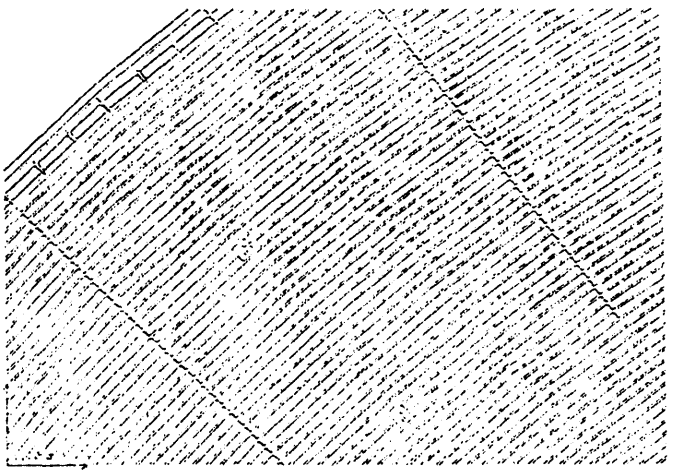


Fig. 2. Portion of the CDD detector with anodes on the outside.

one (241) concentric rings of rectifying junction were designed on both sides of the 3-inch diameter wafer with 140 micron radial pitch. To be precise, these "rings" are not circular, but had the shape of a 120 sided polygon. The width of each rectifying junction ring was three times that of the silicon dioxide ring. Electrons produced by ionization particles drift radially inside the silicon potential minimum towards the outside circle of the detector where the 360 anodes with an anode pitch of 500 micrometer were located. The drift time measured the radial coordinate of the particle's hit and the charge sharing between anodes measured the angular coordinate. The active area was practically the entire 3 inch diameter of the silicon wafer with a small hole in the center to allow the non interacting particle beam to pass. Two hundred forty resistors (usually called voltage dividers) integrated on each side of the wafer. The arrangement of the resistors was such that the voltage difference between the neighbor rings was constant. Another important design of the CDD is the structure called a "river" which allows the current generated on the Si-SiO_2 interface to "flow" into the guard anode, and thus can minimize the leakage current at signal anode. The detector provides certain pairs of the polar coordinates for events with multiplicities up to several hundred. The position resolution was found to be 20 micrometer in each direction giving about two million two-dimensional elements[6].

III. MATERIALS AND PROCESSING CONDITIONS

The charge transport principle of the CDD requires that the distribution of impurities in silicon must be uniform in order to get a uniform electrical field. The most uniform n-type silicon to date is the neutron transmutation doped (NTD) silicon, and therefore double sided polished NTD n-type (111) 3 inch diameter Wacker silicon wafers were used. The resistivity of each wafer is 5k ohm-cm and the thickness is 250 microns. The minority carrier lifetime after the oxidation process is about 3 msec, the interface state density is $1.3 \times 10^{10}/cm^2$ and the oxide charge density is $2.1 \times 10^{11}/cm^2$.

All detector processing steps, with the exception of the ion implantation, were carried out in BNL's class 100 cleanroom. The photoresist used was ETI 825 positive resist. The photoresist was applied on both sides of the wafer by a photo resist spinner system (Headway Research, Inc. Model MD-EC101D-CB15). The double-sided lithography was realized with the use of a mask aligner that had infrared backside illumination and an infrared viewer. The photoresist developer we used was the ETI 809. Al masks and final metallization were sputtered in a dc sputtering system which has an Al source containing 2% silicon. Sintering was done by a rapid thermal process (RTP) unit (Process Products Corp. Model PTM-2016-M-2F-FC).

IV. FABRICATION

Fig. 3 shows the major processing flow chart of the double-sided planar process technique developed for the fabrication of the CDD[7]. Oxide passivation was achieved by thermal oxidation in three steps called oxide C with a mixture of dry oxygen and TCA (trichloroethane). The resulting thickness of silicon dioxide is 4500 Angstroms. The oxide C is the best among all different oxidation conditions, as shown in Table I. It had the highest minority carrier generation lifetime compared with others and had relative lower flat band voltage and small stretch-out with relative thicker oxide. It was believed that the intrinsic gettering had happened in the oxide C process, resulting in a defect free zone beneath the surface[8].

The photolithographic step was done by the infrared mask aligner which enabled the double-sided lithograph step for opening of the windows in the oxide. In order to protect the wafer from possible contamination and damage from high energy ion bombardment during the implantation, a thin oxide layer of about 1000 Angstroms was left in the ion implantation window. The comparison of leakage currents between the diodes made by implanting through the thin oxide layer and that made by implanting directly into silicon (control samples) are listed on Table II. We can see that there is much less leakage current in the

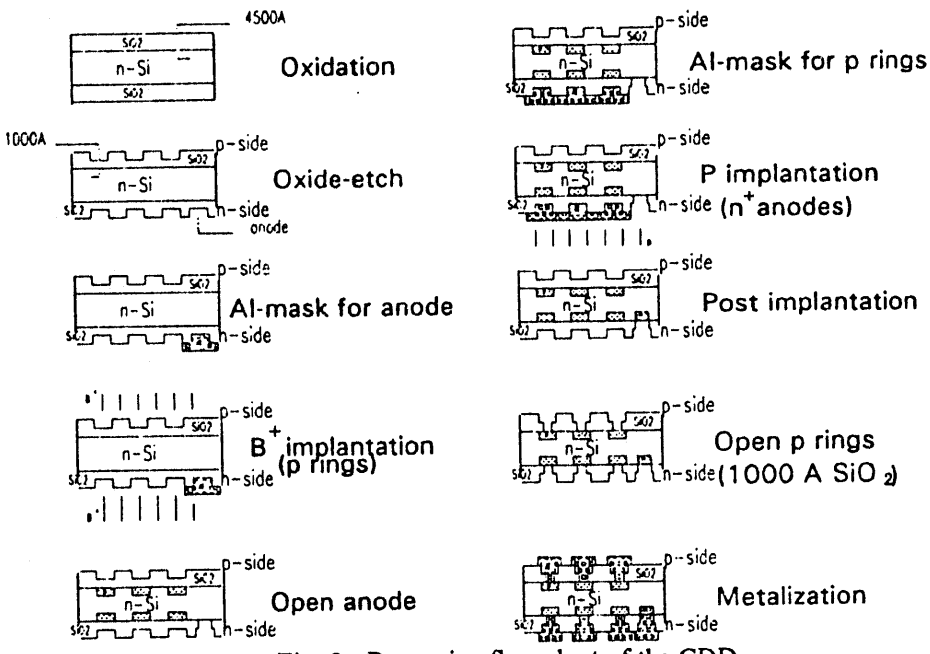


Fig. 3. Processing flow chart of the CDD.

Table I. Comparisons among various oxidations.

Oxide	Condition	V_{Fb} (V)	δV_{Fb} (V)	N_{ox} (Cm^{-2})	N_{it} (cm^{-2})	τ (ms)	Oxide Thickness (Å)
A	975°c, 18hrs O_2 975°c, 2hrs N_2	-8.40	0.70	$5.43x10^{11}$	$4.53x10^{10}$	1.10	3350
C	1100°c, 6hrs O_2+TCA 700°c, 16hrs O_2+TCA 1000°c, 5hrs O_2+TCA 1000°c, 2hrs N_2	-3.10	0.23	$1.39x10^{11}$	$0.89x10^{10}$	4.92	4573
B	1030°c, 4hrs O_2+TCA 1000°c, 1hr N_2	-2.60	0.30	$2.46x10^{11}$	$2.84x10^{10}$	1.57	2043
D	1200°c, 20hrs O_2 1000°c, 2hrs N_2	-8.60	0.90	$1.95x10^{11}$	$2.04x10^{10}$	0.92	9340

ones made by implanting through the thin oxide layer than those implanted directly into silicon. In the table, the average leakage current referred to is for 350 μm thick wafers. Another advantage of having such a thin layer of oxide is to prevent a short circuit that could be produced by the contamination during the implantation process. Fig. 4 demonstrates how this thin layer of oxide can prevent a short circuit effect. This thin layer of oxide also prevents the absorption into the silicon of fast diffusion metallines (C_u, C_r) that can be sputtered onto the wafer during ion implantation from surrounding fixtures.

There were three groups of the CDD fabricated. In the first group there was no 1000 Angstroms oxide layer

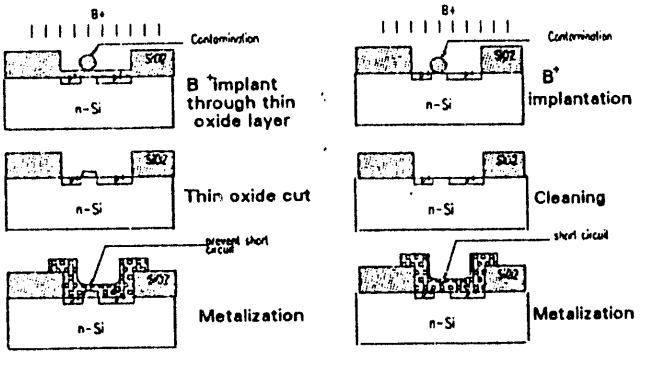


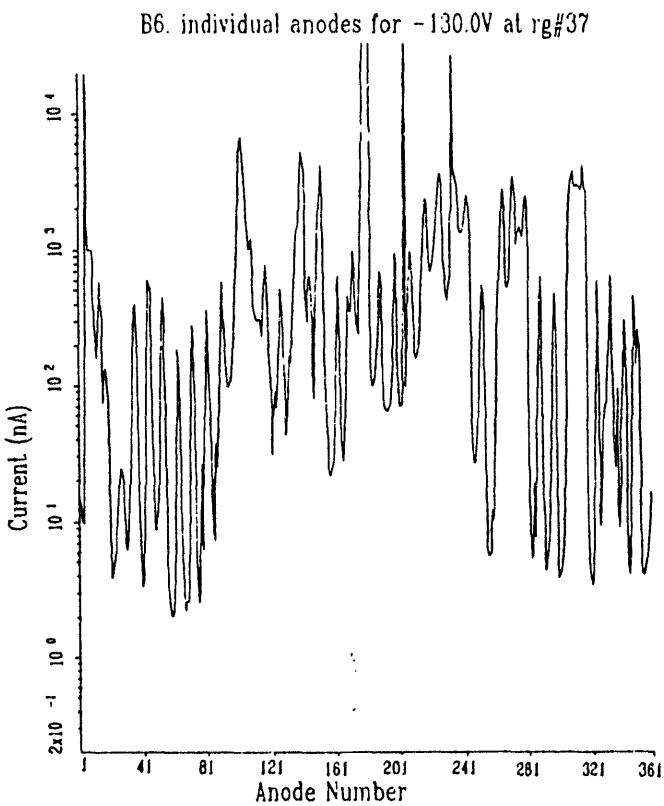
Fig. 4. Illustrations of the advantage of using the method of implanting through an oxide layer.

Table II. Leakage current decrease for detectors implanted through oxide.

#	B^+ implant through	Sheet Resistance	Average Leakage Current I at 100V (nA/cm^2)	$\frac{I}{I_C}$
		B(Ω/□)	0.25cm^2dot	
1000	control	1.15K	115.onA/cm^2	13.9%
	400A	1.65K	16.onA/cm^2	
1001	control	1.2K	145.onA/cm^2	9.9%
	500A	1.85K	14.4nA/cm^2	
1002	control	1.4K	88.onA/cm^2	12.6%
	600A	2.45K	11.1nA/cm^2	
1003	control	1.52K	150.onA/cm^2	14.0%
	700A	2.86K	21.onA/cm^2	

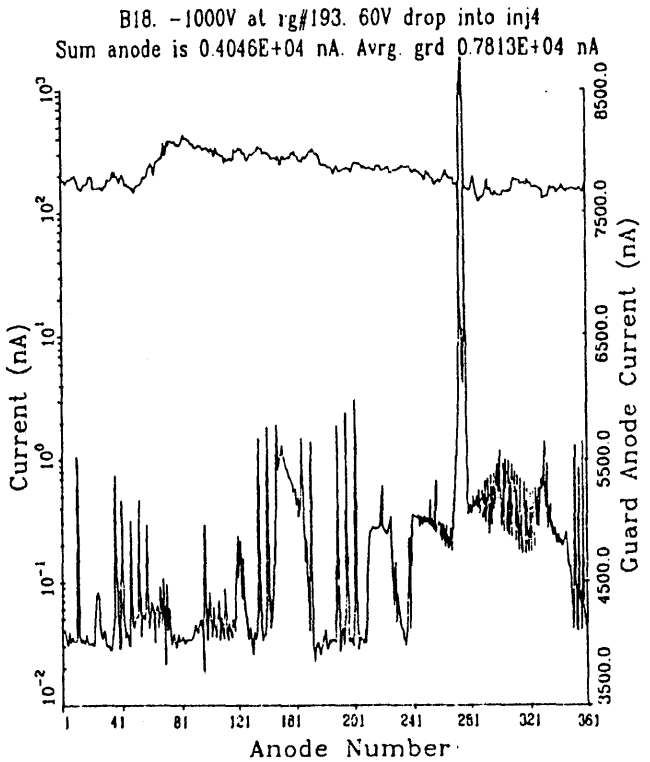
for protection, while in the second group the protective oxide layer was introduced and the third group followed the same process steps as those for the second group. Since both the anode and the p-ring were built on the one side of the wafer usually called the n-side, two extra protection masks were needed on the n-side to implant the boron and the phosphorus separately. Therefore on the n-side two additional steps were required to make the 2500 Angstroms thick Al protection masks before each boron and phosphorus ion implantation. The first group produced six detectors, but test results showed the existence of the problem as shown in Fig. 5(a). It shows many anodes with high leakage currents. The implantation mask used in this group is a positive photoresist mask (instead of Al), which may introduce pinholes and contaminations. In the second and third group of fabrication, an Al implantation mask was used. The overall improvement of the detector performance can be seen in Fig. 5(b), which shows lower leakage current as compared to Fig. 5(a). This indicates that the pinhole free Al mask production is an important step in a two sided detector fabrication process.

After opening the windows on the oxide and making the Al protection mask, the wafers were ready to be sent out for implantation. Boron ion implantation was used for the p-type junction at an energy of 60 keV, and a dose of $0.75x10^{13}$ /cm^2. The low dose was used to ensure a required value of 7k Ω/□ for the voltage divider resistors. The boron activation plot is shown in Fig. 6, on which the 600°C and 800°C curves are illustrated. In order to be able to anneal at 700°C, as the following paragraph demonstrates, the value



a) First batch.

Fig. 5. Leakage current through each of the 360 anodes for the CDD detector.



b) Second batch.

Fig. 5. Leakage current through each of the 360 anodes for the CDD detectors.

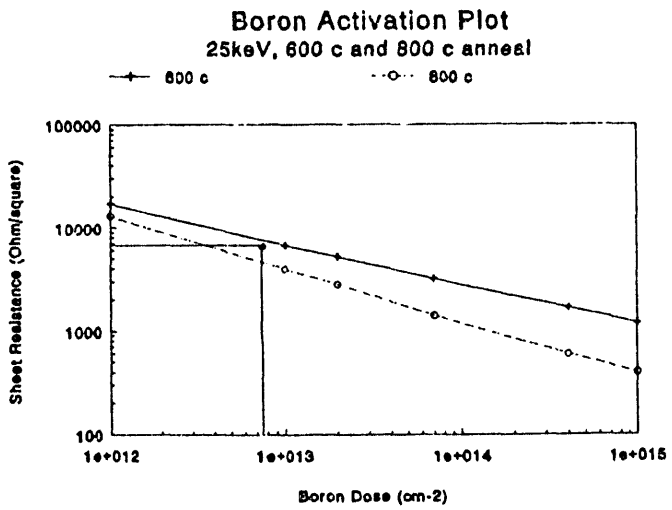


Fig. 6. Sheet resistance as a function of the boron fluence.

of 0.75×10^{13} /cm^2 was chosen to obtain a 7k Ω/□ sheet resistance.The anode was implanted using phosphorous at an energy of 50 keV and a dose of 1×10^{14} /cm^2.

Post implantation annealing was done in the thermal furnace at 700°C for 30 minutes in a dry nitrogen atmosphere. From Fig. 7 we can see that 700°C is the lowest temperature at which the sheet resistance is stabilized. Higher temperatures increase risk of introducing impurities or activating other ions produced by the implantation.

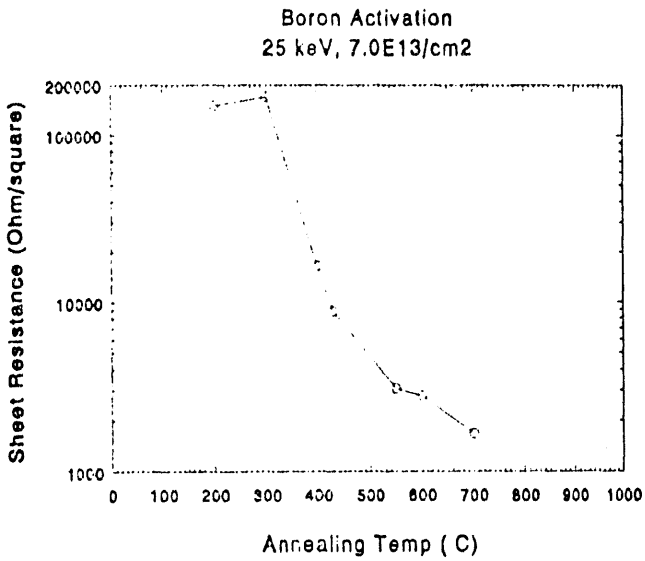
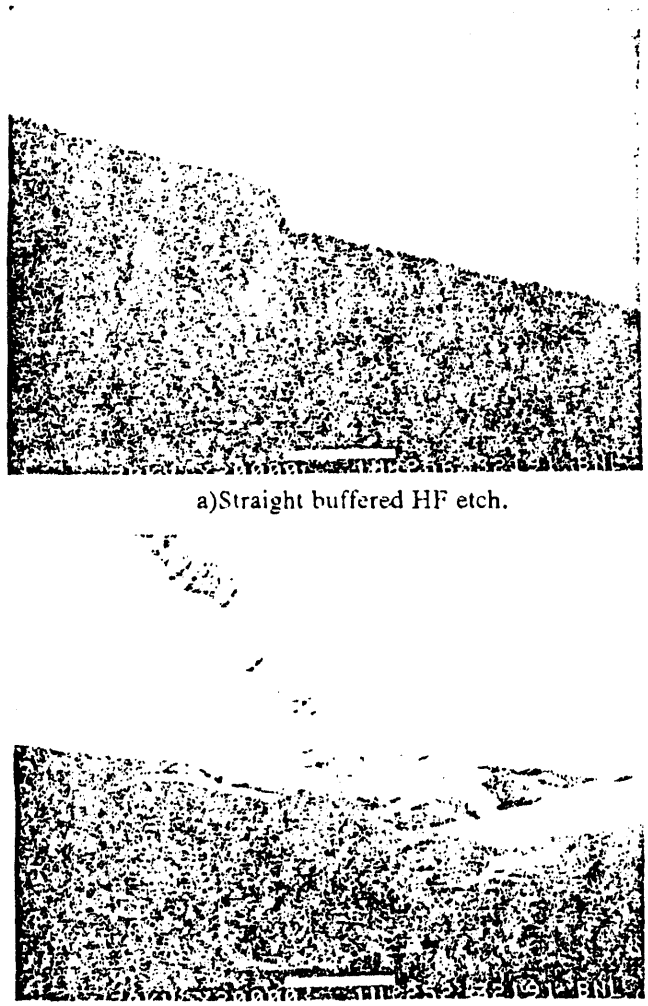


Fig. 7. Activation of boron implants.



a)Straight buffered HF etch.

b) Diluted HF (H_2O: buffered HF = 10:1) etch.

Fig. 8. SEM pictures of the etched oxide steps.

After post implantation anneal, an additional cut of 1000 Angstroms oxide was performed on both sides with diluted (10:1) buffered HF solution. In the first group of fabrication we used straight buffered HF solution for oxide cut. In the second group we changed to a 10:1 diluted buffered HF for oxide cut. Diluted buffered HF, used during the oxide step cut, is another factor improving overall performance of the CDD, since it gives an inclined edge of oxide which can prevent spiking in a later stage of the fabrication and gives a more gradual Boron implant concentration at the junction edge. Spiking is most likely to happen near the oxide cut edge. Fig. 8 shows the cross section of the oxide cut in different etching solutions as seen through an electron microscope. Fig. 8(a) shows the steep cut edge from the pure buffered HF etching and Fig. 8(b) shows the inclined cut edge from the diluted HF etching.

Metallization was done by sputtering Al, containing 2% Si, and was followed by a RTP sintering step to avoid spiking[9]. The use of the Al-Si alloy and short sintering time serves to eliminate the spiking problem. Since silicon diffusion into Al polycrystalline film is the mechanism causing spiking[10], a saturated silicon concentration in the Al results in a less amount silicon to diffuse into the Al; a shorter annealing time results in a shorter diffusion distance for silicon traveling into the Al; this occurs since the distance(d) silicon travels inside aluminum is $d = \sqrt{Dt_a}$, (where D is the diffusion coefficient of silicon and t_a is the annealing time) and therefore less spiking results.

V. DISCUSSIONS AND SUGGESTIONS

The difficulty of the fabrication process for the CDD is the need of special care on handling the overall surface area of the entire 3 inch wafer during each step. The active area of the detector is so large that the local contamination may cause local defects which can change the distribution of the electrical potential inside the Si bulk, and this in turn may compromise the high performance of the detector. Therefore inspection and necessary "surgery" after each critical process are required.

Important improvements of the double-sided planar process in this CDD fabrication are the introduction of aluminum implantation mask and the remaining 1000 Angstrom oxide layer in the p-window during the implantation, which is expected to protect the window area from the damage and contamination during high energy ion bombardment. This oxide layer should be thick enough to prevent 50 keV phosphorus ions (anode implantation) from being implanted into the p-type junctions even if there are pinholes on the aluminum protection mask. Therefore this thin oxide actually reduces the probability of the formation of pinholes which can only happen in the case that the pinholes on the aluminum mask and those on the thin oxide layer are aligned to each other.

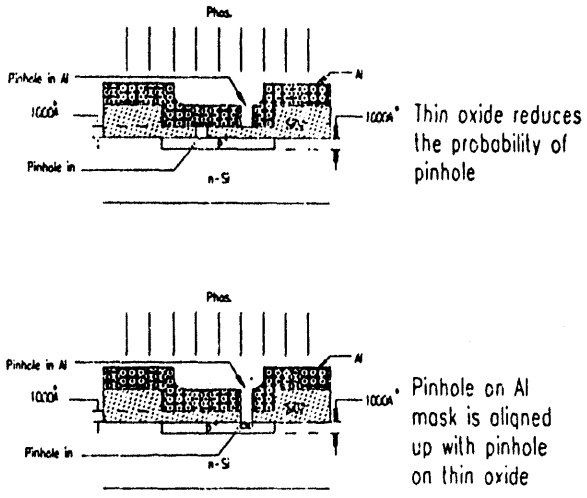


Fig. 9. Illustration of the advantage of using an Al mask.

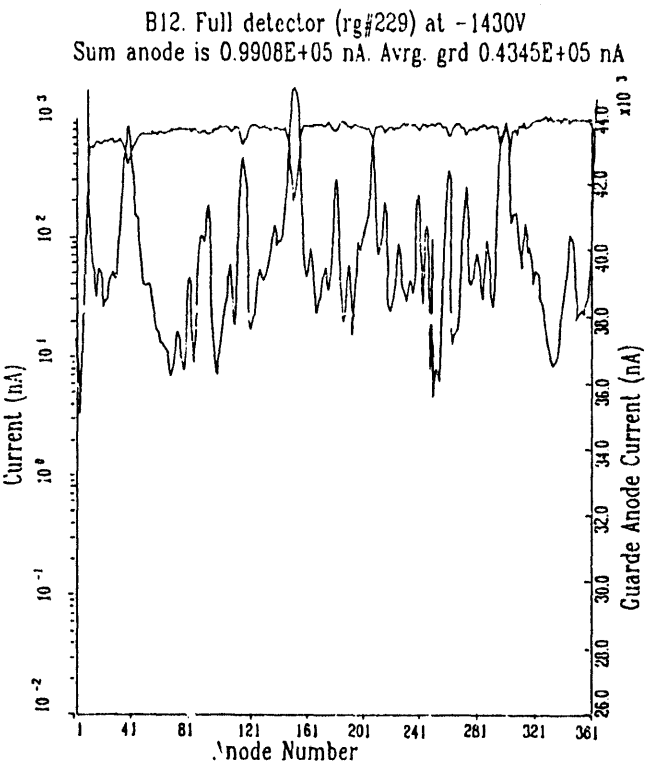


Fig. 10. Full detector(B12) characteristics at V=-1430V.

A graphic demonstration is shown in Fig. 9. The energy of the phosphorus ions should be such as to prevent phosphorus ions from penetrating through the depth of existing p-type junctions even if the pinholes on the aluminum protection mask aligned up with the ones on the thin oxide.

We have run three groups of the CDD fabrications. Following the improvement steps of the second group, we repeatedly produced successful detectors in the third group. The test result showed that for the best detector in Fig. 5(b), most of the signal anodes have the leakage currents of about

0.3 nA/cm^2. From this number one can calculate a generation lifetime of 80ms. Those results indicate that a surface component has been successfully surpressed by the "rivers" and does not appear at anode. Those values prove the fabrication method and the idea of structure design such as "river" to be sufficient.

Detectors B12 and B25 have been installed in the NA45 experiment at CERN. Detector B12 with 360 readout-channels was tested in 1991, but it had defects of about 20% of the total area, mainly due to an insufficient center hole cut method. Fig. 10 shows full detector operation at -1430V. During the ^{32}S- and P-beam time in 1992, an improved version of the CDD B25 was installed. It is now completely operational with remaining defects less than 3% and compares well with expectations. Fig 11 shows the full detector operated at -1392V. The laser test results and the performance under beam conditions will be separately reported.

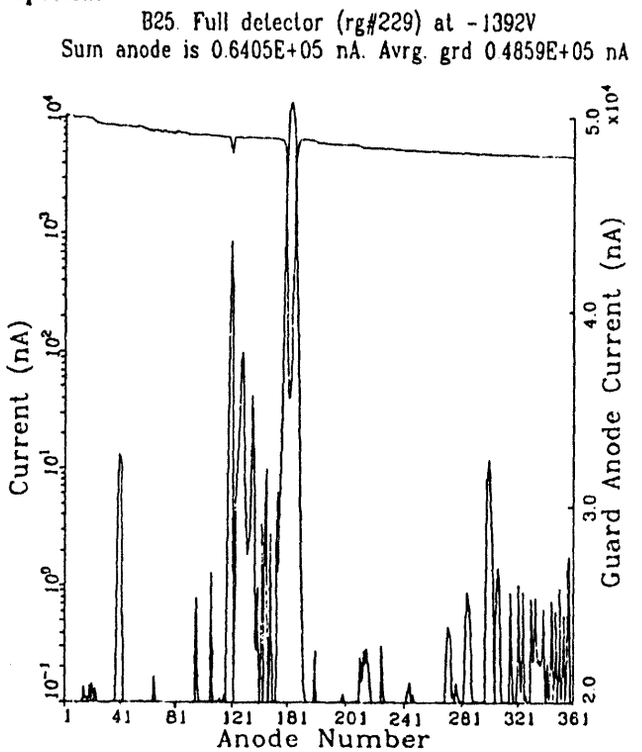


Fig. 11. Full detector (B25) characteristics at V=-1392V.

We would like to conclude with the following suggestions: First, the wet aluminum etching step is usually accompanied by a little overetching, because of the results of isotropic etching, therefore compensation must be made for the line width lost in transferring the mask pattern to the etched metal. The minimum width of aluminum mask design should be larger than 4 micrometers. Secondly, the smaller the area of the oxide step cut, which is the aluminum contact region, the better it is for the elimination of the defects. Third, we believe that lift off technology can also be applied to some fabrication steps to avoid misalignment when higher accuracy is required. The lift-off technique can also reduce the number of mask steps in the detector production. Finally, there is good reason to believe that larger area , 4 inch diameter drift devices might be fabricated in the future.

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