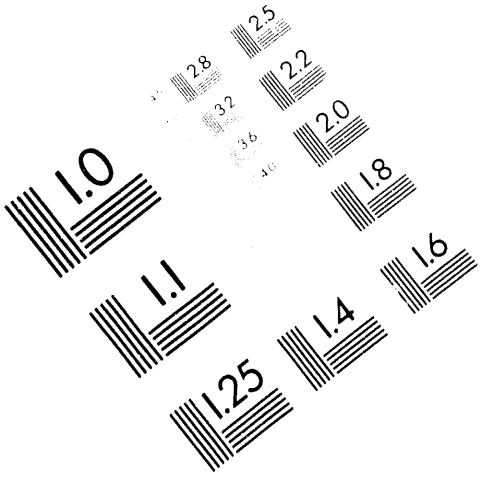
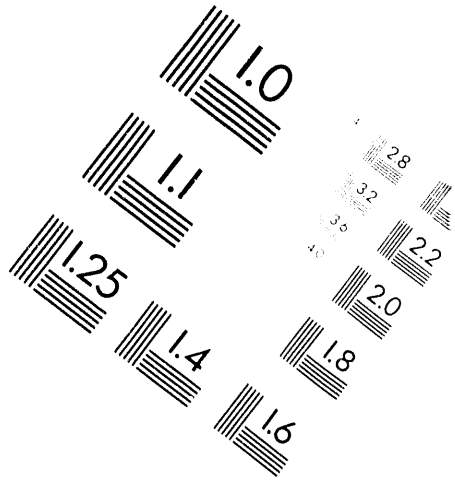
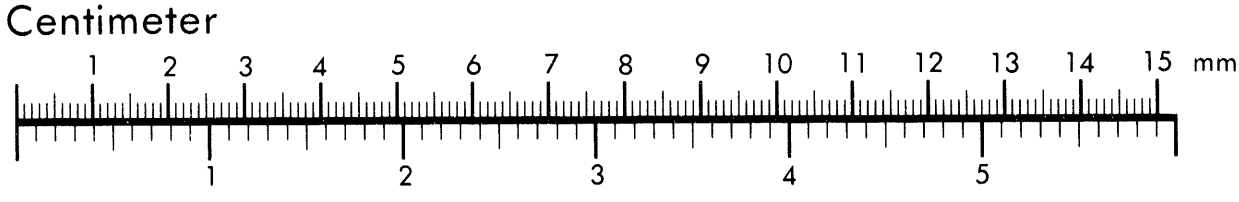
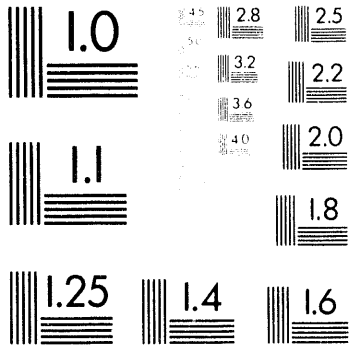


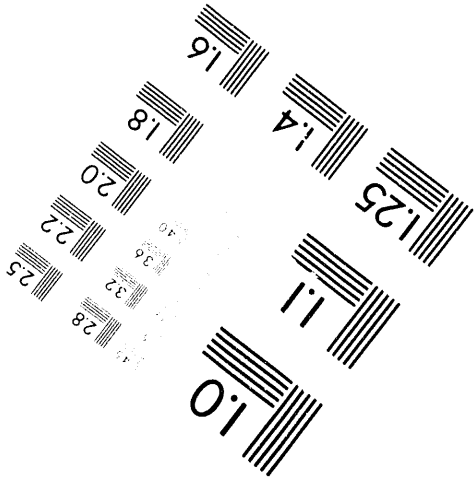
Association for Information and Image Management

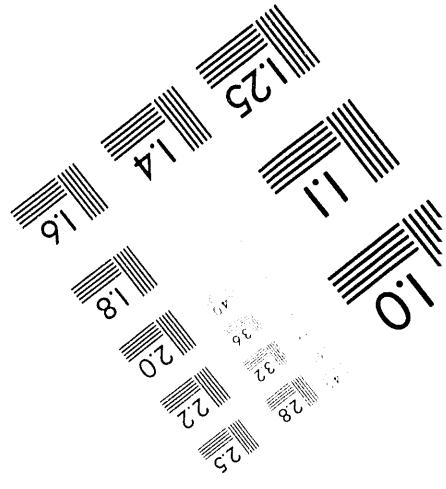
1100 Wayne Avenue, Suite 1100
Silver Spring, Maryland 20910
301/587-8202











MANUFACTURED TO AIIM STANDARDS
BY APPLIED IMAGE, INC.

1 of 1

Final Report
Support for Development of a Custom VLSI and FPGA Logic Chips based on a VHDL Top-Down Design Approach

Subcontract Number:
2676L0013-9Q

Prepared by:
InnovASIC, Inc.
1107 Woodland NW.
Albuquerque, NM 87107

Prepared for:
University of California
Los Alamos National Laboratories
SST-11
P.O. Box 990
Los Alamos, NM 87545

Abstract

The objective of this contract was to perform the beginning stages of development for two Application Specific Integrated Circuits: CMOS-1 and CMOS-2D. This work includes specification writing, behavioral modeling, and beginning design. In addition, the design work is required to be done in the VHSIC Hardware Description Language (VHDL).

InnovASIC, Inc. completed all the tasks required of this contract. The specifications were written, VHDL for CMOS-1 was completed, a behavioral model of CMOS-2D was written, and a system simulation was performed.

Contract Objectives

This section describes the objectives as defined in the Statement of Work, and the accomplishments toward achieving each objective.

I. Methodology Development. This task required the development of a design methodology that was used in the remaining tasks.To achieve this objective, InnovASIC, Inc. wrote a document named Development Plan for the CMOS-1 ASIC. This document is included in Attachment 1.

II. Specification Generation. This task required the development of a specification that describes the functional requirements of the CMOS-1 ASIC. InnovASIC, Inc. wrote a specification named Specification for the CMOS-1 ASIC to accomplish the objective.This document is included in Attachment 2.

III. Partitioning. The partitioning task was to result in the breakdown of the design into pieces that are codable and synthesizable in VHDL.Although no formal documents were developed for this task, the partitioning can be seen from the VHDL code structure.

IV. CMOS-1 RTL Model Development.This task was the major task of the contract. It required writing VHDL code for each of the partitions described above, simulating each piece individually, tieing all the pieces together, and simulating the whole entity. This was accomplished by coding the VHDL on a Personal Computer, simulating each piece using the Model Technologies Simulator, writing a Test Bench in VHDL, and simulating the entire design. The following figure shows the file structure used to create the design.

Testbench testbnch.vhd	Top-level CMOS-1 c1_func.vhd	Input Stage in_stg.vhd				
		Data Driven Storage dds_top.vhd	DDS entity dds_ent.vhd	Timetag counter timetag.vhd		
				Mode Control modecntl.vhd		
				Storage stor_ent.vhd	counter cnt3_ent.vhd	
					comparator comp_ent.vhd	
					memory mem_ent.vhd	
		Compression Engine compress.vhd	compression register compreg.vhd			
			header builder header.vhd			
			edge detector edge_ent.vhd			
			hit detector hitlogic.vhd			
			edge counter edgcount.vhd			
			block counter selcount.vhd			
			input mux mux16.vhd			
			compression controller compcntl.vhd			
		Output Stage out_stg.vhd	read out controller rd_cntl.vhd			
			ouput buffer omem_ent.vhd			
			Hit tracker hitrckr.vhd			
			Buffer write control wrt_cntl.vhd	Write address generator wadd_ent.vhd	address counter cnt5_ent.vhd	
						Math Package math_pak.vhd

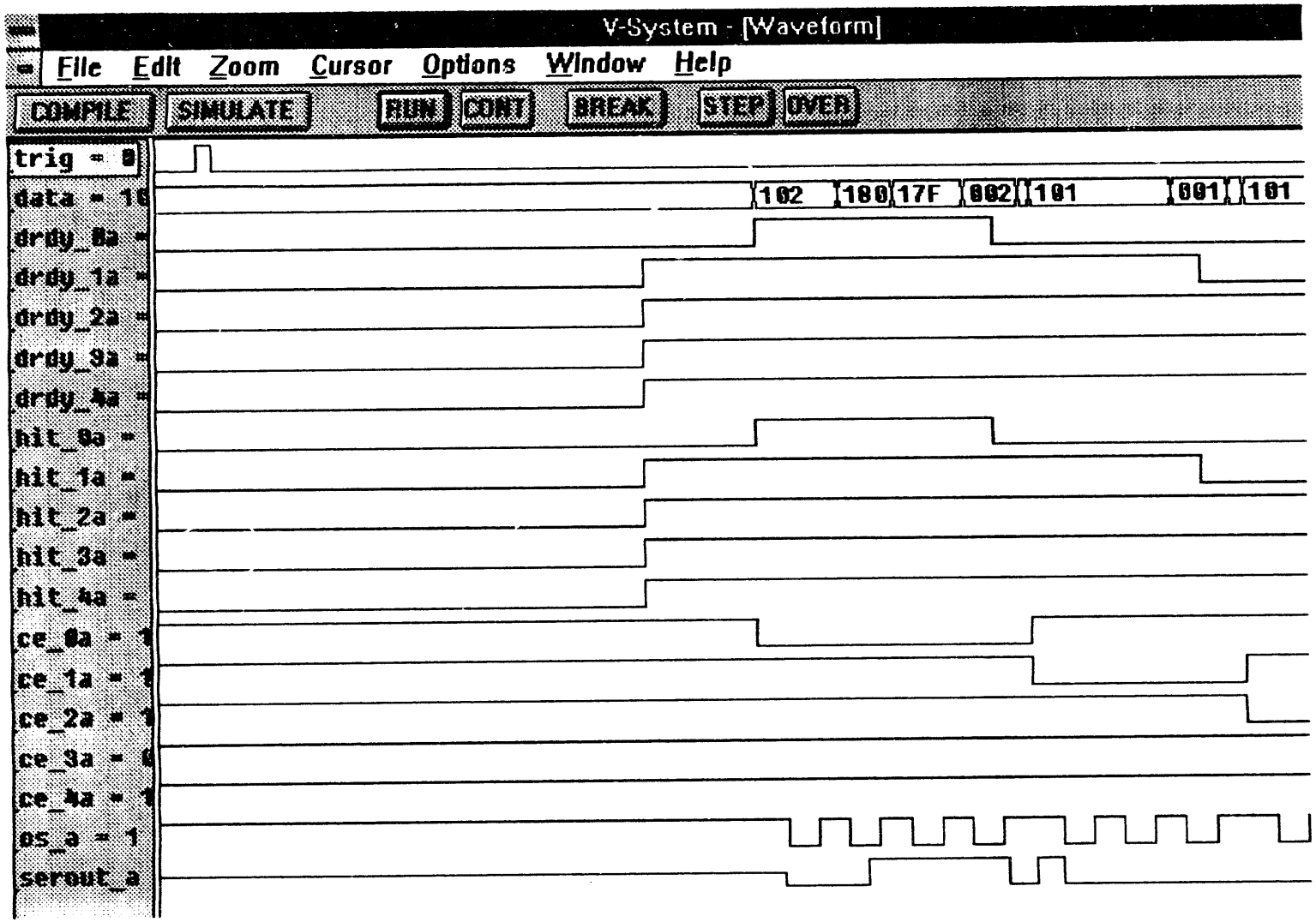
Extensive simulations were run on the VHDL code to make sure the design met LANL's requirements. This was reviewed during the code review as described below. A partial simulation result is shown in the following diagram. In addition to the above code, JTAG code for the CMOS-1 chip was generated. This code was not fully tested or integrated into the entire simulation.

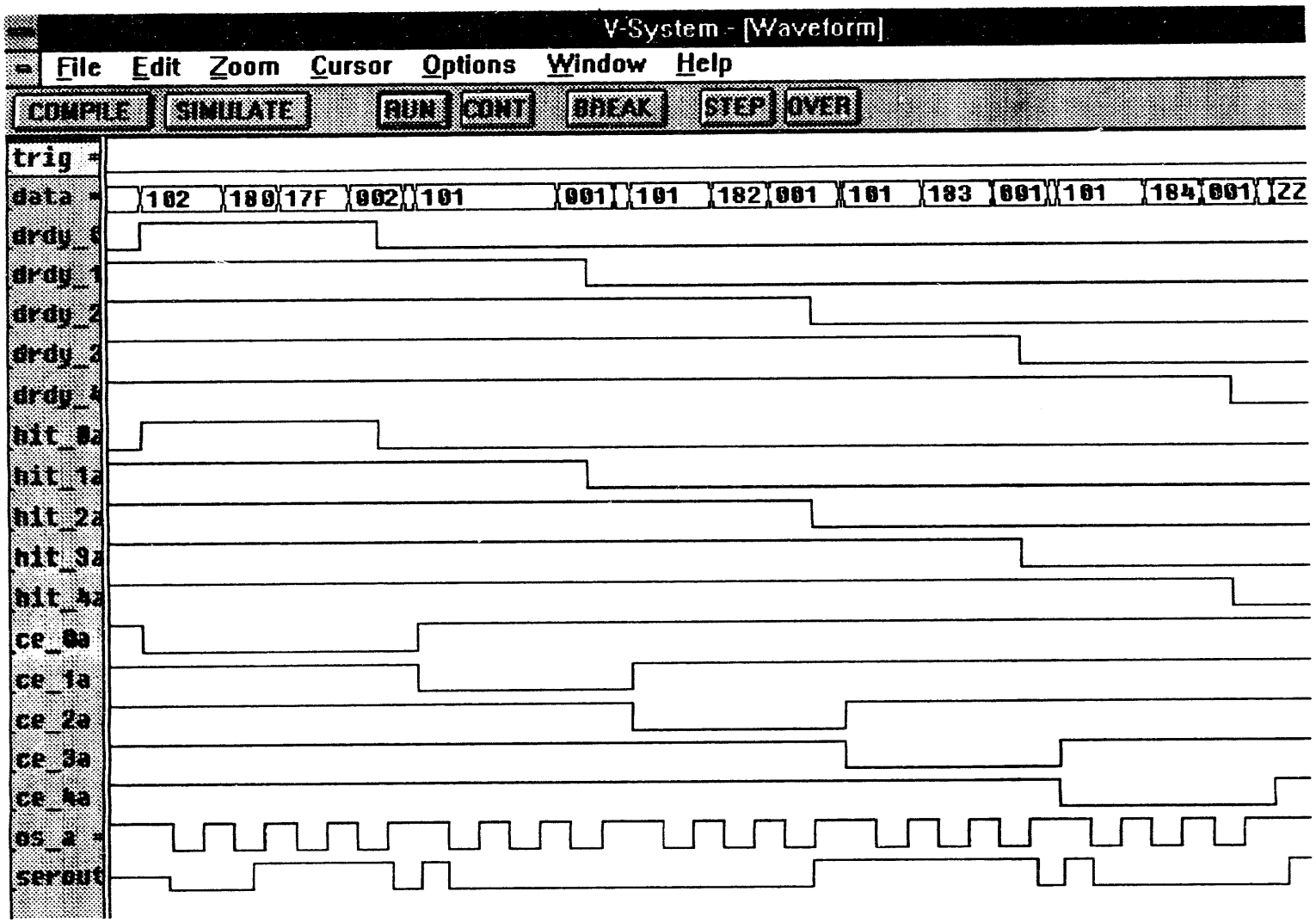
All code generated is contained on the floppy disk delivered with this document, as well as printed in Attachment 3.

V. CMOS-2 Specification Generation. This task entailed generating a preliminary specification for the CMOS-2D ASIC. InnovASIC, Inc. wrote a specification named Specification for the CMOS-2D ASIC to accomplish the objective.This document is included in Attachment 4.

VI. CMOS-2 Behavioral Model/System Simulation. This task was the culmination of the effort for the contract. The first objective was to write, in VHDL, a behavioral model of the CMOS-2D chip. The second objective was to modify the testbench to tie the CMOS-2 behavioral model together with 5 instantiations of the CMOS-1 model, and simulate the two together. InnovASIC completed the task using the Model Technologies Simulator on a Personal Computer. The following file structure under the CMOS-2 directory was used for this:

Test Bench testbnch.vhd	CMOS-1 model c1_func.vhd	As shown above
	CMOS-1 behavioral model behave.vhd	


V-System - [Waveform]
File Edit Zoom Cursor Options Window Help
COMPILE SIMULATE RUN CONT BREAK STEP OVER
trig = 0
data = 16
drdy_0a =
drdy_1a =
drdy_2a =
drdy_3a =
drdy_4a =
hit_0a =
hit_1a =
hit_2a =
hit_3a =
hit_4a =
ce_0a = 1
ce_1a = 1
ce_2a = 1
ce_3a = 0
ce_4a = 1
os_a = 1
serout_a
102
100
17F
002
101
001
101


V-System - [Waveform]
File Edit Zoom Cursor Options Window Help
COMPILE SIMULATE RUN CONT BREAK STEP OVER
trig
data
drdy_0
drdy_1
drdy_2
drdy_3
drdy_4
hit_0a
hit_1a
hit_2a
hit_3a
hit_4a
ce_0a
ce_1a
ce_2a
ce_3a
ce_4a
os_a
serout
102
180
17F
002
101
001
101
182
001
101
183
001
101
184
001
ZZ

VII. Design Reviews

3 Design reviews were held at Los Alamos National Laboratories. The first was the Specification review held on July 28, 1993. The objective of this was to review the CMOS-1 specification to ensure that it meet LANL's needs.

The second review was the code review held on September 1st. The objective was to review the CMOS-1 code and simulation results of the CMOS-1 VHDL model. The code structure was reviewed and a simulation was run at LANL's site.

The third review was held on September 30, and was a final review. The objective of the review was to go over the CMOS-2 simulation results and cover any issues related to what is needed for completion of the ASIC design. The simulation results were reviewed, and the issues as shown in the Issues section of this document were discussed.

Deliverables

The following is a list of items delivered for this contract. All of them have been included on the floppy disk included with this document.

I. Development Plan. Included in this document as attachment 1, and on the floppy in WordPerfect 5.1 format.

II. CMOS-1 Specification. Included in this document as attachment 2, and on the floppy in WordPerfect 5.1 format.

III. Vendor study Statement of Work. Included in this document as attachment 5, and on the floppy in WordPerfect 5.1 format.

IV. CMOS-2 Specification. Included in this document as attachment 4, and on the floppy in WordPerfect 5.1 format.

V. VHDL code. Included in this document as attachment 3, and on the floppy in ASCII text format.

VI. Simulation Files. Files included in the ./source/test directory on the floppy with an extension of .do are the files used to simulate the individual entities of the design. The file ./source/test/testvect.txt contains the test vectors used to simulate the CMOS-1 design. The file ./cmos2/testvect.txt contains the test vectors used to simulate the CMOS-1/CMOS-2 system.

Issues

I. Tasks needed to be completed for a final ASIC design

A. The JTAG code must be completed and integrated with the rest of the CMOS-1 code.

B. The specifications should be scrubbed thoroughly and revised.

C. The CMOS-1/CMOS-2D system should be reviewed to determine if the manner it is handling hit and trigger overloads is adequate. There is a question whether the system will perform well if more triggers are received than can be processed.

D. The CMOS-2 synthesizable VHDL needs to be written.

E. Area studies should be performed on both CMOS-1 and CMOS-2.

F. The handling of adders needs to be modified to fit into Mentor Graphics synthesis scheme.

G. Full VHDL simulation with both CMOS-1 and CMOS-2 synthesizable code should be run.

H. Synthesis, gate simulation, layout, etc.

II. The interface between the analog and digital portions of the system are not completely defined. This needs to be faced before the entire system can be finished.

DATE
FILMED
7/8/94
END