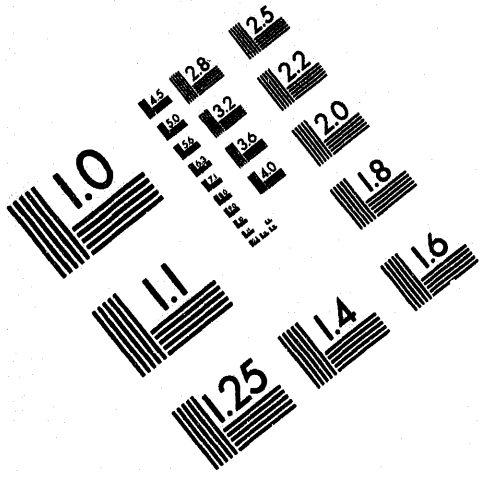
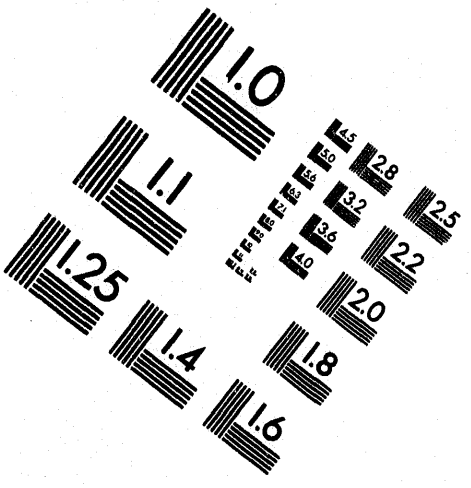
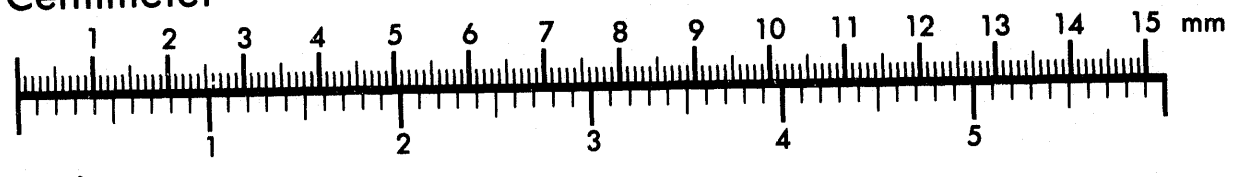
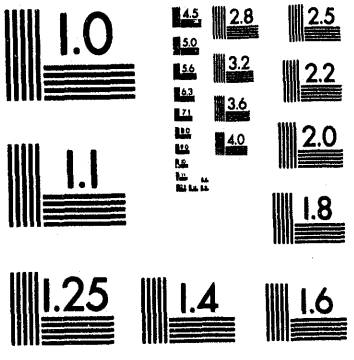
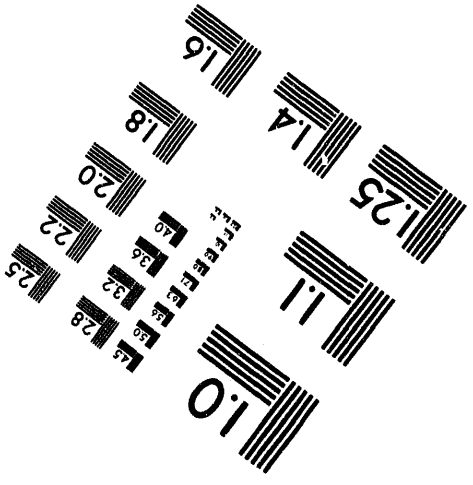


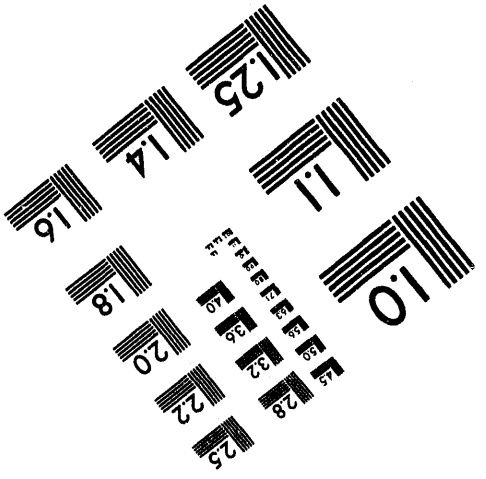
Association for Information and Image Management
1100 Wayne Avenue, Suite 1100
Silver Spring, Maryland 20910
301/587-8202











MANUFACTURED TO AIIM STANDARDS
BY APPLIED IMAGE, INC.

1 of 2

Basic Mechanisms of Radiation Effects in the Natural Space Radiation Environment

James R. Schwank
Sandia National Laboratories
Albuquerque, NM 87185-1083

This work was supported by the U. S. Department of Energy through contract number DE-AC04-94AL85000.

Basic Mechanisms of Radiation Effects in the Natural Space Environment

James R. Schwank
Sandia National Laboratories
Radiation Technology and Assurance Department

1.0 INTRODUCTION

Electronics in a satellite system can be degraded significantly by the natural space radiation environment. A major goal of the radiation effects community has been to provide devices that can function as intended in the harsh environment of space. This has required the development of process techniques to fabricate radiation-hardened devices and the development of reliable, cost-effective hardness assurance test procedures. To qualify a device for use in a space system, one must rely on laboratory measurements typically at dose rates from 50 to 300 rad/s in which the radiation exposure may take only minutes to hours to complete. These laboratory measurements must be correlated to a space environment in which the radiation

exposure may take place over a period of many years. To make these correlations, it is necessary to have a thorough understanding of the mechanisms that govern the radiation response of the devices to be used. This is especially true for systems employing commercial, non-radiation-hardened devices where the margin between system requirements and device capability is much lower than for radiation-hardened devices. Thus, as commercial devices become increasingly more popular, the need for understanding radiation-response mechanisms becomes increasingly more important. Knowledge of the mechanisms of device radiation response has also enabled the fabrication of radiation-hardened devices. Therefore, understanding the basic mechanisms of radiation effects is of practical importance to the system, design, and technology engineer.

In this portion of the Short Course, the basic mechanisms of radiation effects in the natural space environment are presented. The primary manners in which the natural space environment can cause degradation of electrical devices and systems are through total-dose ionizing-radiation damage, single-event related soft and hard errors, and displacement damage. Of these three, I cover total-dose and single-event effects. The goal of this portion of the course is to provide the student with the basic knowledge required to understand the mechanisms underlying the development of hardness assurance test guidelines and hardened-process technologies. Knowledge of the mechanisms will give the student more confidence in applying hardness assurance test guidelines for space and other applications. This portion of the Short Course is also intended to set the stage and provide the fundamentals for the remainder of the Short Course. Although the material presented focuses on device response in the natural space environment, much of the material presented is also applicable to the mechanisms of device response at short times after a pulse of irradiation (e.g., weapon application) and device response for moderate-dose-rate exposures.

We begin with a description of the natural space radiation environment. This is the first step in determining the mechanisms governing device response. The mechanisms of device response depend on the type, energy, and concentrations of particles present in the space environment. The second step is to study the manner in which the particles interact with materials. For instance, protons can cause total-ionizing-radiation damage, single-event upset, and displacement damage. On the other hand, electrons cause primarily total-dose ionizing radiation damage and high-energy ions cause primarily single-event soft and hard errors. Once the manner in which radiation interacts with materials is determined, the third step is to determine the mechanisms that govern the response for the device type of interest for the particle(s) of interest. I focus in this portion of the Short Course on the mechanisms that govern the total-dose response of MOS devices. MOS devices constitute a major portion of the electronics of nearly all modern space systems. The material presented can be applied to the understanding of both commercial and radiation-hardened device response. Knowledge of the mechanisms that govern MOS device response can also be used to understand the mechanisms governing a number of other device types, including SOI and SOS devices and leakage current in advanced bipolar integrated circuits. I present the mechanisms of MOS device response at short times following high-dose-rate irradiations. Although knowledge of the short time response is not important for characterizing low-dose-rate space irradiations, the short-time response provides insight into the mechanisms governing radiation effects in both high- and low-dose-rate environments. Examples of case studies where knowledge of the basic mechanisms of radiation

effects has led to technological improvements in device hardening and in hardness assurance test methodology are presented. I next discuss the basic mechanisms of device response for two device types that may see increased commercial use in the future: SOI and nitrided oxide devices. Finally, I cover the basic mechanisms of charge collection in silicon and GaAs devices leading to single-event effects. Mechanisms are covered at the transistor level. The mechanisms for heavy-ion induced single-event burnout and single-event gate rupture are also discussed.

2.0 NATURAL SPACE RADIATION ENVIRONMENT

The natural space environment can cause damage to electronic systems in a number of ways. It contains high energy protons and electrons that can cause total-dose ionizing radiation-induced damage. Protons can also cause displacement damage. Heavy ions and high-energy protons can upset system operation and sometimes cause permanent damage to electronics. The concentration and types of particles vary significantly with altitude and angle of inclination, recent solar activity, and amount of spacecraft shielding. As such, it is nearly impossible to define a "typical" space environment. Particles present in the earth's natural space radiation environment can be grouped into two general categories: 1) particles trapped by the earth's magnetic field (primarily electrons and protons), and 2) cosmic rays: heavy ions and high-energy protons of galactic or solar origin. In this section, some of the general properties of the natural space environment are presented.

2.1 Particles Trapped by the Earth's Magnetic Field

The earth's magnetic field creates a geomagnetic cavity known as the magnetosphere [1]. The magnetic field lines trap low-energy charged particles. These trapped particles consist primarily of electrons and protons, although some heavy ions are also trapped. The trapped particles gyrate spirally around the magnetic field lines and are reflected back and forth between the poles where the fields are confined. The motion of the trapped particles is illustrated in Fig. 1 [1]. As charged particles gyrate along the magnetic field lines, they also drift around the earth with electrons drifting in an easterly direction and protons drifting in a westerly direction. The motion of charged particles forms bands (or domains) of electrons and protons around the earth and form the earth's radiation belts.

The boundaries of the domains at the equator are illustrated in Fig. 2 [1]. Distances are specified in earth radii (one earth radius is equal to 6380 km) referenced to the center of the earth, i.e., one earth radius is at the earth's surface. Because of the variation in the magnetic field lines with latitude, the boundaries of the domains vary with latitude (angle of inclination). Most satellites are operated in near-earth orbits at altitudes from slightly above 1 earth radius to 10 earth radii. Geosynchronous orbit (GEO) is at an altitude of approximately 35,800 km corresponding to approximately 6.6 earth radii. The domains can be divided into five regions. The trapped proton distribution exists primarily in regions one and two that extend from slightly above 1 earth radius to 3.8 earth radii. The distribution of proton flux as a function of energy and radial distance is given in Fig. 3 [1]. [Flux is the rate at which particles impinge upon a unit surface area. It is normally given in units of particles/cm^2-s. The time integral of flux is the fluence. Thus, fluence is equal to the total number of particles that impinge upon a unit surface

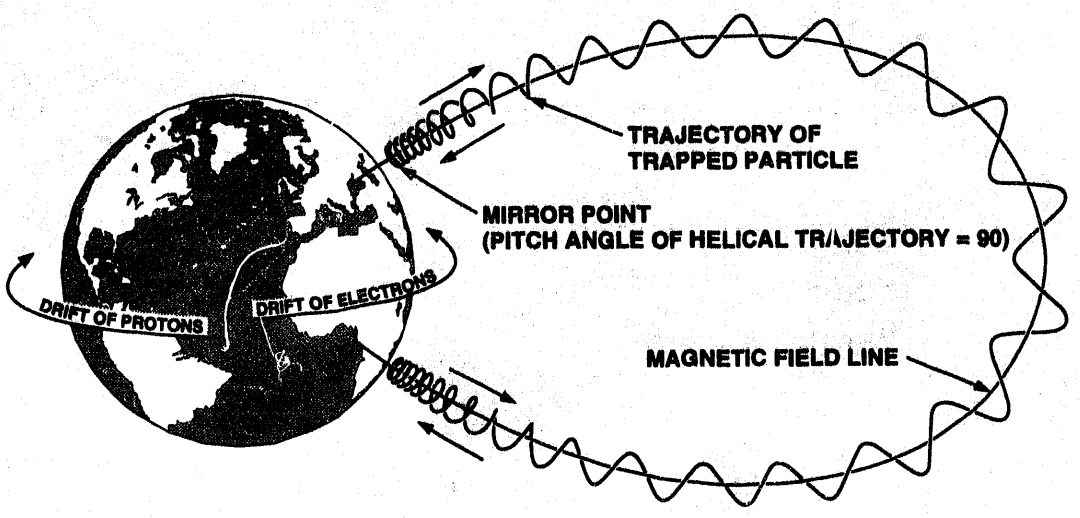


Figure 1: Motion of trapped particles in the earth's magnetosphere. (After Ref. 1)

area for a given time interval and it is normally given in units of particles/cm^2.] Trapped protons can have energies as high as 500 MeV [1]. Note that the altitude corresponding to the peak in flux decreases with proton energy for any given energy. Protons with energies greater than 10 MeV primarily occupy regions one and two below 3.8 earth radii [1]. Typical spacecraft shielding attenuates protons with energies below 10 MeV [2]. Thus, the predominantly low-energy trapped protons present above 3.8 earth radii are normally ineffective in producing radiation-induced damage. For proton energies greater than 30 MeV, the highest proton flux occurs at about 1.5 earth radii. Protons originating from solar flares (discussed below) are present predominantly in regions four and five (Fig. 2) and extend from ~5 earth radii to beyond 14 earth radii.

Above the Atlantic Ocean off the coast of South America the geomagnetic sphere dips toward the earth causing a region of increased proton flux at relatively low altitudes. This region is called the South Atlantic anomaly (SAA). In this region, the flux for protons with energies greater than 30 MeV can be as much as 10^4 times higher than in comparable altitudes over other regions of the earth. At higher altitudes the magnetic sphere is more uniform and the South Atlantic anomaly disappears [3].

Electrons are present predominantly in regions one to four and extend up to 12 earth radii [1]. The electron domain is divided into two zones, an inner zone extending to about 2.8 earth radii and an outer zone extending from 2.8 to 12 earth radii. The outer zone electrons have higher fluxes (~10 times) and energies than the inner zone electrons. For electrons with energies greater than 1 MeV, the peak in flux is located between 3 and 4 earth radii [4]. The maximum energy of trapped electrons is approximately 7 MeV in the outer zone; whereas, the maximum energy is less than 5 MeV for electrons in the inner zone [1]. At these energies electron interactions are unimportant for single-event effects, but must be considered in determining total-dose effects.

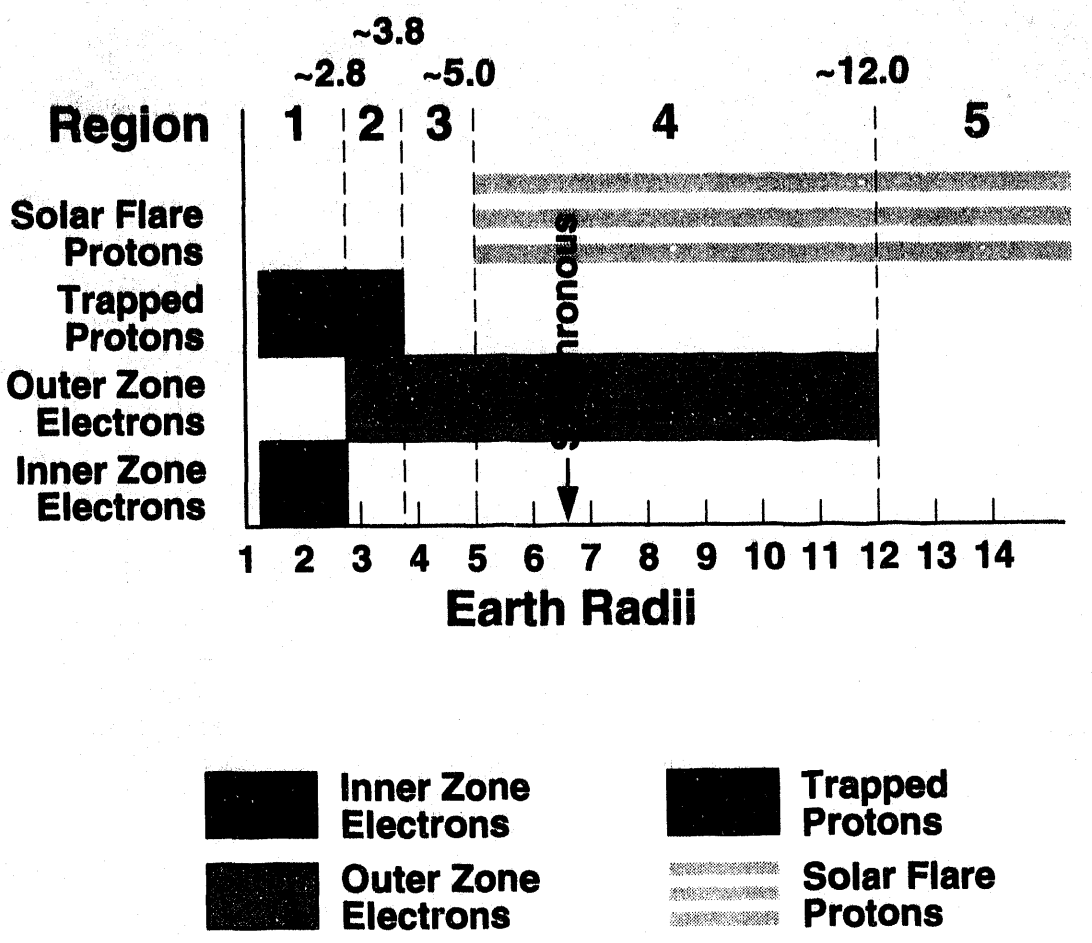


Figure 2: Boundaries of the domains for solar flare and trapped protons and outer and inner zone electrons. (After Ref. 1)

Fluxes of electrons and protons in particular orbits can be estimated from existing models. Two models that provide reasonable estimates of the proton and electron fluxes as a function of the satellite orbit are AP8 [5] for protons and AE8 [6] for electrons. An example of a calculation for a low earth orbit (LEO) (altitude of 500 km and latitude of 60 degrees) at solar minimum and maximum is presented in Fig. 4 [1]. Solar minimum and maximum refer to periods of minimum and maximum solar activity. Note that the flux of electrons decreases rapidly at high energies.

2.2 Cosmic Rays

Cosmic rays originate from two sources, the sun (solar) and sources outside our solar system (galactic). Galactic cosmic rays are always present. In the absence of solar activity, cosmic radiation is composed entirely of galactic radiation. Outside of our solar system, the spectrum of galactic cosmic rays is believed to be uniform. Its composition as a function of atomic mass is given in Fig. 5 [2,7]. It consists mostly of protons (85%) and alpha particles (helium nuclei) (14%). Less than 1% of the galactic cosmic ray spectrum is composed of high-energy heavy ions. This is not an indication that heavy ions are not as important as protons in

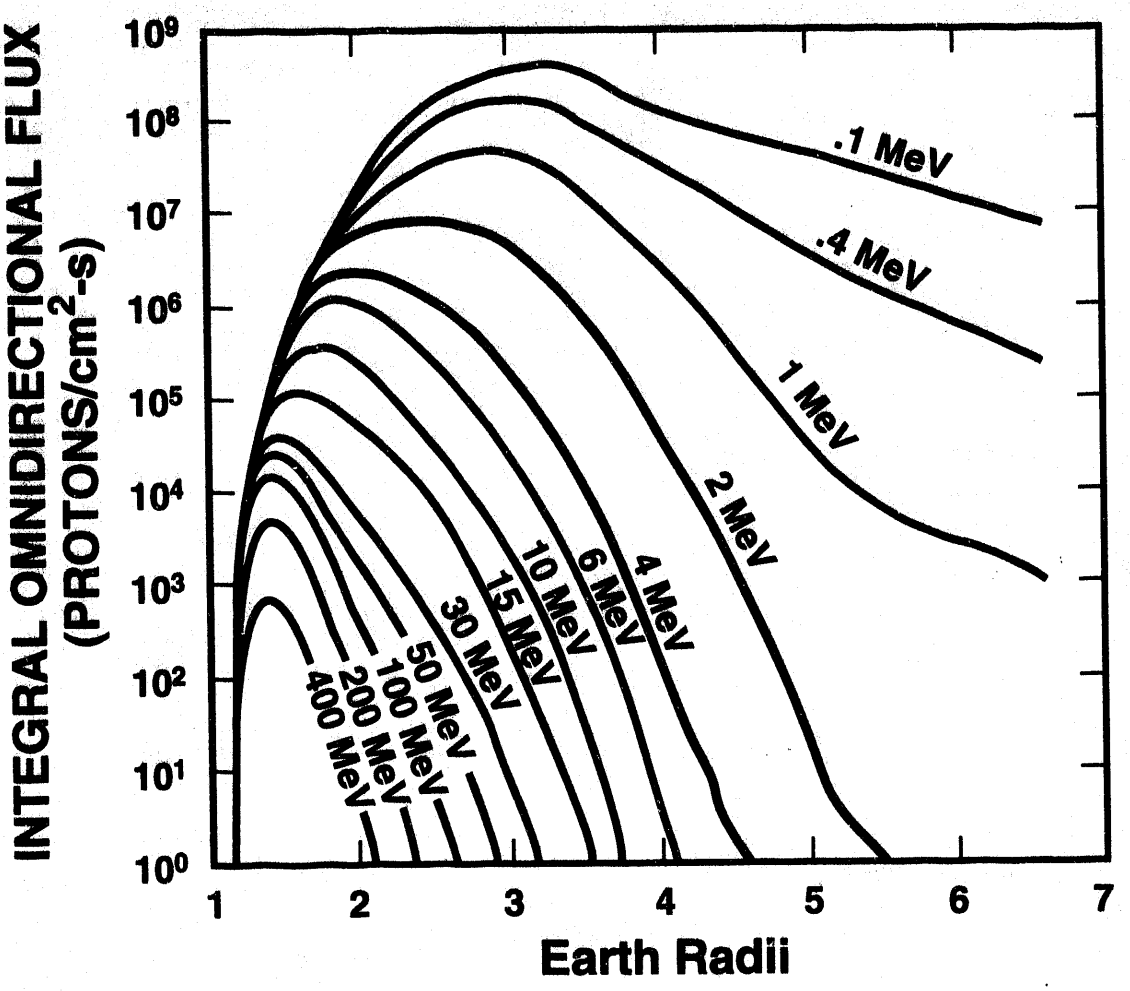


Figure 3: Distribution of proton flux as a function of energy and radial distance. (After Ref. 1)

space radiation effects. As will be discussed below, heavy ions deposit more energy per unit depth in a material than protons, and can actually cause greater numbers of single-event effects. As illustrated in Fig. 5, the flux of protons is more than two orders of magnitude higher than the flux of either carbon or oxygen and approximately five orders of magnitude higher than the flux of nickel. The energy spectrum of galactic cosmic rays is given in Fig. 6 [8]. Note that the x-axis of Fig. 6 is given in units of MeV/nucleon. Thus, for carbon with 12 nucleons, the point at 100 MeV/nucleon on the x-axis corresponds to an energy of 1.2 GeV. For most ions, the flux peaks between 100 and 1000 MeV/nucleon. For carbon, the peak flux is at an energy of approximately 2.4 GeV. For protons and alpha particles, the energy of the ion can be more than 100 GeV/nucleon. At these high energies, it is nearly impossible to shield electronics inside a spacecraft from cosmic rays.

As cosmic rays penetrate into the magnetosphere, low-energy particles are attenuated, modifying the cosmic ray spectrum. Only the more energetic particles are able to penetrate the magnetosphere. Figure 7 [1] illustrates the attenuation of low-energy particles for a low-earth

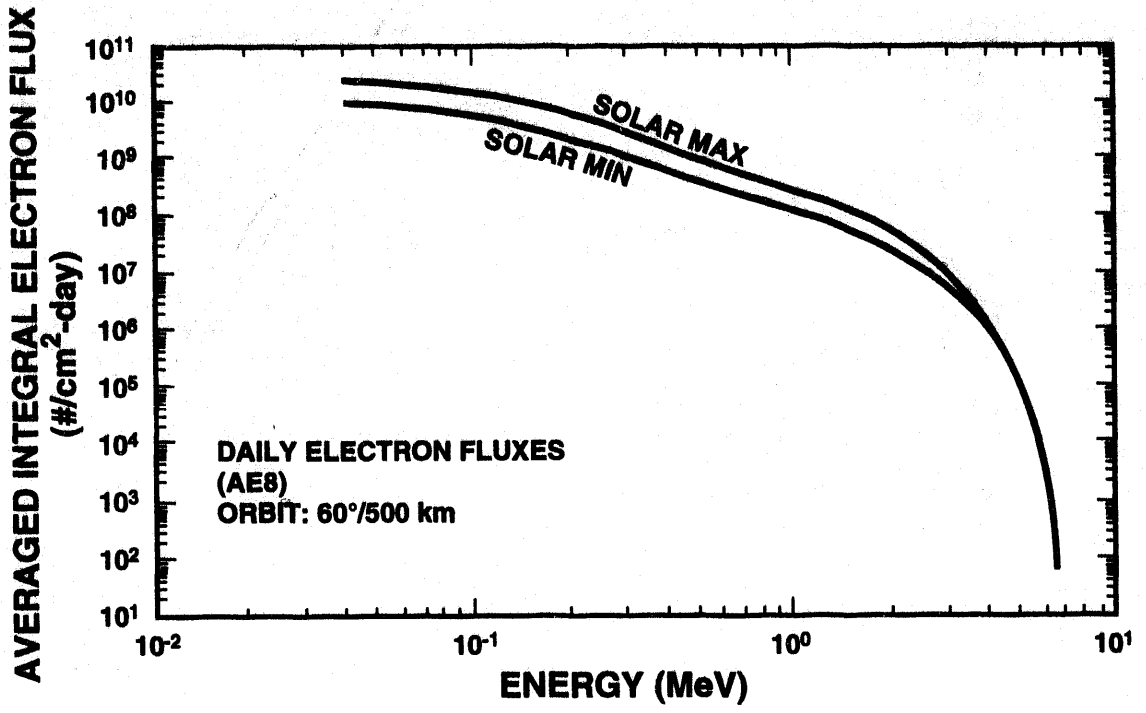


Figure 4: Calculated flux of electrons using the AE8 model for a low-earth orbit. (After Ref. 1)

orbit (LEO) for several angles of inclination. Note that geomagnetic shielding decreases with higher inclination orbits as the magnetic field lines converge near the poles.

The amount of solar cosmic rays is naturally dependent on the amount of solar activity. Solar flares are random in nature and account for a large part of all solar cosmic rays. After a solar flare occurs, particles begin to arrive near the earth within tens of minutes, peak in intensity within two hours to one day, and are gone within a few days to one week (except for some solar flare particles which are trapped in the earth's radiation belts). In a solar flare, energetic protons, alpha particles and heavy ions are emitted. In most solar flares the majority of emitted particles are protons (90-95%) and alpha particles. Heavy ions constitute only a small fraction of the emitted particles, and the number of heavy ions is normally insignificant compared to the background concentration of heavy ions from galactic cosmic rays. In a large solar flare the number of protons and alpha particles can be greatly enhanced (~10^4 times) over the background galactic cosmic ray spectrum; whereas, the number of heavy ions for a large solar flare approaches up to ~50% of the background galactic cosmic concentration of heavy ions [9]. Associated with a solar flare is the solar wind or solar plasma. The solar wind usually arrives near the earth within one to two days after a solar flare [10]. As the solar wind strikes the magnetosphere, it can cause disturbances in the geomagnetic fields (geomagnetic storm), compressing them towards the earth. As a result, the solar wind can enhance the total-dose that a device receives in a low-earth orbit.

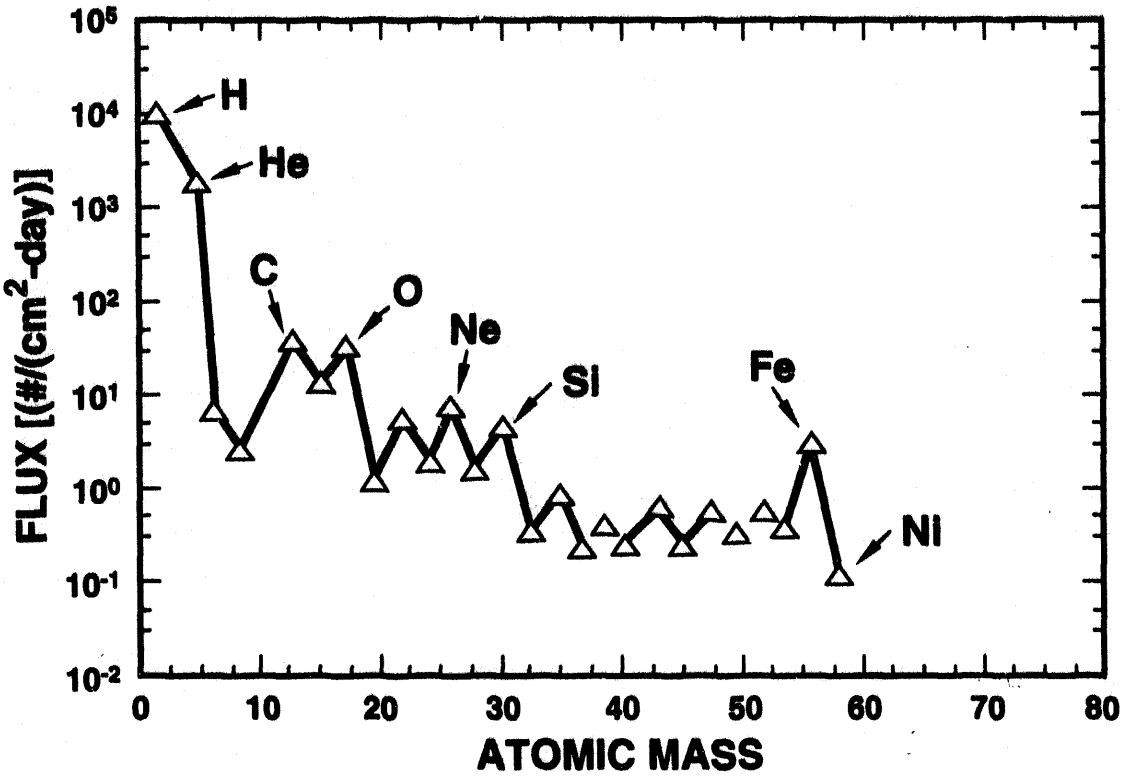


Figure 5: Flux of galactic cosmic ray particles for atomic masses up to 60. (After Refs. 2 and 7)

Figure 8 [11] is a plot of the angular flux of cosmic ray particles (both solar and galactic) during solar minimum and maximum inside a spacecraft in geosynchronous orbit with 25 mils of aluminum shielding as a function of linear energy transfer (LET). [LET is the mass stopping power of cosmic rays and is given in the units of MeV/mg/cm^2. It is a measure of the amount of energy a particle transfers to a material per unit path length.] The solar cycle is approximately 22 years long with peaks in intensity approximately every 11 years. Solar maximum refers to periods of maximum solar activity, and solar minimum refers to periods of minimum solar activity. The solar wind during periods of high solar activity reduces the galactic cosmic ray flux. Thus, the minimum in galactic cosmic ray flux occurs during solar maximum, and the maximum in galactic cosmic ray flux occurs during solar minimum. The flux at solar minimum describes the actual environment for 40% of the time. Also shown in Fig. 8 is the Adams' 10% worst-case environment. The actual environment is more intense than the Adams' 10% worst-case environment only 10% of the time. It includes contributions from both galactic and solar cosmic rays. This environment is often used in assessing the single-event upset hardness of electronic devices.

2.3 Radiation Environment Inside a Spacecraft

Thus far, we have explored the natural space radiation environment outside a spacecraft. To determine the effects of the natural space environment on electronics inside the spacecraft, the effects of shielding must be taken into account. Shielding not only modifies the radiation environment inside a spacecraft by altering the energy and concentration of incoming particles,

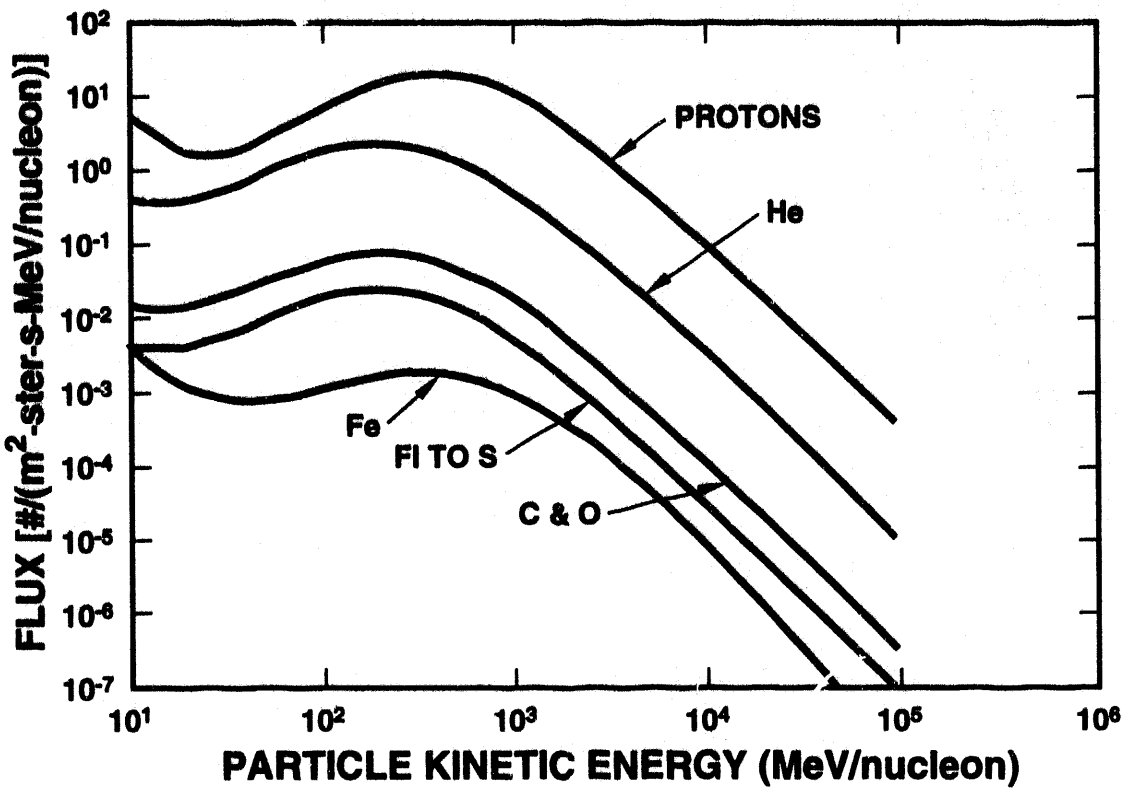


Figure 6: Energy spectrum of galactic cosmic rays. (After Ref. 8)

but also can create secondary particles as the incoming particles pass through the shielding. For instance, bremsstrahlung radiation in the form of x rays is emitted as energetic electrons decelerate in the shielding. For modest amounts of shielding, the effects of shielding can be estimated by taking into account only the energy loss of particles as they pass through the shielding [11].

The amount of energy loss as a particle passes through shielding depends on the thickness of the material. Typical spacecraft shielding is in the range of 100 to 250 mils. Figure 9a [12] is a plot of flux for a large solar flare versus LET for aluminum thicknesses of 0.173 to 10.8 g/cm^2. Note that increasing aluminum thickness results in decreasing solar flare flux for the relatively low-energy particles associated with a solar flare. However, the qualitative variation in flux with LET is relatively unaffected by the shielding. For LETs above 30 MeV-cm^2/mg increasing the shielding thickness from 0.17 g/cm^2 (25 mils) to 10.8 g/cm^2 (1570 mils) reduces the intensity of the spectrum by five orders of magnitude. The effect of spacecraft thickness on galactic cosmic ray flux is shown in Fig. 9b [12]. It takes much more shielding to reduce the intensity of galactic cosmic rays. Spacecraft thicknesses of aluminum from zero up to 10 g/cm^2 (1450 mils) only slightly affect the LET spectrum. By comparing Figs. 9a and 9b, we conclude that spacecraft shielding can attenuate the low-energy nuclei from a solar flare, but has little effect on the attenuation of nuclei in the galactic cosmic ray spectrum. Thus, for practical shielding thicknesses, additional shielding may prove effective against soft components of a solar flare environment, but is relatively ineffective in reducing the galactic cosmic ray spectrum [2].

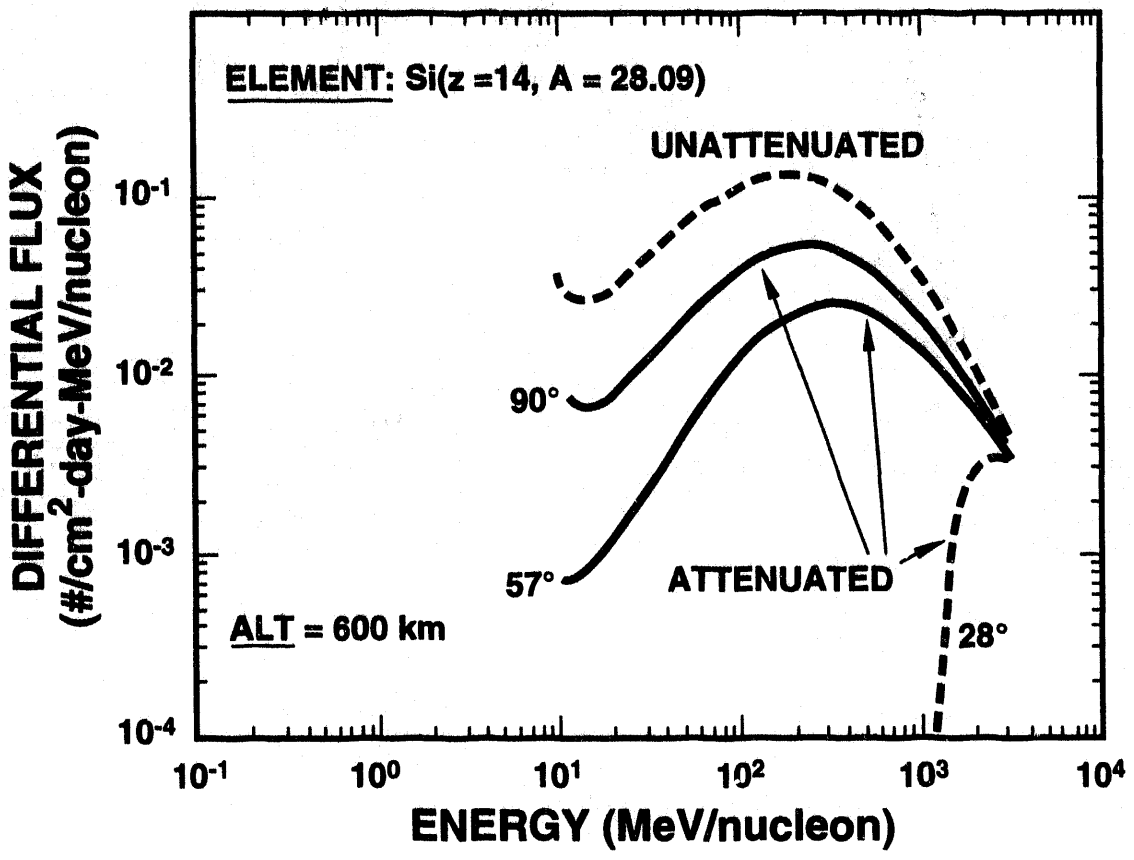


Figure 7: Attenuation of electron flux as a function of electron energy and angle of inclination for a low-earth orbit. (After Ref. 1)

Figure 10 [13] is a plot of the contribution of protons, electrons, and bremsstrahlung to the total dose received after a period of 139 days as a function of aluminum thickness measured aboard the Explorer 55 spacecraft [13]. The data were taken during a period of minimum solar activity. [Note that we have specified total-dose in units of rad(Al). A rad is defined as radiation absorbed dose. It is a measure of the amount of energy deposited in the material and is equal to 100 ergs of energy deposited per gram of material. The energy deposited in a device must be specified for the material of interest. Thus, for a MOS transistor, total dose is measured in units of rad(Si) or rad(SiO_2).] For small aluminum thicknesses, both electrons and protons contribute to the total-absorbed dose. However, for aluminum thicknesses greater than ~150 mils, the electron contribution to the total dose is negligible. The contribution of bremsstrahlung radiation to the total absorbed dose is negligible for all aluminum thicknesses. Increasing the shielding thickness from 100 to 250 mils of aluminum decreases the proton dose by less than a factor of two. Although these data are for a specific satellite orbit, the trends indicated in Fig. 10 are typical for those of other orbits.

As is apparent from Figs. 2 and 3, the total dose that a device is exposed to in a space environment is highly dependent on the orbit. To determine the total dose, one must include contributions from both electrons and protons. The dose rate can vary over a wide range, from less than 10^{-6} to mid 10^{-3} rad(Si)/s. For a five year mission life, these dose rates correspond to a

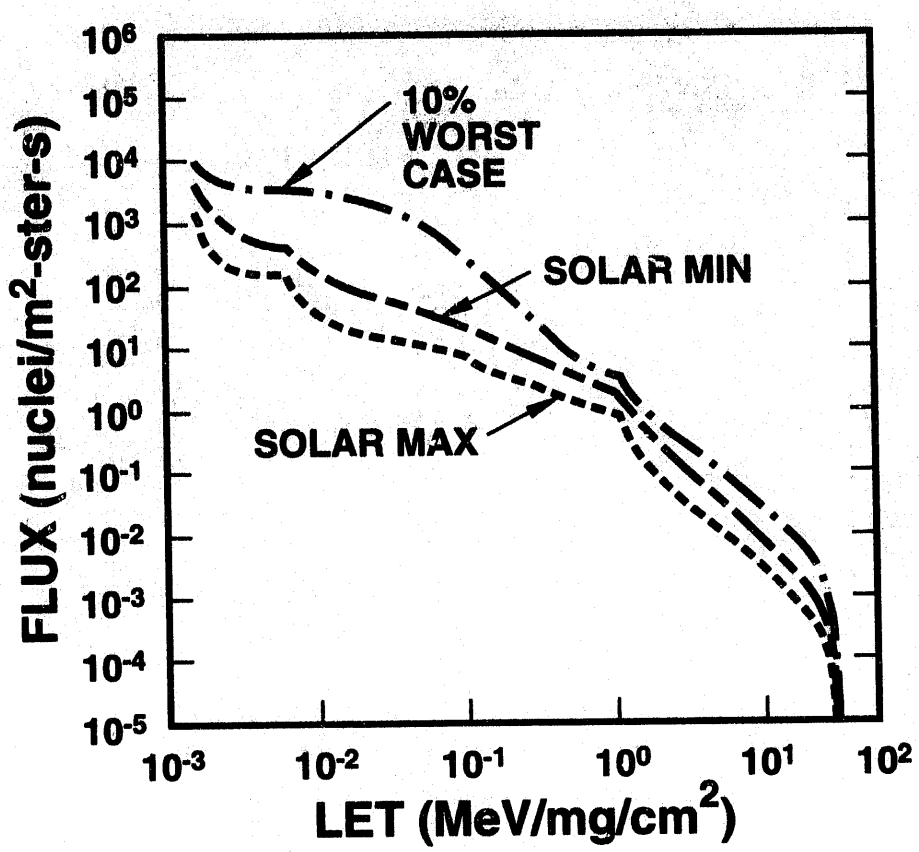


Figure 8: Flux of cosmic ray particles at solar maximum, at solar minimum, and for Adams' 10% worst-case environment. (After Ref. 11)

total-dose range of less than 1 krad(Si) to more than 5 Mrad(Si). For low-earth orbits at high inclination, 200 mils of aluminum shielding can limit the total proton dose to less than 1 krad(Si) per year [14]. Other orbits can result in total doses several orders of magnitude higher. At altitudes corresponding to roughly 1/2 the altitude at geosynchronous orbit (near worst case), the total dose that a device can receive inside a spacecraft with light shielding can approach 1 Mrad(Si) per year [1,15].

2.4 Laboratory Radiation Sources

A wide range of laboratory sources are available to characterize the response of electronic devices. For total-dose effects, these sources range from very high-dose-rate sources for characterizing device response in weapon environments or for investigating the basic mechanisms of radiation effects to very low-dose-rate sources for simulating the total-dose response of electronic devices in the natural space environment. The most common laboratory sources are moderate-dose-rate Co-60 and x-ray sources. Co-60 sources emit gamma rays with a nominal energy of 1.25 MeV. These sources can have dose rates up to 400 rad(Si)/s. The present U. S. military standard test guideline MIL-STD-883D, Method 1019.4 specifies that laboratory acceptance testing must be performed at dose rates from 50 to 300 rad(Si)/s. Thus, Co-60 sources can normally meet these requirements. Another common type of laboratory

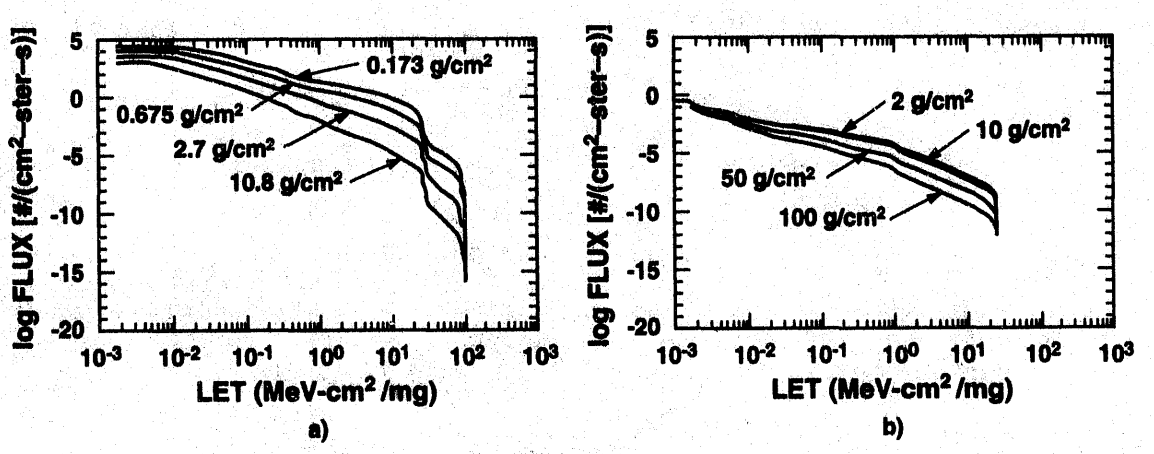


Figure 9: The effects of aluminum shielding on the attenuation of the flux from a large solar flare a) and of the flux from the galactic cosmic ray spectrum b) as a function of the LET of the incident particles. (After Ref. 12)

source is the 10-keV x-ray source. Laboratory x-ray sources are available that can achieve dose rates from below 300 rad(Si)/s to above 3600 rad(Si)/s and that can test unlidded package devices or devices on a wafer. X-ray sources have a nominal energy of 10 keV. The high dose rate of x-ray sources and the capability for testing at the wafer level allows for rapid feedback on radiation hardness during device fabrication [16].

Two high-dose-rate sources that can be used to investigate the total-dose response of electronic devices at short times after a pulse of radiation are electron linear accelerators (LINACs) and proton cyclotrons. Electron LINACs are pulse type sources with pulse widths ranging from less than 20 ns to more than 10 μs with energies from 10 MeV to more than 40 MeV. Dose rates greater than 10^{11} rad(Si)/s can be obtained from electron LINACs. Proton cyclotrons are quasi-continuous sources and can have dose rates as high as 1 Mrad(Si)/s with energies from around 40 MeV to greater than 200 MeV. They can also be operated in low current modes suitable for characterizing proton-induced single-event effects.

For simulating low-dose-rate total-dose effects, Co-60 and Cs-137 sources are available. Cs-137 sources emit gamma rays with a nominal energy of 0.66 MeV. Dose rates below 0.01 rad(Si)/s can be obtained from Cs-137 radiation sources.

There are a wide range of sources available for characterizing heavy-ion induced single-event effects. These sources vary widely in ion species, energy, and flux. Two often used sources in the U. S. are Brookhaven National Laboratories' Twin Tandem van de Graaff accelerator and Lawrence Berkeley Laboratories' 88-inch cyclotron. At the Brookhaven facility, ions are available, ranging from protons with energies of 30 MeV (maximum) and LETs of 0.02 MeV-cm^2/mg to gold with energies of 350 MeV and LETs of 81 MeV-cm^2/mg (in silicon at normal incidence and maximum energy). At Berkeley's facility, ions are available ranging from protons with energies of 60 MeV (maximum) and LETs of 0.009 MeV-cm^2/mg to bismuth with energies of 803 MeV and LETs of 95 MeV-cm^2/mg (in silicon at normal incidence and

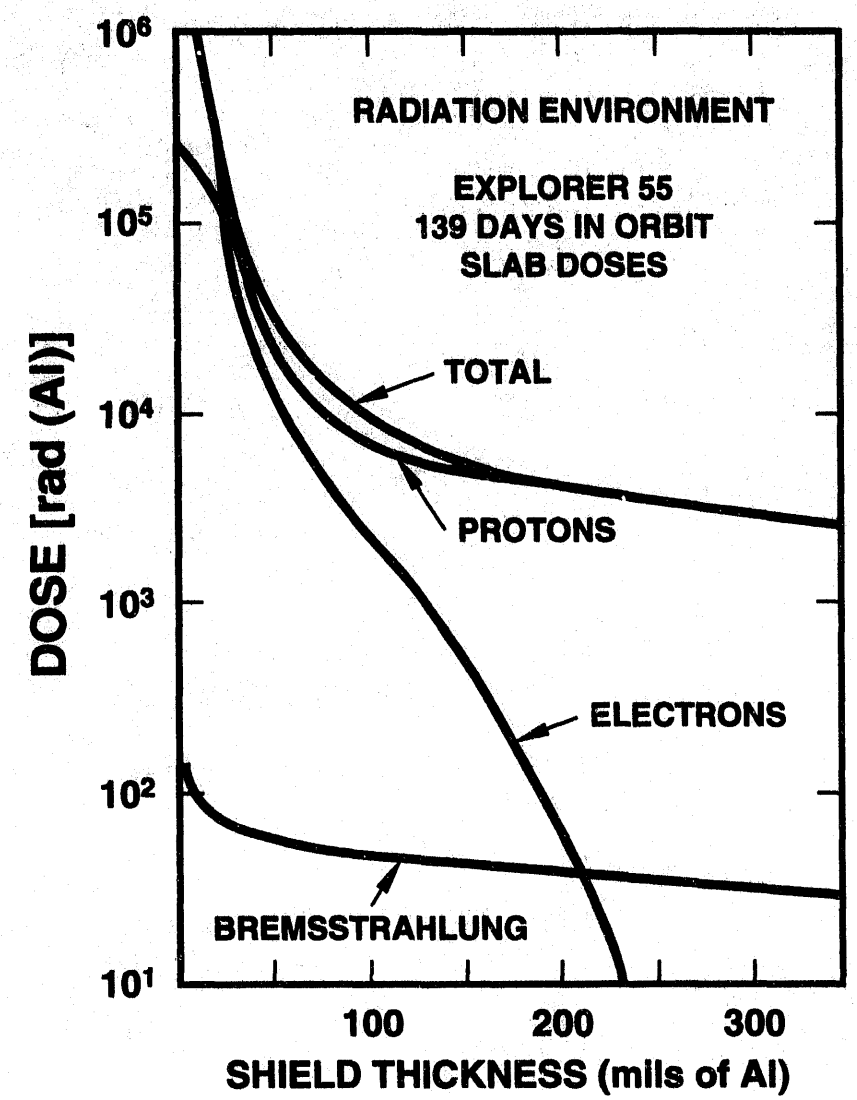


Figure 10: Contributions of protons, electrons, and bremsstrahlung to total dose as a function of aluminum shielding. The data were taken after a 139-day exposure during the Explorer 55 space mission. (After Ref. 13)

maximum energy). In addition to these facilities, other facilities are available in the U. S. and throughout the world for characterizing the single-event upset properties of electronic devices.

3.0 INTERACTION OF RADIATION WITH MATERIALS

The manner in which radiation interacts with solid material depends on the type, kinetic energy, mass, and charge state of the incoming particle and the mass, atomic number, and density of the target material. In this section, we discuss the manner in which the different types of radiation interact with materials.

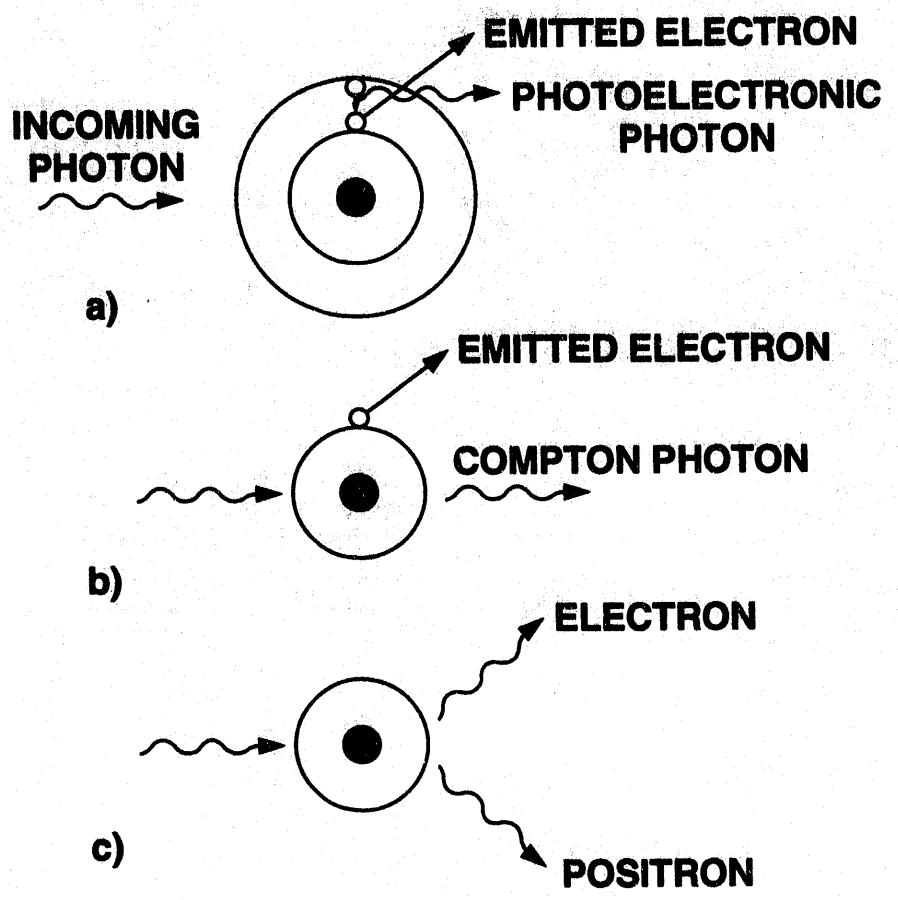


Figure 11: Schematic drawing of three processes through which photons interact with material: a) photoelectric effect, b) Compton scattering, and c) pair production.

3.1 Ionization Effects

Ionization of the target material occurs for photons, electrons, protons, and energetic heavy ions. Photon interactions are not a primary concern for satellites in the natural space environment. However, we include photon interactions in this discussion because of their importance in hardness assurance testing. Most laboratory sources used to simulate total-dose space environment effects emit either low-energy x rays or high-energy gamma rays.

3.1.1 Photon Effects

Photons interact with material through three different processes, namely the photoelectric (or fluorescent) effect, the Compton effect, and pair production [17]. These processes are illustrated in Fig. 11. For each of these processes, the primary result of the interaction is the creation of energetic secondary electrons.

Low-energy photons interact with material predominantly through the photoelectric effect. The photoelectric effect is illustrated in Fig. 11a. In this process, an incident photon excites an electron from an inner shell of a target atom to a high enough state to be emitted free

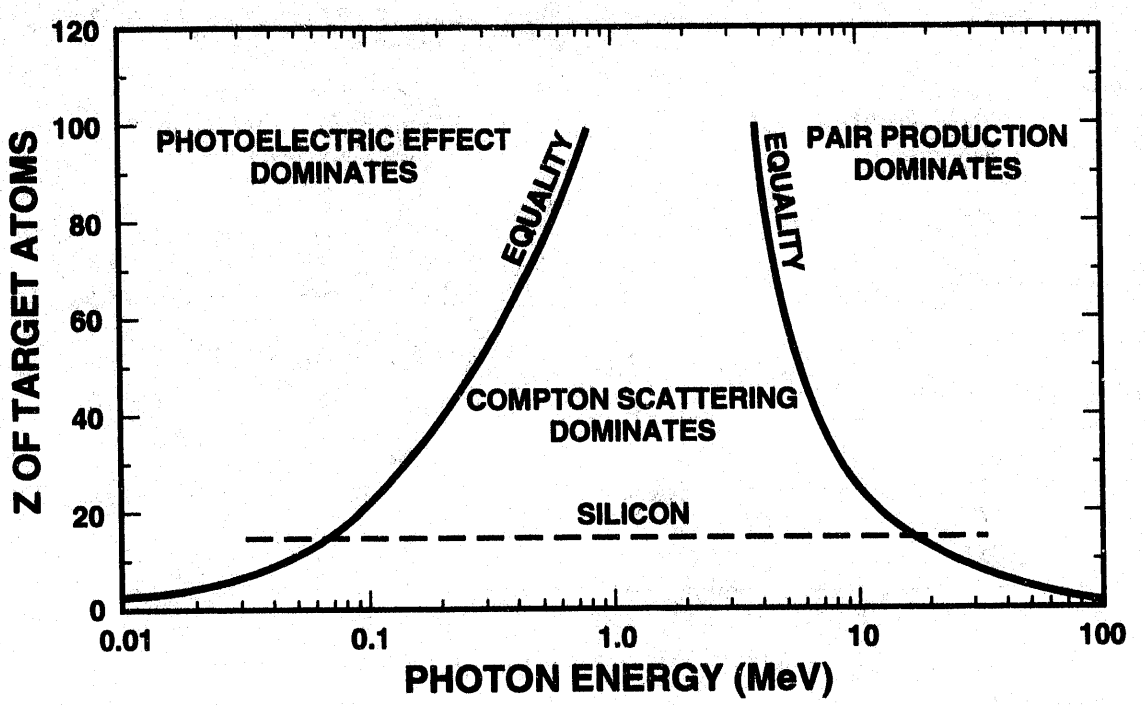


Figure 12: Relative importance of the photoelectric effect, Compton scattering, and pair production as a function of photon energy. (After Ref. 18)

of the target atom. For the photoelectric effect, the incident photon is completely absorbed. Thus, the photoelectric effect creates a free electron (photoelectric electron) and an ionized atom. In addition, as the photoelectric electron is emitted, an electron in an outer orbit of the atom will fall into the spot vacated by the photoelectron causing a low energy photon to be emitted.

For higher energy photons, Compton scattering will dominate over the photoelectric effect. Compton scattering is illustrated in Fig. 11b. In this process, as a photon collides with an atom, the photon transfers a fraction of its energy to an electron of the target atom, giving the electron sufficient energy to be emitted free of the target atom. For Compton scattering, a photon of lower energy is created which is free to interact with other target atoms. It also creates a free electron and an ionized atom.

Pair production occurs only for very-high energy photons (E>1.02 MeV). It is illustrated in Fig. 11c. In pair production, the incident photon collides with a target atom creating an electron-positron pair. A positron has the same properties as an electron (charge and mass), except that the charge is positive. The incident photon is completely annihilated in pair production.

The relative importance of the three processes as a function of photon energy and atomic mass of the target material is illustrated in Fig. 12 [18]. Indicated in the Fig. 12 are the regions where each process dominates. The solid lines correspond to equal probabilities for the different interactions. The dashed line corresponds to the atomic mass of silicon (Z=14). Thus for silicon, x rays emitted from a low-energy (typically 10 keV) x-ray irradiator will interact predominantly

through the photoelectric effect, while high-energy gamma rays (typically 1.25 MeV) from a Co-60 source will interact predominantly through Compton scattering.

3.1.2 Electron-Hole Pair Generation

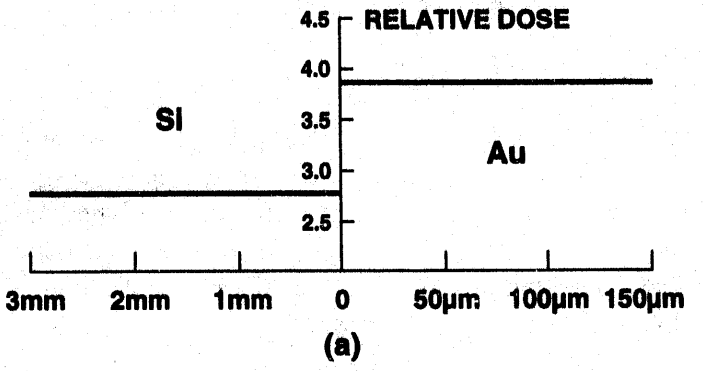
High-energy electrons (secondary electrons generated by photon interactions or electrons present in the environment) and protons can ionize atoms, generating electron-hole pairs. As long as the energies of the electrons and holes generated are higher than the minimum energy required to create an electron-hole pair, they can in turn generate additional electron-hole pairs. In this manner, a single, high enough energy incident photon, electron, or proton can create thousands or even millions of electron-hole pairs. The minimum energy required for creating an electron-hole pair, E_p, in silicon, silicon/dioxide and GaAs is given in Table I [17,19,20]. Also given in Table I are the densities [21] for the three materials and the initial charge pair density per rad deposited in the material, g_0 [17]. The latter quantity is obtained from the product of the material density and the deposited energy per rad (1 rad = 100 erg/g = 6.24×10^{13} eV/g) divided by E_p [17].

Table I: Minimum energies for creating electron-hole pairs and densities for GaAs, silicon, and silicon dioxide.

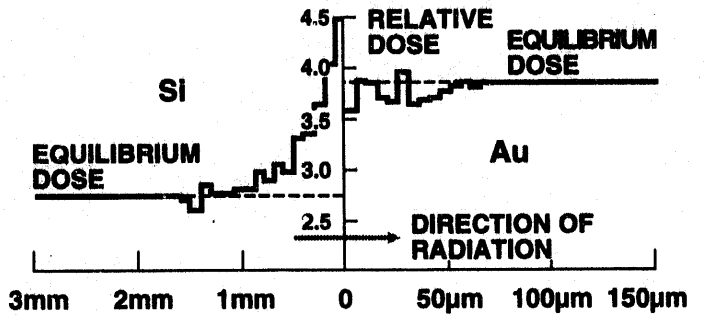
Material	E_p (eV)	Density (g/cm^3)	Pair density generated per rad, g_0 ($pairs/cm^3$)
GaAs	~4.8	5.32	$\sim 7 \times 10^{13}$
Silicon	3.6	2.328	4×10^{13}
Silicon Dioxide	17	2.2	8.1×10^{12}

3.1.3 Dose Enhancement

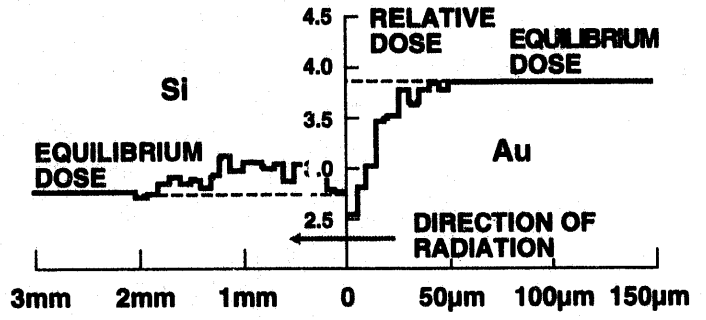
One additional factor that must be taken into account in determining the total number of electron-hole pairs generated in a material is dose enhancement. Dose enhancement arises when an incident particle travels through two adjacent materials with different atomic masses. Close to the interface of two materials, charge particle equilibrium is not maintained. Charge particle equilibrium is defined as the condition where the total energy carried out of a given mass element by electrons is equal to the energy carried into it by electrons [4]. For two adjacent materials with different atomic masses, close to the interface of the materials the number of electrons generated in the low-atomic mass material will be higher than for the case where charge particle equilibrium is maintained (i.e., far away from the interface). This effect is called dose enhancement. It is illustrated in Fig. 13 [4]. In charge particle equilibrium (Fig. 13a) the ratio of the relative doses in two materials depends on the absorption properties of the materials. It can be defined as



(a)



(b)



(c)

Figure 13: Relative dose enhancement at the silicon/gold interface. Figure 13a is the relative dose in charge-particle equilibrium, b) for the direction of the incident radiation going from the silicon to the gold, and c) for the direction of the incident radiation going from the gold to the silicon. (After Ref. 4)

$$\frac{D_{eq}(1)}{D_{eq}(2)} = \frac{(\mu_{en}/\rho)_1}{(\mu_{en}/\rho)_2}, \quad (1)$$

where $D_{eq}(1,2)$ are the relative doses for materials 1 and 2, and $(\mu_{en}/\rho)_{1,2}$ are the mass energy absorption coefficients of materials 1 and 2. ρ_1 and ρ_2 are the material densities. However, close to the interface of the materials, charge particle equilibrium is not maintained and the relative dose in the low atomic mass material can be much higher than it is in charge particle equilibrium as indicated in Figs. 13b and 13c. For example, as indicated in Fig. 13b, charge particle equilibrium is maintained for distances of more than ~1.5 mm in the silicon away from the interface and of more than ~75 mm in the gold. However, close to the interface, dose enhancement has increased the relative dose in the silicon by approximately 40%. Note that the direction of the incident particles significantly affects the magnitude of dose enhancement.

The amount of dose enhancement will depend on the mechanism by which an incident photon interacts with a material. It will be largest for low-energy photons (<<1 MeV) which interact through the photoelectric effect [22]. For an MOS transistor with a polysilicon gate, the atomic mass of silicon is slightly above the atomic mass of silicon dioxide and the amount of dose enhancement is negligible for 1.25 MeV Co-60 gamma rays (which interact through the Compton scattering). On the other hand, for low-energy 10-keV x rays (which interact through the photoelectric effect) the amount of dose enhancement can be relatively large (~1.8) [23,24]. Thus, for 1.25 MeV gamma rays, dose[rad(Si)] ≈ dose[rad(SiO_2)] and for 10-keV x rays, dose[rad(Si)] ≈ 1.8xdose[rad(SiO_2)]. Higher dose enhancement factors will result for metal silicide gates with higher atomic masses (e.g., tungsten and tantalum) [22,25]. For those materials in which significant dose enhancement can occur, the number of electron-hole pairs generated by the incident radiation must be multiplied by a dose-enhancement factor to determine the total number of electron-hole pairs generated.

3.2 Displacement Effects

In this section, we give a very brief overview of the basics of displacement damage in materials. In addition to ionization effects, high-energy protons can also cause displacement damage in silicon and other semiconductor materials [17,26-28]. As a high-energy proton collides with an atom, the atom will recoil from its lattice site. If the energy transferred to the atom is high enough, the atom can be knocked free from its lattice site to an interstitial site. The minimum energy required to knock an atom free of its lattice site is called the displacement threshold energy. As the atom is displaced from its original position it leaves behind a vacancy. The combination of the interstitial atom and its vacancy is called a Frenkel pair. If the displaced atom has sufficient energy it can in turn displace other atoms. Thus, for very high energy recoils a defect cascade can be created with large defect clusters. A "typical" distribution of clusters produced by a 50-keV silicon recoil atom is illustrated in Fig. 14 [26]. As the primary silicon atom travels through the silicon, it knocks free other atoms and it is in turn reflected, altering its path. Towards the ends of the paths of the reflected atoms (and the primary atom) large clusters of defects may be formed (terminal clusters). About 90% of the displaced atom and vacancy pairs recombine within a minute after irradiation at room temperature.

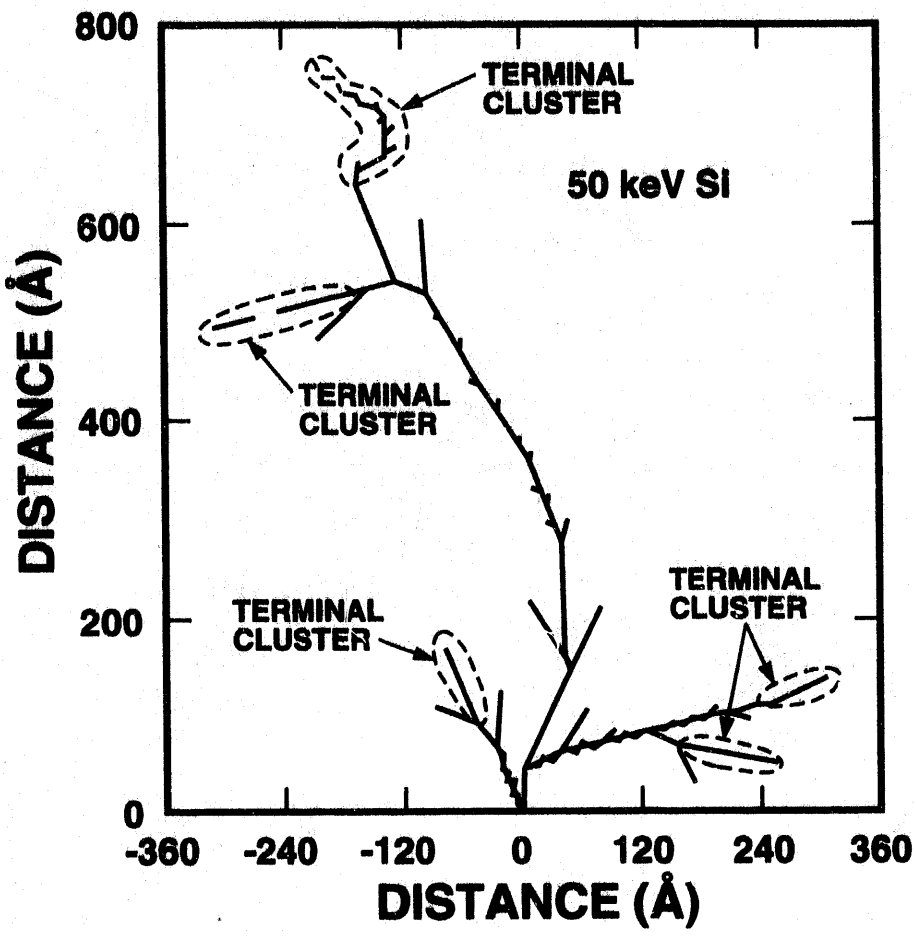


Figure 14: Defect cascade created by a 50-keV silicon recoil atom. (After Ref. 26)

The primary effect of displacement damage is the creation of deep and shallow level traps in the material [26-28]. The shallow level traps can compensate majority carriers and cause carrier removal. Deep level traps can act as generation, recombination, or trapping centers. These centers can decrease the minority carrier lifetime, increase the thermal generation rate of electron-hole pairs, and reduce the mobility of carriers. As a result, displacement damage is a concern primarily for minority carrier (e.g., bipolar transistors) and optoelectronic devices. It is relatively unimportant for MOS transistors.

4.0 TOTAL-DOSE EFFECTS — MOS DEVICES

If an MOS transistor is exposed to high-energy ionizing irradiation, electron-hole pairs will be created uniformly throughout the oxide. The generated carriers induce the buildup of charge which can lead to device degradation. The mechanisms by which device degradation occurs are depicted in Fig. 15 [17]. Figure 15 is a plot of an MOS band diagram for a positively applied gate bias. Immediately after irradiation, electrons will rapidly drift (within picoseconds) toward the gate and holes will drift toward the Si/SiO_2 interface. However, even before the electrons leave the oxide, some fraction will recombine with holes. The fraction of electron-hole pairs that escape recombination is the electron-hole yield. Those holes which escape "initial"

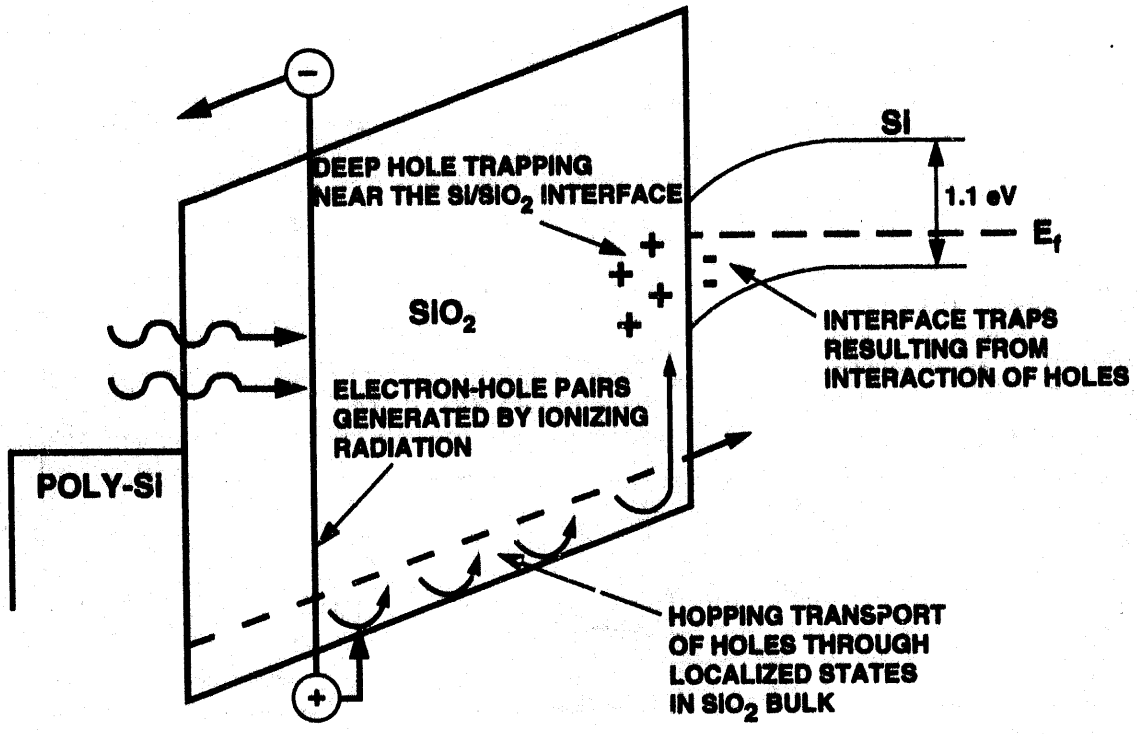


Figure 15: Band diagram of an MOS device with a positive gate bias. Illustrated are the main processes for radiation-induced charge generation. (After Ref. 17)

recombination will transport through the oxide toward the Si/SiO_2 interface by hopping through localized states in the oxide. As the holes approach the interface, some fraction of the holes will be trapped, forming a positive oxide-trap charge. Large concentrations of oxide-trap charge can cause increased leakage current of an integrated circuit. Hydrogen ions are likely released as holes "hop" through the oxide or as they are trapped near the Si/SiO_2 interface. The hydrogen ions can drift to the Si/SiO_2 where they may react to form interface traps. At threshold, interface traps are predominantly positively charged for p-channel transistors and negatively charged for n-channel transistors. Large concentrations of interface-trap charge can decrease the mobility of carriers and increase the threshold voltage of n-channel transistors. These effects will tend to decrease the drive of transistors, degrading timing parameters of an IC. In this section, we present the details of oxide-trap and interface-trap charge buildup in MOS transistors.

4.1 Measurement Techniques

Before we begin to discuss mechanisms and device properties for the buildup of charge in MOS transistors and capacitors, let us first take a look at some of the measurement techniques used to electrically and microscopically characterize defects in MOS capacitors and transistors. In this section, we discuss some of the more common characterization techniques.

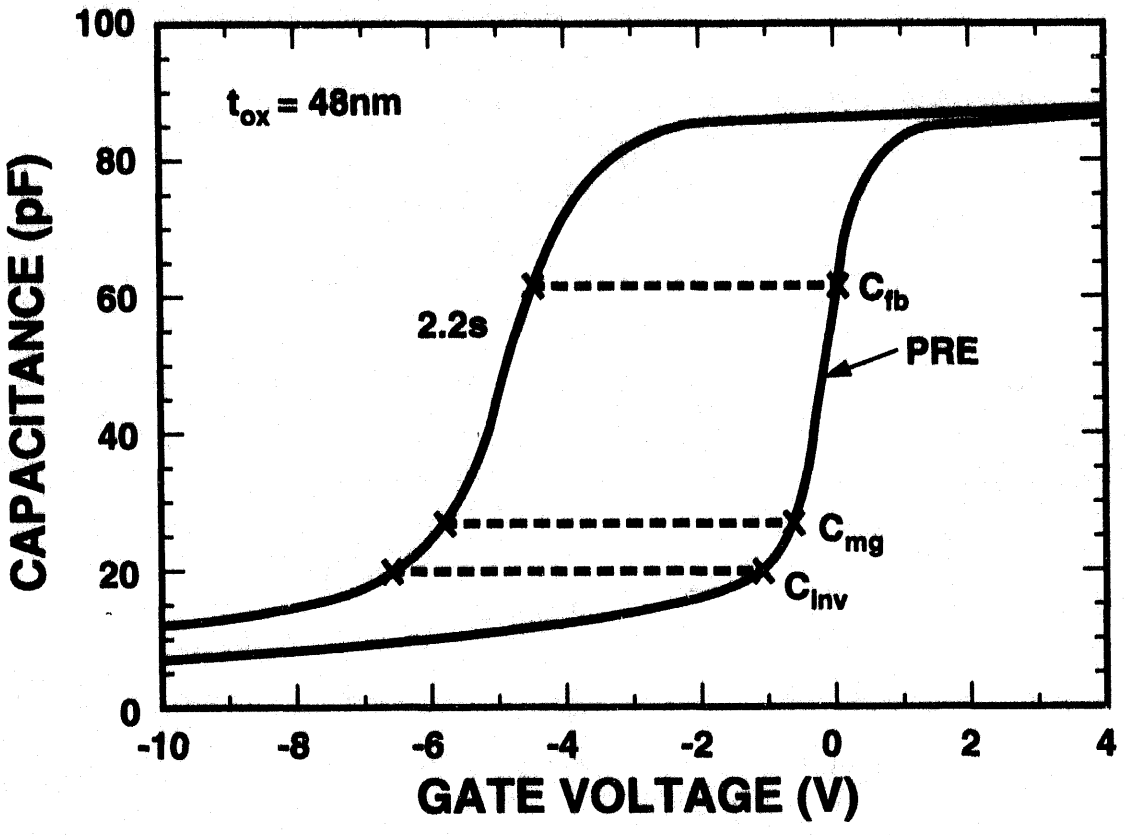


Figure 16: Typical C-V traces taken on an MOS capacitor preirradiation and 2.2 s after a 1 Mrad(Si) irradiation. Noted on the C-V traces are the points corresponding to flatband (C_{fb}), midgap (C_{mg}), and inversion (C_{inv}) capacitance.

4.1.1 Electrical Techniques

To characterize hole transport and oxide-trap and interface-trap charge buildup, either capacitor and transistor test structures are used. MOS capacitors are characterized by analyzing high-frequency and/or low-frequency quasi-static capacitance-voltage (C-V) curves. Figure 16 is a typical set of high-frequency C-V traces pre- and postirradiation. Plotted is the capacitance versus gate voltage for an n-substrate capacitor preirradiation and 2.2 s after irradiating to 1 Mrad(Si). The C-V curves were taken using a 1 MHz sinusoidal signal superimposed on top of a 10 mV/s ramp. Noted on the C-V traces are the points corresponding to flatband, midgap, and inversion capacitance. These points are defined as the silicon surface potential at 0, ϕ_B, and $2\phi_B$, respectively, where ϕ_B is the bulk potential given by [21]

$$\phi_B = \frac{kT}{q}\ln\left(\frac{N_D}{N_i}\right), \tag{2}$$

q is the magnitude of the charge of an electron, k is Boltzmann's constant, T is the absolute temperature, and N_D and N_i are the substrate and intrinsic carrier doping concentrations,

respectively. Assuming that interface traps are approximately charge-neutral at midgap [29-32], the difference in the voltage shift at midgap between the pre- and postirradiation C-V curves is equal to the threshold-voltage shift due to oxide-trap charge, ΔV_{ot}. The number of interface traps can be estimated from the stretchout in the C-V curves. For instance, the number of interface traps from flatband to midgap can be determined from the voltage shift at flatband, pre- and postirradiation, minus the voltage shift at midgap, pre- and postirradiation. Similarly, the number of interface traps from midgap to inversion can be determined from the voltage shift at midgap, pre- and postirradiation, minus the voltage shift at inversion, pre- and postirradiation. Defining the voltage stretchout in the C-V curves as ΔV_{it}, the number of radiation-induced interface traps, ΔN_{it}, is given by

$$\Delta N_{it} = \frac{C_{ox}\Delta V_{it}}{q} , \tag{3}$$

where C_{ox} is the oxide capacitance per unit area. For C-V curves taken on an n-type substrate as shown in Fig. 16, analyzing the C-V curves from midgap to inversion gives the number of interface traps in the lower part of the silicon band gap corresponding to the number of interface traps near threshold for a p-channel transistor. The flatband-voltage shift contains contributions from both interface-trap and oxide-trap charge. However, short times after a pulse of irradiation, interface-trap buildup may be small (see Section 4.5.1), and the flatband-voltage shift is dominated often by the number of holes in the oxide: either those in transport through the oxide or trapped at defects near the Si/SiO_2 interface. Time constants are short at flatband [30] making it possible to make high-speed C-V measurements near flatband. Thus, flatband-voltage shift measurements are a good monitor of hole transport and trapping effects shortly after a pulse of irradiation.

There are a number of techniques that have been used to electrically characterize radiation-induced defects in MOS transistors. Threshold voltages are normally determined by measuring I-V curves in either the linear region (small drain bias) or in the saturation region (large drain bias). For small drain bias ($V_{DS} << V_{GS} - V_{th}$), the drain current in the linear region, $I_{DS}(lin)$, varies as [21]

$$I_{DS}(lin) = \frac{\mu C_{ox} W}{L}(V_{GS} - V_{th})V_{DS} , \tag{4}$$

where μ is the carrier mobility, W is the width of the device, L is the length, V_{GS} is the gate-to-source bias, V_{DS} is the drain-to-source bias, and V_{th} is the threshold voltage. Thus, the threshold voltage can be determined from the voltage intercept of a plot of I_{DS} versus V_{GS} curve. Note that the threshold voltage determined from Eq. (4) does not give the same value as the inversion voltage for capacitors defined as the surface potential equal to $2\phi_B$ [29,33]. The carrier mobility can be determined from the slope of the curve.

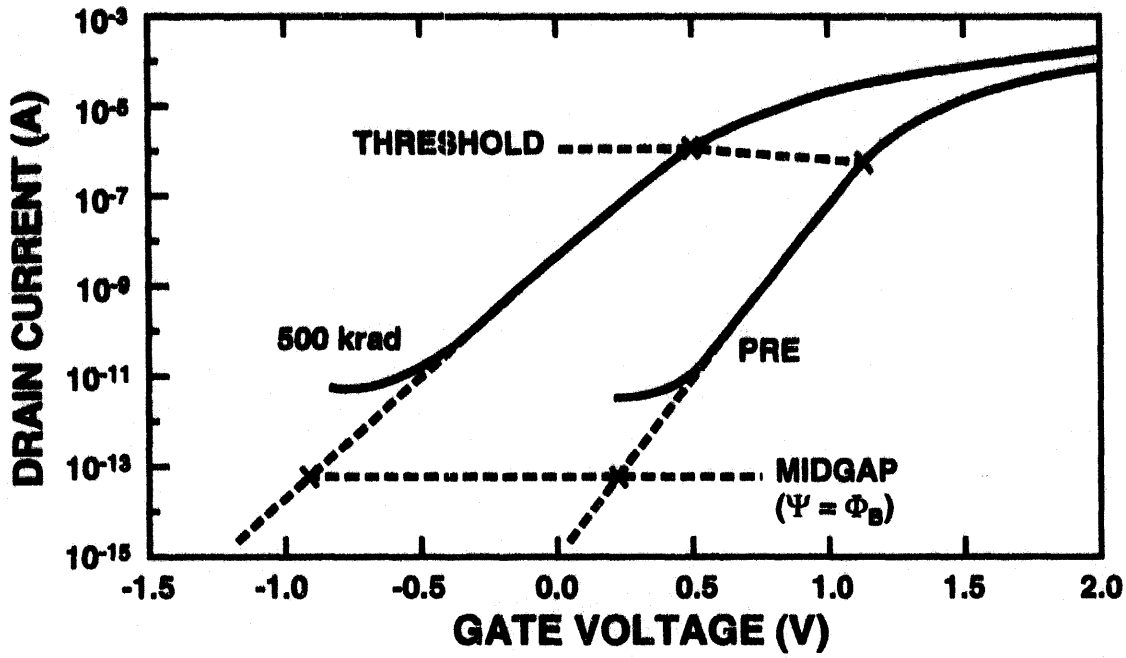


Figure 17: I-V traces taken on an MOS transistor preirradiation and after irradiating to 500 krad(Si). Noted on the I-V traces are the points corresponding to threshold and midgap.

In the saturation region, the drain current, $I_{DS}(sat)$, varies as [21]

$$I_{DS}(sat) \cong \frac{mW}{L}\mu_n C_{ox}(V_{GS} - V_{th})^2 \ , \qquad (5)$$

where m is a constant dependent on the doping concentration and approaches a value of 1/2 at low doping levels. The threshold voltage in the saturation region can be determined from the voltage intercept of the square root of the drain-current versus gate-voltage curve.

To characterize the individual contributions of interface- and/or oxide-trap charge in transistors, two common techniques are the midgap I-V technique [29] and the charge-pumping technique [34,35]. The midgap technique is very similar in nature to the high-frequency C-V technique discussed above. It can be used to obtain estimates of the threshold-voltage shifts due to interface-trap and oxide-trap charge. Figure 17 is a set of I-V curves for an n-channel transistor taken preirradiation and after irradiating to 500 krad(Si). The I-V curves were taken by ramping the gate voltage from -1.5 V to 2 V at a ramp rate of ~4 V/s and with a drain voltage of 5 V. Noted on the I-V curves are the points corresponding to the threshold and midgap voltage points. The midgap voltage is determined by calculating the midgap current [21] and extrapolating the I-V curves to the voltage point corresponding to the calculated midgap current. Similar to high-frequency C-V analysis, the threshold-voltage shift due to oxide-trap charge, ΔV_{ot}, is determined from the voltage shift between the pre- and postirradiation I-V curves at the midgap point, and the total-threshold-voltage shift, ΔV_{th}, is determined from the voltage shift between the pre- and postirradiation I-V curves at the threshold-voltage point. The threshold-

voltage shift due to interface-trap charge, ΔV_{it}, is determined from the stretchout in the I-V curves, i.e., the difference in the voltage shift at threshold pre- and postirradiation minus the voltage shift at midgap pre- and postirradiation.

In addition to these techniques, other techniques for determining ΔV_{it} and ΔV_{ot} have been developed. These include single-transistor techniques based on mobility measurements [36,37] and dual-transistor techniques combining mobility and threshold-voltage measurements [38,39].

The charge-pumping technique is a very sensitive technique that can be used to measure small changes in interface-trap density, ΔD_{it} [34,35]. It is considerably more sensitive in this regard than either the midgap I-V technique or high-frequency C-V techniques. It is also relatively insensitive to charge lateral non-uniformities [35] and can be used for short time (<1 s) measurements [35]. However, charge pumping directly measures neither ΔD_{it} nor ΔV_{it}. Instead, both of these parameters are inferred from the charge-pumping current. By itself, charge pumping cannot be used to provide accurate and direct measurements of ΔV_{ot} [33].

When a transistor is continuously pulsed from inversion to accumulation by applying a charge-pumping signal between its gate and substrate, a charge-pumping current in the substrate results, as minority and majority carriers are captured and emitted from traps at the Si/SiO_2 interface. For a triangular charge-pumping waveform, the charge-pumping current, I_{cp}, is related to the average density of interface traps, D_{it}, through the equation [34]

$$I_{cp} \cong 2qD_{it}fAkT\left[\ln(v_{th}N_i\sqrt{\sigma_n\sigma_p}) + \ln\left(\frac{|V_{fb}-V_{th}|}{2|\Delta V_g|f}\right)\right], \tag{6}$$

where A is the transistor area, v_{th} is the thermal velocity of the carriers, N_i is the intrinsic carrier concentration, σ_n and σ_p are the electron and hole capture cross-sections, V_{fb} is the flatband voltage, and f and ΔV_g are the frequency and amplitude of the measurement signal, respectively. To accurately calculate D_{it}, one must know the effective interface-trap capture cross-section as a function of dose [40]. Also, due to uncertainties caused by geometric components of the charge-pumping current, there is some question about the accuracy of calculating D_{it} in some devices from the charge-pumping current [34,41,42]. In addition, there are difficulties in converting ΔD_{it} into ΔV_{it} due to uncertainty about which portion of the band gap contributes to the charge-pumping current [33]. Nevertheless, charge pumping is a very useful tool for characterizing interface-trap buildup in MOS transistors.

4.1.2 Microstructural Techniques — Electron Spin Resonance

A powerful measurement technique that has greatly increased our knowledge of the structure of defects in SiO_2 at the microscopic level is electron paramagnetic resonance (EPR) or electron spin resonance (ESR) [43]. In EPR, the energy associated with the intrinsic angular momentum (spin) of an electron is measured. Spin is quantized with quantum number 1/2, i.e., it can have only two orientations with respect to the axis of an applied magnetic field. The

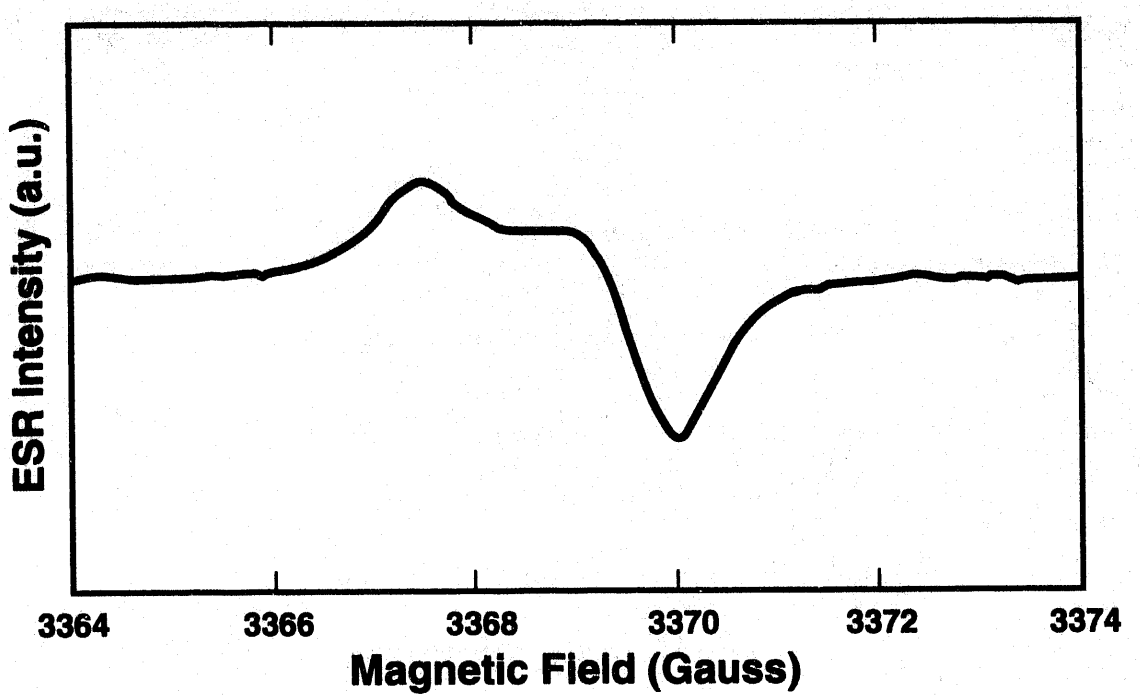


Figure 18: Typical electron paramagnetic resonance spectrum. (After Ref. 44)

difference in energy between two states with different spin is given by $E = h\nu = g\beta H$, where ν is the microwave frequency, H is the magnetic field strength, β is the Bohr magneton ($\beta = eh/4\pi mc$), and g is a dimensionless tensor which gives information on the amount of splitting, characteristic of the atom or ion, and information regarding the symmetry of the defect. In an electron paramagnetic resonance system, the sample under test is placed in a microwave cavity and a DC magnetic field is applied. The magnetic field is varied. If a point is reached where the microwave energy, $h\nu$, is equal to $g\beta H$, an unpaired electron can resonate between the two energy levels. Measurement of the "resonance absorption" point gives information on the g-value or tensor. Note that the atom or ion must be paramagnetic, i.e., have an unpaired electron or electrons, in order to observe a resonance absorption (EPR signal). If the atom or ion is diamagnetic, i.e., it has no net electronic magnetic moment, an EPR signal will not be measured. An example of an EPR spectrum taken on an irradiated thermally grown oxide is shown in Fig. 18 [44]. The double humped feature is characteristic of axially symmetric point defects in amorphous materials. The defect contributing to the signal in Fig. 18 is called an E' center. Details of the E' center are given in Section 4.4.3. Information on the g-tensor as a function of the angle of the magnetic field, hyperfine interactions or multiple signals, and the width of the absorption lines can often be used to identify the structure of the atom or ion.

4.2 Electron-Hole Yield

We now begin our discussion of radiation effects in MOS devices which builds on the previous discussion of the interaction of radiation with materials (Section 3.0). If an electric field exists across the oxide of an MOS transistor, once generated, electrons in the conduction band and holes in the valence band will immediately begin to transport in opposite directions.

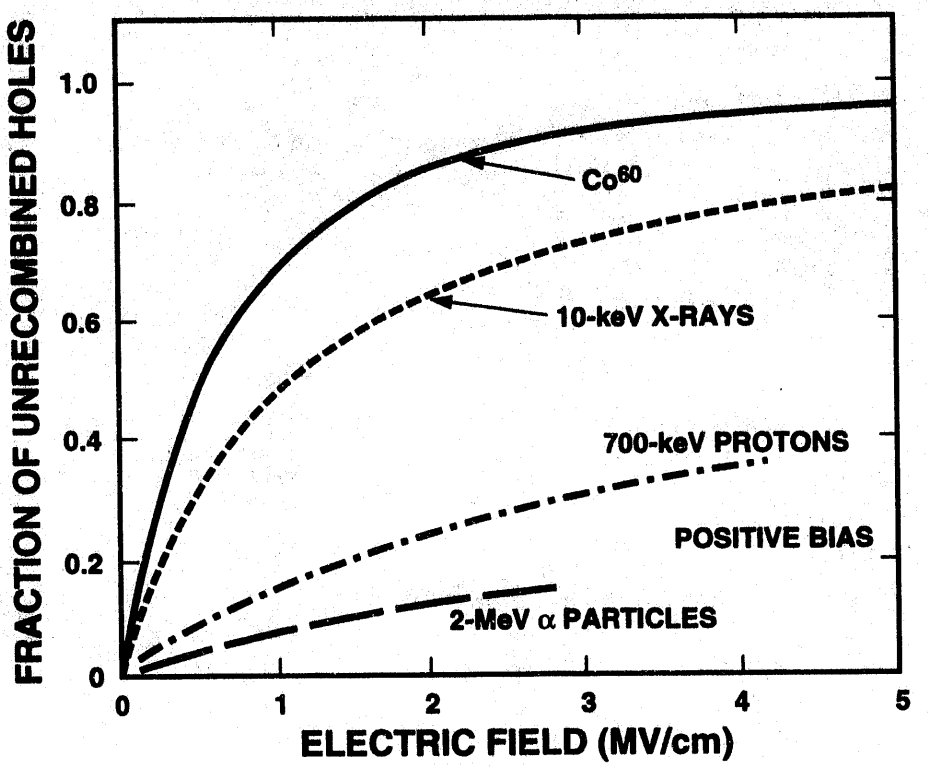


Figure 19: Charge yield for x rays, protons, gamma rays, and alpha particles. (After Refs. 17 and 48)

Electrons are extremely mobile in silicon dioxide and are normally swept out of silicon dioxide in picoseconds [45,46]. However, even before the electrons can leave the oxide, some fraction of the electrons will recombine with holes in the oxide valence band. This is referred to as initial recombination. The amount of initial recombination is highly dependent on the electric field in the oxide and the energy and type of incident particle [47]. In general, strongly ionizing particles form dense columns of charge where the recombination rate is relatively high. On the other hand, weakly ionizing particles generate relatively isolated charge pairs, and the recombination rate is lower [47]. The dependence of initial recombination on the electric field strength in the oxide for protons, alpha particles, gamma rays (Co-60), and x rays is illustrated in Fig. 19 [17,48]. Plotted in Fig. 19 is the fraction of unrecombined holes (hole yield) versus electric field in the oxide. The data for the Co-60 and 10-keV x-ray curves were taken from Ref. 48. The remainder of the curves were taken from Ref. 17. For all particles, the fraction of unrecombined holes increases as the electric field strength increases. Taking into account the effects of hole yield and electron-hole pair generation, the total number of holes generated in the oxide (not including dose enhancement effects) that escape initial recombination, N_h, is given by [17]

$$N_h = f(E_{ox}) g_0 D t_{ox} , \tag{7}$$

where $f(E_{ox})$ is the hole yield as a function of oxide electric field, D is the dose, and t_{ox} is the oxide thickness (in units of cm). Values of g_0 for GaAs, silicon, and silicon dioxide are given in Table I. Specifying the dose in rad(SiO_2), Eq. (7) becomes,

$$N_h = 8.1\text{x}10^{12} f(E_{ox}) D t_{ox} . \quad (8)$$

If metal or silicide gate materials with a high atomic mass are used, N_h must be multiplied by a dose-enhancement factor. Assuming all holes are created uniformly throughout the oxide, the maximum threshold-voltage shift prior to hole transport is given by [17]

$$\Delta V_{th\,max} = -1.9\text{x}10^{-8} f(E_{ox}) D t_{ox}^{\,2} . \quad (9)$$

Eq. (9) is determined by integrating over the charge distribution in the oxide [See Section 4.7, Eq. (20)].

4.3 Hole Transport

Holes generated in the oxide transport much more slowly through the lattice than electrons. In the presence of an electric field, holes can transport to either the gate/SiO_2 or Si/SiO_2 interface. Due to its charge, as a hole moves through the SiO_2 it causes a distortion of the local potential field of the SiO_2 lattice. This local distortion increases the trap depth at the localized site, which tends to confine the hole to its immediate vicinity. Thus, in effect, the hole tends to trap itself at the localized site. The combination of the charged carrier (hole) and its strain field is known as a polaron [49]. As a hole transports through the lattice, the distortion follows the hole. Hence, holes transport through SiO_2 by "polaron hopping" [17,50,51]. Polarons increase the effective mass of the holes and decrease their mobility.

Polaron hopping makes hole transport dispersive (causing hole transport to occur over many decades in time after a radiation pulse) and highly temperature and oxide thickness dependent [17,50,51]. The dispersive nature of hole transport and its temperature dependence is illustrated in Fig. 20 [52]. In this figure the flatband-voltage shift (ΔV_{fb}), normalized to its value immediately after a pulse of ionizing irradiation, measured on a MOS capacitor is shown as a function of temperature. The thickness of the oxide was 96.5 nm, the silicon substrate was n-type, and the oxide electric field was 1 MV/cm. For these measurements, the flatband-voltage shift is an indication of the number of holes in the oxide. As holes transport out of the gate oxide, the flatband voltage will tend to recover to its initial value preirradiation. Note in Fig. 20 that the recovery of the flatband voltage (and hence hole transport) occurs over many decades and is a strongly thermally activated process. At T = 293 K, the time for 50% recovery is less than 1 ms; whereas, for T = 181 K, the time for 50% recovery is approximately 500 s. For temperatures of 124 and 141 K, very little recovery (~20%) occurs for times as long as 1000 s.

The dependence of hole-transport time on electric field strength is illustrated in Fig. 21 [53]. In this figure, the flatband-voltage shift is shown measured on 96.3 nm oxide capacitors normalized to its value immediately after a pulse of ionizing irradiation. The capacitors were irradiated and annealed at 79 K in order to minimize hole transport at low electric fields. The electric field was varied from 3 to 6 MV/cm. As noted in the figure, the flatband voltage recovery time, and hence, the hole transport time, is strongly dependent on the electric field strength. For an electric field of 3 MV/cm very little recovery occurs at the longest measurement

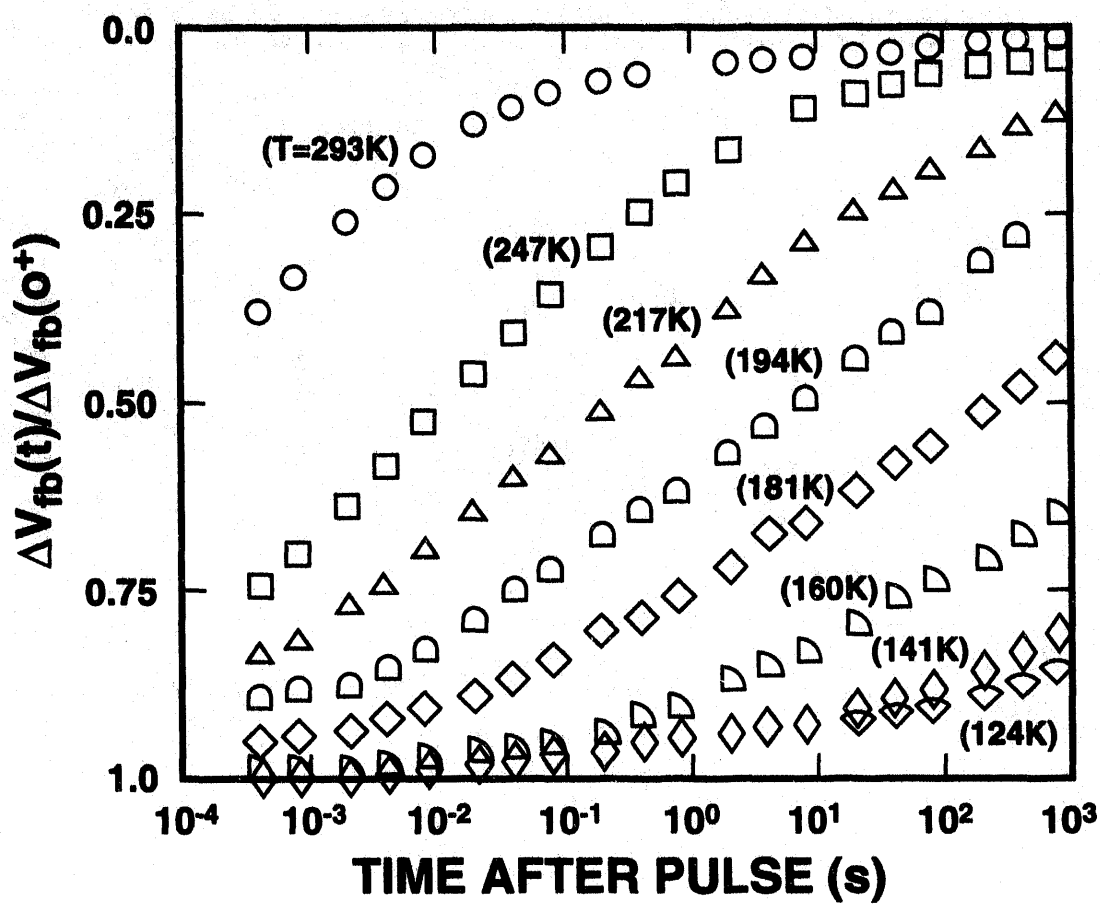


Figure 20: Temperature dependence of the flatband-voltage shift after a single radiation pulse. For this curve the flatband-voltage shift is a measure of the number of holes in the oxide. (After Ref. 52)

time (1000 s). Thus, without a large electric field across the oxide, at low temperatures holes are relatively immobile in the oxide. At higher electric field strengths, the hole transport time is greatly reduced. For an electric field of 6 MV/cm the time for 50% recovery of the flatband voltage is approximately 0.02 s. The temperature and electric field dependence of the recovery time, τ, follow the relationship [53],

$$\tau \sim \tau(0)e^{(-cE/kT)}, \qquad (10)$$

where E is the electric field strength, T is the temperature, and c and $\tau(0)$ are constants. This behavior is characteristic of polaron hopping.

The dependence of flatband voltage recovery time on oxide thickness is illustrated in Fig. 22 [53]. This figure is a plot of the recovery time at a temperature of 220 K and an electric field of 1 MV/cm. Plotted is the flatband voltage normalized to its value immediately after a pulse of ionizing irradiation versus the logarithm of time as a function of oxide thickness. The capacitors

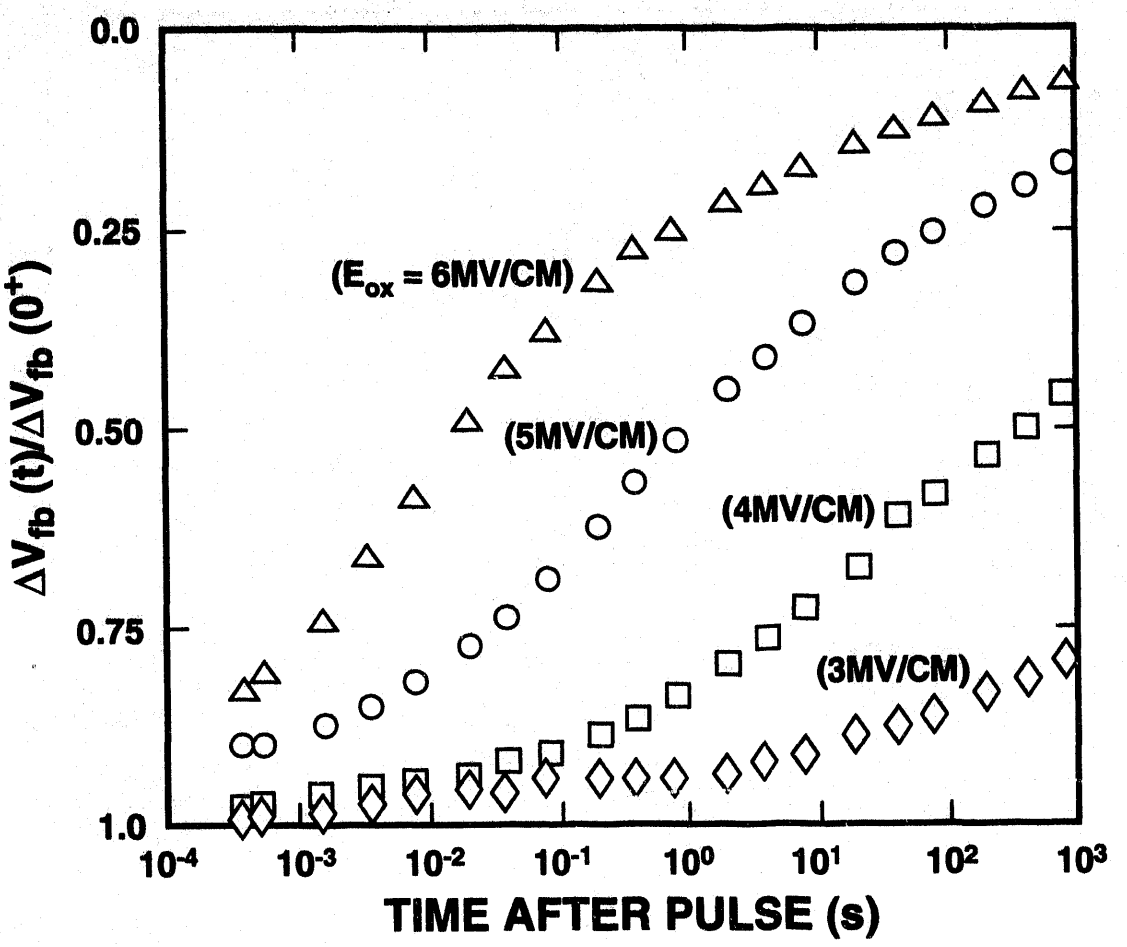


Figure 21: Electric field dependence of the flatband-voltage shift after a single radiation pulse. For this curve the flatband-voltage shift is a measure of the number of holes in the oxide. (After Ref. 53)

were fabricated with the oxides grown at different times. The time for 50% recovery follows approximately a t_{ox}^4 thickness dependence [53].

4.4 Oxide Traps

With the application of a positive gate bias, holes transport to the Si/SiO_2 interface. Close to the interface there are a large number of oxide vacancies due to the out-diffusion of oxygen in the oxide [54] and lattice mismatch at the surface. These oxide vacancies can act as trapping centers. As holes approach the interface, some fraction of the holes will become trapped. The number of holes that are trapped is given by the capture cross-section near the interface which is highly device fabrication dependent, with only a few percent of the holes being trapped in hardened oxides to as much as 50 to 100% for soft oxides. The positive charge associated with trapped holes causes a negative threshold-voltage shift for both n- and p-channel transistors.

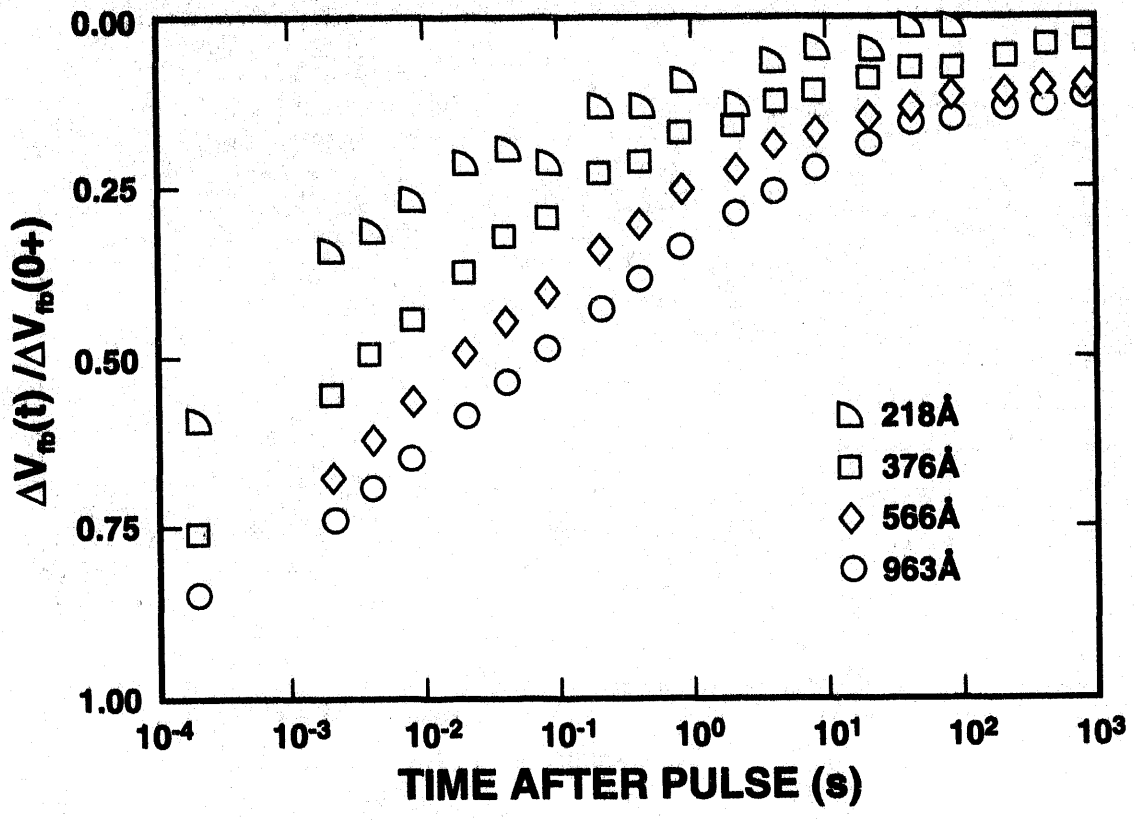


Figure 22: Oxide thickness dependence of the flatband-voltage shift after a single radiation pulse. For this curve the flatband-voltage shift is a measure of the number of holes in the oxide. (After Ref. 53)

The effect of the capture cross-section on trapped-hole buildup can be observed in the electric field dependence of the buildup of oxide traps shortly after irradiation. Figure 23 [55] is a plot of the threshold-voltage shift due to oxide-trap charge, ΔV_{ot}, versus oxide electric field. The solid circles are the measured data, the open circles are the measured data adjusted for hole yield, and the dashed line is a plot of $E^{-1/2}$. For electric fields greater than 0.5 V/cm, ΔV_{ot} adjusted for hole yield decreases with approximately an $E^{-1/2}$ electric field dependence. This is the same electric field dependence for the hole capture cross-section near the Si/SiO_2 interface [47,56-60]. This indicates that the field dependence of oxide-trap charge buildup is determined primarily by the hole capture cross-section.

4.4.1 Time, Temperature, and Electric Field Dependence of Oxide-Trap Charge Neutralization

Immediately after oxide-trap charge is created it begins to be neutralized. Insight into the mechanisms for oxide-trap charge neutralization can be obtained from the time dependence of neutralization, its temperature, and its electric field dependence. The time dependence for trapped-hole neutralization at room temperature is illustrated in Fig. 24 [61] where the voltage shift due to oxide-trap charge, ΔV_{ot}, is plotted versus time for hardened n-channel polysilicon gate transistors irradiated to 100 krad(SiO_2) at dose rates from 6×10^9 to 0.05 rad(SiO_2)/s and then annealed at room temperature. The bias during irradiation and anneal was 6 V and the gate oxide

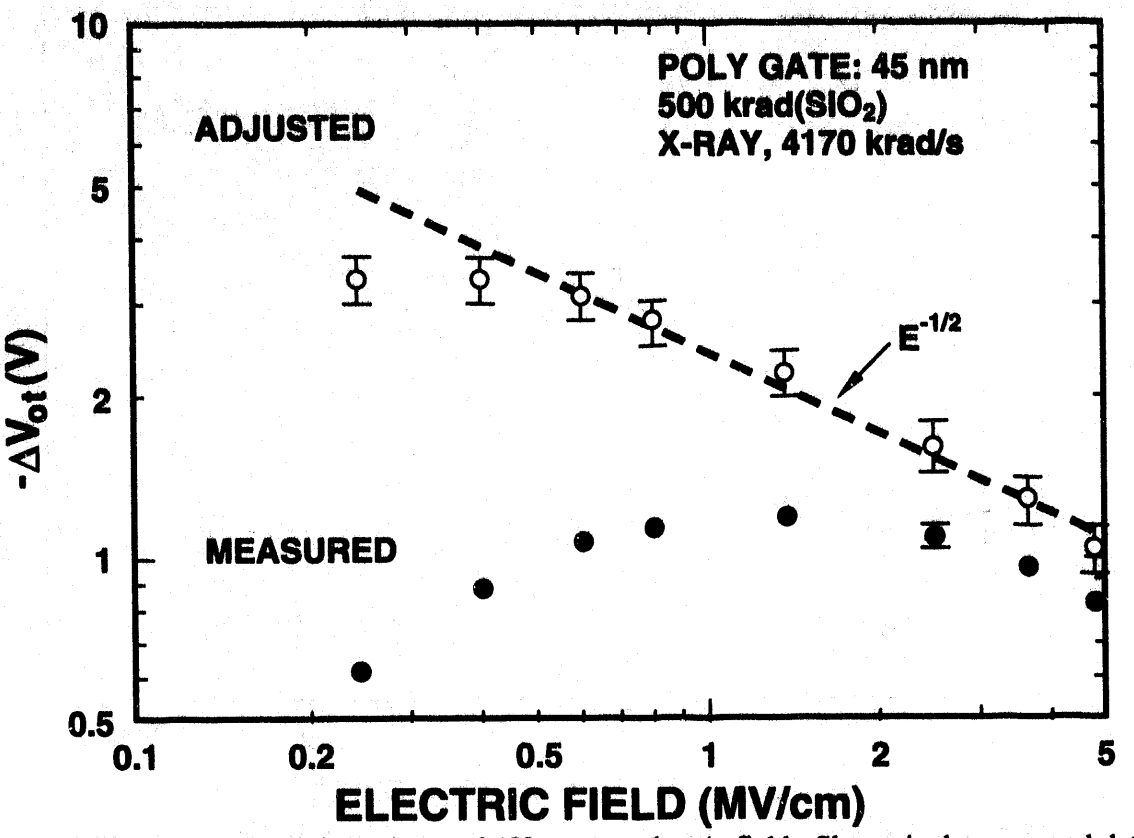


Figure 23: Electric field dependence of ΔV_{ot} versus electric field. Shown is the measured data (solid circles) and the measured data adjusted for charge yield (open circles). (After Ref. 55)

thickness of the transistors was 60 nm. During anneal, the decrease in ΔV_{ot} follows a logarithmic time dependence. At each dose rate, ΔV_{ot} falls on the same straight line. Thus, the rate at which ΔV_{ot} is neutralized is dose-rate independent. The qualitative nature of the time dependence for neutralization of ΔV_{ot} given in Fig. 24 is typical of that for devices fabricated using other hardened and most commercial technologies. However, the rate at which ΔV_{ot} is neutralized can depend on the details of the device fabrication process [62].

The logarithmic decrease in ΔV_{ot} can be described by linear system response analysis [63-65]. Several investigators have found that the long-term annealing response can be empirically characterized using the equation [63,64]

$$-\Delta V_o(t) = \frac{-A\ln\left(\frac{t}{t_0}\right)+C}{\gamma_0}, \qquad (11)$$

where $\Delta V_o(t)$ is the transient annealing curve per unit dose, γ_0 is the total dose used to obtain the transient annealing curve, A is the magnitude of the slope of the transient annealing curve, and C is the intercept at $t = t_0$. Assuming device response is linear with dose, Eq. (11) can be used to

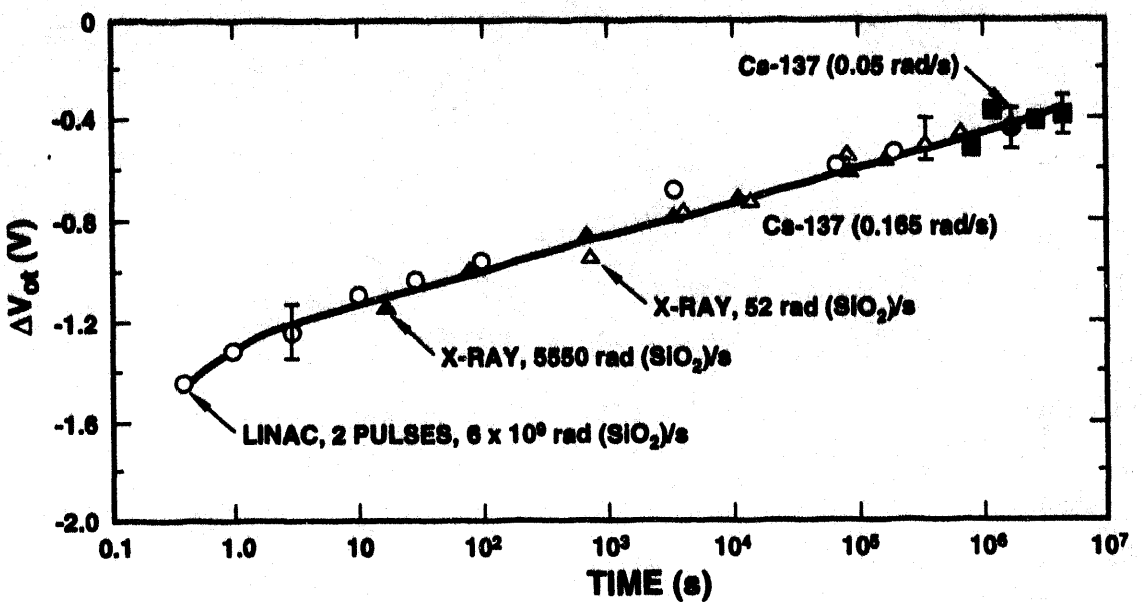


Figure 24: The change in ΔV_{ot} during anneal at room temperature for transistors irradiated at dose rates from 6 x 10^9 to 0.05 rad(Si)/s. (After Ref. 61)

determine ΔV_{ot} by convolving the dose rate, $\dot{\gamma}(t)$, with the transient annealing curve, ΔV_o, i. e., [63,64]

$$\Delta V_{ot} = \int_0^t \dot{\gamma}(\tau)\Delta V_o(t-\tau)d\tau \,. \tag{12}$$

Using Eq. (12), one can determine ΔV_{ot} at any dose or dose rate from a single set of irradiation and anneal measurements. This is especially important for space systems, where it is not practical to test devices at space-like dose rates. Thus, using linear systems theory, ΔV_{ot} can be predicted using standard laboratory measurements [63-65].

The logarithmic decrease in ΔV_{ot} in time is characteristic of most hardened and commercial technologies. Some commercial technologies exhibit much less oxide-trap charge neutralization [66]. For these technologies, nearly the same value of ΔV_{ot} may be measured whether one irradiates at moderate dose rates or at very low dose rates due to the low charge-neutralization rate.

We will next discuss the temperature and bias dependence for the neutralization of oxide-trap charge. The neutralization of oxide-trap charge has been found to be a function of temperature for some technologies [67,68] and nearly independent of temperature for other technologies [69-71]. An example of a technology with a temperature dependence is illustrated in Fig. 25 [67]. This figure is a plot of the threshold voltage versus time for hardened n-channel transistors irradiated at room temperature to 1 Mrad(Si) and then annealed under bias at varying temperatures. The bias during irradiation and anneal was 10 V and the oxide thickness was

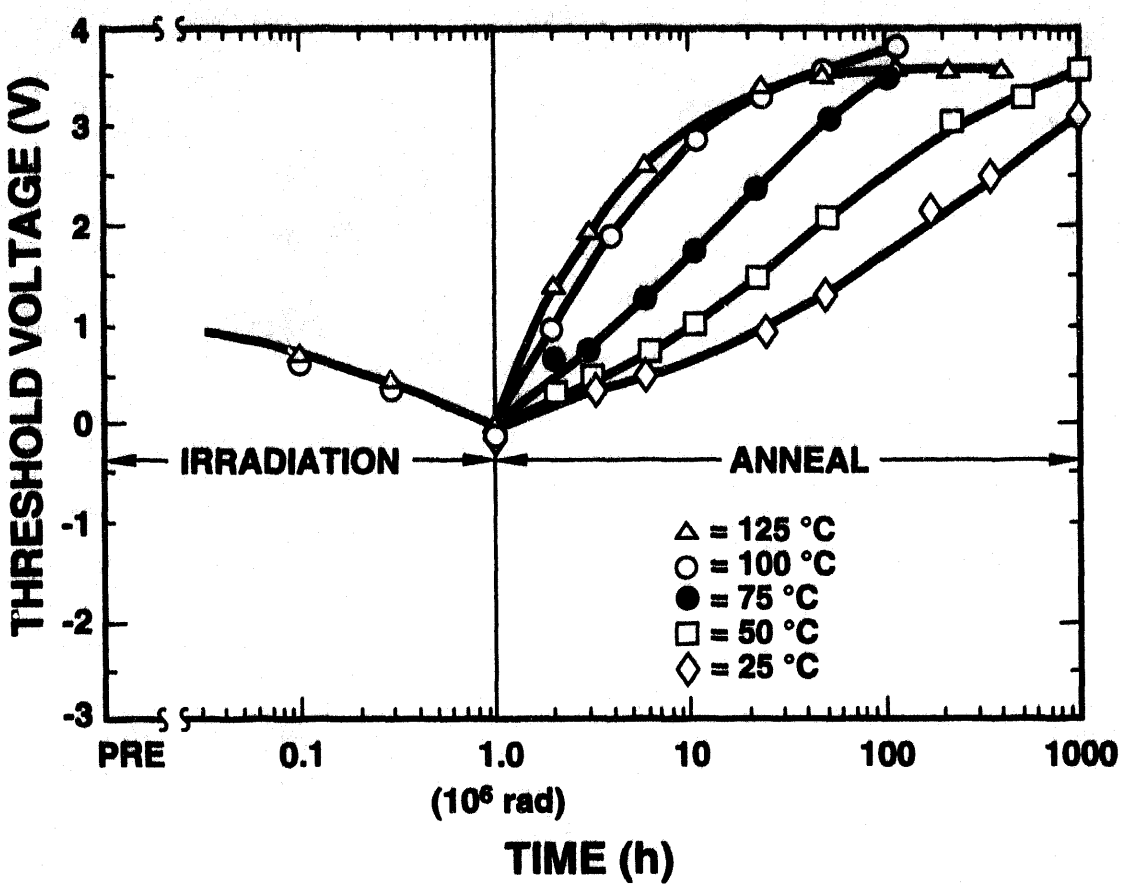


Figure 25: Temperature dependence of trapped-positive charge neutralization. For this data the change in threshold voltage is dominated by a decrease in oxide-trap charge. (After Ref. 67)

45 nm. For these transistors the increase in threshold voltage is due almost entirely to a decrease in oxide-trap charge. Very little change in interface-trap charge (discussed below) occurs during anneal for these transistors. It is clear in Fig. 25 that the increase in the threshold voltage, and thus, the decrease in oxide-trap charge, is a strongly thermally activated process. The time for 50% neutralization of the threshold voltage varies from approximately 4.3×10^6 s at 125°C to 1.1×10^4 s at 25°C. This gives an activation energy of ~0.41 eV [67]. These data suggest that for this technology it should be possible to simulate the neutralization of oxide-trap charge that occurs for a low-dose-rate space irradiation by irradiating the transistors using a laboratory radiation source and then annealing the transistors at elevated temperatures. Whether or not a technology exhibits a temperature dependence will depend on the energy distribution of the oxide traps as discussed below in Section 4.4.2.

Neutralization of oxide-trap charge for hardened transistors is also bias dependent as is illustrated in Fig. 26 [67] for transistors from a hardened technology. This figure is a plot of ΔV_{ot} versus time for n-channel transistors irradiated at room temperature to 1 Mrad(Si) and annealed at 100°C under bias. The irradiation bias was 10 V and the anneal bias was varied from 0 to 10 V. Transistors were annealed at 100°C to accelerate the neutralization of oxide-trap charge. Qualitatively similar results are obtained for room temperature anneals. For these transistors,

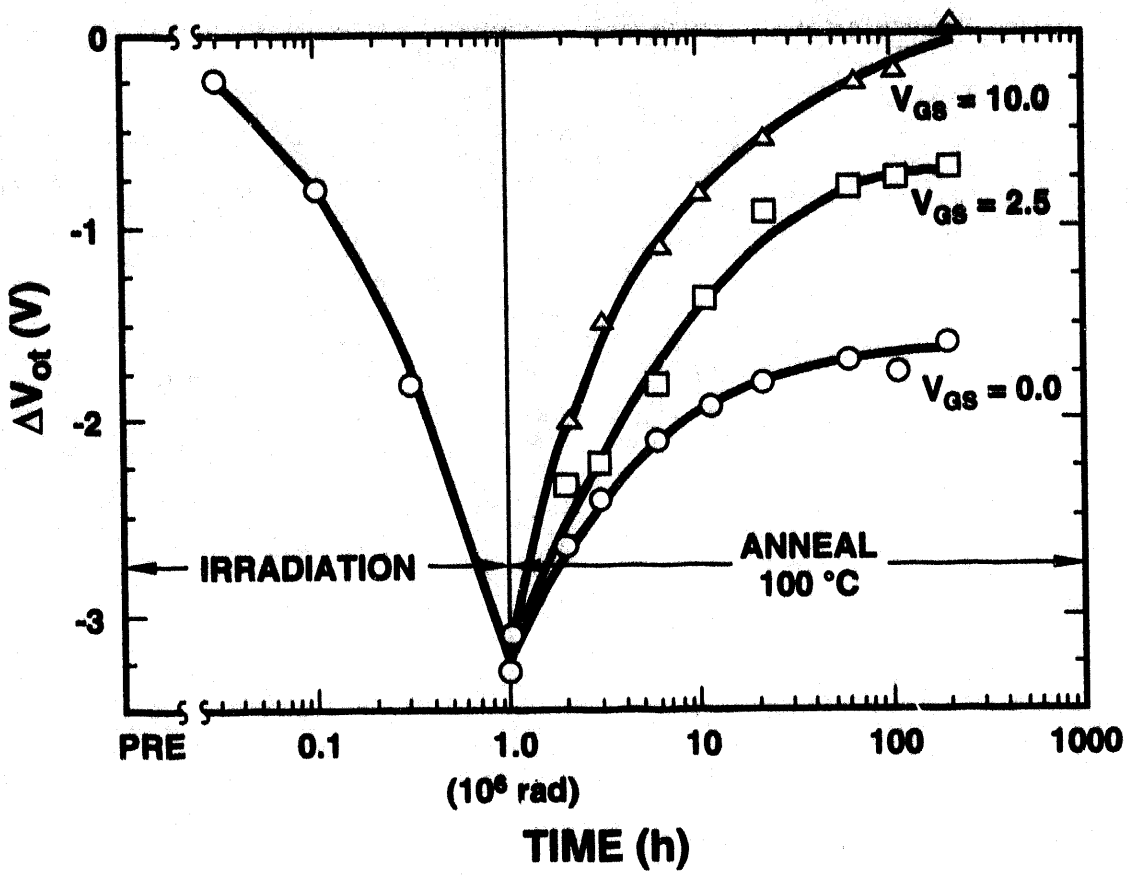


Figure 26: Bias dependence for the neutralization of oxide-trap charge. (After Ref. 67)

increasing the anneal bias greatly accelerates the neutralization of oxide-trap charge and increases the amount of neutralized charge [67,72]. For an anneal bias of 0 V, only 50% of the oxide-trap charge is neutralized, as compared to virtually 100% of the oxide-trap charge for an anneal bias of 10 V.

The neutralization of oxide-trap charge is often reversible [67,69,73]. Figure 27 [67] is a plot of ΔV_{ot} for n-channel transistors irradiated to 1 Mrad(Si) at room temperature, annealed with a 10 V bias for 200 h at 100°C, and then annealed with a -10 V bias for an additional 30 h at 100°C. During the anneal with positive bias (+10 V), ΔV_{ot} is completely neutralized (within experimental uncertainty). After the bias is switched from positive to negative, some oxide-trap charge reappears. This indicates that for these devices a large fraction of the oxide-trap charge is not permanently annealed under these anneal, bias, and temperature conditions. Instead, the defect centers associated with the oxide-trap charge are still present and the charge is merely compensated. The decrease and increase in oxide-trap charge by switching bias can continue for many cycles [69,73].

The energy distribution of oxide traps has been inferred from combined thermally-stimulated-current (TSC) and capacitance-voltage measurements [74]. In a TSC measurement, a MOS capacitor is slowly heated under bias. This causes a gate-to-substrate current (TSC current)

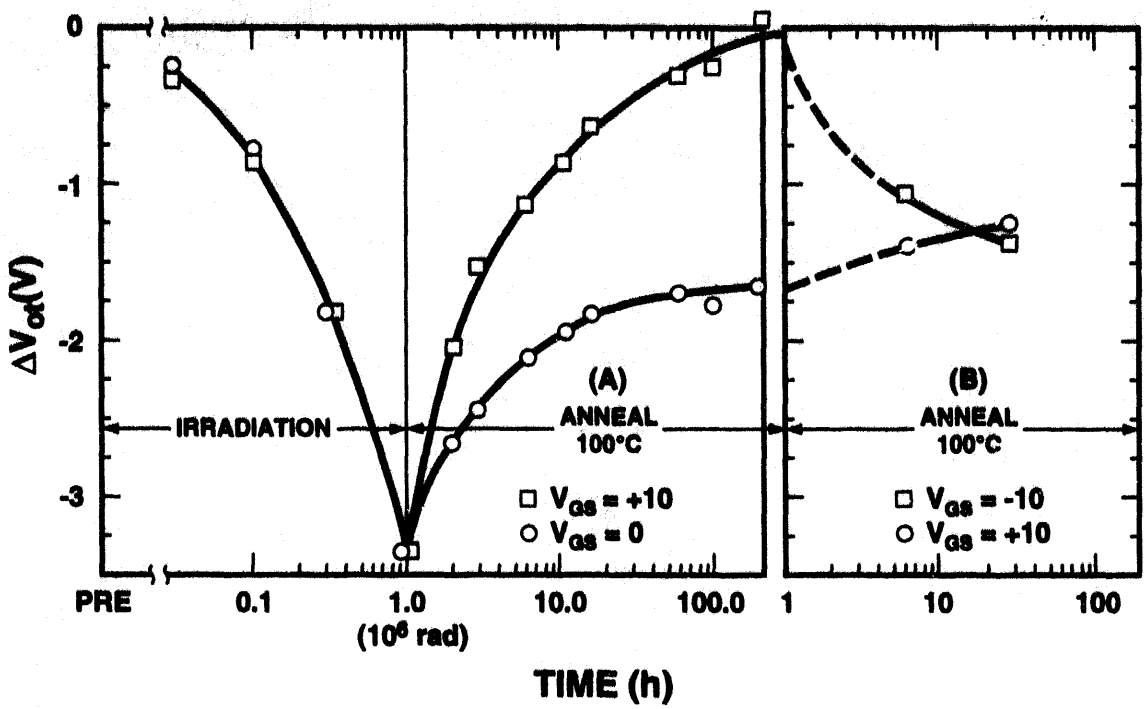


Figure 27: The change in oxide-trap charge for transistors irradiated with a +10 V bias, annealed with a +10 V for 200 h, and annealed with a -10 V bias for 30 h (squares), and for transistors irradiated with a +10 V bias, annealed with a -10 V for 200 h, and annealed with a +10 V bias for 30 h (circles). (After Ref. 67)

as holes are de-trapped [75]. The TSC current is recorded as a function of temperature. From these measurements the concentration of oxide-trap charge can be determined as a function of energy in the band gap. Figure 28 is a plot of the energy distribution of oxide traps measured on capacitors fabricated in five different technologies [74]. All of the devices show an energy distribution of the same basic form. Except for possibly the AT&T 18-nm technology, each technology shows a minor peak at around 1.2 eV and they all show a larger broad peak at around 1.7 to 2.0 eV.

4.4.2 Mechanisms for Neutralization

The bias, temperature and logarithmic time dependence of the neutralization of oxide-trap charge can be accounted for by invoking two mechanisms: 1) the tunneling of electrons from the silicon into oxide traps, and 2) the thermal emission of electrons from the oxide valence band into oxide traps. These two mechanisms are depicted in Fig. 29 [76]. The tunneling of electrons has been examined by several workers [62,76-79]. The probability of an electron tunneling from the silicon to an oxide trap is given by [62,76,77],

$$p_{tun} = \alpha e^{-\beta x} , \qquad (13)$$

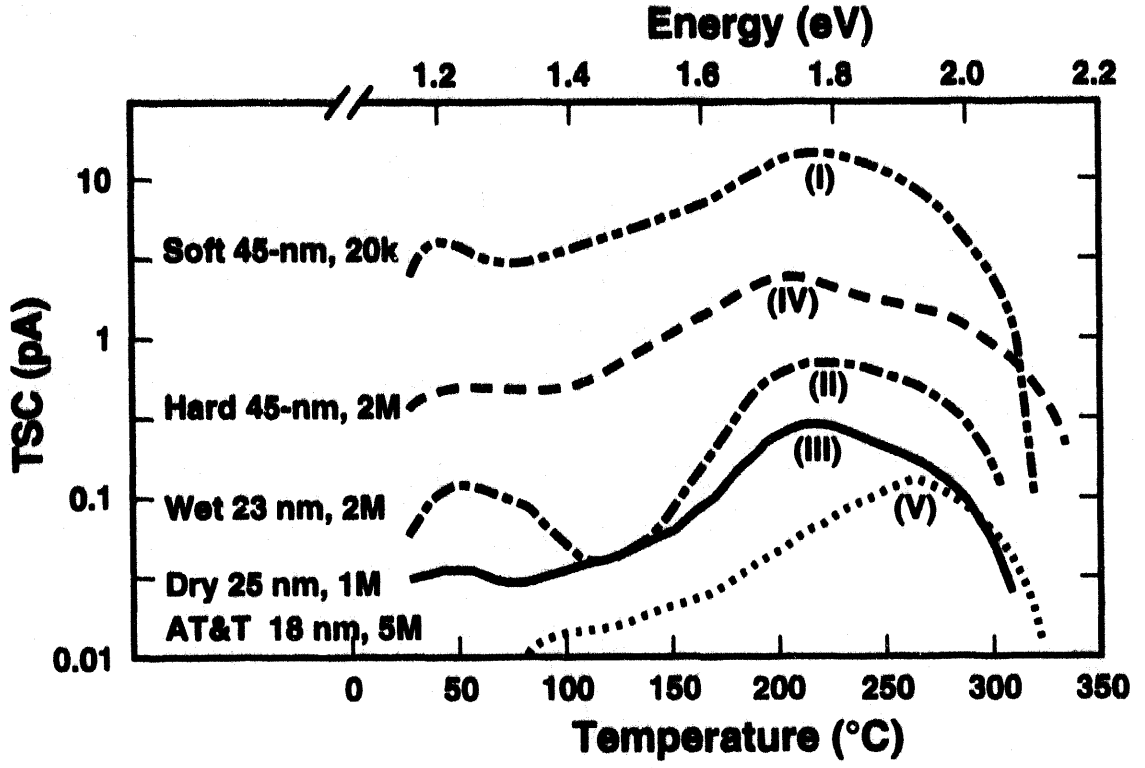


Figure 28: Energy distribution of hole traps determined from combined TSC and C-V measurements for five technologies. (After Ref. 74)

where α is the attempt to escape frequency, x is the distance of the trap from the Si/SiO_2 interface, and β is a tunneling parameter related to the electron barrier height. Note that p_{tun} is independent of temperature, but varies exponentially with the distance of the trap from the Si/SiO_2 interface. The tunneling process can be depicted as a tunneling front moving into the oxide. If the tunneling front is defined as the position corresponding to the maximum rate of tunneling, $x_m(t)$, then the distance of the front into the oxide at a given time t is given by [62,76,77],

$$x_m = \frac{1}{2\beta}\ln(\alpha t) \; . \tag{14}$$

Note that the distance that the front moves into the oxide varies logarithmically with time. Therefore, for an electron to tunnel into a trap on a reasonably short time scale, the trap must be very close to the Si/SiO_2 interface. For SiO_2, the tunneling front moves into the oxide at a rate of 0.2 to 0.4 nm/(decade in time) [62]. If the trap is more than ~4 nm from the interface, it will be essentially inaccessible to an electron tunneling from the silicon into the trap. Thus, the rate and number of oxide traps neutralized by electron tunneling is highly dependent on the spatial distribution of traps in the oxide. The spatial distribution of traps in the oxide is in turn highly dependent on the device fabrication process. Thus, the rate and number of traps neutralized by electron tunneling will also depend on device fabrication techniques [62].

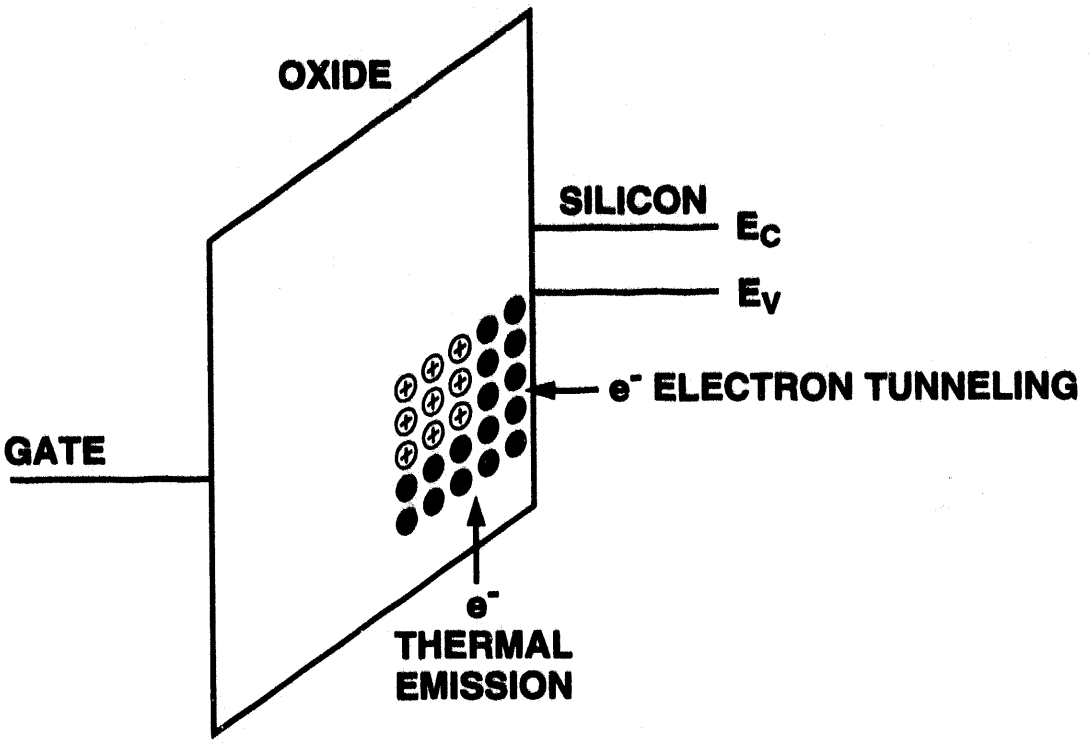


Figure 29: Schematic diagram illustrating the neutralization of oxide-trap charge by electron tunneling from the silicon and by thermal emission of electrons from the oxide valence band. (After Ref. 76)

Trap neutralization by thermal emission of electrons from the oxide valence band has also been examined by several workers [68,76,80,81]. For a thermal emission process, the probability, p_{em}, of an electron being emitted from the oxide valence band into a trap is given by [76,80,81]

$$p_{em} = AT^2 e^{-\phi_t q/(kT)} , \tag{15}$$

where ϕ_t is the difference in energy between the trap and the oxide valence band and A is a constant which depends on the capture cross-section of the trap and other parameters. For the thermal emission process, p_{em} varies exponentially with temperature, but is independent of the spatial position of the trap. This mechanism accounts for the strongly thermally activated neutralization of holes noted in Fig. 25. Similar to a tunneling front, a thermal emission front as a function of time can also be defined. Defining the thermal emission front as the time corresponding to the point of maximum emission, $\phi_m(t)$, it can be written as [76,80,81]

$$\phi_m(t) = \frac{kT}{q} \ln(AT^2 t) . \tag{16}$$

McWhorter, et al. [76], combined tunneling and thermal emission into a single model of trapped-hole annealing. Combining tunneling and thermal emission, the distribution of trapped holes $p_t(x,\phi_t, t)$ as a function of position, energy, and time can be written as [76]

$$p_t(x,\phi_t,t) = p_0(x,\phi_t)e^{-(p_{tm}+p_{em})t} , \quad (17)$$

where $p_0(x,\phi_t)$ is the initial density of trapped holes in energy and position immediately following irradiation. Using Eq. (17) the temperature and electric field dependence of oxide-trap charge neutralization can be determined.

Clearly, the spatial and energy distributions of the oxide traps will strongly affect the rate at which charge neutralization occurs. For tunneling, the spatial distribution of the oxide traps must be close enough to the Si/SiO_2 interface. For thermal emission, the energy distribution of the oxide traps must be close enough to the oxide valence band. Not only will the spatial and energy distributions of the oxide traps affect the rate of neutralization at room temperature and constant bias, but they will also affect its temperature and bias dependence. The spatial and energy distributions are affected by device fabrication conditions [62]. For the hardened device data of Figs. 25-27 which show a temperature and bias dependence, the oxide traps are apparently accessible to neutralization by both thermal emission and tunneling. For commercial transistors which show less neutralization [66], the oxide traps are apparently less accessible by thermal emission or tunneling for the bias and temperature conditions examined.

By reversing the bias, the oxide charge can be recovered [67,68,73]. Similar requirements apply for an electron to leave a hole trap as for an electron to neutralize a trap. For an electron to be emitted from a neutralized hole trap, thermal emission requires an empty hole in the oxide valence band and tunneling requires an empty hole in the silicon valence band.

In addition to the neutralization of oxide-traps by electron tunneling or thermal emission, oxide-trap charge also can be compensated as electrons are trapped at electron trap sites associated with the trapped holes. Combined TSC and C-V measurements have shown that there can be large concentrations of electron traps in a thermal oxide [74]. Figure 30 is a plot of the number of electron traps relative to the number of hole traps for two different technologies [74]. Note that for the dry-gate oxide technology, the number of electron traps is approximately 1/2 (0.48±0.09) that of the number of hole traps. For these devices with a positive gate bias, a large fraction of the total number of trapped holes can be compensated by trapped electrons quickly after irradiation (or even during irradiation). For the wet-gate oxide technology, where the fraction of electron traps (0.16±0.06) is considerably less, the oxide traps will be compensated at a much slower rate.

4.4.3 Microscopic Defect Centers

Several microscopic point defects have been identified in irradiated thermally grown oxides [44,82-90]. The most important of these is the E' center [44,82-85]. At least nine variations of the E' center have been identified in either thermally grown oxides or in bulk

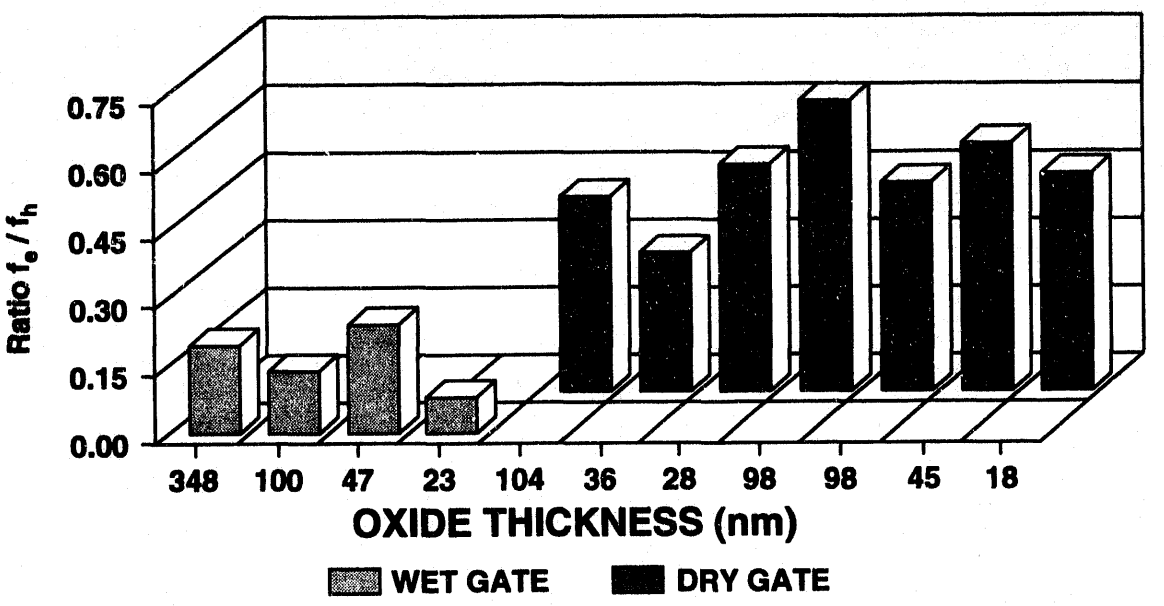
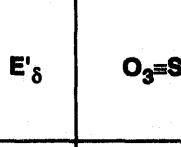
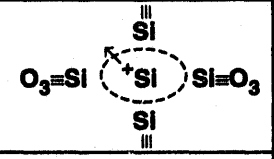


Figure 30: Ratio of trapped electrons to trapped holes for wet- and dry-gate oxide transistors with varying oxide thicknesses. (After Ref. 74)

crystalline or fused oxides. These variations are summarized in Table II [44]. Listed in Table II are the name of the defect (type), precursor state, EPR active state, charge state, g-tensor elements, and the reliability of the assessment of its properties (how sure workers are of the identification with four stars being the most reliable). As a guide for deciphering the notation, the combination $Si{\equiv}O_3$ indicates a silicon atom bonded to three oxygen atoms and an arrow, $\uparrow$ or $\bullet$, indicates a net magnetic moment (EPR center). Most E' centers are characterized by an unpaired electron highly localized on a silicon atom bonded to three oxygen atoms. The chemical notation for the generic E' center is given by $\uparrow Si{\equiv}O_3$ or $\bullet Si{\equiv}O_3$. An EPR trace illustrating an E' signal was given in Fig. 18. The double-humped structure of the E' EPR signal in Fig. 18 is characteristic of an axially symmetric point defect in an amorphous material [44]. One of the more common types of E' centers identified in thermally grown oxides is the E'_γ center. The chemical notation for the E'_γ center is given by $O_3{\equiv}Si\bullet\ {}^{+}Si{\equiv}O_3$. This notation indicates that an E'_γ center is a trivalent silicon atom bonded to three oxygen atoms. It becomes paramagnetic and positively charged when a radiation-induced hole becomes trapped at the vacancy site of one of the silicon atoms. It is identified by an EPR signal with a zero crossing at $g = 2.0005$. A schematic illustration of the precursor and the EPR active state of the E'_γ center is given in Fig. 31 [44]. For thermal oxides, the precursor state exists prior to irradiation. (This is not necessarily true for bulk crystalline oxides [44].) It occurs naturally, usually in greatest density close to the Si/SiO_2 interface due to the lattice mismatch between the silicon substrate and the oxide (which may be an indication of an incomplete oxidation process) or due to out-diffusion of oxygen in the oxide [54].

Three other types of E' centers identified in irradiated thermal oxides are the E'_δ [87] and the 74-G [88-90] and 10.4-G doublets [90]. The E'_δ center likely results from capturing a hole at a silicon interstitial/oxygen vacancy complex. It is identified spectroscopically by differing g-tensors than the E'_γ. The E'_δ center also anneals at lower temperatures than the E'_γ center [91].

TABLE II: List and chemical structure of E' centers that have been identified in thermal gate oxides.

Type	Precursor	ESR Active State	Charge State	g-tensor Elements	Reliability
E'_1	$O_3{\equiv}Si\text{-}O\text{-}Si{\equiv}O_3$	$O_3{\equiv}Si^{\uparrow}$ $^{+}Si{\equiv}O_3$	Positive ?	g_1= 2.00176 g_2= 2.00049 g_3= 2.00029	**
E'_γ	$O_3{\equiv}Si\text{-}Si{\equiv}O_3$	$O_3{\equiv}Si^{\uparrow}$ $^{+}Si{\equiv}O_3$	Positive	g_1= 2.0018 g_2= 2.0006 g_3= 2.0003	****
E'_s	$^{\uparrow}Si{\equiv}O_3$	$^{\uparrow}Si{\equiv}O_3$	Neutral	g_1= 2.0018 g_2= 2.0003 g_3= 2.0003	***
E'_d	$O_3{\equiv}Si\text{-}O\text{-}Si{\equiv}O_3$	$O_3{\equiv}Si^{\uparrow}$ $^{\uparrow}O\text{-}Si{\equiv}O_3$	Neutral ?	g_1= 2.00153 g_2= 2.00012 g_3= 2.00000	**
E'_α	$O_3{\equiv}Si\text{-}O\text{-}Si{\equiv}O_3$	$O\text{-}O\text{-}\vec{Si}{\equiv}O_2$ $^{+}Si{\equiv}O_3$	Positive ?	g_1= 2.0018 g_2= 2.0013 g_3= 1.9998	*
E'_β	$O_3{\equiv}Si\text{-}Si{\equiv}O_3 + H^0$	$^{\uparrow}Si{\equiv}O_3$ $H\text{-}Si{\equiv}O_3$	Neutral ?	g_1= 2.0018 g_2= 2.0004 g_3= 2.0004	*
E'_δ			Positive	g_1= 2.0018 g_2= 2.0021 g_3= 2.0021	***
$E'_{74\text{-}G}$	$O_3{\equiv}Si\text{-}Si{\equiv}O_2$ (H)	$H\text{-}\vec{Si}{\equiv}O_2$ $^{+}Si{\equiv}O_3$	Positive	g = 2.0016 zero-crossing	***
$E'_{10.4\text{-}G}$	?	$H\text{-}O\text{-}\vec{Si}{\equiv}O_2$	?	g_1= 2.0018 g_2= 2.0006 g_3= 2.0004	*

Like the E'_γ center, the E'_δ center has a positive paramagnetic charge state. The 74-G and 10.4-G doublets are hydrogen-associated E' centers [88-90]. The structure of the 74-G doublet has been determined to be an unpaired spin on a silicon atom bonded to two oxygen atoms and one hydrogen atom. Its chemical notation is given by $H\text{–}Si{=}O_2{\bullet}\ {}^{+}Si{\equiv}O_3$. It has a positive paramagnetic charge state. In order to observe the 74-G doublet, thermal oxides must be irradiated to very high radiation levels (~10^8 rad) [89], or subjected to hydrogen following irradiation [90].

Lenahan and Dressendorfer [82] were the first to show a strong correlation between the E' center and radiation-induced positive charge (oxide-trap charge) for some thermal oxides. Using electron spin resonance, C-V, annealing, and etchback measurements, they observed an approximate one-to-one correlation between positive charge and the number of E' centers. Similar increases were observed during irradiation and similar decreases were observed during anneal. This correlation is illustrated as a function of dose in Fig. 32 [82]. Plotted in Fig. 32 are the number of E' centers measured using EPR and $\Delta V_{mg}C_{ox}/q$ measured on capacitors versus dose. ΔV_{mg} is the voltage shift at midgap in units of $10^{12}/cm^2$ and C_{ox} is the oxide capacitance. Assuming that interface-trap charge is neutral at midgap and that oxide-trap charge is located

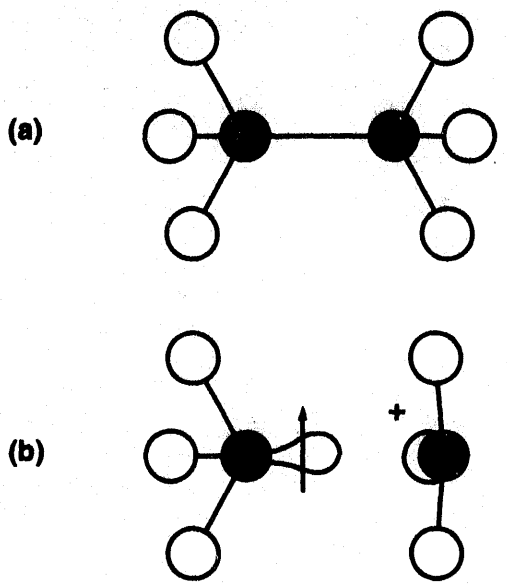


Figure 31: Schematic illustration of the precursor a) and EPR active state b) of the E'_γ center. (After Ref. 44)

very close to the Si/SiO_2 interface, $\Delta V_{mg}C_{ox}/q$ is approximately equal to the concentration of oxide-trap charge. Thus, as noted in Fig. 32, there is approximately a one-to-one correlation between the increase in the number of E' centers and concentration of trapped charge in the oxide with dose. Using etch-back measurements, they also found the same spatial distribution in the oxide for the number of E' centers as for the number of oxide-trap charge. Most of the E' centers and oxide-trap charge were determined to be located close to the Si/SiO_2 interface (within 10 nm for a 1100 nm thick oxide). Additional work has shown that, by selectively injecting electrons and holes into the oxide using ultraviolet illumination, the charge of the E' center (and the trapped positive charge in the oxide) could be reversed [82,92]. These results are consistent with the data of Fig. 27.

Even though the work of Lenahan and Dressendorfer showed a good correlation between the number of E' centers and oxide-trap charge for some oxides, recent works on thick buried oxides for silicon-on-insulator technology (see Section 5.1) and on thermally grown gate oxides [91] have raised several questions about the general correlation between the number of E' centers and oxide-trap charge. Work performed on SIMOX [93,94], BESOI [91], and thermal oxide [91] material has shown the absence of a correlation between the number of E' centers and oxide-trap charge (See Section 5.1). For the buried oxide materials, this is especially puzzling for BESOI materials which are two thermally grown oxides bonded together. One would expect that for BESOI materials they should have the same spectroscopic properties as for standard thermally grown gate oxides except near the bond region. Thus, in general there may or may not be a correlation between the number of E' centers and oxide-trap charge.

4.5 Interface Traps

In addition to oxide traps, radiation also induces interface traps at the Si/SiO_2 interface [95]. Interface traps exist within the silicon band gap at the interface. Because of their location at the interface, the charge of an interface trap can be changed easily by applying an external bias.

Interface traps can be positive, neutral, or negative. Traps in the lower portion of the band gap are predominantly donors, i.e., if the Fermi level at the interface is below the trap energy level, the trap "donates" an electron to the silicon. In this case, the trap is positively charged. A p-channel transistor at threshold samples primarily interface traps in the lower region of the band gap. Therefore, for a p-channel transistor, interface traps are predominantly positive, causing negative threshold-voltage shifts. Conversely, traps in the upper portion of the band gap

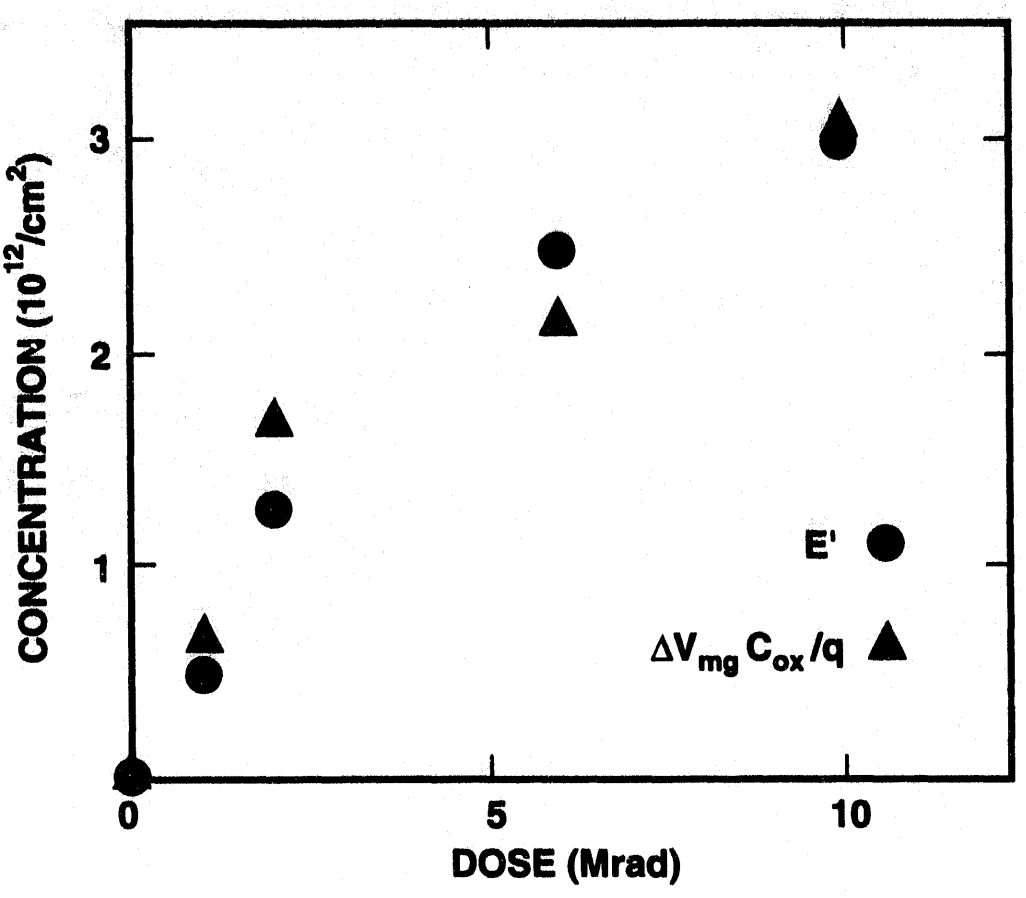


Figure 32: The increase in the number of E' centers and oxide-trap charge (approximated by $\Delta V_{mg}C_{ox}/q$) with dose. (After Ref. 82)

are predominantly acceptors, i.e., if the Fermi level is above the trap energy level, the trap "accepts" an electron from the silicon. In this case, the trap is negatively charged. An n-channel transistor at threshold samples interface traps predominantly in the upper region of the band gap. Therefore, for an n-channel transistor, interface traps are predominantly negative, causing positive threshold-voltage shifts. At midgap, interface-trap charge is approximately neutral [29-32]. Because oxide-trap charge is positive for both p- and n-channel transistors, oxide-trap charge and interface-trap charge compensate each other for n-channel transistors and add together for p-channel transistors.

Interface-trap buildup occurs on time frames much slower than oxide-trap charge buildup. Interface-trap buildup can take thousands of seconds to saturate after a pulse of ionizing irradiation. Unlike oxide-trap charge, interface-trap charge does not anneal at room temperature. These properties make interface-trap charge effects very important for low dose-rate applications, e.g., space. For an n-channel transistor, interface-traps affect device performance primarily through an increase in threshold voltage and a decrease in channel mobility. Both of these degradation mechanisms tend to reduce the drive current of "ON" transistors, leading to increases in timing parameters of an IC.

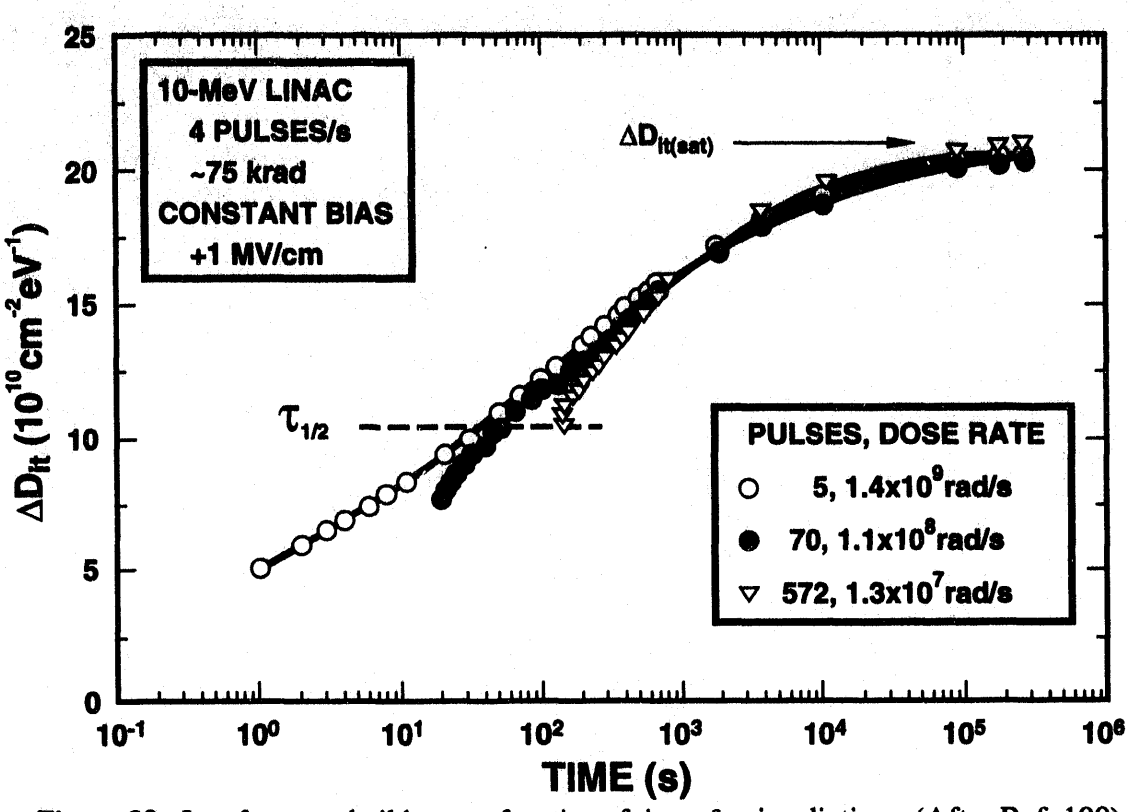


Figure 33: Interface-trap buildup as a function of time after irradiation. (After Ref. 100)

4.5.1 Properties of Buildup

With a positive bias applied to a gate oxide, immediately after a radiation pulse, some "early" interface-trap buildup can occur [96-98]. This early buildup of interface traps is present by the time of the first measurement (a few milliseconds) after a pulse of radiation. Early buildup of interface traps does not occur with a negative gate bias. This is an indication that the early buildup is not created directly by irradiation, but rather is induced by secondary processes. The early buildup is normally a small fraction of the total buildup. It has been shown to account for approximately 0 to 25% of the total buildup [97]. The amount of early buildup depends on the device fabrication process [97].

Most of the buildup of interface traps occurs seconds to thousands of seconds after a pulse of ionizing radiation [99,100]. Fig. 33 [100] is a plot of the density of interface-traps, D_{it}, versus time after a high-dose-rate irradiation. The density of interface traps is the average number of traps in a given interval of the band gap, and has the units of traps/cm^2-eV. The data for this plot were taken on polysilicon gate transistors irradiated to 75 krad(Si) in 5, 70, and 572 pulses at a 4-Hz repetition rate. The gate oxide thickness was 47 nm and the electric field across the oxide during irradiation and anneal was 1 MV/cm. For these measurements, interface-trap buildup had begun by the time of the first measurement (1 s for the data taken with 5 pulses). However, interface-trap buildup does not begin to saturate until ~10^5 s. This curve is typical of that for interface-trap buildup. For the curve taken with 5 pulses, the time for 50% buildup is approximately 35 s.

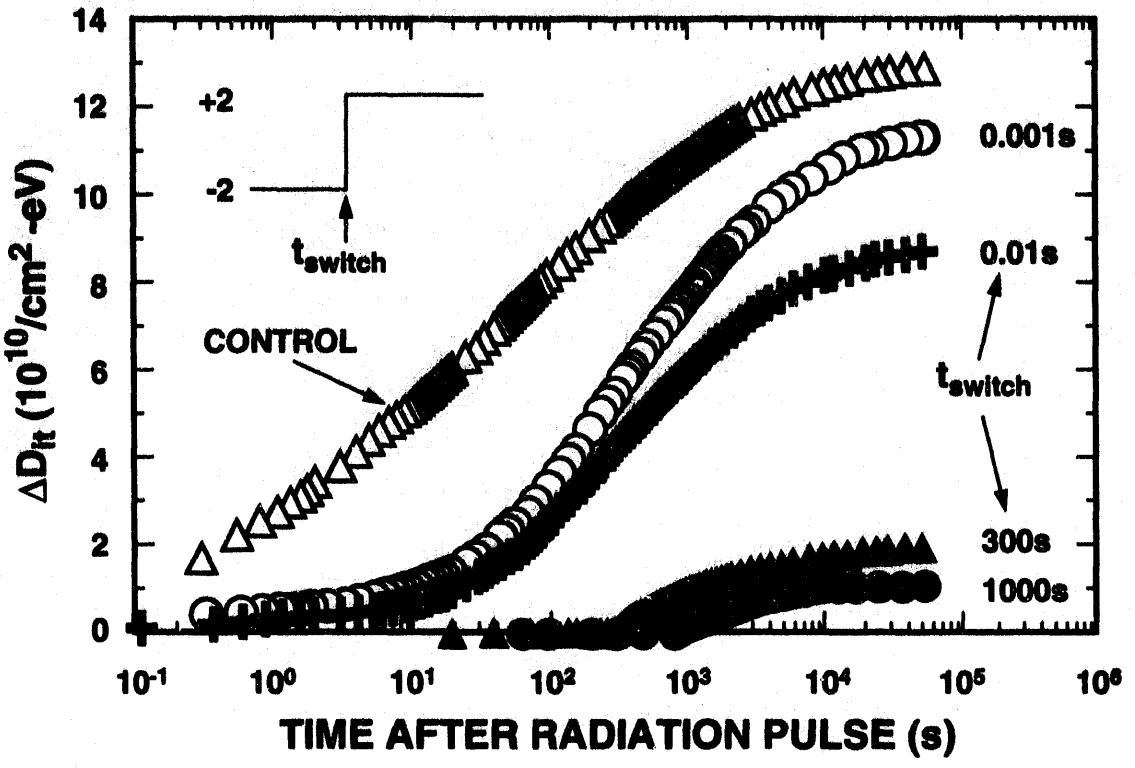


Figure 34: Interface buildup as a function of time after irradiation for transistors irradiated and annealed with a +2 V bias (control) and for transistors irradiated and annealed during the initial stages with a -2 V bias and annealed with a +2 V bias after switching at the time indicated. (After Ref. 101)

Little or insignificant buildup of interface traps occurs if a negative bias is maintained during irradiation and anneal. However, interface-trap buildup can occur for a negative bias during irradiation if the bias is switched positive shortly after irradiation. Figure 34 [101] is a plot of interface trap buildup measured on polysilicon gate transistors irradiated to between 25 and 40 krad(Si) in a single 1.5-μs radiation pulse. The gate oxide thickness was 35 nm. For the data marked "control," the bias during irradiation and anneal was 2 V. The rate of interface-trap buildup depicted in this curve is very similar to the data of Fig. 33. For the data marked 0.001 s, 0.01 s, 300 s, or 1000 s, the bias during irradiation and during the initial stages of annealing was -2 V, and then switched to +2 V at the time indicated. For the case where the bias was switched 0.001 s after irradiation, about 85% of the buildup is obtained as compared to the control (continuous +2 V bias). Note that the initial buildup of interface traps occurs at approximately 10 s for the 0.001 s switched bias irradiations; whereas, for the control data, interface-trap buildup occurs by the time of the first measurement ~0.3 s. The longer time for initial buildup for the switched bias irradiations is likely due to that fact that for the negative bias irradiations holes transport toward the gate-SiO_2 interface releasing hydrogen ions near the gate-SiO_2 interface and/or in the bulk of the oxide. The longer time for buildup is caused by the time it takes for hydrogen ions to drift to the Si/SiO_2 interface after the bias is switched positive. At the interface the hydrogen ions can react to form interface traps (see Section 4.5.5). For the positive bias irradiations, holes transport toward the Si/SiO_2 interface and hydrogen ions are released

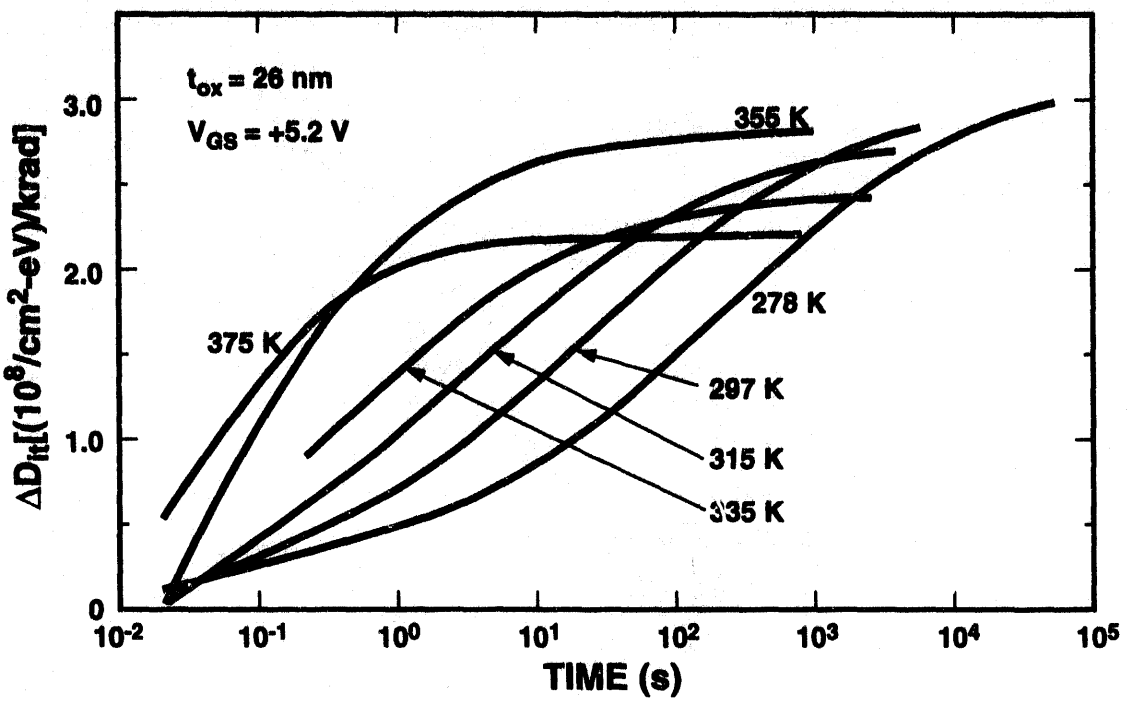


Figure 35: Interface-trap buildup after a radiation pulse for temperatures from 278 to 375 K. (After Ref. 97)

much closer to the Si/SiO_2 interface and the time it takes for hydrogen ions to drift to the Si/SiO_2 interface is significantly less. The longer the negative bias is left on, the lower is the eventual buildup. Very little interface-trap buildup occurs for either the 300 s or 1000 s switched biased irradiations.

The rate at which interface traps build up depends on the temperature of the anneal following irradiation [97,102]. Figure 35 [97] is a plot of the density of interface-trap buildup divided by the irradiation dose versus time for polysilicon-gate transistors irradiated to ~50 krad(Si) in a single 1.5-μs radiation pulse for temperatures from 278 to 375 K. The oxide electric field during irradiation and anneal was 2 MV/cm and the oxide thickness was 26 nm. The rate at which buildup occurs increases as the anneal temperature increases. The activation energy for the buildup of interface traps is ~0.71 eV for these devices. Similar activation energies have been measured on 42 nm polysilicon-gate transistors (0.79 eV) [97] and 96.5 nm metal-gate capacitors (0.8 eV) [102].

At low temperatures (<150 K), the buildup of interface traps is significantly retarded [103]. Figure 36 [103] is a plot of the density of interface traps for transistors irradiated in a single pulse at a temperature of 78 K. After irradiation, the temperature was increased, transistors were annealed at the indicated temperature for twenty minutes and then re-cooled to 78 K, and measurements were repeated. The gate bias during irradiation was 5.2 V, and the bias was varied from -5.2 to 10.4 V during anneal. From 78 to 150 K, very little interface trap buildup occurs (1 to 10% of the total). Most of the buildup (>90%) occurs at temperatures from 200 to 300 K.

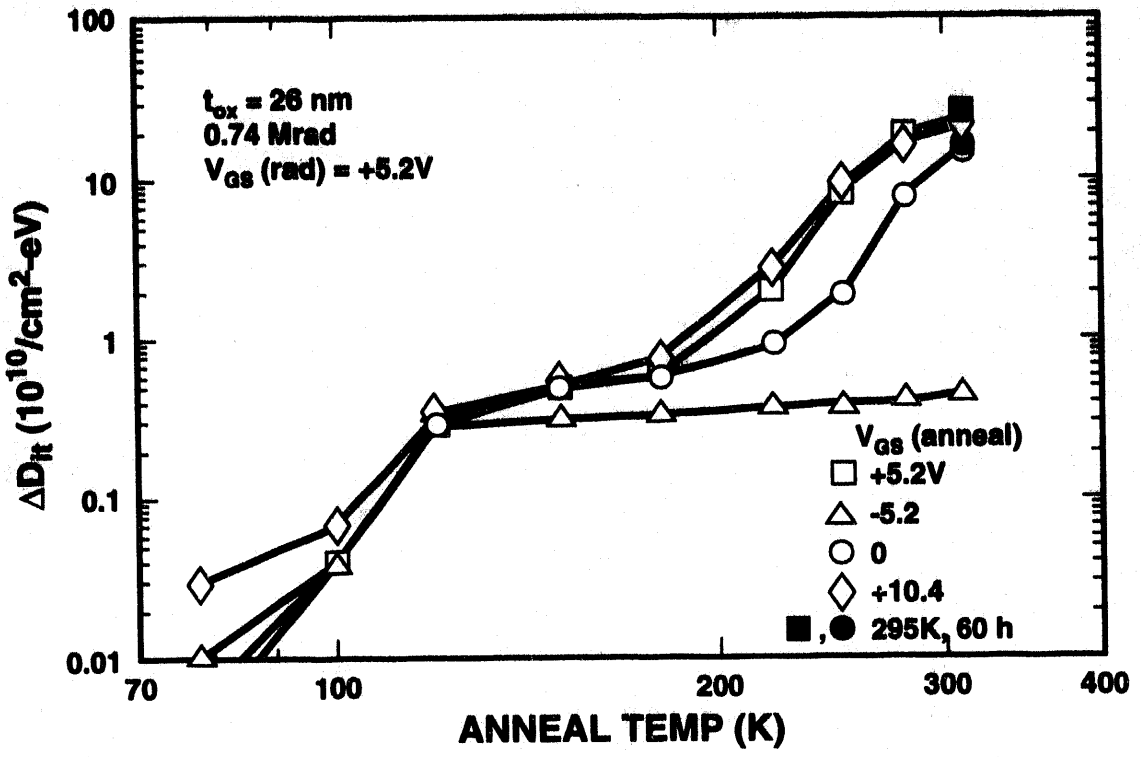


Figure 36: Interface-trap buildup after a radiation pulse for transistors annealed at temperatures from 78 to 300 K. (After Ref. 103)

For low-dose-rate irradiations, the temperature *during* irradiation can have a large impact on the number of radiation-induced interface traps. Figure 37 [104] is a plot of ΔV_{th}, ΔV_{it}, and ΔV_{ot} versus temperature for transistors irradiated to 500 krad(Si) at a dose rate of 0.27 rad(Si)/s at temperatures from 25 to 125°C with a bias of 5 V. All measurements were taken at room temperature. As the temperature during irradiation increases, the amount of radiation-induced charge increases. There are approximately twice the number of interface traps for transistors irradiated at a temperature of 125°C than for transistors irradiated at a temperature of 25°C. This large increase in interface-trap charge, coupled with a small decrease in oxide-trap charge, leads to significantly higher threshold voltages for transistors irradiated at 125°C. The large increase in threshold voltage cannot be explain by the combination of room temperature radiation response and the preirradiation dependence of the threshold voltage on anneal temperature. These data indicate that there are significant interactions between radiation and temperature for MOS device response. A large difference in threshold voltage was not observed for transistors irradiated with a gate bias of zero volts. Figure 38 [104] is a plot of the threshold-voltage shift versus temperature during irradiation for transistors irradiated to 500 krad(Si) with a gate bias of 0 and 5 V. Note that there is relatively little change in threshold voltage with the temperature during irradiation for transistors irradiated with V_{GS} = 0 V. The difference in response at 0 and 5 V can lead to a large "imbalance" (1.6 V at 125°C) in the threshold voltages of "ON" and "OFF" transistors which can cause unexpected IC failure. This can be of special importance to electronics in a space system operating at elevated temperatures (e.g., space-based nuclear reactor platform [105]).

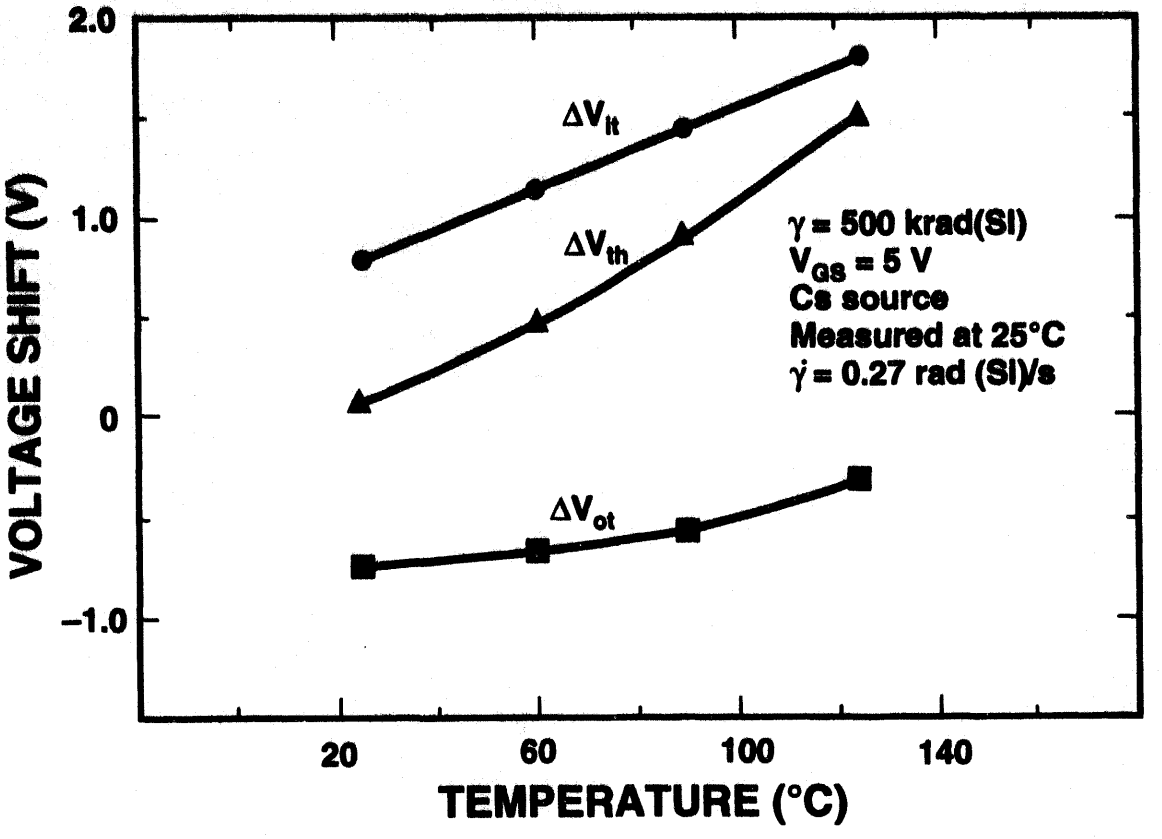


Figure 37: Dependence of the change in ΔV_{ot}, ΔV_{it}, and ΔV_{th} with the temperature during irradiation. (After Ref. 104)

For polysilicon-gate transistors the electric field dependence of interface-trap buildup is very similar to the electric field dependence of oxide-trap charge buildup [55,96]. Figure 39 [55] is a plot of the density of interface traps versus oxide electric field during irradiation for n-channel transistors irradiated to 500 krad(SiO_2) and annealed under bias. The oxide electric field during irradiation was varied from 0.3 to 5 MV/cm and kept constant at 3 MV/cm during a one-week anneal. Shown are the measured data (solid circles) and data adjusted for charge yield (open circles) by dividing the measured data by the hole yield (see Section 4.2 above). The adjusted data follow an $E^{-0.6}$ field dependence (dashed line), within experimental uncertainty equal to the electric field dependence of oxide-trap charge trapping and the hole capture cross-section near the interface. This is an indication that both oxide-trap charge and interface-trap charge buildup are linked to hole trapping near the Si/SiO_2 interface.

For metal-gate technologies, interface-trap charge buildup may or may not follow the same electric field dependence as for polysilicon-gate technologies. For metal-gate technologies, interface-trap charge has been found to increase with increasing electric field strength [102,106] and to decrease with increasing electric field strength [55].

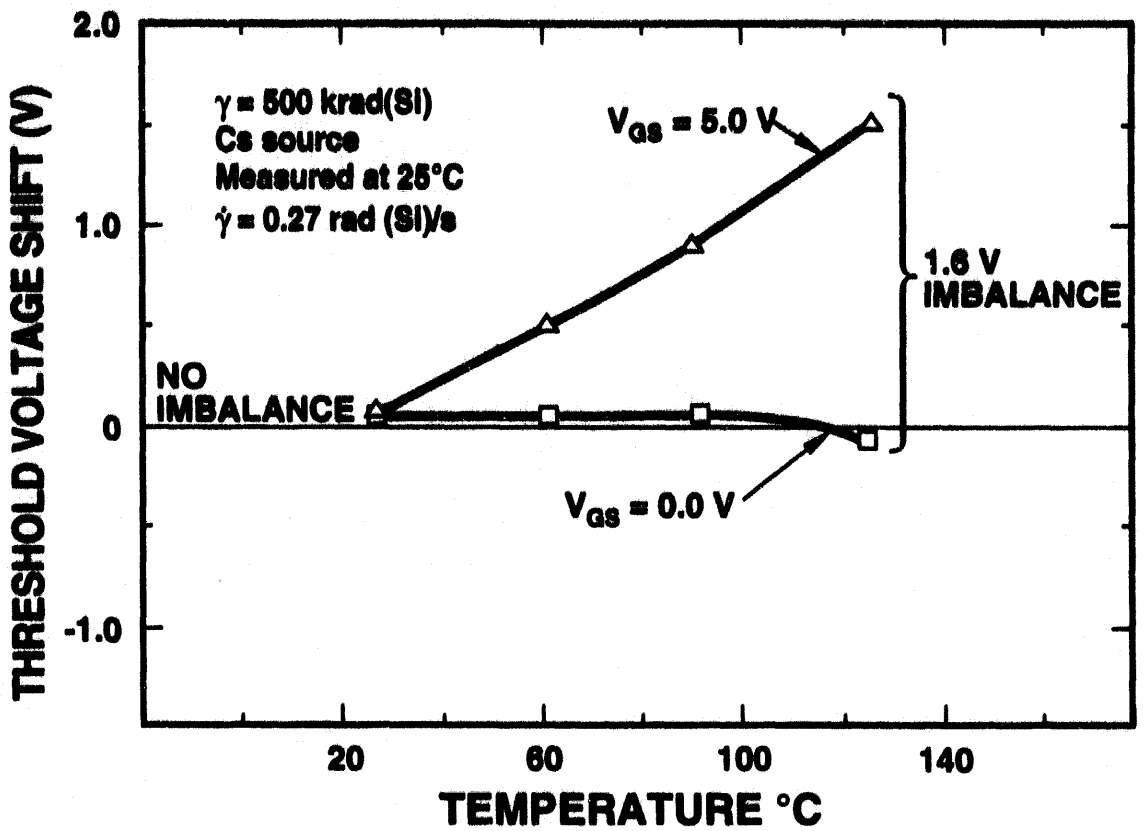


Figure 38: The change in threshold-voltage shift with the temperature during irradiation for transistors irradiated with a gate-to-source bias of 0 and 5 V. (After Ref. 104)

4.5.2 Latent Buildup of Interface Traps

Following the "normal" saturation of interface traps within 10^2 to 10^5 s after irradiation, large increases in the number of interface traps can occur [107,108]. This second buildup of interface traps can occur at long times after irradiation (>10^6 s), and can be quite significant. Figure 40 [107,108] illustrates the "latent" buildup with a plot of the threshold-voltage shift due to interface traps, ΔV_{it}, normalized to its maximum value versus time for commercial p-channel transistors irradiated to 75 krad(SiO_2) and annealed at 25°C. The bias during irradiation and anneal was 6 V. Conventional interface-trap buildup stops at approximately $\Delta V_{it}/\Delta V_{itmax} = 0.3$ within 300 s after irradiation. After this, there is a window from ~300 s to 10^6 s in which no interface-trap buildup occurs ("normal" saturation). At approximately 10^6 s after irradiation, there is a sudden increase (on a log scale) in interface-trap charge. This latter increase is the "latent" buildup of interface traps. As illustrated in Fig. 40, this latent buildup of interface traps can increase the interface-trap charge density to levels as much as four times higher than the "normal" saturated interface-trap charge density, measured 300 s after irradiation. The data of Fig. 40 were taken from transistors fabricated in a commercial technology. A latent buildup has been observed also for some hardened technologies [108]. However, in some cases, hardened technologies did not exhibit a latent buildup (for the times, biases, and temperatures examined)

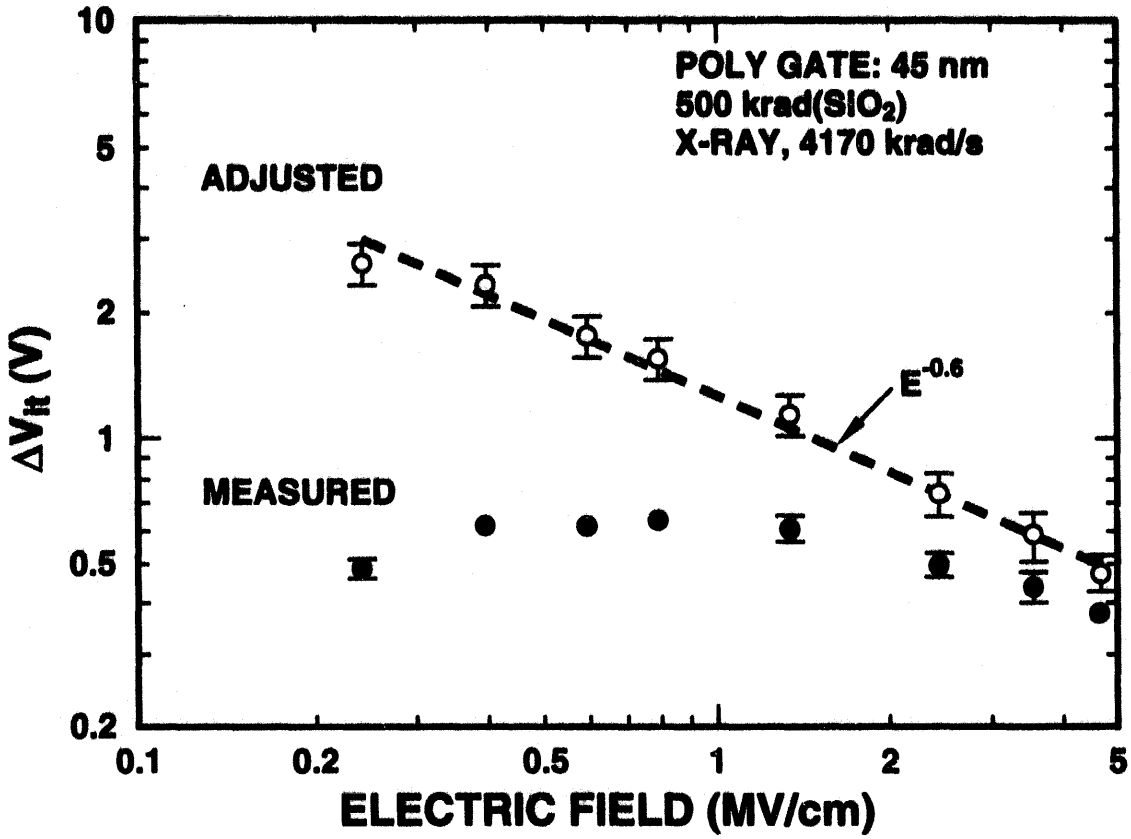


Figure 39: Electric field dependence for interface-trap buildup for as measured data (solid circles) and data adjusted for charge yield (open circles). During the one-week anneal the oxide electric field was 3 MV/cm. (After Ref. 55)

[108]. Coincident with the latent buildup is a rapid decrease in carrier mobility and in the magnitude of oxide-trap charge [107,108].

The latent buildup of interface traps is a strongly thermally activated process with an activation energy of 0.47 eV [107,108]. Note that this activation energy is much lower than the activation energy for the "normal" buildup of interface traps (~0.7-0.8 eV [97,102], see Section 4.5.1). However, the activation energy for the latent buildup is equal within experimental uncertainty to the activation energy for trapped-hole annealing (~0.41 eV [67], see Section 4.4.1) and the activation energy for the diffusion of molecular hydrogen in bulk-fused silica (~0.45 eV) [109].

Two possible mechanisms for the latent buildup have been proposed [108]. The first is the direct conversion of oxide traps into interface traps or "border traps." Border traps are oxide traps that can communicate with the silicon on the time scale of a measurement and can act electrically like interface traps (see Section 4.6) [110]. The conversion of oxide traps into interface traps may occur as electrons from the silicon tunnel into oxide traps during a biased anneal. As electrons neutralize the oxide traps, there will be a decrease in oxide-trap charge and possibly a corresponding buildup of interface traps from the release of hydrogen ions (discussed

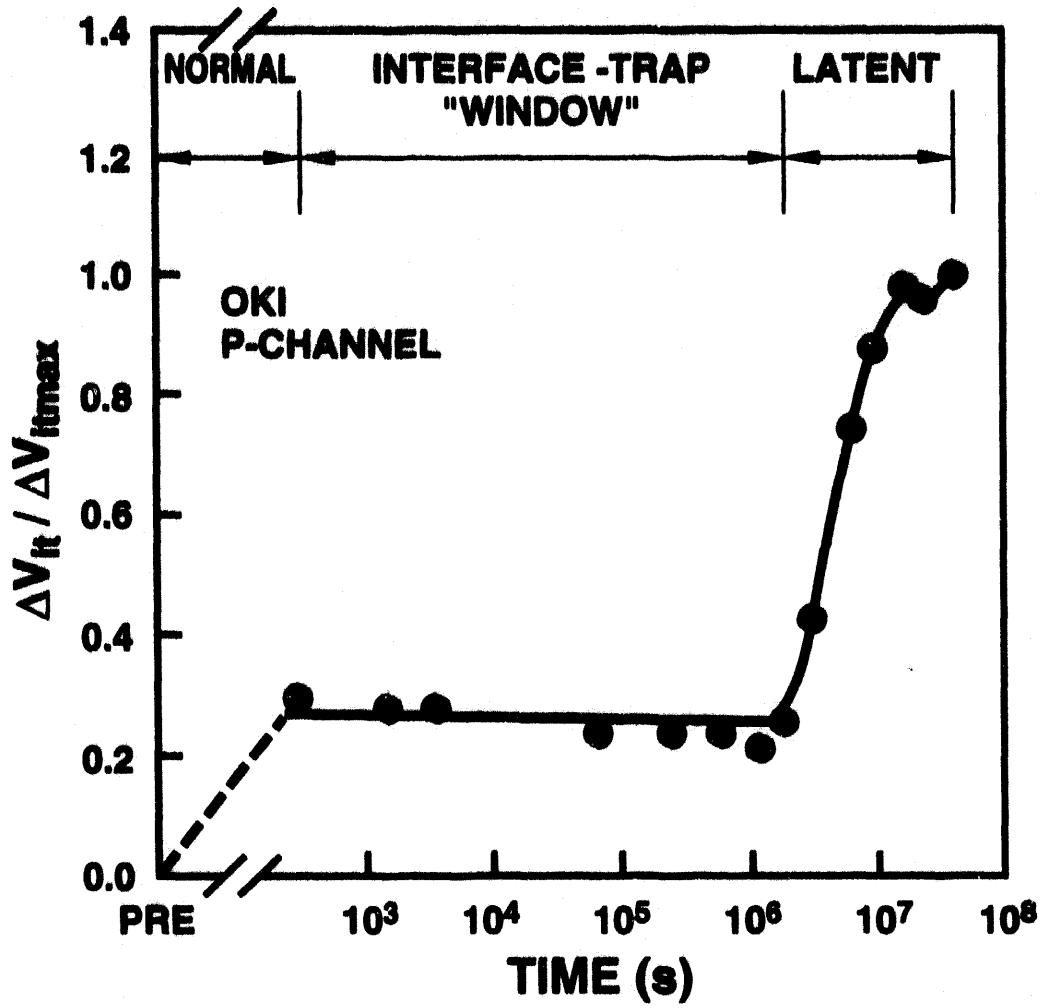


Figure 40: Latent buildup of interface traps measured on commercial transistors. (After Refs. 107,108)

below) in the neutralization process. A second possible mechanism for the latent buildup is due to the release of hydrogen atoms during irradiation in an adjacent structure and the diffusion of the hydrogen atoms to the Si/SiO_2 interface. The activation energy for the latent buildup is equal within experimental uncertainty to the activation energy for diffusion of molecular hydrogen in bulk fused silica (~0.45 eV) [109]. Near the interface the hydrogen atoms can crack at positively charged oxide traps forming hydrogen ions [111]. The hydrogen ions are then free to drift to the Si/SiO_2 interface to form interface traps (see Section 4.5.5).

The large buildup of interface traps at late times is clearly a concern for space systems. The latent buildup of interface traps can degrade the performance of ICs in space systems and may cause system failure at long times. The latent buildup of interface traps may not be predictable from laboratory measurements. For technologies in which a latent buildup is known to occur, one may increase the overtest margin or time of post-irradiation anneals used to simulate the space environment [108].

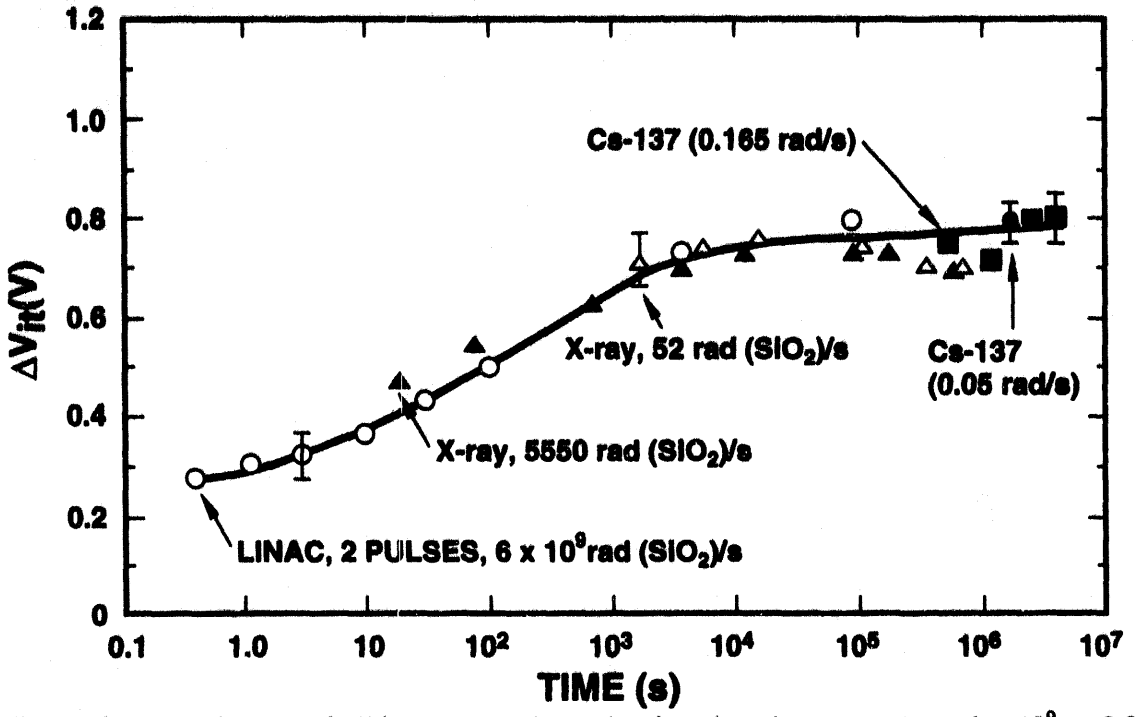


Figure 41: Interface-trap buildup for transistors irradiated at dose rates from 6 x 10^9 to 0.05 rad(Si)/s and annealed under bias at room temperature. (After Ref. 61)

4.5.3 Dose-Rate Dependence

There does not appear to be a "true" dose-rate dependence for the buildup of interface traps [61]. Figure 41 [61] is a plot of ΔV_{it} versus time for transistors irradiated to a total dose of 100 krad(SiO_2) at dose rates from $6x10^9$ to 0.05 rad(SiO_2)/s. After irradiation each transistor was annealed under bias. The bias during irradiation and anneal was 6 V. Note that as long as the total irradiation plus anneal time is the same, the same threshold-voltage shift due to interface traps is measured, regardless of the dose rate of the radiation source. If there were a "true" dose-rate dependence, the data taken at different dose rates would not fall on the same response curve.

However, if transistors are not annealed, irradiating at different dose rates can result in different values of ΔV_{it} [112]. Figure 42 [112] is a plot of ΔV_{it} and ΔV_{ot} versus dose for transistors irradiated at dose rates from 0.1 to 200 rad(Si)/s with no post-irradiation anneal. At the lower dose rates, ΔV_{it} is higher and the magnitude of ΔV_{ot} is lower than at the higher dose rates. The lower values for ΔV_{it} at high dose rates occur because for these transistors, the buildup of interface traps has not saturated for the shorter times associated with the higher dose rates. The lower values for the magnitude of ΔV_{ot} at low dose rates occur because more neutralization of oxide-trap charge takes place during irradiation for the longer times associated with the low-dose-rate irradiations. Thus, if transistors are not annealed after irradiation, a laboratory irradiation (e.g., 200 rad(Si)/s) will overestimate the amount of oxide-trap charge and underestimate the amount of interface-trap charge in space. Since these two parameters tend to compensate each other for an n-channel transistor, the net effect is a higher threshold-voltage shift for a low-dose-rate irradiation. For the data of Fig. 42, after irradiating to 1 Mrad(Si), there

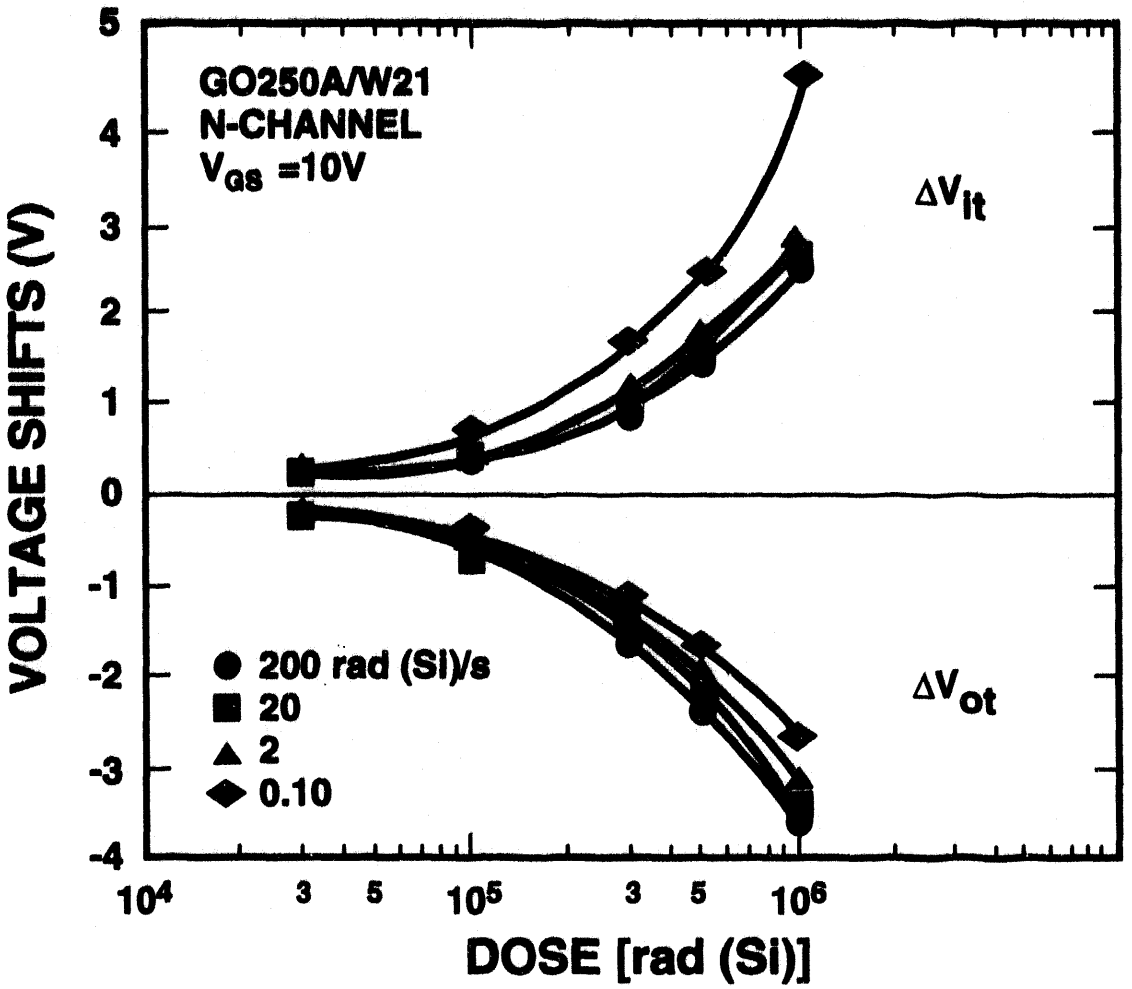


Figure 42: Interface-trap and oxide-trap charge voltage shifts for transistors irradiated at dose rates from 0.10 to 200 rad(Si)/s. (After Ref. 112)

is approximately a 3 V difference in threshold-voltage shift between the transistors irradiated at 0.1 and 200 rad(Si)/s.

4.5.4 Anneal of Interface Traps

Unlike oxide-trap charge, interface traps do not anneal at room temperature. Some interface-trap annealing at 100°C has been reported by several workers [101,113,114]. However, higher temperatures are normally required to have significant interface-trap annealing [70,115]. Figure 43 [70] is a plot of ΔV_{th}, ΔV_{it}, and ΔV_{ot} for polysilicon gate transistors irradiated to 3 Mrad(Si) and then subjected to isochronal anneals at successively higher temperatures. At each temperature transistors were annealed for 30 minutes. The oxide electric field during irradiation and anneal was 2.3 MV/cm. For temperatures from 25 to 125°C there is a buildup of interface traps. For temperatures greater than 125°C, the number of interface traps begins to decrease. After annealing at 300°C, ΔV_{it} has decreased by more than a factor of five from its peak value at

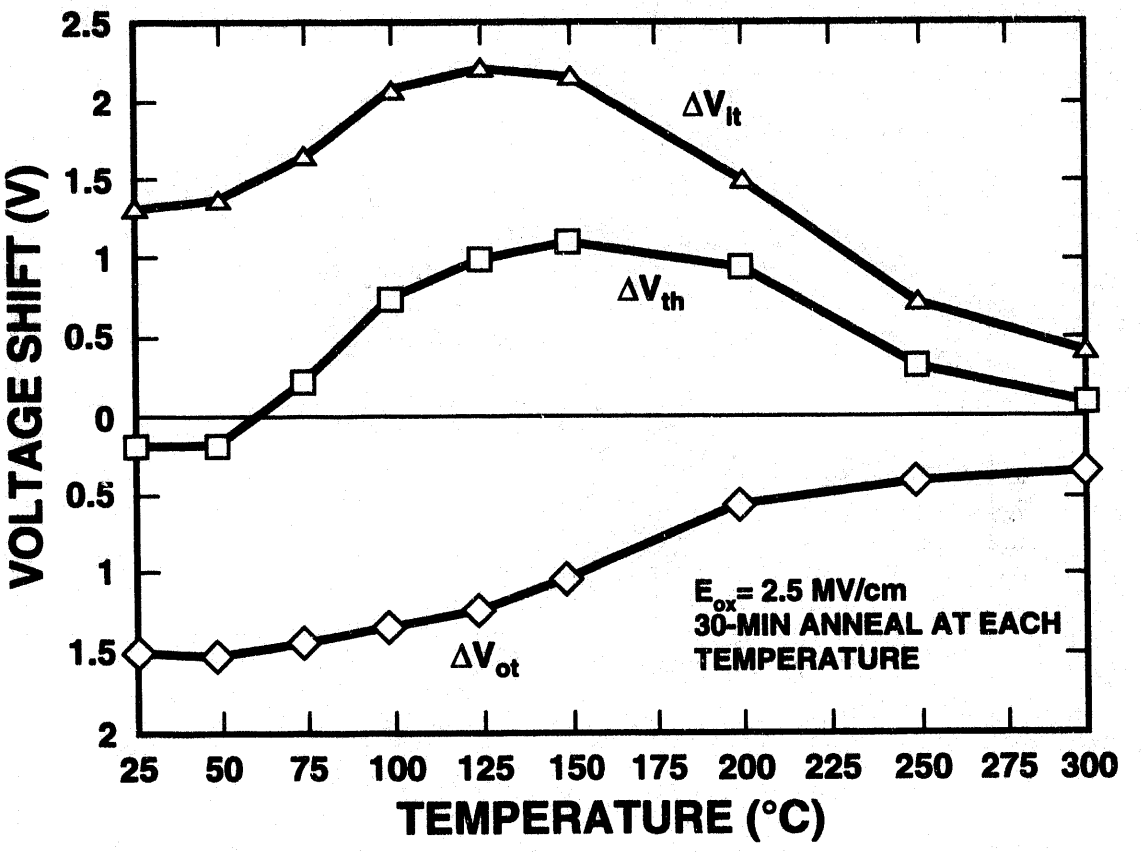


Figure 43: Annealing of interface-trap charge at elevated temperatures. (After Ref. 70)

125°C. Even though a significant amount of the interface traps have been annealed, there is still some interface-trap buildup present after the 300°C anneal.

4.5.5 Mechanisms for Interface-Trap Buildup

The mechanisms for interface-trap buildup presently are much more uncertain than the mechanisms for the buildup and neutralization of oxide charge. Several different mechanisms for interface-trap buildup have been proposed, including the direct creation of interface traps by ionizing irradiation, interface-trap creation by hole trapping, or interface-trap buildup through secondary mechanisms. The direct creation of interface traps by ionizing irradiation can be ruled out as a significant contributor to interface-trap buildup. Vacuum ultraviolet radiation experiments [116-118] showed that interface traps can be created by non-penetrating radiation. In these experiments, the top of capacitors with thin metal gates were illuminated with non-penetrating VUV radiation. All light was absorbed within the top oxide layer and none of the light reached the Si/SiO_2 interface. However, with a positively applied bias, interface trap buildup was observed to occur, similar to that for penetrating irradiation (high-energy gamma irradiation) [116,117]. These experiments confirmed that a negligible number of interface traps are created directly by irradiation. Instead, these experiments suggest that a necessary precursor to interface-trap buildup is the generation of electron-hole pairs in the bulk of the oxide and the subsequent transport of holes through the oxide.

The role of hole transport in interface-trap buildup is not well understood. Recall from Section 4.5.1 above, that interface-trap buildup takes place over relatively long times: from seconds to thousands of seconds. On the other hand, for thin gate oxides, holes can transport through a gate oxide in microseconds. Thus, the time frames for interface-trap buildup are many orders of magnitude longer than the time frames associated with hole transport. Interface-trap buildup cannot depend solely on hole trapping at the interface. Insight into the role of hole transport in interface-trap buildup was first provided by Svensson [119] and later by Winokur, et al. [113], and McLean [120].

Svensson was the first to propose a two-stage model for interface-trap buildup. In the first stage, radiation-generated holes break Si–H bonds in the bulk of the oxide, liberating neutral interstitial hydrogen atoms. In the second stage of buildup, the liberated hydrogen atoms are free to diffuse to the Si/SiO_2 interface and break Si–H bonds at the interface creating dangling silicon bonds (interface traps) and molecular hydrogen. This model accounts for the slow buildup of interface traps. However, this model is inconsistent with the experimental observation that interface-trap buildup only occurs with a positive bias following irradiation. For a diffusion process, interface-trap buildup should occur for either a negative or positive bias. This inconsistency was resolved by Winokur and McLean, who also proposed a modified two-stage model. The first stage of Winokur and McLean's model is similar to the first stage of Svensson's model. With an applied bias (either positive or negative), radiation-generated holes in the oxide can transport by polaron hopping toward either the Si/SiO_2 or gate-SiO_2 interface. As they transport through the bulk of the oxide or become trapped, they can release sufficient energy (~5 eV) by localized excitation to break a strained Si–O bond or a weak H or OH bond with trivalent silicon. However, unlike the model of Svensson, the model of Winokur and McLean assumes that, instead of a neutral hydrogen atom being released, a charged ion is released as a bond is broken. The ion that is released is most likely a hydrogen ion [103,119-126]. In the second stage of buildup, with an applied positive bias, the ions can drift to the Si/SiO_2 interface. As ions reach the interface, they can rapidly break either Si–H or Si–OH bonds to form interface traps. In this model, the time dependence of buildup is governed by the time it takes for positive ions to drift to the Si/SiO_2 interface and buildup will occur only with a positive gate bias, consistent with experimental data. The magnitude of the buildup is governed by the number of ions released in the bulk of the oxide during the first stage of buildup.

Even though the Winokur and McLean model can explain the time dependence of interface-trap buildup, it is inconsistent with the experimentally observed electric field dependence for interface-trap buildup in polysilicon-gate and some metal-gate devices. In the Winokur and McLean model, ions are released as holes transport through the oxide by polaron hopping. As a hole transports through the bulk of the oxide, one expects [120] that an increase in electric field strength will increase the energy a hole imparts to the SiO_2 lattice, increasing the probability of releasing an ion and hence subsequently creating an interface trap. Thus, for the Winokur and McLean model, interface-trap buildup should increase with increasing electric field strength. Such a dependence was observed in early work on Al-gate capacitors [102,106]. However, as noted in Fig. 39 for polysilicon-gate transistors, interface-trap buildup *decreases* with approximately an $E^{-0.6}$ field dependence. A model which can account for this electric field

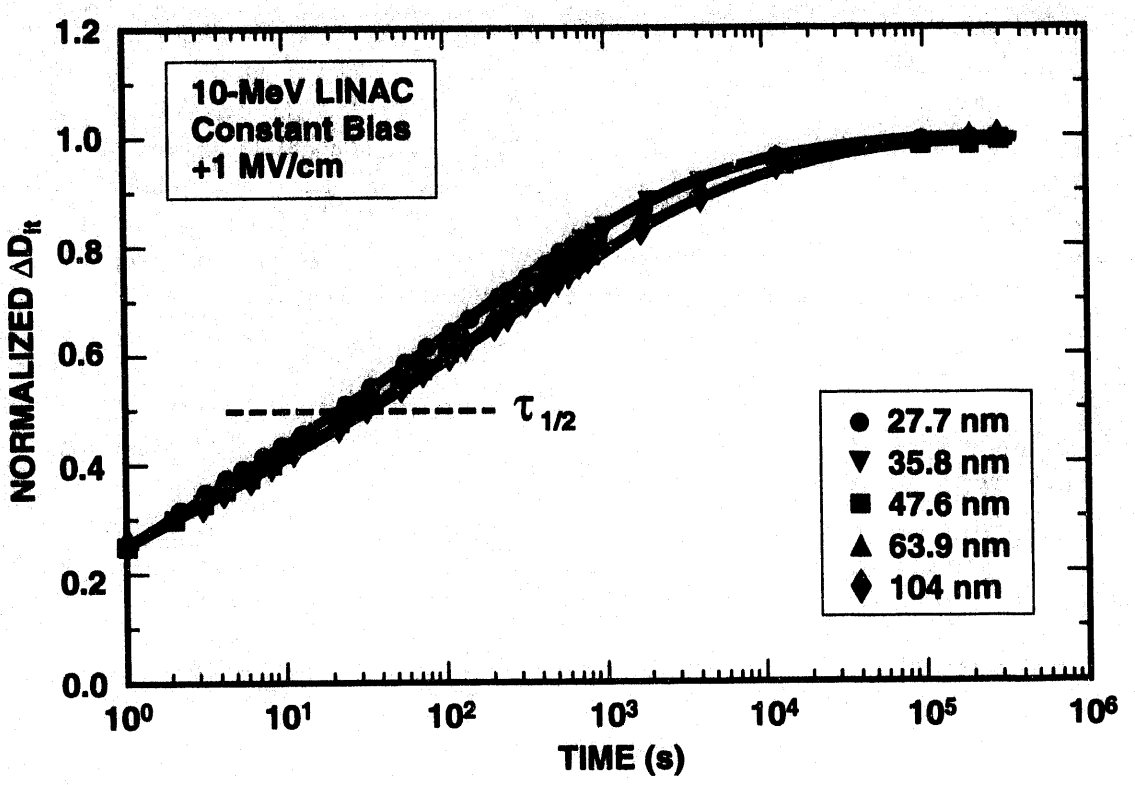


Figure 44: Interface-trap buildup after irradiation for dry-oxide polysilicon-gate transistors with gate-oxide thicknesses from 27.7 to 104 nm. (After Ref. 100)

dependence is the hole-trapping/hydrogen transport $(HT)^2$ model of Shaneyfelt, et al. [100]. According to the $(HT)^2$ model, for positive bias during irradiation, holes transport toward the Si/SiO_2 interface and become trapped near the interface. As the holes are trapped, near-interfacial hydrogen ions are released, which transport to the Si/SiO_2 interface, interact at the interface, and create interface traps. The rate-limiting step according to Shaneyfelt's model is the rate at which hydrogen ions drift to the interface. The electric field dependence according to this model will be governed predominantly by the capture cross-section for holes near the interface. This has been shown to follow approximately an $E^{-1/2}$ field dependence. Thus, Shaneyfelt's model correctly predicts the experimentally observed electric field dependence.

If interface-trap buildup results from hole trapping close to the Si/SiO_2 interface, there is no obvious reason for the rate of interface-trap buildup to depend significantly on gate oxide thickness [97,100,127]. Except for very thick oxides, hole transport is complete within milliseconds after irradiation. Thus, for moderately thick or thin oxides, hole transport is over before significant interface-trap buildup occurs. However, if interface-trap buildup results from the drift of hydrogen ions generated in the bulk of the oxide, the thicker the oxide, the longer it will take for hydrogen ions to drift to the Si/SiO_2 interface and the rate of interface-trap buildup should depend on gate oxide thickness. Figure 44 [100] is a plot of interface-trap buildup for gate oxides grown in dry oxygen (dry oxides) versus time after irradiation for transistors with gate oxide thicknesses from 27.7 to 104 nm. To first order, there is no dependence of the rate of interface-trap buildup on gate oxide thickness. Therefore, this data tends to support the $(HT)^2$

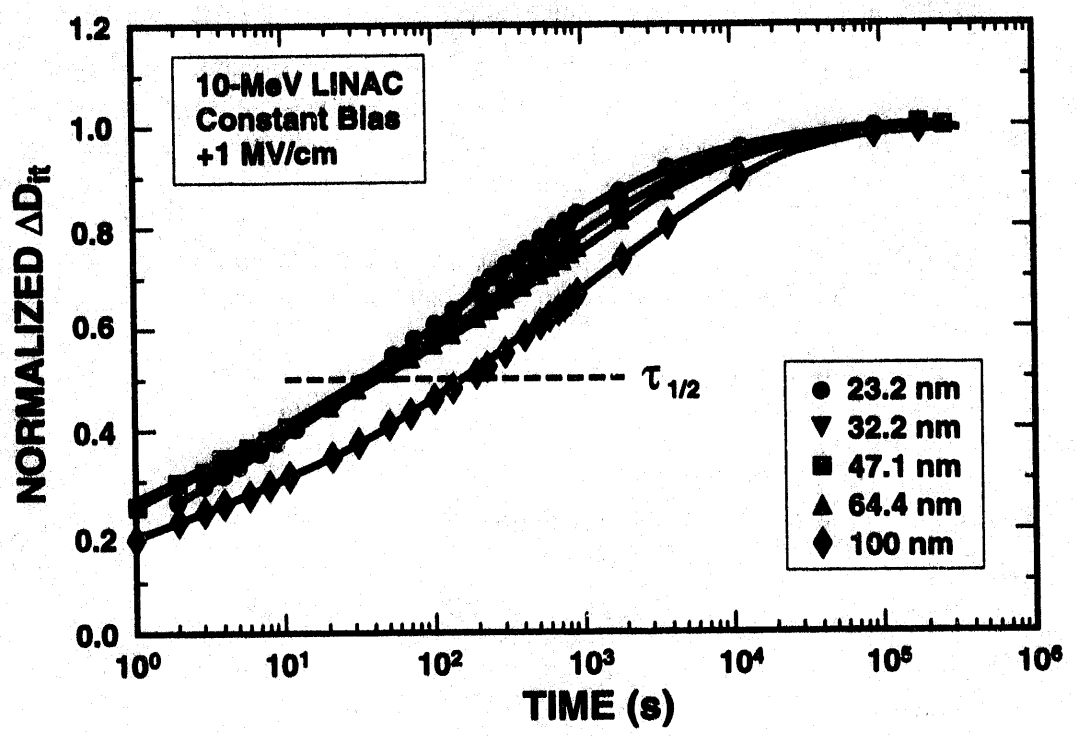


Figure 45: Interface-trap buildup after irradiation for wet-oxide polysilicon-gate transistors with gate-oxide thicknesses from 23.2 to 100 nm. (After Ref. 100)

model. In contrast, Fig. 45 [100] is a plot of interface-trap buildup for gate oxides grown by steam oxidation (wet oxides) versus time after irradiation for transistors with gate oxide thicknesses from 23.2 to 100 nm. For the wet oxide transistors, there is a large difference in the time dependence of buildup between the 100 nm oxides and the other oxides. At longer times, there is also a difference in the amount of buildup for all oxide thicknesses. The data for the wet oxide devices doesn't support either the $(HT)^2$ model or the model of Winokur and McLean. For these devices, it is possible that for the thicker oxide transistors, there is some interface-trap buildup from hole-trapping near the interface and some from drift of hydrogen ions from the bulk of the oxide. Additional work investigating the dependence of the rate of interface-trap buildup on oxide thickness has shown a stronger oxide-thickness dependence versus time for interface-trap buildup [97,127]. This work suggests that, in other types of devices, most of the hydrogen ions are released in the bulk of the oxide. Clearly, more work needs to be performed to clarify the role of hole trapping and transport in interface-trap buildup.

The ion that is released causing interface-trap buildup is almost certainly hydrogen. Hydrogen has long been known or suspected of being a key player in radiation-induced interface-trap buildup [119,125,128]. The amount of hydrogen used in the ambient gases of high temperature anneals during device fabrication has been shown to strongly affect the number of radiation-induced interface traps [126]. The physical reaction to produce an interface trap is likely [109,124,129]

$$H^+ + e^- + H - Si \equiv Si \rightarrow H_2 + \bullet Si \equiv Si\,, \tag{18}$$

where H–Si≡Si indicates a silicon atom bonded to one hydrogen atom back bonded to three silicon atoms, and •Si≡Si indicates a silicon atom with a dangling bond (interface trap) back bonded to three silicon atoms. This equation indicates that an interface trap is created as a hydrogen atom breaks a H–Si bond at the interface.

Note that, even though the details of the Winokur and McLean and the $(HT)^2$ models are different, the general concepts of the two models are very similar. Both of the models depend on the generation of holes in the oxide, hole transport, and the release of hydrogen in order for interface-trap buildup to occur. These two models are the two most convincing models for interface-trap buildup. Whether hydrogen is more often released in the bulk of the oxide, near the Si/SiO_2 interface, or a combination of the two remains to be seen.

In summary, the details of the mechanisms for interface-trap buildup still need to be resolved. However, several important observations can be made. First, interface-trap buildup depends on the generation of electron-hole pairs in the bulk of oxide. Interface-trap buildup is not caused directly by irradiation. Second, interface-trap buildup is linked in some manner to hole transport and/or trapping either in the bulk of the oxide or at traps near the Si/SiO_2 interface. Third, the release of hydrogen ions is apparently involved in most, if not all, interface-trap buildup.

4.5.6 Microscopic Defect Centers

The microscopic structure of the radiation-induced interface-trap defect center has been identified as a P_b defect [82-85,130,131]. A P_b center is a trivalent silicon defect site [132-134], similar to the E' center except that the P_b center is back bonded by three silicon atoms. The chemical notation for the P_b center is $\bullet Si{\equiv}Si_3$. It has a magnetic field zero crossing at 2.008 with the magnetic field perpendicular to the (111) axis and a magnetic field zero crossing at 2.0014 for the magnetic field parallel to the (111) axis. It was first identified in irradiated MOS capacitors on (111) silicon using electron spin resonance. Within a factor of two in experimental uncertainty, the absolute magnitude of the number of P_b centers was correlated to the number of interface-traps measured using capacitance-voltage measurements during irradiation and during post-irradiation anneals [82,130]. The distribution of P_b centers peaks at midgap and decreases toward either the conduction or valence band [82,130]. This distribution is consistent with the assumption that at midgap an interface-trap is paramagnetic and neutral [82]. In the upper part of the band gap, an interface trap is acceptor-like (can accept an electron), negatively charged, contains two electrons, and the P_b center diamagnetic. Recall that for an EPR signal to be observed it must be paramagnetic (contain an unpaired electron). In the lower part of the band gap, an interface trap is donor-like (can give up an electron), positively charged, contains no electrons, and diamagnetic. In the middle of the band gap the interface trap is neutral, contains one electron, and paramagnetic.

In (100) silicon, two distinct types of P_b centers have been identified preirradiation [135,136]. These centers are noted P_{b0} and P_{b1}. The g tensor for the P_{b0} center is similar to the g tensor for the P_b center, indicating that these two centers are structurally similar [135,136]. The

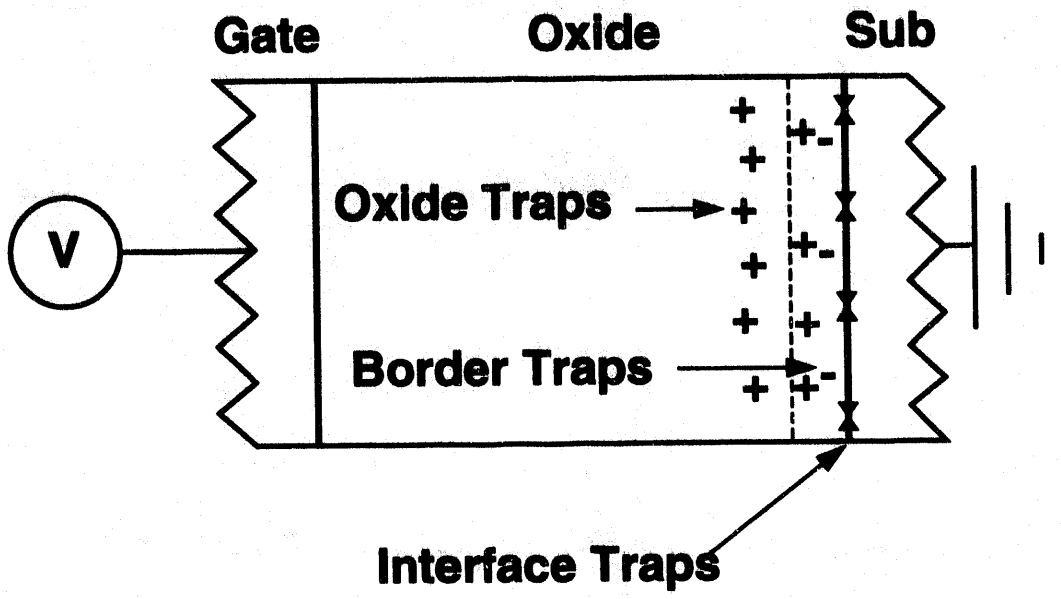


Figure 46: Illustration of the concept of border traps. Note that border traps are near-interfacial oxide traps. (After Ref. 110)

g-tensor for the P_{b1} center is unlike most all other centers in either silicon or silicon dioxide [135,136]. The nature of the P_{b1} center is presently unknown. Early work [135,136] suggested that it is a variant of the P_{b0} center. In respect to crystal symmetry, the P_{b1} center is consistent with $\bullet Si{\equiv}Si_2O$ centers [135,136]. However, theoretical calculations [137] and ^{17}O experiments [138] strongly indicate that this isn't the chemical identity. In fact, in these studies it appears as though the P_{b1} center is a closer analog to the P_b in (111) than the P_{b0}. More work needs to be performed to identify the chemical structure of the P_{b0} and P_{b1} centers. For irradiated oxides on (100) silicon, the dominant type of P_b center appears to be the P_{b0} center [31].

4.6 Border Traps

In the above discussion, we have identified two types of radiation-induced defects in MOS oxides, i.e., interface traps and oxide-trap charge. As we discussed in Section 4.4.2, oxide traps may be neutralized by electrons tunneling from the silicon into an oxide trap. This process can be reversed with the application of a negative bias. The time that it takes for an oxide trap to be neutralized depends on the distance the trap is from the Si/SiO_2 interface. Thus, traps close to the interface can transfer charge back and forth from the silicon relatively easily and traps far from the interface may not transfer charge at all. If a trap can exchange charge with the silicon on the time frame of an electrical measurement, it will act like an interface trap rather than an oxide trap. These types of traps are called border traps [110]. The location of border traps, oxide traps, and interface traps in a MOS device is illustrated in Fig. 46 [110]. They are near-interfacial traps in the oxide, but act electrically like an interface trap. For electron tunneling, the rate of tunneling from the silicon into an oxide charge is given by Eq. (13). As the distance from the interface increases, the time frame for tunneling increases exponentially. Thus, a border trap must be very close to the silicon/silicon dioxide interface. In one minute, tunneling electrons will passivate virtually all of the trapped charge in SiO_2 that lies within ~3 nm of either the Si/SiO_2 or

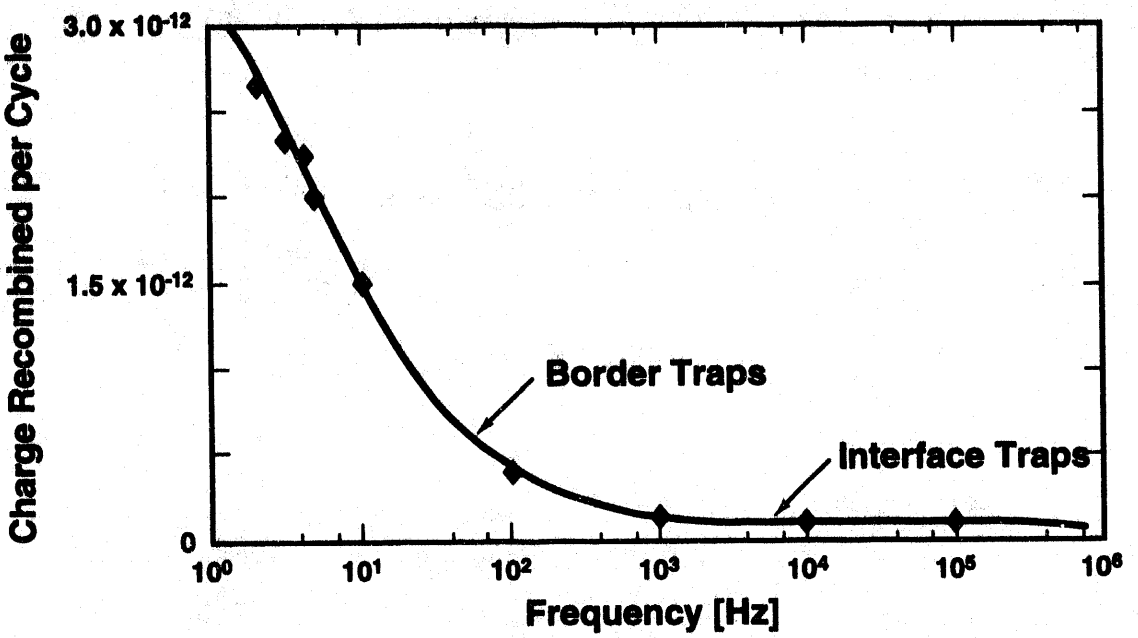


Figure 47: Amount of recombined charge versus measurement frequency. Increase in recombined charge is due to the filling and emptying of border traps. (After Ref. 142)

the gate SiO_2 interface [47,62,110,139]. For an order of magnitude more or less increase in tunneling time, this distance changes by only ±0.25 nm. Thus, near-interfacial traps less than ~3 nm of the interface are likely to be border traps in typical measurements, while traps more than 3 nm from the interface are likely to be oxide traps [110,140]. However, the exact "cutoff" line between oxide traps and border traps will depend on process and measurement conditions. Note that for both border traps and oxide traps the defect center may be the same (e.g., E'_γ center).

To estimate the number of border traps, a new analysis technique has recently been developed [141]. This analysis technique combines threshold-voltage and charge-pumping measurements on n- and p-channel transistors. In some cases, the number of border traps measured on irradiated MOS transistors exceed the number of radiation-induced interface traps. This indicates that the number of border traps can be quite significant in some devices.

The frequency of the measurement signal obviously plays an important role in determining whether a trap acts like a border trap or an oxide trap. For instance, I-V measurements which are routinely measured with sweep rates ~ 4 V/s (equivalent to ~1-4 Hz), may count an oxide trap as an interface trap if the oxide trap is within ~3 nm of the interface. On the other hand, charge-pumping measurements which are typically performed at higher frequencies (~1 MHz), may not measure traps as interface traps as far into the oxide as the I-V measurements. This is illustrated in Fig. 47 [142]. Figure 47 is a plot of charge captured and emitted from traps (from interface traps or border traps) during a charge pumping measurement as the charge pumping signal is swept from inversion to accumulation (recombined charge per cycle) versus measurement frequency for an MOS transistor irradiated to 1 Mrad. For

frequencies below ~1 kHz, there is a rapid increase in recombined charge as the frequency is lowered. At the lower frequencies, electrons can tunnel farther into the oxide filling and emptying a higher number of oxide traps. Thus, as the frequency is decreased, there will be an increasing number of border traps.

The concept of border traps has been useful in clarifying several phenomena that depend on "near-interfacial traps." For example, present evidence indicates that 1/*f* noise is caused almost entirely by near-interfacial oxide traps [110,140,143-148]. Depending on the measurement method, a near-interfacial oxide trap can be measured as either an oxide trap or an interface trap. Thus, although the same defect is involved, in some cases 1/*f* noise has been correlated with the number of oxide traps [144-147] and in other cases it has been correlated with the number of interface traps [143,147-150]. The latter case suggests that 1/*f* noise is associated with the number of P_b centers which is unlikely. 1/*f* noise most likely correlates to the number of border traps. Thus, by distinguishing between interface traps (P_b) and border traps one can explain the confusion in the literature on 1/*f* noise [110].

4.7 Device Properties

The total threshold-voltage shift for a transistor is the sum of the threshold-voltage shifts due to oxide-trap and interface-trap charge, i.e.,

$$\Delta V_{th} = \Delta V_{ot} + \Delta V_{it} \,. \tag{19}$$

ΔV_{ot} and ΔV_{it} can be determined from

$$\Delta V_{ot,it} = \frac{-1}{C_{ox} t_{ox}} \int_0^{t_{ox}} \rho(x) x dx \,, \tag{20}$$

where $\rho(x)$ is the charge distribution of radiation-induced charge. It includes contributions from both radiation-induced oxide-trap and interface-trap charge. Note the change in sign between the charge distribution and the threshold-voltage shift. For positive charge, the threshold-voltage shift is negative; conversely, for a negative charge, the threshold-voltage shift is positive. Thus, for devices where oxide-trap charge dominates, the threshold-voltage shift will be predominantly negative.

At high dose rates and short times, little neutralization of oxide-trap charge will occur and ΔV_{ot} can be large and negative. Conversely, interface-trap charge at high dose rates and short times will have had insufficient time to build up and ΔV_{it} is normally small. Thus, at high dose rates and short times for either n- or p-channel transistors the threshold-voltage shift can be large and negative. For an n-channel transistor, large negative threshold-voltage shifts will significantly increase the drain-to-source leakage current, which in will turn cause significant increases in IC static supply leakage current, I_{DD}, leading to potential IC failure.

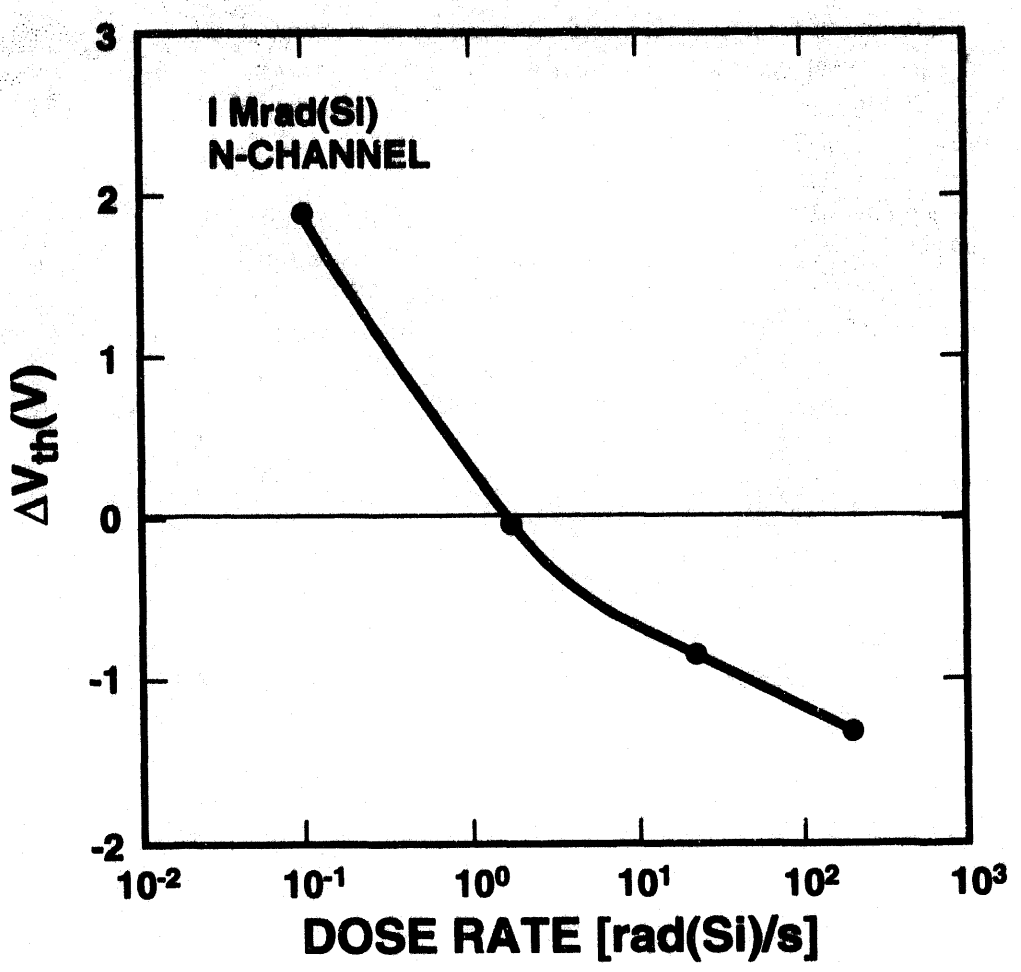


Figure 48: The change in threshold voltage versus dose rate. The data for this figure were taken from the data of Fig. 42.

At moderate dose rates, some neutralization of oxide-trap charge will take place and some buildup of interface traps will also occur. Thus, for this case, both ΔV_{ot} and ΔV_{it} can be large. For an n-channel transistor, ΔV_{ot} and ΔV_{it} tend to compensate each other. Therefore, at moderate dose rates, even though the individual components (ΔV_{ot} and ΔV_{it}) of the threshold-voltage shift can be large, the net threshold-voltage shift for an n-channel transistor can be small and the failure level of an IC may be relatively high.

For the long times associated with low-dose-rate irradiations, a large fraction of the oxide-trap charge in hardened transistors will be neutralized during irradiation. Thus, ΔV_{ot} is normally small. In contrast, the long times associated with low-dose-rate irradiations allow for interface-trap buildup to saturate. This results in a positive increase in threshold voltage in n-channel transistors and a decrease in carrier mobility which tend to reduce the current drive of a transistor and can lead to timing related failures for an IC. The dependence of threshold-voltage shift on dose rate is illustrated in Fig. 48. The data for this figure were taken from the data of Fig. 42. Note that at the highest dose rate (200 rad(Si)/s), the threshold-voltage shift is

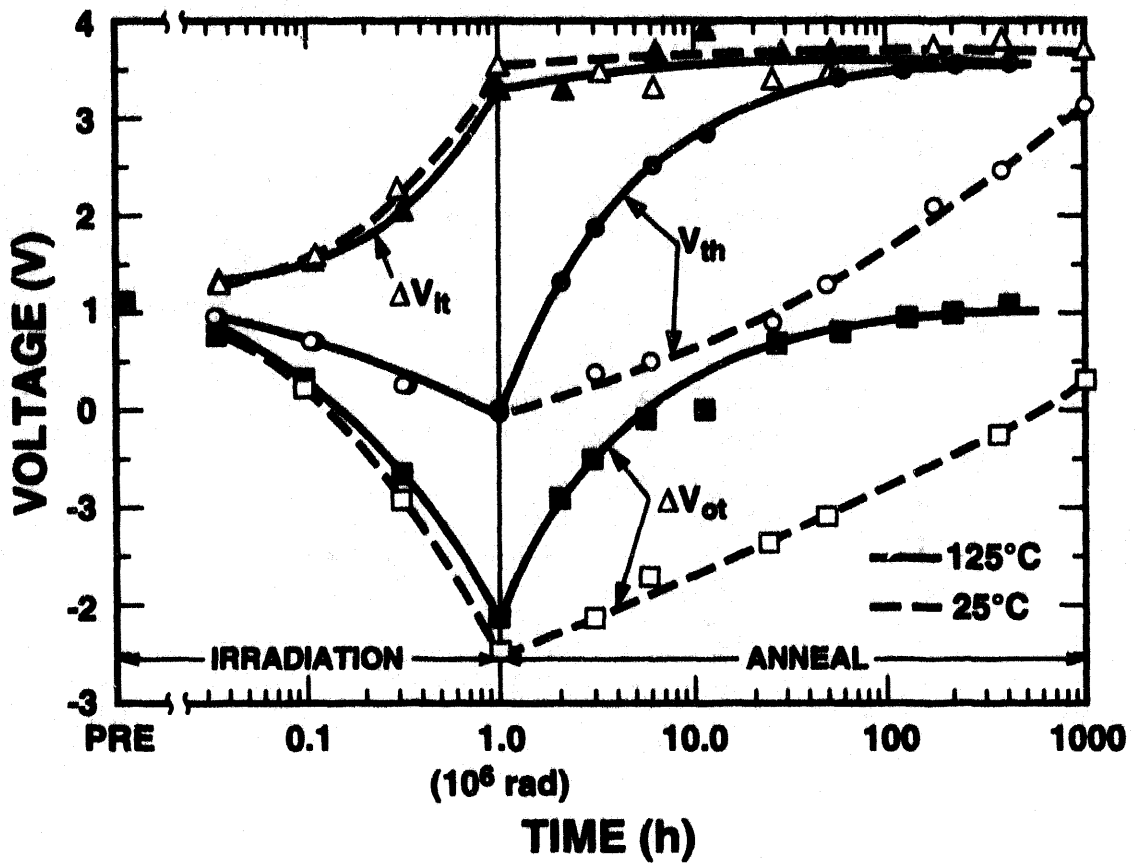


Figure 49: The variation in ΔV_{th}, ΔV_{ot}, and ΔV_{it} during room temperature irradiation and after a postirradiation biased anneal at temperatures of 25 and 125°C. This figure illustrates the concept of rebound. (After Ref. 67)

large and negative. At the lowest dose rate (0.1 rad(Si)/s), the threshold-voltage shift is large and positive. At a dose rate of 2 rad(Si)/s, the threshold-voltage shift is approximately zero.

For some commercial technologies, much less oxide-trap neutralization will occur even for the long times associated with space irradiations [66]. For these devices, the device response may be dominated by oxide-trap charge buildup similar to that for the short time response of hardened transistors after a pulse of radiation. Thus, for some commercial technologies, the cause of IC failure in a space environment may be dominated by large negative threshold-voltage shifts of n-channel transistors, leading to large increases in static supply leakage current of an IC. For other commercial technologies and most hardened technologies the cause of IC failure in a space environment may be dominated by large positive threshold-voltage shifts. (Note that, for a few hardened technologies, the rate of oxide-trap charge neutralization can be low and IC failure at low dose rates also can be dominated by increases in IC leakage [151].)

One consequence of the time dependence of oxide-trap charge neutralization and interface-trap charge buildup is "rebound" [67,152,153]. Figure 49 [67] is a plot of threshold voltage versus irradiation and anneal for n-channel transistors irradiated at room temperature and annealed at either room temperature or at 125°C. An elevated temperature biased anneal

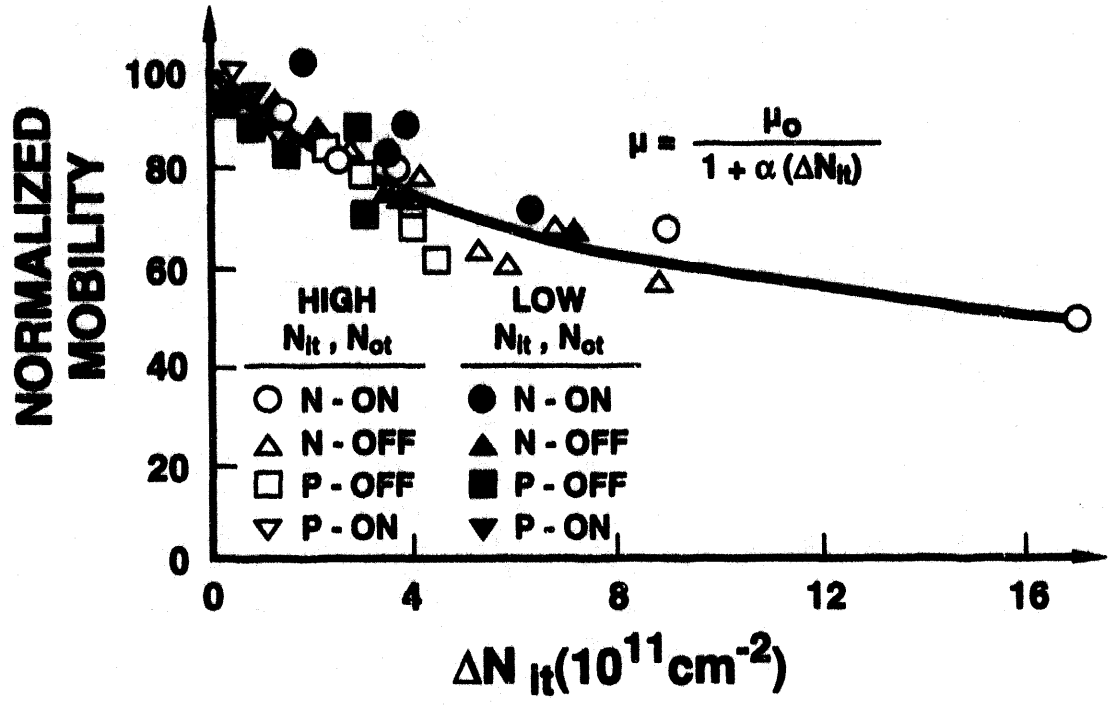


Figure 50: The change in carrier mobility versus interface-trap charge buildup. (After Ref. 154)

performed after irradiation is often referred to as a rebound test. A typical temperature for a rebound test is 100°C. The bias during irradiation and both anneals was 10 V. The total threshold voltage is divided into its components due to oxide-trap and interface-trap charge. Note that for this plot ΔV_{ot} and ΔV_{it} are referenced to the initial threshold voltage value (~1 V). During irradiation, there is a large buildup of oxide-trap charge and interface-trap charge. For these devices and radiation conditions, the buildup of oxide-trap charge is larger than the buildup of interface-trap charge leading to a negative threshold-voltage shift. This is common for many technologies for a laboratory irradiation at a moderate dose rate. During either the room temperature or the 125°C anneal, oxide-trap charge is neutralized. During the same time period there is little change in interface-trap charge (a slight increase). The net result is that after either anneal the threshold voltage is large and positive. The threshold voltage has thus "rebounded" from a value lower than its preirradiation value right after irradiation to a value greater than its preirradiation value after anneal. In effect, the rebound test has simulated a space environment by neutralizing a large fraction of the oxide-trap charge, without annealing interface-trap charge.

An increase in the number of interface traps will reduce carrier mobility. The degradation of mobility with interface-trap buildup is illustrated in Fig. 50 [154] where the effective channel mobility normalized to its preirradiation value is plotted versus the number of interface traps for devices fabricated using several different process conditions. High and low N_{it} and N_{ot} refer to devices that were intentionally processed to result in high or low concentrations of radiation-induced interface-trap and oxide-trap charge. The degradation in mobility with interface-trap charge follows the general relationship [154],

$$\mu = \frac{\mu_0}{1+\alpha \cdot \Delta N_{it}}, \tag{21}$$

where μ_0 is the preirradiation mobility and α is a constant. This equation is often referred to as the Sun-Plummer relation [155], which was derived for the change in mobility due to preirradiation fixed oxide charge. This relationship has been used to determine ΔV_{it} from mobility [36,37] and combined threshold and mobility measurements [38,39]. Equation 21 has been found to be valid under most conditions, except for short times (<0.1 s) after a pulse of irradiation [156]. At early times after irradiation (~0.01 s), there can be a significant concentration of oxide-trap charge close to the Si/SiO_2 interface which can affect, and in some cases dominate, the degradation in mobility. However, as the electron tunneling front moves into the oxide, neutralizing oxide charge close to the interface, the importance of charged hole traps on mobility becomes increasingly less [156]. Recent work by Zupac, et al. [157], has also suggested that for some technologies Eq. 21 must be modified to include oxide-trap charge scattering even for long times after irradiation.

4.8 Application of the Knowledge of Basic Mechanisms — Case Studies

The time and effort that has been spent in investigating the mechanisms of radiation effects cannot be justified if the only benefit was to the academic community. To justify the costs, one must be able to apply the understanding of radiation effects towards improved technological capabilities for system applications. In practice, the knowledge of the basic mechanisms of radiation effects has enabled the scientist and engineer to make significant advances in technology development and hardness assurance testing. In this section, three examples are presented of where the knowledge of the basic mechanisms of radiation effects has been used to advance capabilities.

4.8.1 Process Hardening

Historically, to develop a hardened technology, process steps were usually chosen on the basis of those that minimized the radiation-induced threshold-voltage shift of n-channel transistors using a moderate dose-rate laboratory radiation source (e.g., Co-60). This criterion was chosen in order to prevent n-channel transistors from going into depletion mode and, thus, to minimize the radiation-induced increase in static supply leakage current of an IC. As we discussed above, for an n-channel transistor irradiated at moderate laboratory dose rates, oxide-trap charge and interface-trap charge tend to compensate each other. This can lead to small threshold-voltage shifts, even though the individual components of oxide- and interface-trap charge are large. At very low dose rates, hardened transistor response is often governed primarily by interface-trap charge, while at very high dose rates, transistor response is governed primarily by oxide-trap charge. Thus, minimization of the n-threshold voltage at laboratory dose rates does not necessarily guarantee maximal performance in either a low-dose-rate (e.g., satellite) or high-dose-rate (e.g., weapon) application. In fact, as shown below, in some cases those process steps that minimize the radiation-induced threshold-voltage shift for laboratory irradiation at one particular dose rate may lead to degraded response in a satellite or weapon environment.

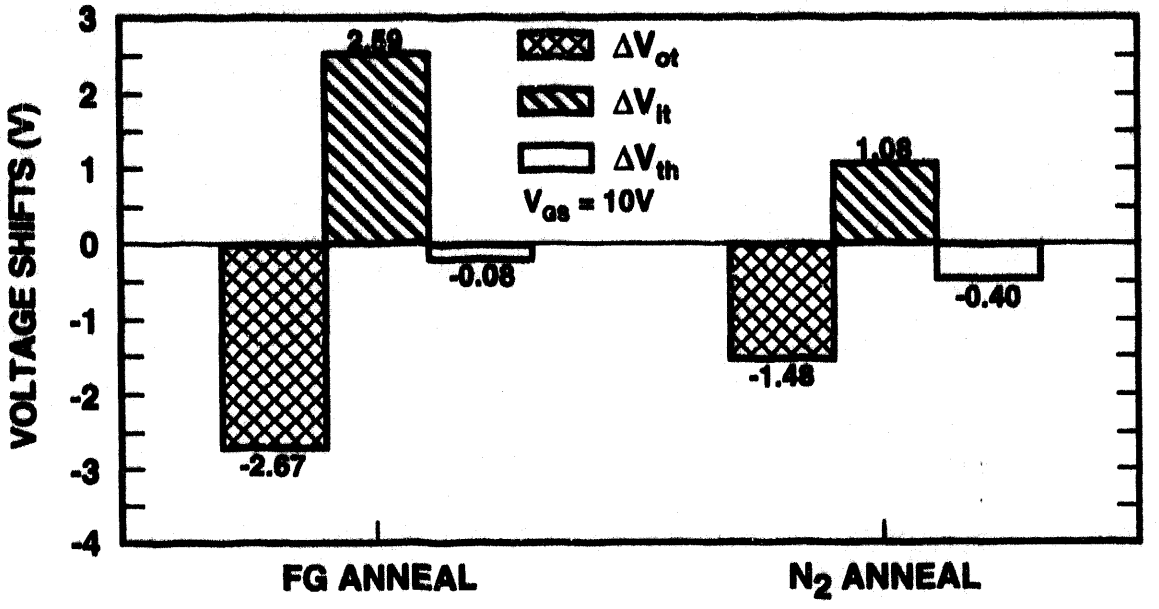


Figure 51: The variation in ΔV_{th}, ΔV_{ot}, and ΔV_{it} for devices fabricated with an intermediate oxide annealed in forming gas (90% nitrogen, 10% hydrogen) or in pure nitrogen. (After Ref. 106)

Based on our knowledge of radiation effects, we can hypothesize that it would be better to identify and use process steps that minimize individually either (or both) interface-trap charge or oxide-trap charge. Note that, by separately minimizing the individual components of radiation-induced charge, the threshold-voltage shift for a laboratory Co-60 irradiation may be larger, but the threshold-voltage shift for either a satellite or weapon exposure will be smaller. This is illustrated in Fig. 51 where the total threshold-voltage shift and the threshold-voltage shifts due to interface-trap and oxide-trap charge measured on capacitors are shown for anneals of a deposited oxide in different ambient gases [106]. The deposited oxide was used as an intermediate oxide between polysilicon and metal in a hardened technology. The anneals were all at a temperature of 900°C. The original process step included a forming gas anneal (10% hydrogen, 90% nitrogen) of the deposited oxide. This step was chosen to minimize the threshold-voltage shift as shown in Fig. 51 where ΔV_{th} was only -0.08 V after irradiating to 1 Mrad(Si). However, as noted above, incorporating hydrogen in the ambient gases of anneals after polysilicon deposition increases the amount of interface-trap charge [126]. To minimize interface-trap charge, an anneal without hydrogen in pure nitrogen was evaluated. As shown in Fig. 51, the pure nitrogen anneal lead to a decrease in oxide-trap charge and a larger decrease in interface-trap charge. As a result, the total threshold-voltage shift was larger for the capacitors annealed in nitrogen than for the capacitors annealed in forming gas. Based on the old method of determining process procedures, the nitrogen anneal would have been discarded because it resulted in a larger, negative threshold-voltage shift. However, because it reduced the amount of interface-trap charge (important for space applications) and oxide-trap charge (important for both space and weapon applications), this process step was adopted in developing an improved hardened technology. Note that, in order to minimize the threshold-voltage shift, the old process

step incorporating hydrogen actually caused more degradation in device response in a satellite or weapon environment.

4.8.2 Development of Reliable Hardness Assurance Test Guidelines

Radiation test guidelines have been written with the intent to ensure device functionality in either a tactical or space environment. One such guideline in the U. S. is MIL-STD 883, Method 1019. The latest version of this test guideline is MIL-STD 883D, Method 1019.4 [151,158,159]. Earlier versions of this test guideline were written based on the often erroneous assumption that, if a device was irradiated at low dose rates, significant annealing of the radiation damage would occur during irradiation exposure leading to less degradation than for moderate-dose-rate laboratory irradiations. Thus, it was assumed for a satellite environment, a simple test to the dose level of the system application would be sufficient to guarantee system performance requirements. As we noted above, this assumption is only true if oxide-trap charge dominates space response. Significant neutralization of oxide-trap charge can occur for a low-dose-rate irradiation. However, interface-trap charge is at a maximum for low-dose-rate irradiations. Thus, for low-dose-rate irradiations, oxide-trap charge provides less compensation of interface-trap charge, leading to larger positive threshold-voltage shifts for an n-channel transistor. The magnitude of the threshold-voltage shift may be larger for a low-dose-rate irradiation than for a moderate-dose-rate irradiation. Note that, for a moderate-dose-rate laboratory irradiation, the threshold-voltage shift of an n-channel transistor is often negative leading to increases in leakage current of an IC. For a low-dose-rate irradiation, the increase in threshold voltage and decrease in carrier mobility lead to degradation in timing parameters of an IC. Not only are the threshold-voltage shifts different, the potential failure mechanisms may be also different [112]. *If the failure mechanisms of a device using a laboratory radiation source and in the intended environment are different, one cannot directly simulate the intended environment using a laboratory source.*

Knowledge of the basic mechanisms of radiation effects led to an improvement in the test method which was incorporated into Method 1019.4 [151,158,160]. The improvement consisted of a two-part test to ensure that a device will function within acceptable, bounded limits during its lifetime. The first part of the test is a laboratory irradiation at a dose rate between 50 to 300 rad(Si)/s to the specification requirement. As long as the laboratory dose rate is greater than the expected space dose rate, this test will ensure that the threshold-voltage shift of gate- or field-oxide transistors will be more negative for the laboratory irradiation than in space. Thus, this part of the test bounds the contribution of oxide-trap charge. The second part of the test is a 100°C, 1-week "rebound" test following an additional irradiation to 50% of the specification requirement. As long as the rebound anneal does not anneal interface-trap charge, this test will ensure that the threshold-voltage shift will be more positive than in space, and, thus, provide an effective way to test for interface-trap related failures.

4.8.3 Process Control

To reduce costs and the time associated with device qualification, the U. S. Government is pursuing the Qualified Manufacturer's List (QML) methodology to qualify integrated circuits

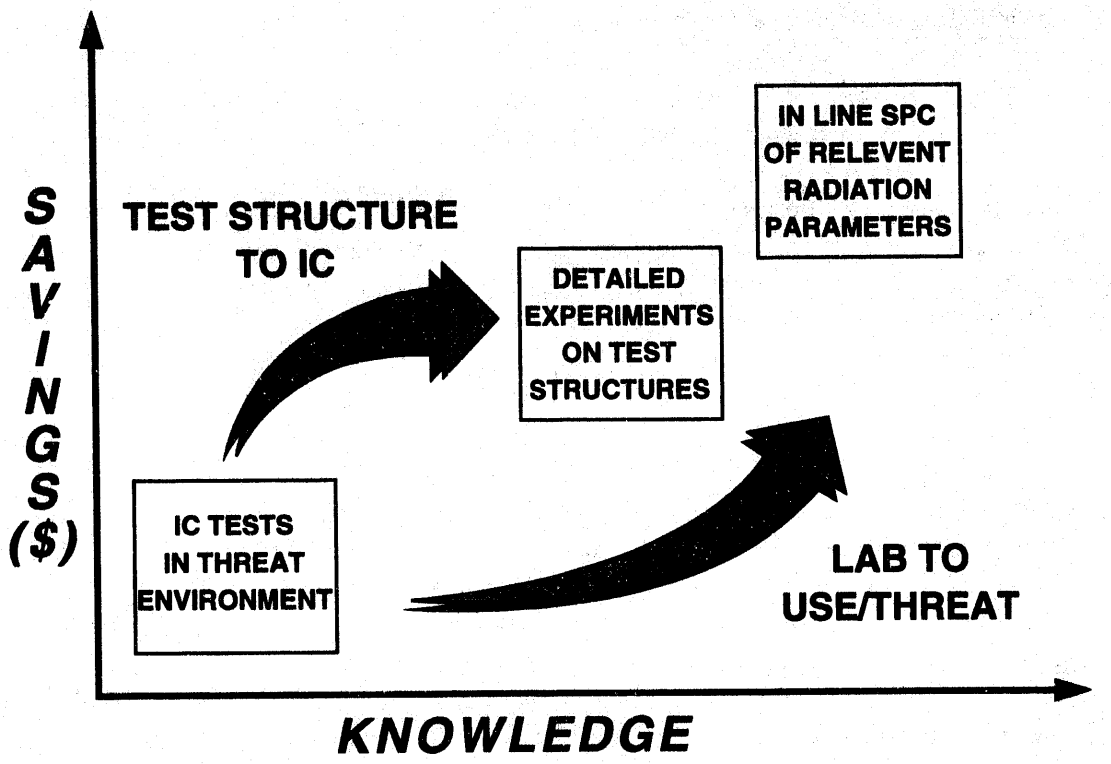


Figure 52: Illustration of increased cost savings that can be obtained in device qualification by increasing our knowledge base. (After Ref. 161)

for high reliability and radiation hardness. There are three phases to QML implementation: certification, qualification, and quality assurance [161]. During certification a manufacturer's process is "baselined" and the radiation hardness assurance capability level for the technology is demonstrated. During quality assurance the radiation hardness of individual wafer lots is verified.

As our knowledge base increases, higher levels of QML methodology can be employed, resulting in increased cost savings as illustrated in Fig. 52 [161]. The highest level of QML implementation involves in-line statistical process control (SPC) of relevant radiation parameters and test structures for certification and quality assurance. Key to defining relevant radiation parameters is a thorough understanding of mechanisms of radiation response and improved physical models, statistical models, circuit simulators, etc. At present, our knowledge base is not sufficient to fully implement in-line SPC QML methodology. However, as our knowledge base increases, we will eventually be able to qualify integrated circuits for radiation hardness using in-line process controls. This will result in considerable cost savings in qualification testing.

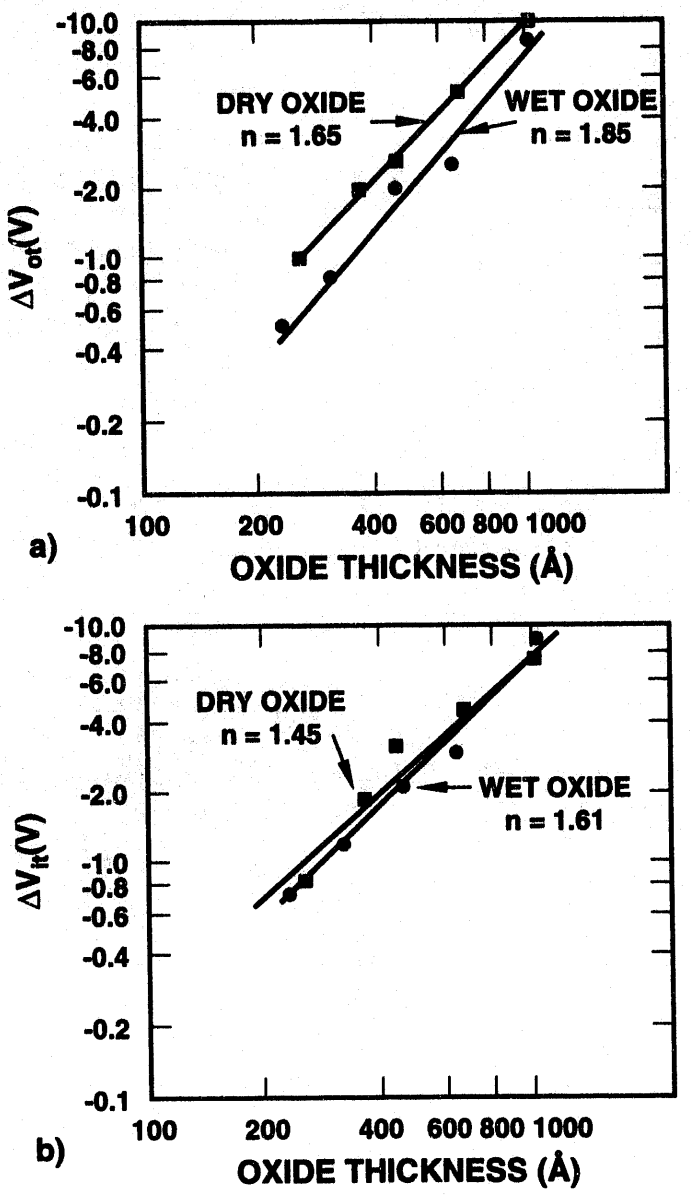


Figure 53: The dependence of the threshold-voltage shift due to oxide-trap and interface-trap charge on oxide thickness.

4.9 Special Concerns for Commercial Devices

4.9.1 Ultra-Thin Oxides

The general trend in commercial MOS devices is towards ultra-thin oxides. As the oxide thickness decreases, the amount of interface-trap and oxide-trap charge decreases with slightly less than a t_{ox}^2 thickness dependence [162,163]. This is illustrated in Fig. 53 where ΔV_{it} and ΔV_{ot} are plotted versus gate oxide thickness for dry and wet gate oxide transistors. The thickness dependence varies from ~ $t_{ox}^{-1.5}$ to $t_{ox}^{-1.8}$. For very thin oxides (<20 nm), there is evidence that the amount of radiation-induced oxide-trap charge decreases with even a faster dependence on

oxide thickness [164]. Thus, the total-dose hardness of commercial gate oxides should improve as the gate oxide thickness is decreased.

However, the basic mechanisms of radiation effects for ultra-thin oxides is different than that for moderately-thick gate oxides. For ultra-thin oxides, oxide-trap charge can be neutralized by electrons tunneling from either the gate or the Si/SiO_2 interface. As presented in Section 4.4.2, the distance of the tunneling front into the oxide is given by Eq. (14). A tunneling front can be described for each interface. If the distances the tunneling fronts extend into the oxide are defined as x_{mg} and x_{msi} for the gate and silicon interfaces, respectively, then the total depth of oxide charge that is neutralized is given by $x_{mg} + x_{msi}$. If the sum of the two fronts is equal to the gate oxide thickness, *all* oxide traps in the oxide will be neutralized. The rapid loss of trapped holes in the oxide for very thin oxides (<20 nm) is caused by tunneling of electrons from the gate or silicon interface [164].

Because a relatively higher number of the oxide traps will be accessible to electron tunneling, there will also be a relatively higher number of oxide traps that can act as border traps [110]. Recall that border traps are traps in the oxide that can communicate with the silicon on the time frames of an electrical measurement. In fact, for very thin oxides (<6 nm), there may be no "bulk-like" traps, and all traps in the oxide have the potential to function as border traps. Thus, for ultra-thin oxides, it is possible that to have no net positive radiation-induced oxide-trap charge, and all traps may function electrically like interface traps (either true interface traps or border traps).

4.9.2 Field Oxides

Even though the radiation hardness of commercial gate oxides may improve as the IC industry tends towards ultra-thin oxides, field oxides of advanced commercial technologies may still be very soft to ionizing irradiation. A relatively small dose in a field oxide [~10 krad(Si) for many commercial devices] can induce sufficient charge to cause field-oxide induced IC failure.

Field oxides are much thicker than gate oxides. Typical field-oxide thicknesses are in the range of 200 nm to 1000 nm [47]. Unlike gate oxides, which are routinely grown by thermal oxidation, field oxides are produced using a wide variety of deposition techniques. Thus, the trapping properties of a field oxide may be poorly controlled and can be considerably different than for a gate oxide.

Even for thermally grown thick oxides, the buildup of charge in gate and field oxides can be qualitatively different [165,166]. In thick SiO_2 capacitors (>100 nm), interface-trap buildup has been observed within 4 ms following a pulse of ionizing irradiation [165]. The buildup was found to be independent of oxide field and polarity and occurred with approximately the same efficiency at room temperature and 77 K. This suggests that some "prompt" interface traps could have been created directly by irradiation. On similar devices, a significant amount of hole trapping was observed in the bulk of the oxide [166].

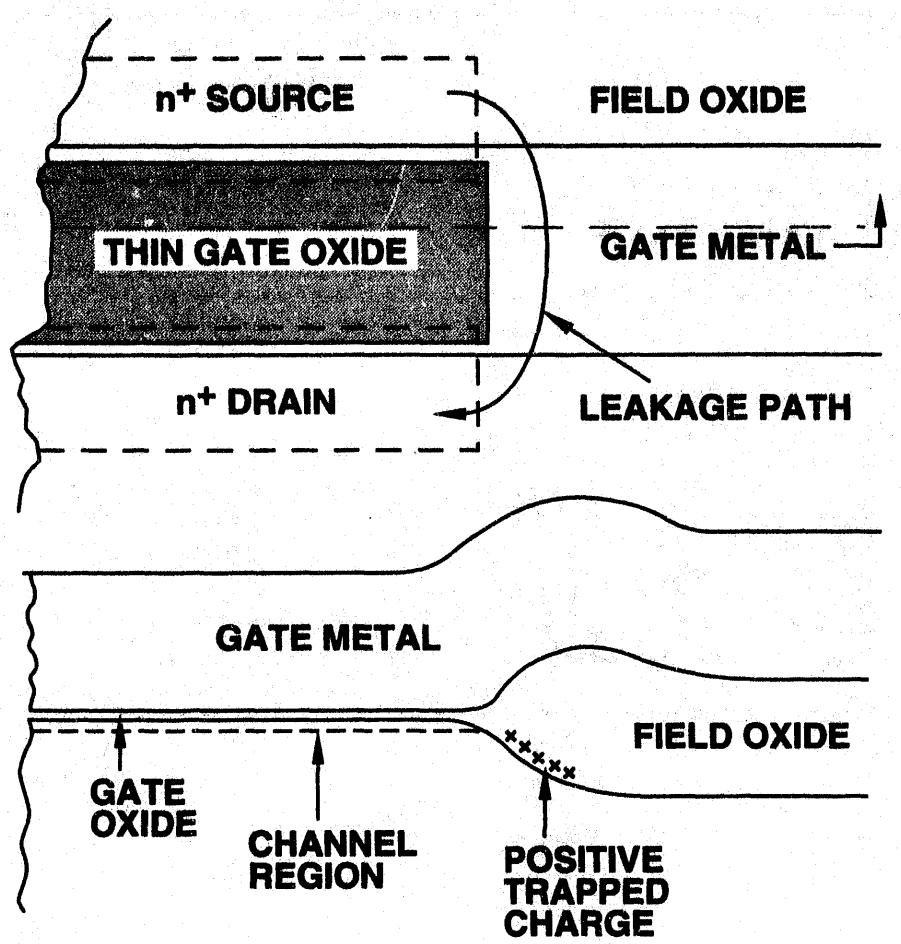


Figure 54: Cross-section of a parasitic field oxide transistor showing the primary leakage current paths. (After Ref. 167)

A cross-section of a typical commercial field oxide is shown in Fig. 54 [167]. The threshold voltages of parasitic field oxide transistors are initially very large. As radiation-induced oxide charge builds up in a field oxide, it causes the threshold voltage of the field oxide to tend to go toward depletion mode for field oxides over a p substrate (equivalent to an n-channel field oxide transistor). If the buildup of charge is large enough, excessive leakage current can flow from the source to drain of the gate-oxide transistors and between transistors. The excess leakage current is illustrated in Fig. 55 [167]. Plotted in Fig. 55 are the drain-to-source leakage current versus gate-to source voltage curves for an n-channel gate-oxide transistor with (combined curve) and without field-oxide leakage and for a parasitic field-oxide transistor. The field-oxide leakage significantly adds to the drain-to-source current at zero gate voltage. Thus, the field-oxide leakage prevents the transistor from being completely turned off. This will greatly add to the static supply leakage current of an IC. Field oxide leakage current limits the radiation hardness of most commercial integrated circuits and it is a major problem for advanced hardened technologies, both at high and low dose rates. Details of commercial field-oxide fabrication and its affect on IC performance are given in part three of this Short Course.

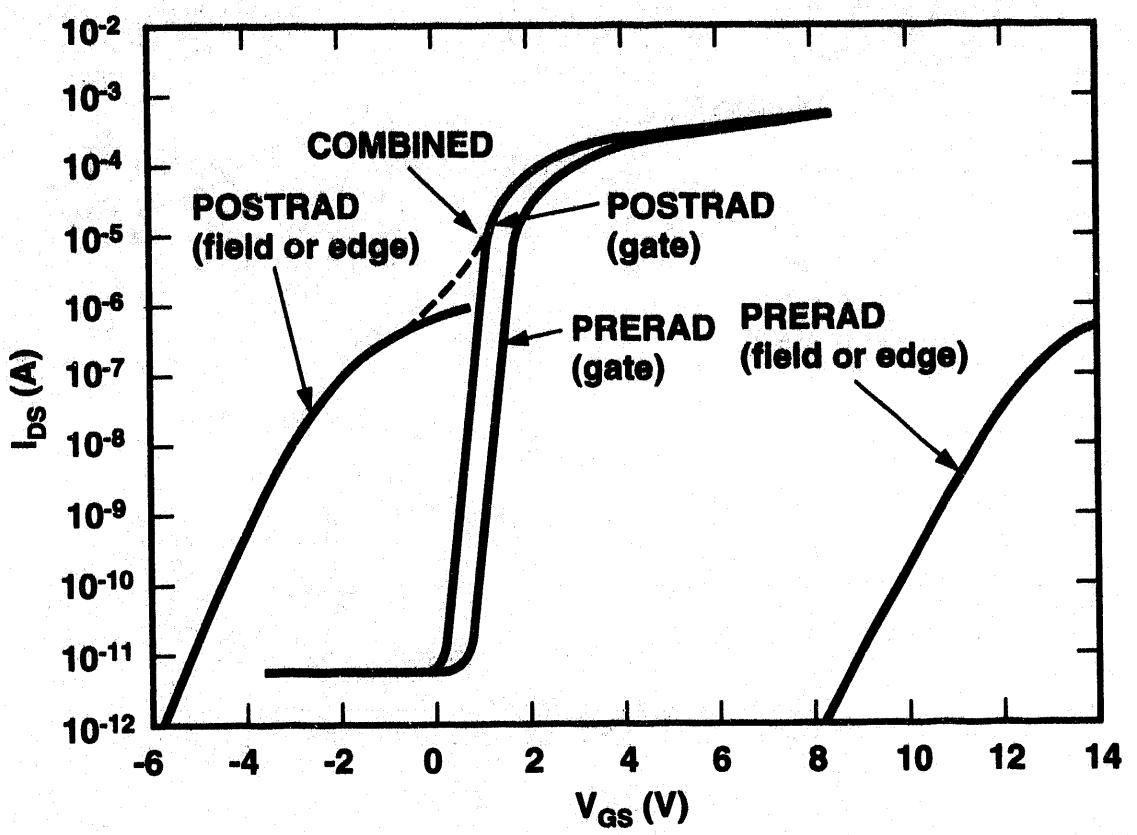


Figure 55: I-V curves for a gate-oxide transistor and a parasitic field-oxide transistor showing the increase in leakage current of the gate oxide-transistor caused by the parasitic field-oxide transistor. (After Ref. 167)

4.9.3 Process-Induced Defects

To fabricate commercial (and hardened) integrated circuits, it is sometimes necessary to use fabrication techniques that can lead to radiation-induced interface traps and oxide charge. This is especially true for advanced technologies that require special tools for defining small geometries, including electron, ion, and x-ray sources used to replace optical lithography; ion and plasma sources used for etching; and plasma and e-beam sources used for material deposition. The total dose that a device may be exposed to during fabrication can easily exceed that during device operation in the natural space environment. For example, the total dose that a device may be exposed to during a single resist patterning step using e-beam or x-ray techniques can well exceed 10 Mrad(Si) [168]. Fortunately, most damage created by these sources is annealed out during the normal course of the process flow in high-temperature anneals and oxidations following the process exposure. Most of the damage caused by electron, x-ray, and ion irradiation can be annealed out by a moderate temperature metal sinter (~450°C) step, as long as a large number of new vacancies are not created in the oxide [169]. However, in some cases higher temperature anneals are required to prevent increased radiation-induced degradation [168]. Details of process-induced defects are discussed in part three of this Short Course.

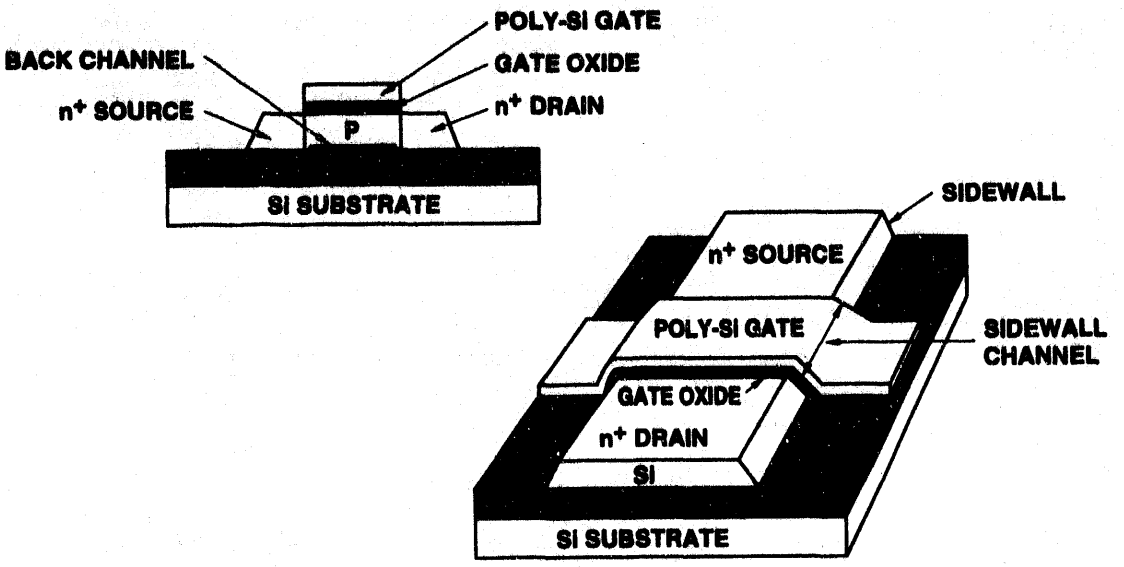


Figure 56: Cross-sections of a silicon-on-insulator transistor (SOI). (After Ref. 162)

5.0 TOTAL-DOSE EFFECTS — OTHER DEVICE TYPES

5.1 SOI Devices

Silicon-on-insulator (SOI) devices are an attractive alternative to bulk CMOS devices for space applications. A cross-section of a SOI transistor is illustrated in Fig. 56 [162]. As shown in the figure, the active silicon channel region is an "island" built on top of an insulating (buried oxide) layer instead of a silicon substrate. Two common fabrication methods are separation by implanted oxygen (SIMOX) and bonded and etch back SOI (BESOI). SIMOX substrates are prepared by implanting oxygen into a silicon substrate at very high energies and to very high implant levels. After implantation, the substrate must be annealed at very high temperatures. BESOI substrates are prepared by growing thermal oxides on two silicon wafers, bonding the wafers together at moderate temperatures (~900°C), and etching down one of the surfaces to obtain the active channel. Because SOI/MOS transistors are fabricated on an insulating layer, the amount of p-n junction area is greatly reduced. The reduced junction area leads to lower parasitic capacitance for faster operation, and to a reduction in the generation volume leading to a considerable reduction in the sensitivity of SOI ICs to single-event upset and other transient effects. The absence of a conducting path underneath the MOS transistor completely eliminates parasitic pnpn paths that can cause latchup. However, the fabrication conditions of a SOI transistor add to the complexity of the total-dose response of SOI devices. In this section, the mechanisms for total-dose ionizing radiation effects in SOI transistors are presented.

The total-dose hardness of an SOI transistor depends primarily on the radiation hardness of three oxides: 1) gate, 2) sidewall, and 3) buried oxide. The mechanisms for the radiation-induced degradation of the gate oxide of a MOS/SOI transistor are identical to the mechanisms for the gate oxide of a MOS transistor fabricated on a bulk silicon substrate discussed above. The sidewall and back-channel (associated with the buried oxide) leakage paths are illustrated in Fig. 56. The sidewall oxide exists as the gate oxide extends over the edges of the silicon island

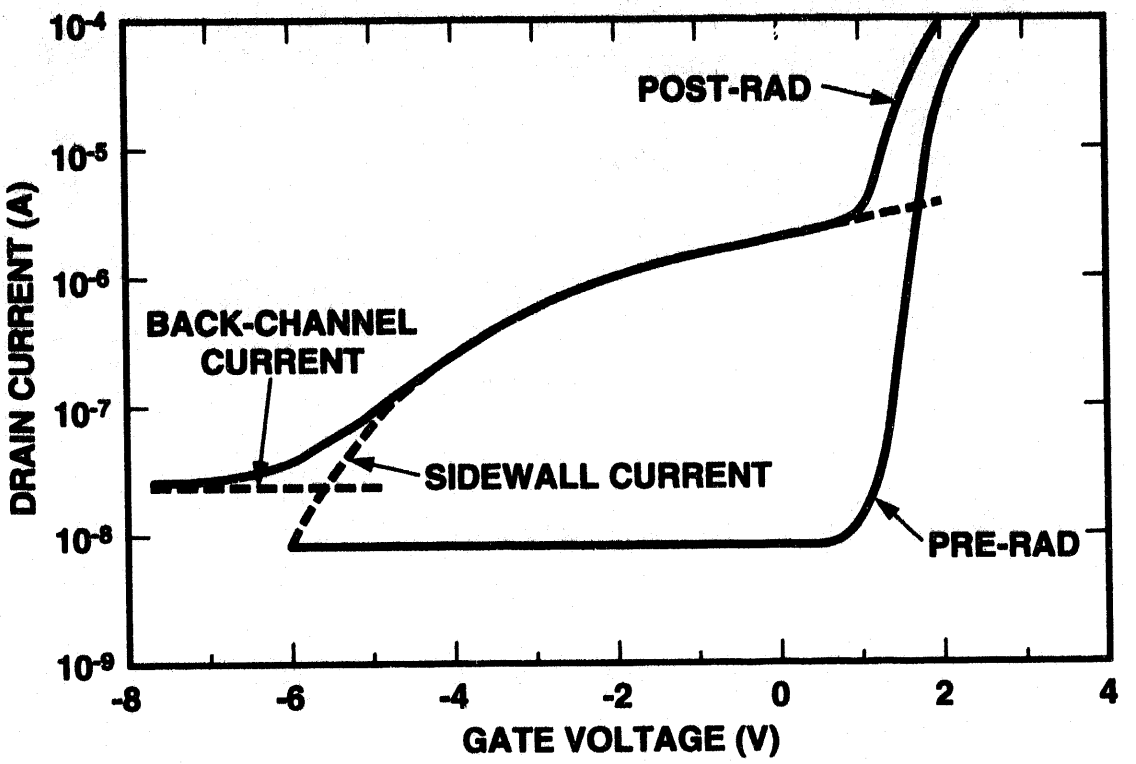


Figure 57: I-V curves for a gate oxide transistor on a silicon-on-sapphire substrate. Illustrated are the contributions of back-channel and sidewall leakage to the leakage current. (After Ref. 170)

and forms a parasitic transistor in parallel with the top transistor. In some cases, the sidewall oxide is less radiation tolerant than the top oxide and can greatly increase the top oxide transistor leakage current. The sidewall oxide induced leakage forms a shoulder in the MOS transistor I-V curve as illustrated in Fig. 57 [170]. (Figure 57 was actually taken from an MOS transistor fabricated on a silicon-on-sapphire (SOS) substrate. However, an MOS transistor fabricated in a SOI substrate has the same qualitative nature for sidewall and back-channel leakage current.) Note that the leakage current caused by a parasitic sidewall transistor is similar to that caused by a parasitic field-oxide transistor for a bulk silicon MOS transistor. The sidewall leakage can be eliminated by proper processing of the sidewalls [170-173]. For example, heavily doping the sidewall by selective implantation can be used to increase the threshold voltage of the parasitic sidewall transistor, reducing its importance to the radiation response [170,171].

Ionizing radiation induces the buildup of positive charge near the silicon/buried oxide interface and interface traps at the interface. The radiation-induced charge can invert the bottom surface of the silicon channel forming a conducting channel (back channel) between the source and the drain of the transistor. If the channel is not fully depleted, the gate bias of the MOS transistor has only a weak effect on the back-channel leakage current. Thus, for non-fully depleted channels, the buried oxide causes a fixed increase in leakage current which is relatively independent of gate bias as illustrated in Fig. 57.

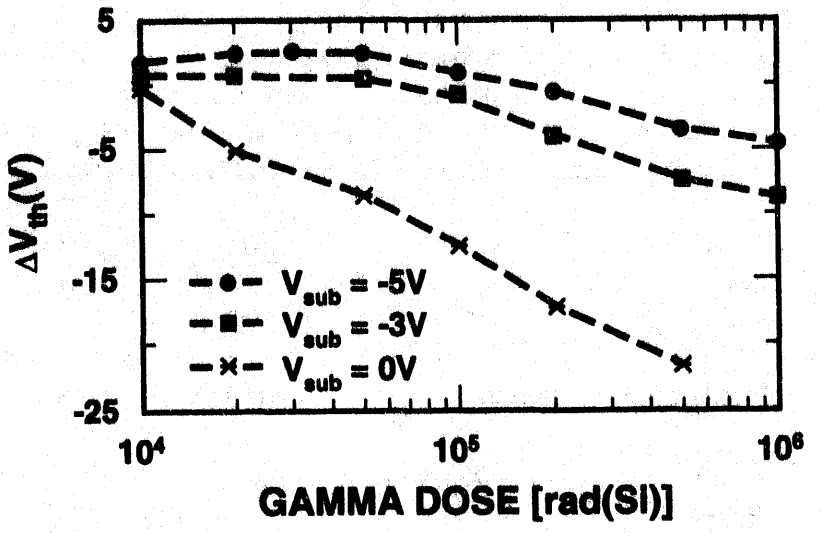


Figure 58: Back-channel transistor threshold-voltage shift versus dose for varying substrate biases. (After Ref. 174)

However, the bias on the bottom substrate can strongly affect the radiation response. By applying a negative bias to the bottom substrate, holes generated in oxide during irradiation will preferentially drift toward the back electrode, reducing the charge accumulated at the surface of the silicon channel/buried oxide interface, thus, reducing the back-channel leakage current. This is illustrated in Fig. 58 [174] where the back-channel threshold-voltage shift is plotted versus dose for n-channel transistors. (Note from Fig. 56 that, if the SOI transistor structure is flipped upside down, the transistor still looks like an MOS capacitor with the substrate as the gate electrode. This is often referred to as a back-channel transistor.) The data of Fig. 58 were taken from SIMOX SOI transistors with the front (top) channel transistor biased in accumulation to separate the effects of the front- and back-channel transistors. For an n-channel transistor (p-type island), a large negative threshold-voltage shift of the back channel will invert the bottom surface of the channel leading to leakage current. The negative threshold-voltage shift for n-channel back channel transistors is greatly suppressed by applying a large negative substrate bias, which will lead to a reduction in back-channel leakage current.

The radiation response of buried oxides has been found to be highly dependent on the fabrication process [175,176]. SIMOX buried oxides are fabricated by implanting substrates with oxygen at high dose levels and energies. As such, it is natural to expect that the oxide may include numerous implant related defects throughout the buried oxide that can trap radiation-generated charge. Previous work [176-180] has shown that up to 100% of the radiation-generated holes are trapped in the bulk of the oxide at deep trap sites close to their point of origin. This is in contrast to thermal oxides where a smaller fraction (~3% for hardened oxides) of the radiation-generated holes are trapped near the Si/SiO_2 interface. Once trapped, some of the holes are slowly neutralized by electrons by thermal detrapping at room temperature [176-180]. No significant transport of holes through the buried oxide has been observed [176,181] for SIMOX buried oxides fabricated using normal process conditions [181]. However, for SIMOX buried oxides receiving a supplemental oxygen implant and a low temperature anneal, photocurrents have been observed indicating the transport of radiation-induced charge carriers

through the oxide [181]. In addition to hole trapping, electrons are also trapped throughout the bulk of the buried oxide [176]. Most of the trapped electrons are thermally detrapped within <1 s after a pulse of irradiation. This makes electron trapping relatively unimportant for the natural space environment. After the electrons are detrapped, the resultant charge is due to a high concentration of trapped holes causing large negative threshold-voltage shifts of the buried oxide.

BESOI buried oxides are fabricated by bonding together two thermal oxides. As long as the bonding process does not degrade the properties of the thermal oxides, BESOI buried oxides should look more like standard thermal oxides than SIMOX buried oxides [175,182]. Only moderate hole trapping in the bulk of BESOI buried oxides has been observed [175]. However, some electron trapping can occur, presumably at the bond interface [175].

Several microscopic defects have been identified using EPR in SOI buried layers. These defects play a role in instabilities in the buried oxides in radiation environments. The SOI technology most extensively studied is SIMOX technology. In SIMOX material all of the defects in the buried oxide are due to excess silicon indicating that the post-implantation, high temperature anneal step used to form the buried oxide is the source of the defects [91]. The primary defect identified by EPR in SIMOX material is the E'_γ center [93,94,183-187] similar to that for gate oxides. However, in contrast to gate oxides, the variation in the number of E'_γ centers does not track with the variation in positive charge in the buried oxide. Thus, E'_γ are not the primary source of radiation-induced oxide-trap charge [93,94]. The concentration of E' centers has been coupled to electron trap sites in the buried oxide in which a substantial fraction of the E' centers are positive and compensated by trapped negative charge [188]. In addition to the E'_γ center, several other types of defect centers have been identified. One of these is a relatively new class of defect center which has been categorized as a delocalized spin center [186,187,189]. The defect center is delocalized in the sense that the unpaired electron is not associated with any one particular atom. Both E'_γ and delocalized spin centers have also been identified in BESOI material [190]. The delocalized spin center in BESOI material was found to be hydrogen related [190]. In BESOI material, the radiation-induced EPR centers are located near the bonded interface [91]. Therefore, the bonded interface is a potential hole-trap site and may lead to radiation-induced back-channel leakage. In addition, to the defects in BESOI buried oxides, EPR has also identified a new oxygen-related donor defect in the silicon substrate near the bottom Si/SiO_2 interface [191]. The donors appear to result from the nonoxidizing anneal during the bonding process. These donors are also present in SIMOX material [192] and may change the doping concentrations of the substrates.

5.2 Nitrided Oxide Devices

Attractive alternatives to thermal silicon dioxide for ultra-thin oxides for advanced deep submicron technologies are nitrided oxides and reoxidized nitrided oxides (RNO) [193-198]. Nitrided oxides have a lower pin-hole density than SiO_2, can be grown at high temperatures permitting better uniformity and less compressive stress and fixed charge, and can retard the diffusion of dopants through the insulator which can affect the channel resistivity [194]. These properties make nitrided and RNO dielectrics attractive for ultra-thin gate-oxide commercial and

hardened devices [194]. RNO oxides have been shown to be superior to thermal oxides in radiation hardness [199,200] and hot-carrier degradation [201].

Nitrided oxides can be fabricated by several different methods. One of the most straightforward methods is to anneal a thermal oxide in an ammonia (NH_3) ambient. An ammonia anneal results in a large concentration of nitrogen throughout the dielectric with peak concentrations at both interfaces. Nitridation of thermal oxides can result in a large number of electron traps [202]. The electron traps are responsible for higher preirradiation threshold voltages and lower carrier mobilities [202,203]. The nitrided oxide can be reoxidized using a high temperature oxygen anneal, forming a reoxidized nitrided oxide dielectric (RNO). Reoxidizing the nitrided oxide further reduces the amount of nitrogen in the bulk of the dielectric and at the gate interface, leaving a large peak near the dielectric/silicon interface. The RNO process can be optimized to result in transistors with preirradiation interface-trap densities comparable to thermal oxides. Reoxidation also reduces the number of electron traps [204], but it can result in higher preirradiation fixed charge concentrations [199].

The primary difference between thermal and RNO dielectrics in ionizing radiation environments is the nearly total lack of interface-trap buildup for RNO dielectrics [199]. RNO dielectrics can be fabricated in which there is no measurable interface-trap buildup for transistors irradiated to total doses in excess of 50 Mrad(Si) [199]. This makes RNO gates attractive for space applications. For those cases where some interface-trap buildup was observed, the number of interface traps does not increase in time after irradiation [200]. This likely occurs because hydrogen released in the bulk of the dielectric or near the interface (which is responsible for interface-trap buildup in thermal oxides), cannot penetrate the nitrogen rich oxynitride layer near the interface and create an interface trap [200].

RNO dielectrics can be fabricated so that the amount of oxide-trap charge buildup for a RNO oxide is lower to or comparable to that for a thermal oxide. Fig. 59 [199] is a plot of the threshold-voltage shift at midgap for p-channel transistors fabricated with a hardened oxide and with a RNO oxide versus dose. The oxide and RNO dielectric thicknesses were 37 nm and the preirradiation fixed charge levels were ~3×10^{10} and 10^{11} cm^{-2}, respectively. At midgap, interface-trap charge is neutral, thus the threshold-voltage shift at midgap corresponds to the threshold-voltage shift due to oxide-trap charge. The bias during irradiation for the hardened thermal oxide was +5 V and the bias for the RNO oxides was either +5 or -5 V. After irradiating to 10 Mrad(SiO_2), the amount of oxide-trap charge buildup in the hardened thermal oxides is more than twice that for the RNO oxides. Note that for the RNO oxide transistors, the shifts are nearly equal for biases of +5 and -5 V.

The temperature and electric field dependence of hole transport in RNO dielectrics have been investigated [205]. Results show that the charge yield in RNO dielectrics is equal to that in thermal oxides and that the hole transport properties in RNO dielectrics are qualitatively similar to that for hardened thermal oxides in that, for both RNO dielectrics and thermal oxides, hole transport is dispersive in time and strongly temperature and electric field dependent. However, the temperature dependence and electric field dependence are quantitatively different for the two types of oxides [205]. Figure 60 [205] is a comparison of the time for 25, 40, and 50% recovery

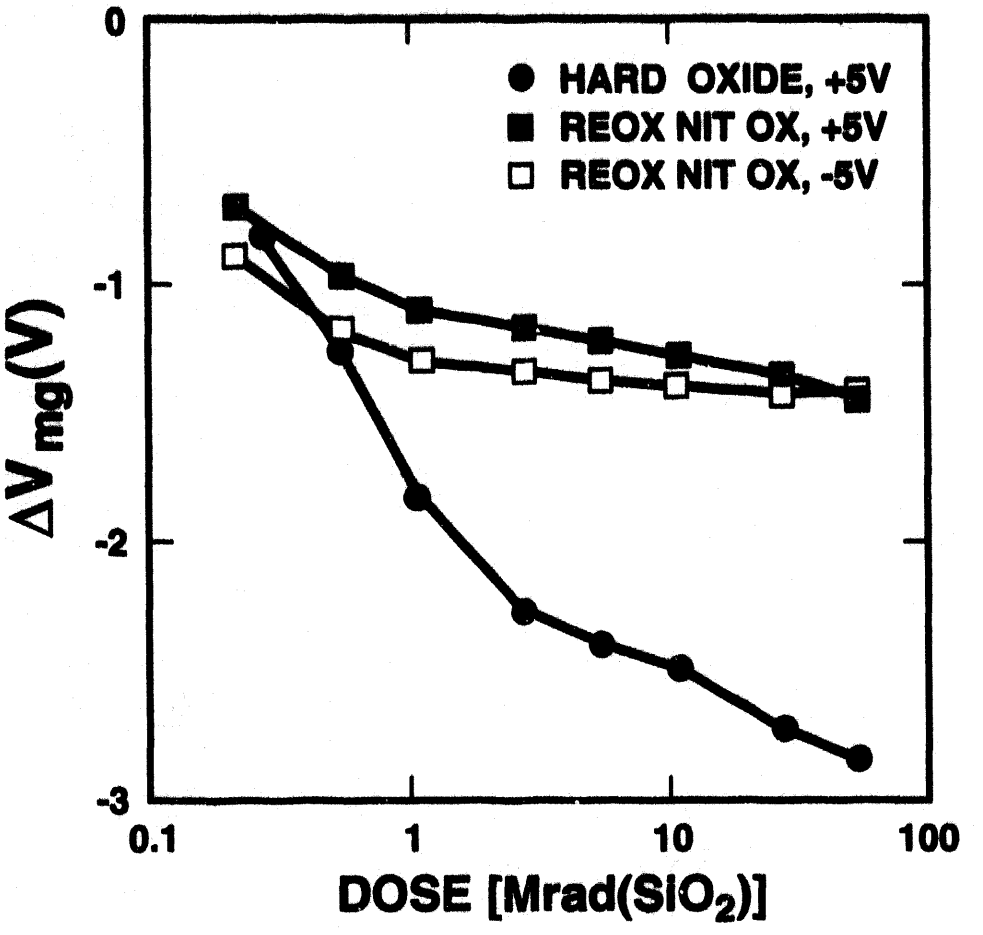


Figure 59: The change in midgap voltage measured on RNO and thermal oxide transistors versus dose. The midgap voltage shift corresponds to the threshold-voltage shift due to oxide-trap charge. (After Ref. 199)

of threshold-voltage shifts for RNO and thermal oxides as a function of temperature. The threshold voltage was measured in the linear region. The electric field in the insulators was 1.35 MV/cm. Note that, at 193 K, the time for 40% recovery is more than 3 orders of magnitude longer in RNO dielectrics (solid symbols) than in thermal oxides (open symbols). For an electric field of 1.35 MV/cm, the thermal activation energies for the RNO and thermal oxides are 0.32 and 0.50 eV, respectively. At higher electric fields and at low temperatures, the recovery time in RNO dielectrics is considerably lower (opposite to that for lower electric fields and higher temperature irradiation and anneals) than for thermal oxides as illustrated in Fig. 61 [205]. For the data of Fig. 61, the temperature during irradiation and anneal was 77 K. Note that, in all cases examined, at electric fields from 2 to 4 MV/cm, the time for recovery in RNO dielectrics is more than an order of magnitude less than for thermal oxides.

To identify the microscopic nature of point defects in nitrided dielectrics, EPR measurements have been performed on nitrided and reoxidized nitrided dielectrics [206]. Nitridation of a thermal oxide tends to reduce the number of radiation-induced E' centers. In addition, nitridation introduces bridging-nitrogen defect-center precursors. Bridging nitrogen

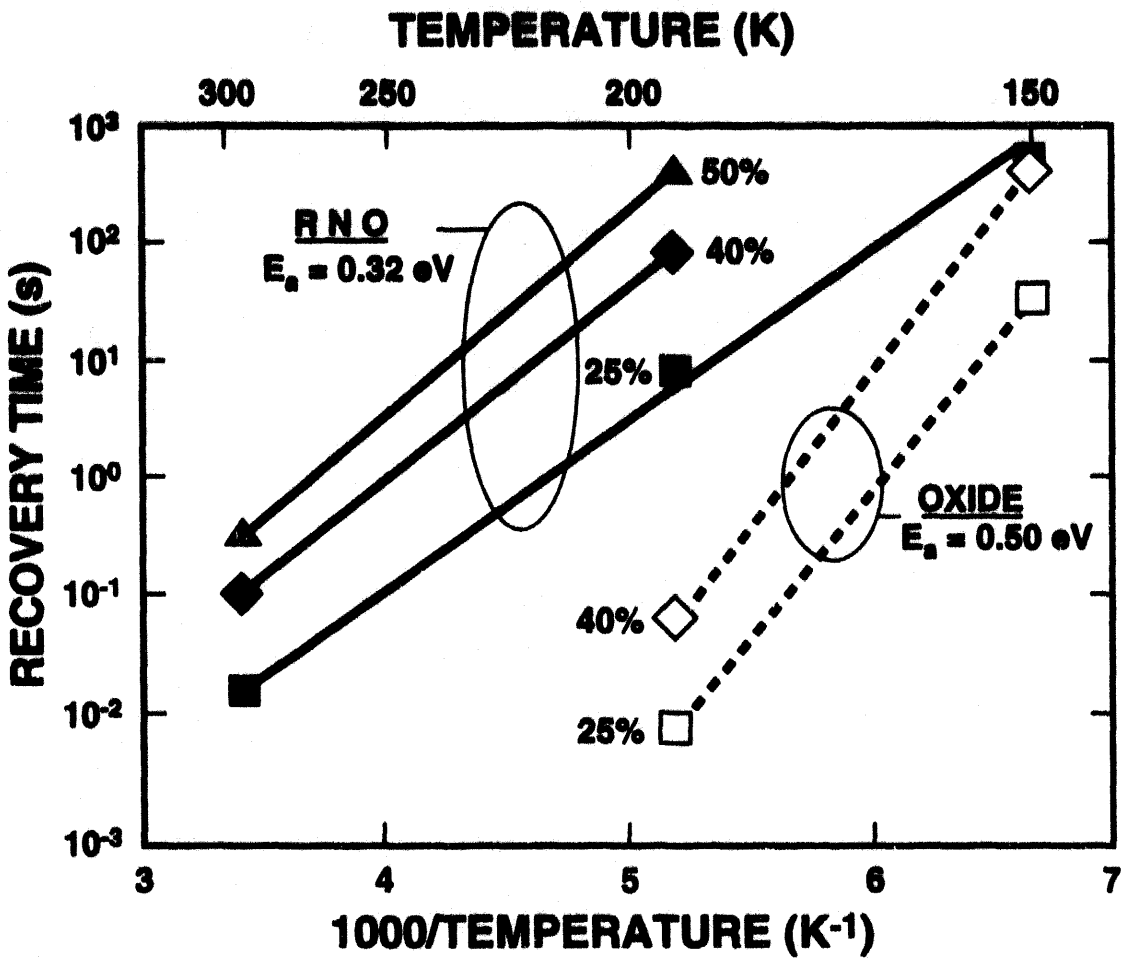


Figure 60: The recovery time versus temperature for RNO and thermal-oxide transistors. (After Ref. 205)

centers are a nitrogen atom bonded to two silicon atoms. This leaves two nitrogen bonds available for trapping charge. Reoxidation causes an increase in the number of radiation-induced E' centers and reduces the number of bridging nitrogen precursors. The bridging nitrogen centers appear to be related to electron trapping effects in nitrided oxides. The E' centers present after reoxidation appear to be different from those in thermal oxides in that they are electrically neutral when paramagnetic [206]. Thus, most of the E' centers in RNO dielectrics do not appear to be associated with radiation-induced oxide-trap charge. Based on etch-back measurements on nitrided and RNO dielectrics, the distribution of bridging nitrogen centers peaks near the gate/SiO_2 interface and radiation-induced E' centers are located uniformly throughout the dielectrics. Recall that for a thermal oxide, radiation-induced E' centers can be located near the Si/SiO_2 interface. Therefore, the nitridation process changes the distribution of radiation-induced E' centers.

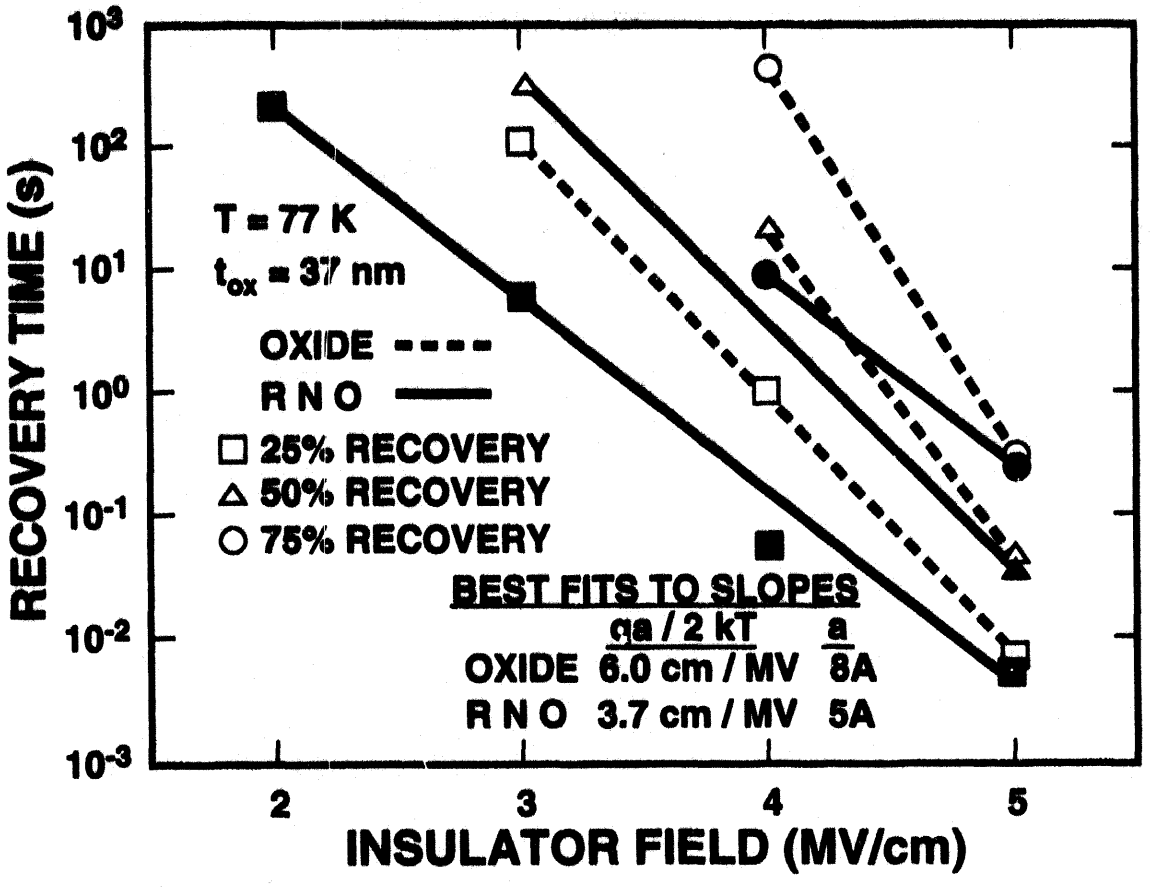


Figure 61: Recovery time versus electric field for RNO and thermal-oxide transistors. (After Ref. 205)

6.0 SINGLE-EVENT PHENOMENA

One of the most detrimental effects of the natural space environment on electronics is single-event effects (SEE). Single event effects were first postulated in 1962 by Wallmark and Marcus [207] and first observed in spacecraft electronics in 1975 by Binder and Smith [208]. In memory circuits, information is stored at nodes in a circuit. If a high-energy heavy ion strikes a circuit node, it can create sufficient charge in a transistor to change the state of the node and cause false information to be stored. This type of failure is known as single-event upset (SEU). This is a non-destructive or soft error. In addition to heavy ions, protons and neutrons can also cause single-event upset. A soft error can be corrected by reprogramming the circuit into its correct logic state or by restarting an algorithm in a central processing unit. The number of soft errors is normally specified in units of errors/bit-day. If the error rate is too large, it can result in performance degradation of a system and potentially mission failure.

Another class of single-event effect that is not correctable by reprogramming is termed a hard error. Hard errors include single-event burnout (SEB), single-event gate rupture (SEGR), latchup, and snapback. If a hard error occurs, a circuit element can be physically damaged and the error cannot be corrected by reprogramming. Latchup is a high current condition that results

from parasitic thyristor (SCR) action in 4-layer structures (e.g., CMOS ICs). Snapback is a high current, low resistance condition that occurs only in n-channel transistors. Both latchup and snapback can be triggered by large current transients created by the incident particle. Once a circuit is "latched up", large currents can flow, and remain unless the power supply to the circuit is interrupted. Unless the power supply current is limited, latchup and snapback can cause permanent damage to a circuit.

In this section the basic mechanisms of single-event upset at the transistor level are presented. In addition, we discuss the mechanisms for two types of heavy-ion induced hard errors: single-event burnout and single-event gate rupture. Single-event induced latchup and snapback are discussed in detail in other parts of this Short Course. For any given transistor, the number of soft errors is highly dependent on the circuit design. Circuit effects also are discussed in other parts of this Short Course.

6.1 Mechanisms of Charge Collection

As a high-energy ion passes through a material, it loses energy by excitation and ionization of atoms, creating a very high density electron-hole plasma along the path of the ion [2]. The amount of energy that an ion deposits per unit depth in a material is given by its stopping power. The mass-stopping power is defined as the linear energy transfer, LET, and is given by

$$LET = \frac{1}{\rho}\frac{dE}{dx} \tag{22}$$

where ρ is the density of the material and $\frac{dE}{dx}$ is the rate of energy loss in the material. LET has the units MeV-cm^2/mg. The integral of LET over path length gives the total deposited energy. Figure 62 [2] is a plot of stopping power (LET) for 2.5-MeV helium ions as a function of depth in silicon. The point of maximum stopping power is called the Bragg peak. The LET for a given ion depends on the target material and energy. Experimental and theoretical values of stopping power for most ions in several materials have been published by Northcliffe and Schilling [209] and Ziegler [210]. Stopping powers can be calculated for silicon, germanium, GaAs, and many compounds using the TRIM code [211] on most IBM compatible personal computers [2].

In addition to heavy ions, high-energy protons can deposit sufficient energy to cause a single-event upset. However, protons cannot directly cause single-event upsets in most present-day GaAs or silicon circuits. For instance, for proton energies from 50 to 200 MeV, the linear-energy transfer (LET) for protons in GaAs varies from ~3×10^{-3} to 8×10^{-3} MeV-cm^2/mg and is below that necessary to cause single-event upset. (For digital GaAs enhancement/depletion mode MESFET circuits, typical LET thresholds are ~0.5 to 2 MeV-cm^2/mg.) However, protons can induce upsets by dislodging atoms from their lattice sites or through nuclear interactions with lattice atoms. Because the resulting secondary particles (e.g., alpha particles or displaced atoms)

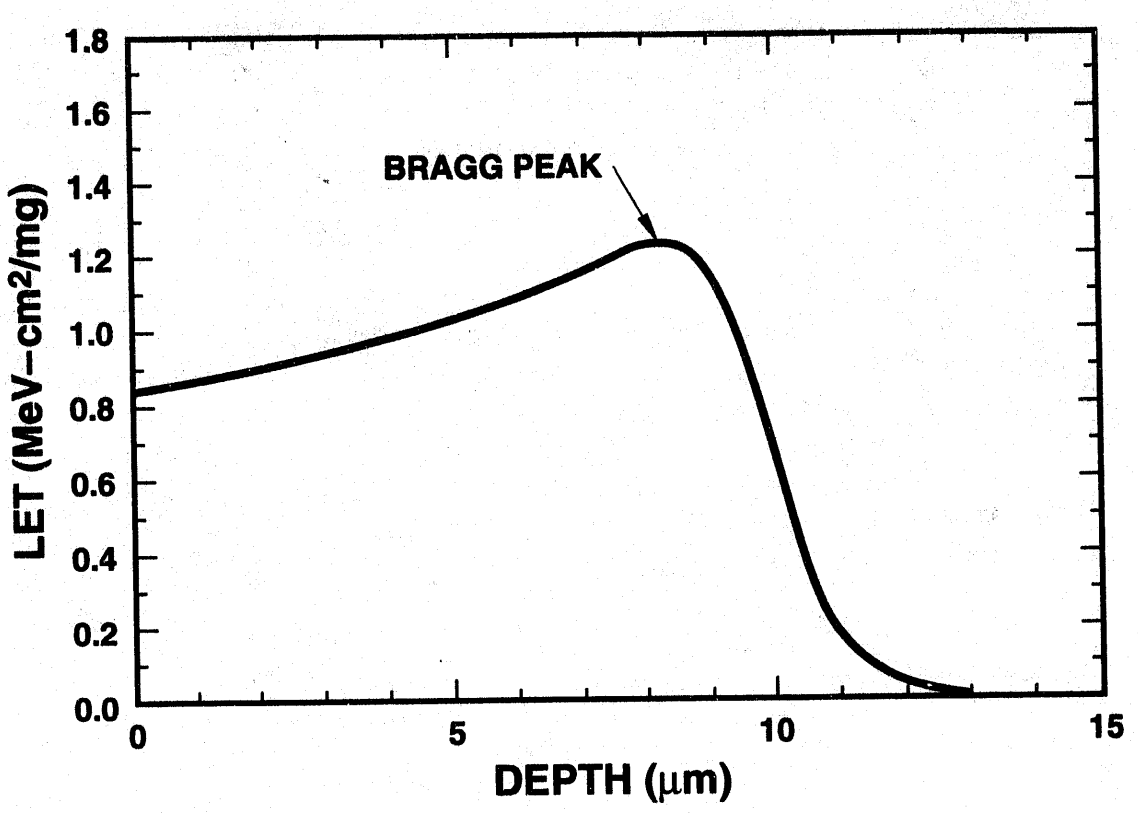


Figure 62: Stopping power (LET) versus depth for a 2.5 MeV helium ion in silicon. (After Ref. 2)

have higher stopping powers, i.e., LET, the secondary particles can cause sufficient ionization to induce single-event upsets.

For single-event effects, an important parameter is the charge deposited in the material. The total deposited charge in a particle track, Q_l, can be calculated from [212]

$$Q_l = \frac{1.6x10^{-2} \cdot LET \cdot \rho}{E_p}, \tag{23}$$

where E_p is the electron-hole pair ionization energy (minimum energy required to create an electron-hole pair) given in units of eV (see Table I), LET is in units of MeV-cm^2/mg, ρ is in units of g/cm^3, and Q_l is given in the units of pC/μm. For silicon, E_{eh} = 3.6 eV and for GaAs, E_{eh} = 4.8 eV. Thus, for an LET of 50-MeV-cm^2/mg, the charge deposited is approximately 0.5 pC/μm and 0.89 pC/μm in silicon and GaAs, respectively.

If the ion passes through a p-n junction, immediately after charge is collected at the electrodes by drift of carriers from within the depletion region. The drift of carriers to the electrodes occurs within hundreds of picoseconds after a heavy-ion strike. This is depicted as Q_D in Fig. 63 [2].

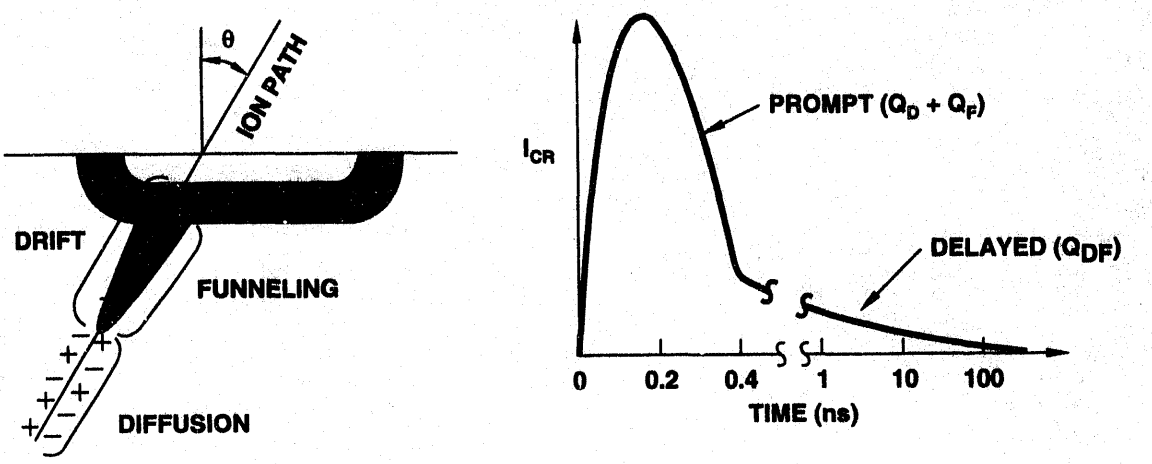


Figure 63: Schematic diagram and time dependence for charge collection by drift, funneling, and diffusion. (After Ref. 2)

Diffusion of carriers to the edge of the junction depletion or funnel region contributes a another component to the collected charge. The diffusion of carriers takes much longer (up to hundreds of nanoseconds to microseconds) than the drift component. The diffusion of carriers is notes as Q_{DF} in Figure 63.

The amount of charge that is collected by drift of carriers within the depletion region can be greatly enhanced by "field funneling." Funneling was first proposed by Hsieh, et al. [213,214], in 1981. The density of the electron-hole plasma (10^{18} to 10^{21} cm^{-3}) created by the ion strike is considerably greater than the doping concentration of typical p-n junctions [215]. The high concentrations of electron and holes in the plasma will distort the original depletion region of the junction into a cylinder which follows the path of the ion [2,213-216]. As a consequence, the junction field region creates a "funnel region" that extends down into the substrate as depicted in Fig. 63 [2,17,213-216]. The electric fields within the funnel region will cause carriers to be collected rapidly by drift to the electrodes. The funnel will exist as long as the concentration of electron-hole pairs in the plasma created by the ion strike is large compared to the doping concentration of the substrate. The temporal peak of collected current from the drift of carriers by field funneling corresponds roughly to the dielectric relaxation time [216]. The dielectric relaxation time, τ_D, is the characteristic time it takes for a solid to respond to charge imbalance [217]. It is given by $\tau_D = \varepsilon/\sigma$, where ε is the permittivity and σ is the conductivity of the material. For silicon substrates with a doping concentration of 10^{15} cm^{-3}, τ_D is approximately 14 ps, and the potential spreading of the funnel reaches a maximum in approximately 25 ps [216]. For silicon devices, the amount of charge that is collected by drift is greatly enhanced by the funnel region, increasing the sensitivity of silicon ICs to single event upset.

The time, τ_c, that it takes for charge to be collected at a node from within the funnel region can be estimated from [215,218]

$$\tau_c = \left[\frac{3N_o}{8\pi\beta N_A v_p D^{1/2}}\right]^{2/3}, \quad (24)$$

where N_o is the plasma line density at the surface [215], N_A is the doping concentration, v_p is the effective charge separation (hole escape) velocity, and D is the ambipolar diffusion constant. The "β-factor" can be estimated from

$$\beta = \left\langle \left[\ln\left(\frac{N_o}{4\pi N_A Dt}\right)\right]^{1/2} \right\rangle, \quad (25)$$

where <...> denotes an appropriate time average over the drift collection times [215]. Equations (24 and 25) are valid for most particles, but break down for very highly ionizing particles [218]. Based on experimental data, the collection time increases with ionization density. As the collection time increases, the funnel time will collapse before all charge is collected and diffusion of carriers will occur. At this point, carriers can diffuse to adjacent nodes of a circuit causing multiple bit upsets [218].

For GaAs devices built on a semi-insulating substrate, the dielectric relaxation time is long (~100 μs) and the recombination time is very short (1-10 ns). Thus, many of the carriers will recombine or be collected by other processes long before funneling is established [217]. Therefore, funneling is relatively unimportant for GaAs devices fabricated on semi-insulating substrates. For GaAs devices built on semiconducting substrates, the effects of funneling are comparable to those for silicon devices [219].

The reduced importance of funneling for GaAs devices fabricated on a semi-insulating substrate does not necessarily imply that GaAs devices are more immune to single-event upset than equivalent silicon devices. In addition to the collection mechanisms discussed above, other collection mechanisms contribute to charge collection in GaAs devices. In some cases, these collection mechanisms result in *more* charge (up to 8 times) being collected than is deposited by the incident particle [220-225]. Several "enhanced" collection mechanisms have been proposed for GaAs and/or silicon devices. These include 1) a back-channel turn-on mechanism [223,226-228], 2) a bipolar source-drain, or bipolar gain mechanism [220-222,224,225,228], and 3) an ion shunt mechanism [229-231].

Significant enhancement of the collected charge can result from the bipolar source-drain or bipolar gain mechanism. Under normal bias conditions for a depletion- or enhancement-mode MESFET, immediately after a heavy ion strike electrons will be collected at the drain and holes will be collected at the gate as is illustrated in Fig. 64. This is the drift component of charge collection discussed above. As the electric field of the depletion region changes in response to the column of charge created by the heavy ion, holes will also begin to drift toward the source. As the holes approach the source, they will lower the potential barrier at the source. The lowering of the source potential barrier will turn on the transistor causing enhanced electron flow

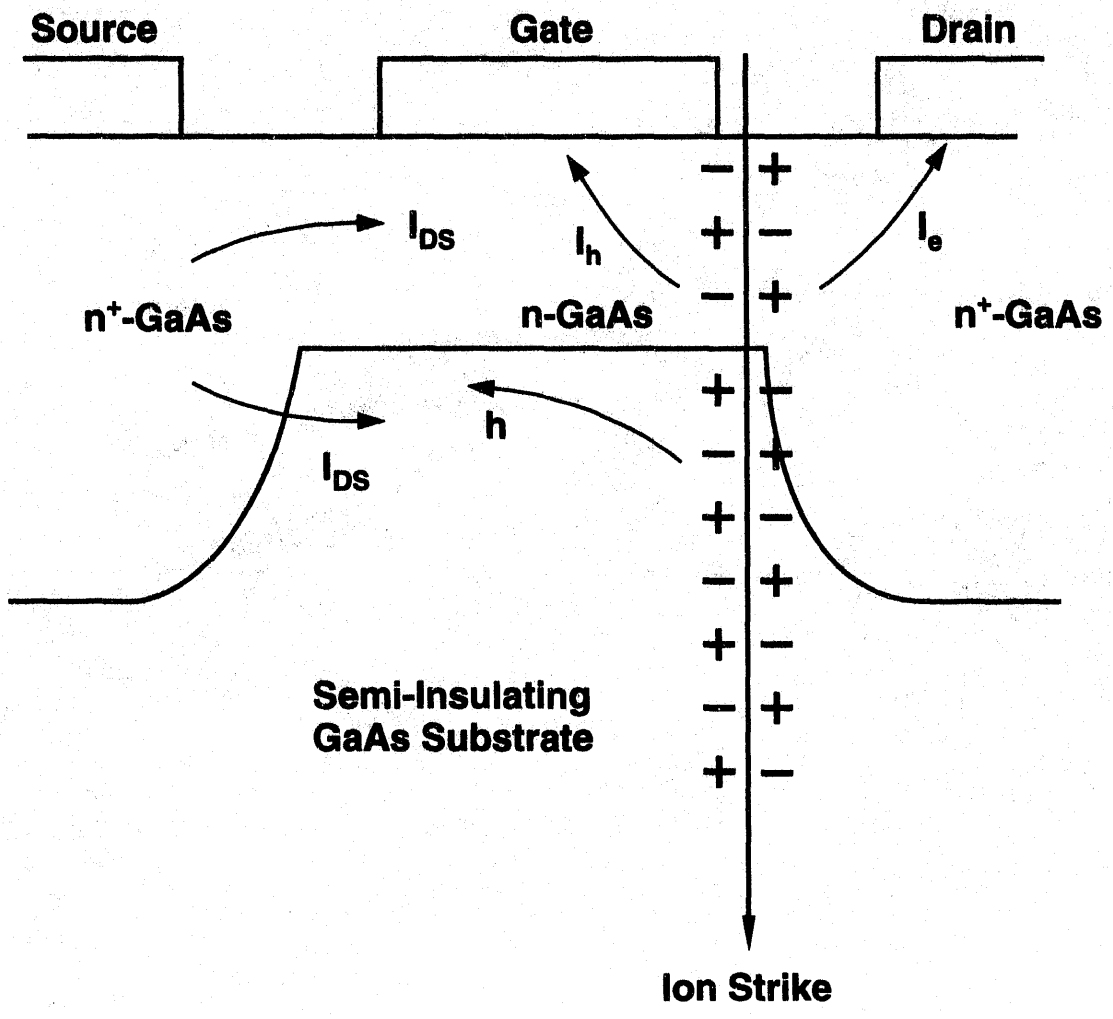


Figure 64: Cross-section of a GaAs MESFET fabricated in a semi-insulating substrate illustrating charge collection mechanisms.

from the source to the drain of the transistor. This effect is referred to as the bipolar source-drain or bipolar gain effect. A large fraction of the electron flow occurs through the bulk of the substrate beneath the implanted n-type channel layer [220]. Electron flow through the bulk of the substrate will continue as long as the concentration of free carriers is more than or comparable to the built-in space charge in the channel-substrate junction [220]. The number of electrons emitted by lowering of the source potential can be significant. The total charge collected at the drain can be as much as 30 times that of the total charge collected at the gate [220]. Figure 65 [232] is a plot of the collected current at the drain, gate, and source for a 1.0-μm enhancement-mode GaAs MESFET illuminated with a 1-ps laser pulse positioned between the drain and gate. The transistor was biased in the "OFF" state with $V_{GS} = 0$ V and $V_{DS} = 1.0$ V . The charge collected at the gate peaks at approximately 50 ps after the laser pulse. Similar results were obtained for a high-energy helium strike [232]. This peak corresponds to the time it takes for holes to drift from within the depletion region to the gate electrode. The charge collected at the drain is composed of two signals. The first signal is due to the drift of electrons to the drain. This signal is similar to the gate signal which peaks in approximately 50 ps. The second signal is

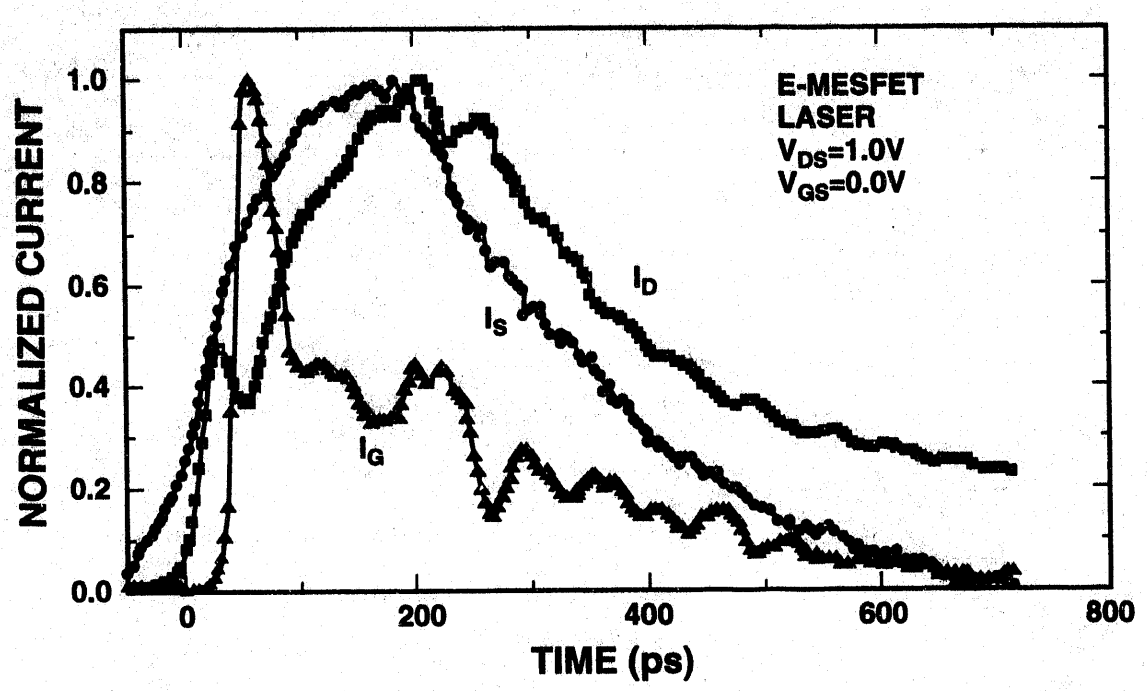


Figure 65: Current collected at the drain, gate, and source of a GaAs MESFET after a 1-ps laser pulse. (After Ref. 232)

much wider than the first signal and peaks at approximately 200 ps. The second signal is probably due to lowering of the source potential resulting a large flow of electrons from the source to drain. The charge collected at the source shows only one peak, qualitatively similar to the second drain peak, which peaks at approximately 200 ps. The source signal also results from the lowering of the source potential. Note that the total collected charge at the drain (the integral of the collected current curve) is greatly enhanced by the bipolar gain effect. This effect can greatly increase the number of soft errors for GaAs parts in a space environment.

Another mechanism that has been suggested to result in enhanced charge collection is the ion shunt mechanism [229-231]. This mechanism is applicable to both silicon and GaAs devices with multiple p-n structures (e.g., silicon bipolar and CMOS transistors and GaAs heterostructure bipolar transistors). The ion-shunt mechanism is illustrated in Fig. 66 [230]. As depicted in Fig. 66, a heavy-ion passes through an n^+-p-n-n^+ junction and deposits charge along the ion track. The high density of charge created by the ion is initially considerably larger than the background concentration of the n and p layers. The charge deposited by the ion effectively shorts together the bottom and top n^+ layers. If a potential field exists between the electrodes, charge will flow between the n^+ layers and a single-event upset can result. Note that, for this mechanism to occur, the ion track must penetrate both n^+ regions. The amount of charge collected by the ion shunt mechanism will increase with the LET of the incident ion [231], and in some cases can be more than that deposited by the ion [231]. The effect of the ion-shunt mechanism on the single-event upset sensitivity will depend on the device structure and operating conditions.

In a memory circuit, a node will change state if the deposited charge is more than the "critical" charge. The critical charge is defined as the minimum charge necessary to upset a

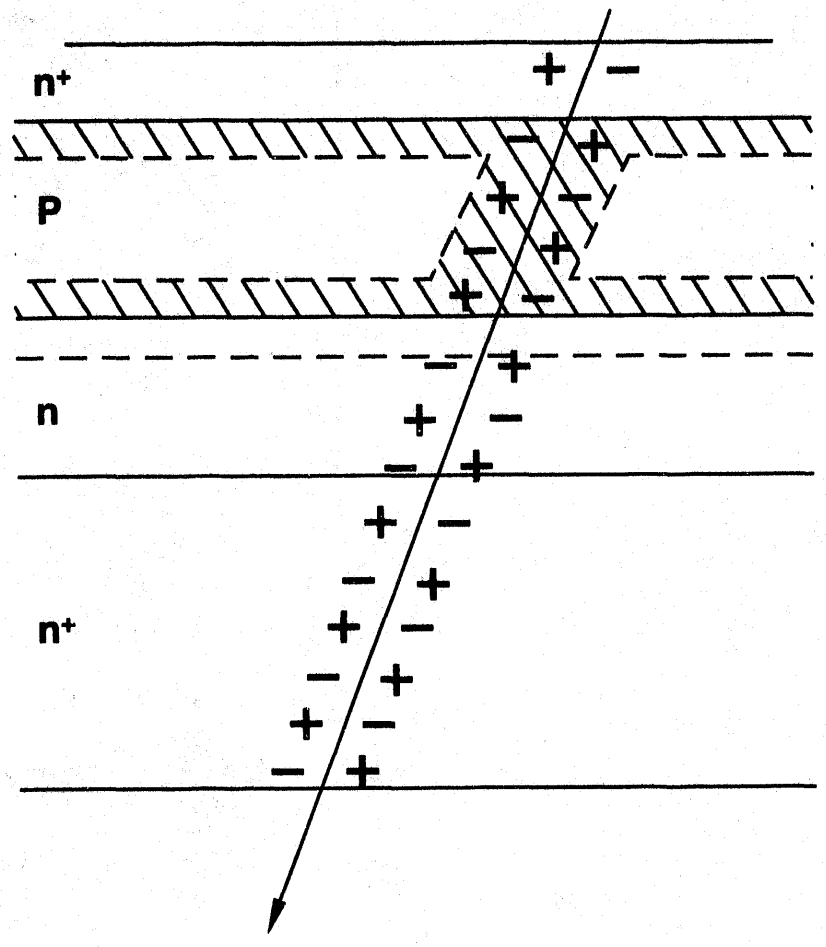


Figure 66: Schematic diagram of a heavy ion penetrating an n^+-p-n-n^+ junction. The cross-hatched regions correspond to the n-p junction depletion regions. (After Ref. 230)

memory bit [2]. For a DRAM this is the difference between the amount of charge stored on the node and the minimum charge that the sense amplifiers require to reliably read the stored data. The critical charge is highly device and circuit dependent. It can be as low as 50 fC [233]. This is equivalent to $3x10^5$ electrons.

6.2 Hard Errors

In addition to soft errors that can be recovered by reprogramming, in some cases heavy ions can cause permanent damage to the transistor [234-244]. This type of error is often referred to as a "hard" error. Two types of hard errors discussed here are single-event burnout (SEB) and single-event gate rupture (SEGR).

6.2.1 Single-Event Burnout

Single-event burnout can cause permanent damage to bipolar power transistors and to power MOSFETs [237-244]. A cross-section of a power MOSFET is shown in Fig. 67 [243]. Note that the structure of a power MOSFET is much different than for a standard MOSFET. The

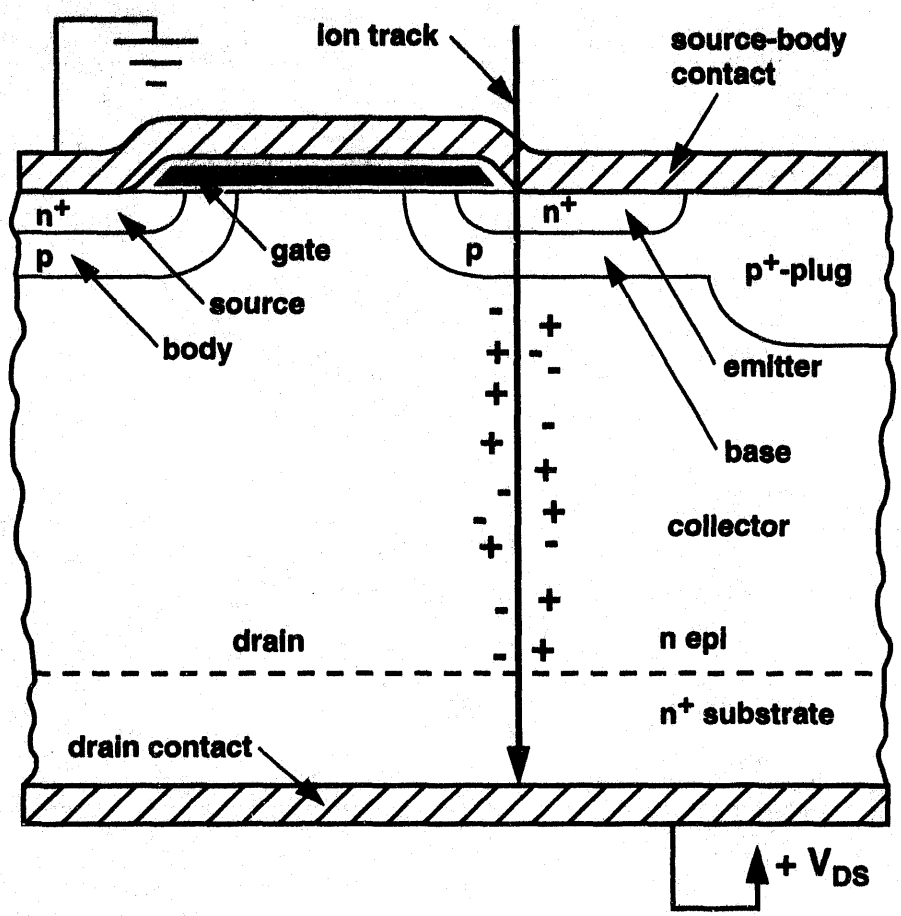


Figure 67: Cross-section of a power MOSFET. (After Ref. 243)

substrate of a power MOSFET acts as the drain. The channel (body) and source regions are formed by a double diffusion. Inherent to this process is a bipolar npn transistor (for the n-channel power MOSFET of Fig. 67) with the drain acting as the collector, the channel region as the base, and the source as the emitter. For normal operation a positive bias on the gate allows electrons to flow from the source to drain near the surface. The bipolar junction is always biased in the "OFF" mode during normal operation by shorting the source to the channel at the surface of the device. If a heavy ion strikes the parasitic transistor, as shown in Fig. 67, the charge deposited by the ion strike will cause current to flow in the base region and it will raise the local potential of the emitter-base junction. If the current flow is high enough, it can forward bias the emitter-base junction. At this point the parasitic transistor turns "ON". After the parasitic bipolar transistor is turned "ON", second breakdown of the bipolar junction transistor can occur. This second breakdown has been referred to as current-induced avalanche [242]. In addition to increased electron injection from the emitter to the base, the avalanche breakdown will also cause holes to flow from the collector to the base. Depending on the current density during current-induced avalanche (and the current supply of the external circuit), the current induced in the parasitic transistor by the heavy ion will either dissipate with no device degradation or will regeneratively increase until (in absence of current limiting elements) the device is destroyed [2,243].

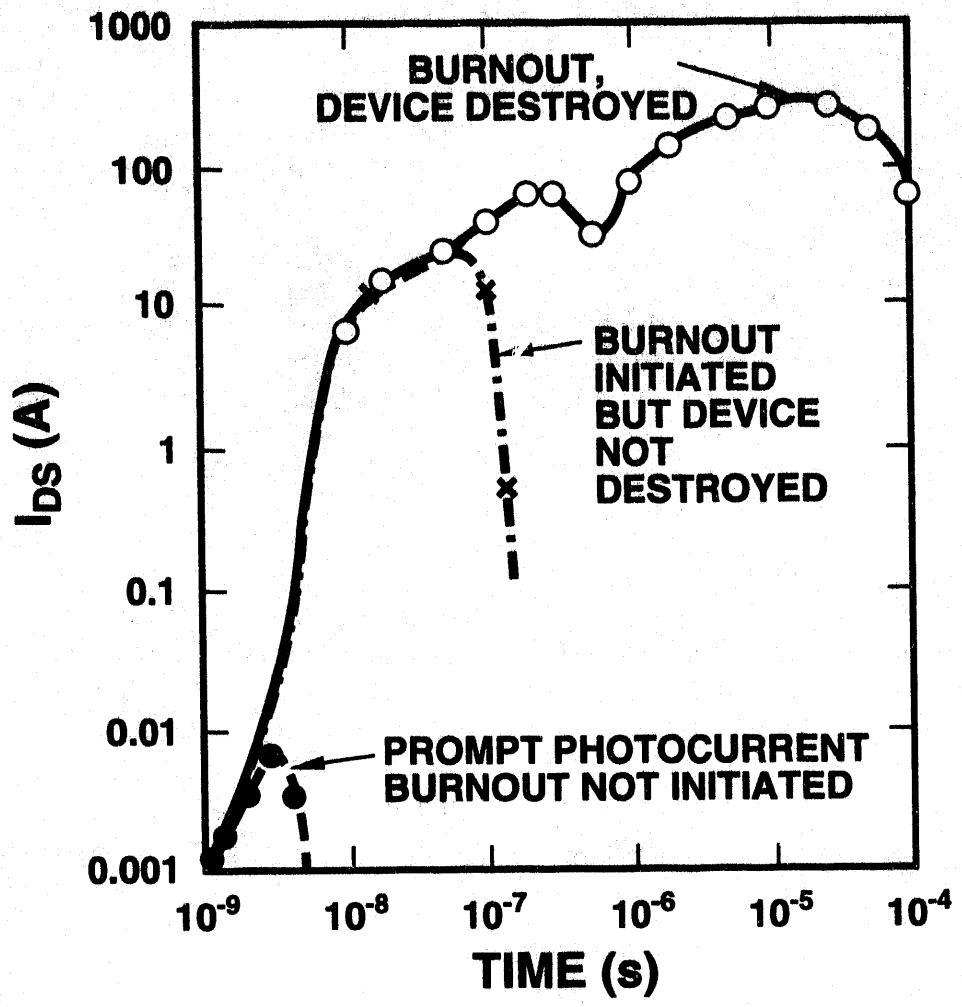


Figure 68: Increase in drain-to-source current in a power MOSFET during varying degrees of single-event burnout. (After Ref. 238)

Experimental results [238] have shown that there is a threshold for the drain-to-source voltage, V_{DS}, in order for SEB to occur. This threshold has been referred to as the failure-threshold voltage (V_{Fth}). If V_{DS} is below the failure-threshold voltage, the heavy-ion strike causes a small prompt photocurrent lasting for approximately 5 ns as depicted in Fig. 68 [238]. Observation of the prompt signal is normally an indication that V_{DS} is close to the failure-threshold voltage. As V_{DS} exceeds V_{Fth} burnout can occur, and the drain-to-source current increases dramatically. If the current is below a critical value, burnout will not destroy the device as indicated in Fig. 68. However, if the current is sufficiently high, SEB will destroy the device. The voltage level at which a device is destroyed is highly device dependent and can vary from 22 to 90% of the rated breakdown voltage for an n-channel transistor [238]. Breakdown voltages for a power MOSEFT can vary widely, from less than 80 V to more than 500 V. Thus, the range of V_{DS} required to initiate burnout can vary from less than 20 V to hundreds of volts. The closer V_{DS} is to V_{Fth}, the lower the current density is in order to initiate burnout [238].

The failure-threshold voltage has also been found to depend on the LET of the incident ion [238]. As the ion LET is increased, it generates higher current densities along its path. A lower voltage is required to sustain current-avalanche breakdown as the current density is increased [242]. Thus, the failure-threshold voltage decreases as LET increases, consistent with experimental results [238]. Increasing temperature has been found [243] to decrease the susceptibility of power MOSFETs to SEB by lowering the avalanche multiplication factor.

Several methods for reducing or eliminating SEB have been proposed [237]. These include 1) using pnp transistors to utilize the lower ionization coefficients of holes, 2) using graded junctions to increase the length of the silicon region over which the voltage is dropped, and 3) using current limiting (inductance, resistance, or both) to prevent the simultaneous high-current, high-voltage condition.

6.2.2 Single-Event Gate Rupture

A single-event gate rupture can occur as a single heavy ion passes through a gate oxide. SEGR occurs only at high oxide electric fields, such as those during a write or clear operation in a nonvolatile SRAM or E^2PROM [2,234,235]. It was first observed [234,235] for metal nitride oxide semiconductor (MNOS) dielectrics used for memory applications. In later works, SEGR was observed in power MOSFETs [238] and MOS transistors [236].

SEGR is caused by the combination of the applied electric field and the energy deposited by the ion [236]. As an ion passes through a gate oxide it forms a highly conducting plasma path between the silicon substrate and the gate dielectric [2,235,236]. With an electric field across the oxide, charge will flow along the plasma path depositing energy in the oxide. If the energy is high enough, it can cause localized heating of the dielectric and potentially a thermal runaway condition. If thermal runaway occurs, the local temperatures along the plasma will be high enough to cause thermal diffusion of the gate material, cause the dielectric to melt, and evaporate overlying conductive materials [2,236]. The resistance of the initial ion track is inversely proportional to the ion LET. If the LET is increased, resistance is lowered and the required voltage across the device to sustain conduction is reduced [236]. In Fig. 69 [236] the failure threshold, V_{FT}, versus LET is shown for 45 nm SiO_2 oxides (bottom curve) and composite oxides composed of 2.2 nm SiO_2 oxide and 35 nm of Si_3N_4 dielectric (top curve). Note that for both the composite and SiO_2 dielectrics the failure threshold increases linearly with the inverse of LET. For thermal SiO_2 oxides with the incident ion normal to the surface, the critical electric field, E_{cr}, for SEGR is given by [236,238,245]

$$E_{cr} = \frac{41}{(LET)^{1/2}} x10^6 \ V/cm. \qquad (26)$$

For a 180 MeV Ge ion with an LET of 36.8 MeV-cm^2/mg, this gives a critical electric field of approximately 6.7 MV/cm. Typical intrinsic breakdown electric field strengths for a thermal gate oxide are in the range of 10 MV/cm [245]. Thus, the critical electric field for SEGR is roughly 67% of the intrinsic breakdown electric field strength under these conditions.

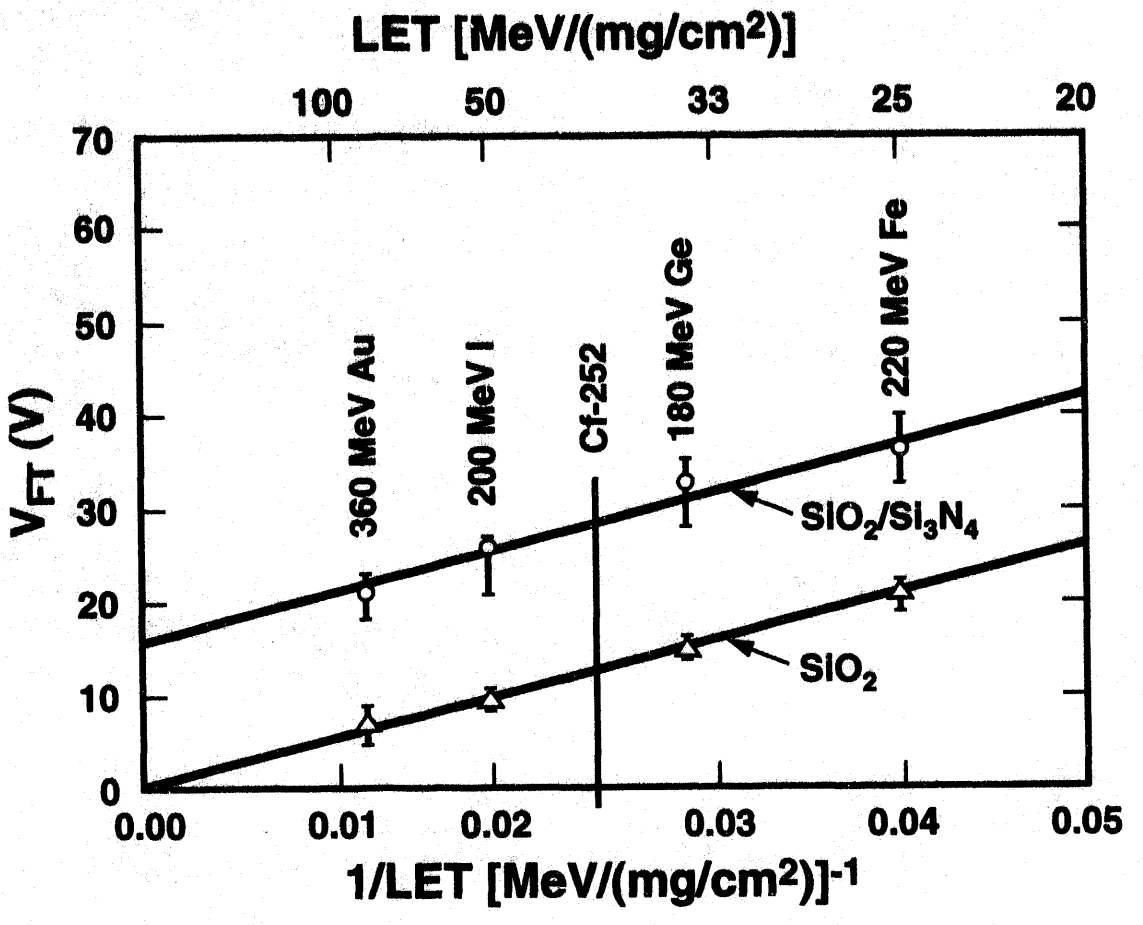


Figure 69: Failure threshold for single-event gate rupture versus heavy-ion LET. (After Ref. 236)

In addition to depending on the oxide electric field and LET, the failure threshold also depends on the incident angle of the ion strike. In Fig. 70 [236] the angular dependence of failure threshold is shown. The failure threshold is noted to increase linearly with $1/\cos\theta$ where θ is the incident angle. As the incident angle increases, the path length between the silicon substrate and gate material increases, increasing the effective resistance along the ion track. This has been proposed as the cause of the angular dependence [236].

For a memory transistor, the probability of a SEGR will depend on the time that the device is in a write, clear, or other high-electric field mode of operation. For a number of nonvolatile memory applications this may be only a small percentage of the total operation time. Clearly the probability of a SEGR is highly dependent on the system application.

7.0 SUMMARY

We have covered the basic mechanisms of radiation effects in the natural space environment. The natural space environment can cause significant damage to spacecraft

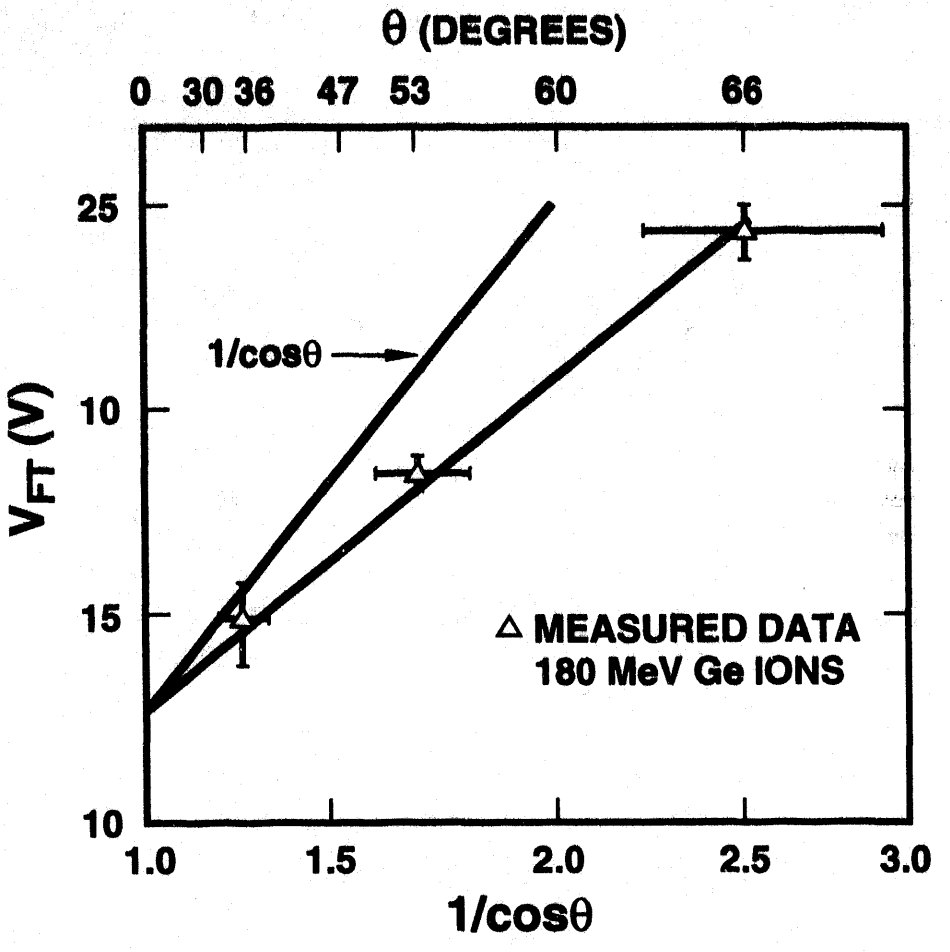


Figure 70: Failure threshold for single-event gate rupture versus heavy-ion incident angle (After Ref. 236)

electronics. It can cause degradation through total-dose ionizing radiation damage, single-event related soft and hard errors, and displacement damage. Of these three, total-dose and single-event effects were discussed. Although we have focused on the natural space radiation environment, the information learned for the most part is applicable to high, moderate, and low-dose-rate applications.

Particles present in the space environment vary widely with altitude and angle of inclination. They can be grouped into two general categories: 1) particles trapped by the earth's magnetic field (primarily electrons and protons) and 2) cosmic rays: heavy ions and high-energy protons of galactic or solar origin. The earth's magnetic field lines form domains or bands of electrons and protons around the earth. Trapped electrons are present predominantly from 1 to 12 earth radii, while trapped protons are present predominantly from 1 to 3.8 earth radii. The galactic cosmic ray spectrum consists mostly of protons (85%) and alpha particles (14%). Less than 1% of the galactic cosmic ray spectrum is composed of heavy ions. In most solar flares, the majority of particles are energetic protons. The number of heavy ions in a solar flare is normally insignificant compared to the background concentration of heavy ions from the galactic cosmic

ray spectrum. The total dose that a device can be exposed to in one year can vary from less than 1 krad(Si) for some low-earth orbits up to 1 Mrad(Si) for other orbits.

Particles present in the space environment can ionize atoms in a material creating electron-hole pairs. For energetic particles present in the space environment, each incident particle can create thousands or even millions of electron-hole pairs. The generated carriers can lead to device degradation.

For an irradiated MOS transistor, electrons created in the oxide will rapidly leave the oxide in picoseconds. However, even before the electrons leave the oxide some fraction of the electrons will recombine with holes. The fraction of electron-hole pairs that escape recombination is the electron-hole yield. The time for hole transport via polaron hopping is much slower than it is for electrons and depends on temperature, bias, and oxide thickness. At room temperature, hole transport takes on the order of microseconds for a gate oxide. With a positively applied gate bias, holes will transport toward the Si/SiO_2 interface, where some fraction of the holes will be trapped at defects near the Si/SiO_2 interface forming a positive oxide-trap charge. Immediately after oxide-trap charge is formed, it begins to be neutralized by electrons tunneling from the silicon or by the thermal emission of electrons from the oxide valance band. The neutralization of oxide-trap charge can be both bias and temperature dependent. Large concentrations of oxide-trap charge can cause increased static supply leakage current in an IC. Thus, for irradiation conditions and for technologies where oxide-trap charge dominates IC radiation response, the primary failure mechanism tends to be increases in leakage current.

As holes "hop" through the oxide or as they are trapped near the Si/SiO_2 interface hydrogen ions are likely released. These hydrogen ions can drift to the Si/SiO_2 interface where they may react to form interface traps. Interface-trap buildup can take thousands of seconds to saturate. The buildup of interface traps is temperature, bias, and time dependent. However, there does not appear to be a "true" dose rate dependence for the buildup of interface traps. Unlike oxide charge, interface traps do not anneal at room temperature. At threshold, interface traps are predominantly positively charged for p-channel transistors and negatively charged for n-channel transistors. Thus, interface-charge charge tends to compensate oxide-trap charge for n-channel transistors and add together for p-channel transistors. Large concentrations of interface-trap charge can decrease the mobility of carriers and increase the threshold voltage of n-channel transistors. These effects tend to decrease the drive of transistors, degrading timing parameters of an IC.

Due to cost and performance requirements, commercial devices are seeing increased use in space systems. Commercial technologies have been fabricated where significant oxide-trap charge neutralization occurs and also where little or no oxide-trap charge neutralization occurs. Thus, in a space environment, the radiation response of some commercial technologies may be dominated by interface-trap charge and for other technologies the radiation response may be dominated by oxide-trap charge. As the IC industry tends towards ultra-thin gate oxides, even commercial gate oxides can be fabricated that are radiation hardened. In both high- and low-dose-rate environments, commercial IC radiation response may be dominated by field oxide

induced leakage current. Even at relatively low dose levels, ~10 krad(Si), field oxides can cause IC failure for some commercial technologies. An additional concern for advanced technologies (commercial and radiation hardened) are process-induced effects caused by the special tools required for defining small geometries. Although most of the damage can be annealed out by a moderate temperature metal sinter step, in some cases higher temperatures are required to prevent increased radiation-induced degradation.

Two technologies that may see increased use in the future are silicon-on-insulator (SOI) and nitrided oxide dielectrics. SOI transistors are built on an insulating layer reducing the amount of p-n junction area. The reduced junction area leads to lower parasitic capacitance for faster operation, and to a reduction in the generation volume leading to a considerable reduction in the sensitivity of SOI ICs to single-event upset and other transient effects. The absence of a conducting path underneath the MOS transistor completely eliminates parasitic pnpn paths that can cause latchup. The major difference between the radiation response of MOS transistors fabricated on bulk silicon substrates and SOI transistors is due to the buried oxide of SOI transistors. Up to 100% of the holes generated by irradiation can be trapped in defects in the bulk of the buried oxide. The buildup of charge can invert the bottom surface of the silicon channel of a MOS/SOI transistor creating a back-channel leakage current.

Reoxidized nitrided oxides (RNO) can be fabricated such that there is no measurable interface-trap buildup and with less oxide-trap charge buildup than comparable thermal oxides. The lack of interface-trap buildup for RNO transistors is likely due to the fact that hydrogen released in the dielectric cannot penetrate the nitrogen rich oxynitride layer present near the interface and create an interface trap.

If a high-energy proton or ion strikes a circuit node it may create sufficient charge in a transistor to change the state of the node and cause false information to be stored. This type of failure is known as a single-event upset. (SEU). This is a non-destructive or soft error. A soft error can be corrected by reprogramming. The number of soft errors will depend on the amount of charge that is deposited in the material by the ion or proton. Charge is collected primarily through three mechanisms: 1) drift of carriers within the depletion region of a p-n junction, 2) field funneling, and 3) diffusion. The drift of carriers normally occurs within hundreds of picoseconds after a heavy ion strike. The high density of electron-hole pairs generated by the ion can distort the depletion region of a p-n junction creating a "funnel region" that extends down into the substrate. For silicon transistors, field funneling can significantly increase the charge collected by drift of carriers. For GaAs transistors fabricated on a semi-insulating substrate, field funneling is not an important contributor to charge collection.

Another class of single-event effect that is not correctable by reprogramming is termed a hard error. Hard errors include single-event burnout (SEB), single-event gate rupture (SEGR), latchup, and snapback. In this portion of the Short Course, only SEB and SEGR were covered. SEB can cause permanent damage to a bipolar power transistor and to a power MOSFET. For a power MOSFET, SEB is caused by large current flows induced by a heavy ion turning "ON" a parasitic bipolar transistor inherent to the power MOSFET structure. As long the drain-to-source bias is above a threshold value, SEB can be initiated. SEGR occurs as a heavy ion passes

through a gate oxide. It has been observed in metal nitride oxide semiconductor dielectrics used for memories, in power MOSFETs, and in thermal gate oxides. It is caused by the combination of an applied electric field and the energy deposited by an ion. The critical electric field for SEGR varies inversely with the square of the LET of the incident ion.

It is hoped that the student has gained an appreciation of the need for basic mechanisms studies. Without the knowledge gained by these studies, we would not be in the position to develop hardened technologies and to develop cost-effective, reliable hardness assurance test guidelines.

Acknowledgments

The author is greatly indebted to numerous discussions and suggestions from his colleagues at Sandia National Laboratories and especially Dan Fleetwood, Marty Shaneyfelt, Bill Warren, Peter Winokur, Fred Sexton, and Gerald Hash. I also wish a special thanks to Peter Winokur for his support during the course of writing this manuscript.

References

[1] E. G. Stassinopoulos and J. P. Raymond, "The Space Radiation Environment for Electronics," Proc. of the IEEE 76, 1423 (1988).

[2] F. W. Sexton, "Measurement of Single Event Phenomena in Devices and ICs," 1992 IEEE NSREC Short Course, pp III-1 - III-55.

[3] E. Petersen, "Soft Error Due to Protons in the Radiation Belts," IEEE Trans. Nucl. Sci. NS-28, 3981 (1981).

[4] K. G. Kerris, "Source Considerations and Testing Techniques," in Ionizing Radiation Effects in MOS Devices and Circuits, edited by T. P. Ma and Paul V. Dressendorfer, John Wiley & Sons, New York, pp. 443-484, 1989.

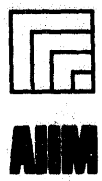
[5] D. M. Sawyer and J. I. Vette, "AP8 Trapped Proton Environment for Solar Maximum and Solar Minimum," Rep. NSSDC76-06, National Space Science Data Center, Greenbelt, MD, Dec., 1976.

[6] "AE8 Trapped Electron Model," National Space Science Data Center, NASA-Goddard Space Flight Center.

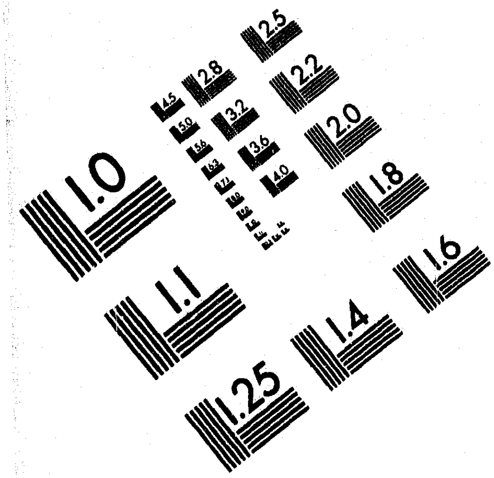
[7] P. Meyer, R. Ramaty, and W. R. Webber, "Cosmic Rays - Astronomy With Energetic Particles," Physics Today, 27, 23 (1974).

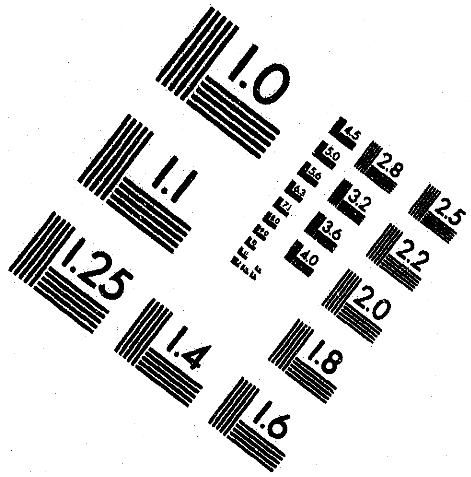
[8] J. H. Adams, Jr., R. Silberberg, and C. H. Tsao, "Cosmic Ray Effects on Microelectronics, Part 1: The Near-Earth Particle Environment," NRL Memorandum Report 4506, August 25, 1981.

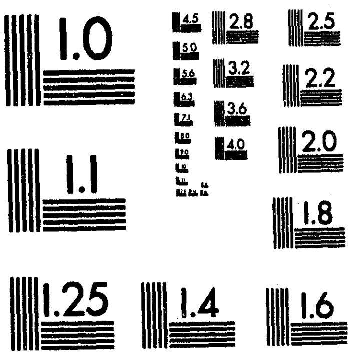
[9] J. H. Adams, R. Silberberg, and L. H. Tsao, "Cosmic Ray Effects on Microelectronics, Part I: The Near-Earth Particle Environment," Naval Research Laboratory Memorandum Report, No. 4506, August 25, 1981.

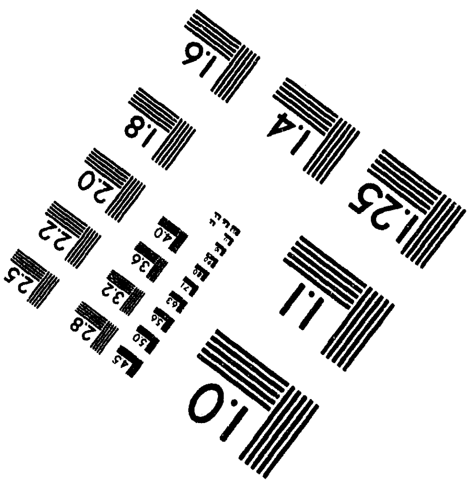


Association for Information and Image Management
1100 Wayne Avenue, Suite 1100
Silver Spring, Maryland 20910
301/587-8202









MANUFACTURED TO AIIM STANDARDS
BY APPLIED IMAGE, INC.

2 of 2

[10] M. A. Shea, "Intensity/Time Profiles of Solar Particle Events at One Astronomical Unit," Proceedings of the Interplanetary Particle Environment Conference, April 1988, Pasadena, California, pp. 75-84.

[11] J. H. Adams, Jr., "The Natural Radiation Environment Inside a Spacecraft," IEEE Trans. Nucl. Sci. NS-29, 2095 (1982).

[12] J. H. Adams, Jr., "The Variability of Single Event Upset Rates in the Natural Environment," IEEE Trans. Nucl. Sci. NS-30, 4475 (1983).

[13] R. A. Cliff, V. Danchenko, E. G. Stassinopoulos, M. Sing, G. J. Brucker, and R. S. Ohanian, "Prediction and Measurement of Radiation Damage to CMOS Devices on Board Spacecraft," IEEE Trans. Nucl. Sci. NS-23, 1781 (1976).

[14] J. L. Kaschmitter, D. L. Shaeffer, N. J. Colella, C. L. McKnett, and P. G. Coakley, "Operation of Commercial R3000 Processors in the Low Earth Orbit (LEO) Space Environment," IEEE Trans. Nucl. Sci. NS-38, 1415 (1991).

[15] S. B. Roeske, private communication.

[16] M. R. Shaneyfelt, K. L. Hughes, J. R. Schwank, F. W. Sexton, D. M. Fleetwood, and P. S. Winokur, "Wafer-Level Radiation Testing for Hardness Assurance," IEEE Trans. Nucl. Sci. NS-38, 1598 (1991).

[17] F. B. McLean and T. R. Oldham, "Basic Mechanisms of Radiation Effects in Electronic Materials and Devices," Harry Diamond Laboratories Technical Report, No. HDL-TR-2129, September 1987.

[18] R. D. Evans, The Atomic Nucleus, McGraw-Hill, New York, 1955.

[19] J. R. Srour, "Basic Mechanisms of Radiation Effects on Electronic Materials, Devices, and Integrated Circuits," Defense Nuclear Agency technical report, DNA-TR-82-20 (August 1982).

[20] J. R. Srour, "Basic Mechanisms of Radiation Effects on Electronic Materials, Devices, and Integrated Circuits," 1983 IEEE Nuclear and Space radiation Effects Conference Short Course, Gatlinburg, Tennessee (July 1983).

[21] See, for example, S. M. Sze, Physics of Semiconductor Devices, Wiley, New York, 1981.

[22] D. M. Fleetwood, P. S. Winokur, R. W. Beegle, P. V. Dressendorfer, and B. L. Draper, "Accounting for Dose-Enhancement Effects with CMOS Transistors," IEEE Trans. Nucl. Sci. NS-32, 4369 (1985).

[23] T. R. Oldham and J. M. McGarrity, "Comparison of ^{60}Co Response in MOS Capacitors," IEEE Trans. Nucl. Sci. NS-30, 4377 (1983).

[24] C. M. Dozier and D. B. Brown, "The use of Low Energy X-Rays for Device Testing — A Comparison with Co-60 Radiation," IEEE Trans. Nucl. Sci. NS-30, 4382 (1983).

[25] J. M. Benedetto, H. E. Boesch, Jr., and T. R. Oldham, "Measurement of Low-Energy Dose-Enhancement in MOS Devices with Metal Silicon Gates," IEEE Trans. Nucl. Sci. NS-34, 1540 (1987).

[26] G. P. Summers, "Displacement Damage: Mechanisms and Measurements," 1992 IEEE Nuclear Space and Radiation Effects Conference Short Course, New Orleans, Louisiana (July 1992).

[27] J. R. Srour, "Displacement Damage Effects in Electronic Materials, Devices, and Integrated Circuits," 1988 IEEE Nuclear and Space Radiation Effects Conference Short Course, Portland, Oregon (July 1988).

[28] J. R. Srour and J. M. McGarrity, "Radiation Effects on Microelectronics in Space," Proc. of the IEEE 76, 1443 (1988).

[29] P. S. Winokur, J. R. Schwank, P. J. McWhorter, P. V. Dressendorfer, and D. C. Turpin, "Correlating the Radiation Response of MOS Capacitors and Transistors," IEEE Trans. Nucl. Sci. NS-31, 1453 (1984).

[30] P. J. McWhorter, P. S. Winokur, and R. A. Pastorek, "Donor/Acceptor Nature of Radiation-Induced Interface Traps," IEEE Trans. Nucl. Sci. NS-35, 1154 (1988).

[31] Y. Y. Kim and P. M. Lenahan, "Electron-Spin Resonance Study of Radiation-Induced Paramagnetic Defects in Oxides Grown on (100) Silicon Substrates," J. Appl. Phys. 64, 3551 (1988).

[32] D. M. Fleetwood, "Long-Term Annealing Study of Midgap Interface-Trap Charge Neutrality," Appl. Phys. Lett. 60, 2883 (1992).

[33] J. R. Schwank, D. M. Fleetwood, M. R. Shaneyfelt, and P. S. Winokur, "A Critical Comparison of Charge-Pumping, Dual-Transistor, and Midgap Measurement Techniques," IEEE Trans. Nucl. Sci. NS-40, 1666 (1993).

[34] G. Groeseneken, H. E. Maes, N. Beltran, and R. DeKeersmaecker, "A Reliable Approach to Charge-Pumping Measurements in MOS Transistors," IEEE Trans. Electron Dev. ED-31, 42 (1984).

[35] N. S. Saks and M. G. Ancona, "Generation of Interface States by Ionizing Radiation at 80 K Measured by Charge Pumping and Subthreshold Slope Techniques," IEEE Trans. Nucl. Sci. NS-34, 1348 (1987).

[36] M. Gaitan and T. J. Russell, "Measurement of Radiation-Induced Interface Traps Using MOSFETs," IEEE Trans. Nucl. Sci. NS-31, 1256 (1984).

[37] K. F. Galloway, M. Gaitan, and T. J. Russell, "A Simple Method for Separating Interface and Oxide Charge Effects in MOS Device Characteristics," IEEE Trans. Nucl. Sci. NS-31, 1497 (1984).

[38] D. M. Fleetwood, "Dual-Transistor Method to Determine Threshold-voltage shifts due to Oxide-Trapped Charge and Interface-Traps in MOS Devices," Appl. Phys. Lett. 55, 466 (1989).

[39] D. M. Fleetwood, M. R. Shaneyfelt, J. R. Schwank, P. S. Winokur, and F. W. Sexton, "Theory and Application of Dual-Transistor Charge Separation Analysis," IEEE Trans. Nucl. Sci. NS-36, 1816 (1989).

[40] W. Chen, A. Balasinski, and T. P. Ma, "Evolution of Capture Cross-Section of Radiation-Induced Interface Traps in MOSFETs as Studied by a Rapid Charge Pumping Technique," IEEE Trans. Nucl. Sci. NS-39, 2152 (1992).

[41] J. S. Brugler and P. G. A. Jespers, "Charge Pumping in MOS Devices," IEEE Trans. Nucl. Sci. NS-16, 297 (1969)

[42] R. E. Stahlbush, R. K. Lawrence, and W. Richards, "Geometric Components of Charge Pumping Current in SOS Devices," IEEE Trans. Nucl. Sci. NS-36, 1990 (1989).

[43] See, for example, P. W. Atkins and M. C. R. Symons, *The Structure of Inorganic Radicals; An Application of Electron Spin Resonance to the Study of Molecular Structure*, Elsevier Publishing Company, New York, 1967.

[44] W. L. Warren, E. H. Poindexter, M. Offenberg, W. Muller-Warmuth, "Paramagnetic Point Defects in Amorphous Silicon Dioxide and Amorphous Silicon Nitride Thin Films," J. Electrochem. Soc. 139, 872 (1992).

[45] R. C. Hughes, "Hole Mobility and Transport in Thin SiO_2 Films," Appl Phys. Lett. 26, 436 (1975).

[46] R. C. Hughes, "Charge Carrier Transport Phenomena in Amorphous SiO_2: Direct Measurement of the Drift Mobility and Lifetime," Phys. Rev. Lett 30, 1333 (1973).

[47] F. B. McLean, H. E. Boesch, Jr., and T. R. Oldham, "Electron-Hole Generation, Transport, and Trapping in SiO_2," in Ionizing Radiation Effects in MOS Devices and Circuits, edited by T. P. Ma and Paul V. Dressendorfer, John Wiley & Sons, New York, pp. 87-192, 1989.

[48] M. R. Shaneyfelt, D. M. Fleetwood, J. R. Schwank, and K. L. Hughes, "Charge Yield for Cobalt-60 and 10-keV X-Ray Irradiations," IEEE Trans. Nucl. Sci. NS-38, 1187 (1991).

[49] Charles Kittel, Introduction to Solid State Physics, John Wiley & Sons, New York, 1968, pp 329-330.

[50] F. B. McLean and G. A. Ausman, Jr., "Simple Approximate Solutions to Continuous-Time Random-Walk Transport," Phys. Rev. B 15, 1052 (1977).

[51] F. B. McLean, G. A. Ausman, Jr., H. E. Boesch, Jr., and J. M. McGarrity, "Application of Stochastic Hoping Transport to Hole Conduction in Amorphous SiO_2," J. Appl. Phys. 47, 1529 (1976).

[52] H. E. Boesch, Jr., J. M. McGarrity, and F. B. McLean, "Temperature- and Field-Dependent Charge Relaxation in SiO_2 Gate Insulators," IEEE Trans. Nucl. Sci. NS-25, 1012 (1978).

[53] H. E. Boesch, Jr., F. B. McLean, J. M. McGarrity, and P. S. Winokur, "Enhanced Flatband Voltage Recovery in Hardened Thin MOS Capacitors," IEEE Trans. Nucl. Sci. NS-25, 1239 (1978).

[54] W. L. Warren, M. R. Shaneyfelt, D. M. Fleetwood, J. R. Schwank, P. S. Winokur, R. A. B. Devine, and D. Mathiot, "Correlations Between Oxide-, Interface-, and Border-Trap Charge in High-Temperature Annealed $Si/SiO_2/Si$ Systems," IEEE Trans. Nucl. Sci. NS-41 (submitted for publication).

[55] M. R. Shaneyfelt, J. R. Schwank, D. M. Fleetwood, P. S. Winokur, K. L. Hughes, and F. W. Sexton, "Field Dependence of Interface-Trap Buildup in Polysilicon and Metal Gate MOS Devices," IEEE Trans. Nucl. Sci. NS-37, 1632 (1990).

[56] C. M. Dozier and D. B. Brown, "Photon Energy Dependence of Radiation Effects in MOS Structures," IEEE Trans. Nucl. Sci. NS-27, 1694 (1980).

[57] C. M. Dozier and D. B. Brown, "Effects of Photon Energy on the Response of MOS Devices," IEEE Trans. Nucl. Sci. NS-28, 4137 (1981).

[58] D. B. Brown and C. M. Dozier, "Electron-Hole Recombination in Irradiated SiO_2 From a Microdosimetry Viewpoint," IEEE Trans. Nucl. Sci. NS-28, 4142 (1981).

[59] C. M. Dozier, D. M. Fleetwood, D. B. Brown, and P. S. Winokur, "An Evaluation of Low-Energy X-Ray and Cobalt-60 Irradiations of MOS Transistors," IEEE Trans. Nucl. Sci. NS-34, 1535 (1987).

[60] J. R. Srour, O. L. Curtice, Jr., and K. Y. Chiu, "Charge Transport Studies in SiO_2: Processing Effects and Implications for Radiation Hardening," IEEE Trans. Nucl. Sci. NS-21, 73 (1974).

[61] D. M. Fleetwood, P. S. Winokur, and J. R. Schwank, "Using Laboratory X-Ray and Co-60 Irradiations to Predict CMOS Device Response in Strategic and Space Environments," IEEE Trans. Nucl. Sci. NS-35, 1497 (1988).

[62] T. R. Oldham, A. J. Lelis, and F. B. McLean, "Spatial Dependence of Trapped Holes Determined From Tunneling Analysis and Measured Annealing," IEEE Trans. Nucl. Sci. NS-33, 1203 (1986).

[63] P. S. Winokur, K. G. Kerris, and L. Harper, "Predicting CMOS Inverter Response in Nuclear and Space Environments," IEEE Trans. Nucl. Sci. NS-30, 4326 (1983).

[64] F. B. McLean, "Generic Impulse Response Function for MOS Systems and Its Application to Linear Response Analysis," IEEE Trans. Nucl. Sci. NS-35, 1178 (1988).

[65] W. J. Stapor, J. P. Meyers, J. D. Kinnison, and B. G. Carkhuff, "Low Dose Rate Space Estimates for Integrated Circuits Using Real Time Measurements and Linear System Theory," IEEE Trans. Nucl. Sci. NS-39, 1876 (1992).

[66] D. M. Fleetwood, P. S. Winokur, and T. L. Meisenheimer, "Hardness Assurance for Low-Dose Space Applications," IEEE Trans. Nucl. Sci. NS-38, 1552 (1991).

[67] J. R. Schwank, P. S. Winokur, P. J. McWhorter, F. W. Sexton, P. V. Dressendorfer, and D. C. Turpin, "Physical Mechanisms Contributing to Device Rebound," IEEE Trans. Nucl. Sci. NS-31, 1434 (1984).

[68] G. F. Derbenwick and H. H. Sander, "CMOS Hardness for Low-Dose-Rate Environments," IEEE Trans. Nucl. Sci. NS-24, 2244 (1977).

[69] A. J. Lelis, H. E. Boesch, Jr., T. R. Oldham, and F. B. McLean, "Reversibility of Trapped Hole Charge," IEEE Trans. Nucl. Sci. NS-35, 1186 (1988).

[70] A. J. Lelis, T. R. Oldham, and W. M. DeLancey, "Response of Interface Traps During High-Temperature Anneals," IEEE Trans. Nucl. Sci NS-38, 1590 (1991).

[71] A. J. Lelis, T. R. Oldham, H. E. Boesch, Jr., and F. B. McLean, "The Nature of the Trapped Hole Annealing Process," IEEE Trans. Nucl. Sci. NS-36, 1808 (1989).

[72] S. Kuboyama, T. Goka, and T. Tamura, "A Bias Voltage Dependence of Trapped Hole Annealing and Its Measurement Technique," IEEE Trans. Nucl. Sci. NS-38, 1140 (1991).

[73] D. M. Fleetwood, M. R. Shaneyfelt, L. C. Riewe, P. S. Winokur, and R. A. Reber, Jr., "The Role of Border Traps in MOS High-Temperature Postirradiation Annealing Response," IEEE Trans. Nucl. Sci. NS-40, 1323 (1993).

[74] D. M. Fleetwood, S. L. Miller, R. A. Reber, Jr., P. J. McWhorter, P. S. Winokur, M. R. Shaneyfelt, and J. R. Schwank, "New Insights into Radiation-Induced Oxide-Trap Charge Through Thermally-Stimulated-Current (TSC) Measurement and Analysis," IEEE Trans. Nucl. Sci. NS-39, 2192 (1992).

[75] Z. Shanfield, "TSC Measurements of Irradiated MOS Capacitors," IEEE Trans. Nucl. Sci. NS-30, 4064 (1983).

[76] P. J. McWhorter, S. L. Miller, and W. M. Miller, "Modeling the Anneal of Radiation-Induced Trapped Holes in a Varying Thermal Environment," IEEE Trans. Nucl. Sci. NS-37, 1682 (1990).

[77] F. B. McLean, "A Direct Tunneling Model of Charge Transfer at the Insulator-Semiconductor Interface in MIS Devices," HDL Report No. HDL-TR-1765, October 1976.

[78] S. Manzini and A. Modelli, "Tunneling Discharge of Trapped Holes in Silicon Dioxide," in Insulating Films on Semiconductors eds. J. F. Verweij and D. R. Wolters, Elsevier Science, 1983, pp. 112-115.

[79] M. Schmidt and K. Koster, Jr. "Hole Trap Analysis in SiO_2/Si Structures by Electron Tunneling," Phys. Stat. Sol. B 174, 53 (1992).

[80] P. J. McWhorter, S. L. Miller, and T. A. Dellin, "Modeling the Memory Retention Characteristics of SNOS Transistors in a Varying Thermal Environment," J. Appl. Phys. 68, 1902 (1990).

[81] B. Ballard and G. Barbottin, Instabilities in Silicon Devices, Vol. 2, (Elsevier Science Publishers, New York, 1989) p. 32.

[82] P. M. Lenahan and P. V. Dressendorfer, "Hole Traps and Trivalent Silicon Centers in Metal/Oxide/Silicon Devices, J. Appl. Phys. 55, 3495 (1984).

[83] P. M. Lenahan and P. V. Dressendorfer, "Radiation-Induced Paramagnetic Defects in MOS Structures," IEEE Trans. Nucl. Sci. NS-29, 1459 (1982).

[84] P. M. Lenahan and P. V. Dressendorfer, "Microstructural Variations in Radiation Hard and Soft Oxides Observed Through Electron Spin Resonance," IEEE Trans. Nucl. Sci. NS-30, 4602 (1983).

[85] P. M. Lenahan, K. L. Brower, P. V. Dressendorfer, and W. C. Johnson, "Radiation-Induced Trivalent Silicon Defect Buildup at the Si-SiO_2 Interface in MOS Structures," IEEE Trans. Nucl. Sci. NS-28, 4105 (1981).

[86] T.-E. Tsai, D. L. Griscom, and E. J. Friebele, "Si E' Centers and UV-Induced Compaction in High Purity Silica," Nucl. Instrum. Meth. B46, 265 (1990).

[87] R. A. B. Devine. D. Mathiot, W. L. Warren, D. M. Fleetwood, and B. Aspar, "Point Defect Generation During High Temperature Annealing of the Si-SiO_2 Interface," Appl. Phys. Lett. 63, 2926 (1973).

[88] T. Takahashi, B. B. Triplett, K. Yokogawa, and T. Sugano, "Electron Spin Resonance Observation of the Creation, Annihilation, and Charge State of the 74-Gauss Doublet in Device Oxides Damaged by Soft X Rays," Appl. Phys. Lett. 51, 1334 (1987).

[89] B. B. Triplett, T. Takahashi, and T. Sugano, "Electron Spin Resonance Observation of Defects in Device Oxides Damaged by Soft X Rays," Appl. Phys. Lett. 50, 1663 (1987).

[90] J. F. Conley and P. M. Lenahan, "Room Temperature Reactions Involving Silicon Dangling Bond Centers and Molecular Hydrogen in Amorphous SiO_2 Thin Films," IEEE Trans. Nucl. Sci. NS-39, 2186 (1992).

[91] W. L. Warren, M. R. Shaneyfelt, J. R. Schwank, D. M. Fleetwood, P. S. Winokur, R. A. B. Devine, W. P. Maszara, and J. B. McKitterick, "Paramagnetic Defect Centers in BESOI and SIMOX Buried Oxides," IEEE Trans. Nucl. Sci. NS-40, 1755 (1993).

[92] H. S. Witham and P. M. Lenahan, "Nature of the E' Deep Hole Trap in Metal-Oxide-Semiconductor Oxides," Appl. Phys. Lett. 51 1007 (1987).

[93] J. F. Conley, P. M. Lenahan, and P. Roitman, "Electron Spin Resonance Study of E' Trapping Centers in SIMOX Buried Oxides," IEEE Trans. Nucl. Sci. NS-38, 1247 (1991).

[94] D. Herve, J. L. Leray, and R. A. B. Devine, "Comparative Study of Radiation-Induced Electrical and Spin Active Defects in Buried SiO_2 Layers," J. Appl. Phys. 72, 3634 (1992).

[95] P. S. Winokur, "Radiation-Induced Interface Traps," in Ionizing Radiation Effects in MOS Devices and Circuits, edited by T. P. Ma and Paul V. Dressendorfer, John Wiley & Sons, New York, pp. 193-255, 1989.

[96] J. R. Schwank, P. S. Winokur, F. W. Sexton, D. M. Fleetwood, J. H. Perry, P. V. Dressendorfer, D. T. Sanders, and D. C. Turpin, "Radiation-Induced Interface-State Generation in MOS Devices," IEEE Trans. Nucl. Sci. NS-33, 1178 (1986).

[97] N. S. Saks, C. M. Dozier, and D. B. Brown, "Time Dependence of Interface Trap Formation in MOSFETs Following Pulsed Irradiation," IEEE Trans. Nucl. Sci. NS-35, 1168 (1988).

[98] H. E. Boesch, Jr., "Time-Dependent Interface Trap Effects in MOS Devices," IEEE Trans. Nucl. Sci. NS-35, 1160 (1988).

[99] J. M. McGarrity, P. S. Winokur, H. E. Boesch, Jr., and F. B. McLean, "Interface States Resulting from a Hole Flux Incident on the SiO_2/Si Interface," Physics of SiO_2 and Its Interfaces, 1978, pp. 428-432.

[100] M. R. Shaneyfelt, J. R. Schwank, D. M. Fleetwood, P. S. Winokur, K. L. Hughes, and G. L. Hash, "Interface-Trap Buildup Rates in Wet and Dry Oxides," IEEE Trans. Nucl. Sci. NS-39, 2244 (1992).

[101] N. S. Saks, D. B. Brown, and R. W. Rendell, "Effects of Switched Bias on Radiation-Induced Interface Trap Formation," IEEE Trans. Nucl. Sci. NS-38, 1130 (1991).

[102] P. S. Winokur, H. E. Boesch, Jr., J. M. McGarrity, and F. B. McLean, "Field- and Time-Dependent Radiation Effects at the Si/SiO_2 Interface of Hardened MOS Capacitors," IEEE Trans. Nucl. Sci. NS-24, 2113 (1977).

[103] N. S. Saks, R. B. Klein, and D. L. Griscom, "Formation of Interface Traps in MOSFETs During Annealing Following Low Temperature Irradiation," IEEE Trans. Nucl. Sci. NS-35, 1234 (1988).

[104] J. R. Schwank, F. W. Sexton, D. M. Fleetwood, R. V. Jones, R. S. Flores, M. S. Rodgers, and K. L. Hughes, "Temperature Effects on the Radiation Response of MOS Devices," IEEE Trans. Nucl. Sci. NS-35, 1432 (1988).

[105] D. M. Fleetwood, F. V. Thome, S. S. Tsao, P. V. Dressendorfer, V. J. Dandini, and J. R. Schwank, "High-Temperature Silicon-On-Insulator Electronics for Space Nuclear Power Systems: Requirements and Feasibility," IEEE Trans. Nucl. Sci. NS-35, 1099 (1988).

[106] P. S. Winokur, E. B. Errett, D. M. Fleetwood, P. V. Dressendorfer, and D. C. Turpin, "Optimizing and Controlling the Radiation Hardness of a Si-Gate CMOS Process," IEEE Trans. Nucl. Sci. NS-32, 3954 (1985).

[107] J. R. Schwank, D. M. Fleetwood, M. R. Shaneyfelt, and P. S. Winokur, "Latent Thermally Activated Interface-Trap Generation in MOS Devices," Electron Device Letters EDL-13, No. 4, 203 (April 1992).

[108] J. R. Schwank, D. M. Fleetwood, M. R. Shaneyfelt, P. S. Winokur, C. L. Axness, and L. C. Riewe, "Latent Interface-Trap Buildup and Its Implication for Hardness Assurance," IEEE Trans. Nucl. Sci. NS-39, 1953 (1992).

[109] D. L. Griscom, "Diffusion of Radiolytic Molecular Hydrogen as a Mechanism for the Post-Irradiation Buildup of Interface States in SiO_2-on-Si Structures," J. Appl. Phys. 58, 2524 (1985).

[110] D. M. Fleetwood, "'Border Traps' in MOS Devices," IEEE Trans. Nucl. Sci. NS-39, 269 (1992).

[111] B. J. Mrstik and R. W. Rendell, "Si-SiO_2 Interface State Generation During X-Ray Irradiation and During Post-Irradiation Exposure to a Hydrogen Ambient," IEEE Trans. Nucl. Sci. NS-38, 1101 (1991).

[112] P. S. Winokur, F. W. Sexton, J. R. Schwank, D. M. Fleetwood, P. V. Dressendorfer, T. F. Wrobel, and D. C. Turpin, "Total-Dose Radiation and Annealing Studies: Implications for Hardness Assurance Testing," IEEE Trans. Nucl. Sci. NS-33, 1343 (1986).

[113] P. S. Winokur, H. E. Boesch, Jr., J. M. McGarrity, and F. B. McLean, "Two-Stage Process for Buildup of Radiation-Induced Interface States," J. Appl. Phys. 50, 3492 (1979).

[114] D. M. Fleetwood, P. V. Dressendorfer, and D. C. Turpin, "A Reevaluation of the Worst-Case Postirradiation Response for Hardened MOS Transistors," IEEE Trans. Nucl. Sci. NS-34, 1178 (1987).

[115] D. M. Fleetwood, F. V. Thome, S. S. Tsao, P. V. Dressendorfer, V. J. Dandini, and J. R. Schwank, "High-Temperature Silicon-On-Insulator Electronics for Space Nuclear Power Systems: Requirements and Feasibility," IEEE Trans. Nucl. Sci. NS-35, 1099 (1988).

[116] P. S. Winokur and M. M. Sokoloski, "Comparison of Interface State Buildup in MOS Capacitors Subjected to Penetrating and Nonpenetrating Radiation," Appl. Phys. Lett. 28, 627 (1976).

[117] P. S. Winokur, J. M. McGarrity, and H. E. Boesch, Jr., "Dependence of Interface-State Buildup on Hole Generation and Transport in Irradiated MOS Capacitors," IEEE Trans. Nucl. Sci. NS-23, 1580 (1976).

[118] R. J. Powell and G. F. Derbenwick, "Vacuum Ultraviolet Radiation Effects in SiO_2," IEEE Trans. Nucl. Sci. NS-18, 99 (1971).

[119] C. M. Svensson, "The Defect Structure of the Si-SiO_2 Interface, A Model Based on Trivalent Silicon and Its Hydrogen 'Compounds'," in *The Physics of SiO_2 and Its Interfaces*, S. T. Pantelides, Ed., Pergamon Press, Elmsford, 1978, pp. 328-332.

[120] F. B. McLean, "A Framework for Understanding Radiation-Induced Interface States in SiO_2 MOS Structures," IEEE Trans. Nucl. Sci. NS-27, 1651 (1980).

[121] N. S. Saks and D. B. Brown, "Observation of H^+ Motion During Interface Trap Formation," IEEE Trans. Nucl. Sci. NS-37, 1624 (1990).

[122] N. S. Saks and R. W. Rendell, "The Time-Dependence of Post-Irradiation Interface Trap Buildup in Deuterium-Annealed Oxides," IEEE Trans. Nucl. Sci. NS-39, 2220 (1992).

[123] M. Pepper, "Low Energy Electron Irradiation of the Si-SiO_2 Interface," Thin Solid Films 14, S7 (1972).

[124] N. S. Saks, D. B. Brown, and R. W. Rendell, "Effects of Switched Gate Bias on Radiation-Induced Interface-Trap Formation," IEEE Trans. Nucl. Sci. NS-38, 1130 (1991).

[125] A. G. Revesz, "Hydrogen in SiO_2 Films on Silicon," in *The Physics of SiO_2 and Its Interfaces*, S. T. Pantelides, Ed., Pergamon Press, Elmsford, 1978, pp. 222-226.

[126] J. R. Schwank, D. M. Fleetwood, P. S. Winokur, P. V. Dressendorfer, D. C. Turpin, and D. T. Sanders, "The Role of Hydrogen in Radiation-Induced Defect Formation in Polysilicon Gate MOS Devices," IEEE Trans. Nucl. Sci. NS-34, 1152 (1987).

[127] D. B. Brown and N. S. Saks, "Time-Dependence of Radiation-Induced Interface Trap Formation in Metal-Oxide-Semiconductor Devices as a Function of Oxide Thickness and Applied Field," J. Appl. Phys. 70, 3734 (1991).

[128] A. G. Revesz, "Chemical and Structural Aspects of the Irradiation Behavior of SiO_2 Films on Silicon," IEEE Trans. Nucl. Sci. NS-24, 2102 (1977).

[129] D. L. Griscom, "Hydrogen Model for Radiation-Induced Interface States in SiO_2 Structures: A Review of the Evidence," J. Electron. Mat. 21, 763 (1992).

[130] P. M. Lenahan and P. V. Dressendorfer, "An Electron Spin Resonance Study of Radiation-Induced Electrically Active Paramagnetic Centers at the Si/SiO_2 Interface," J. Appl. Phys. 54, 1457 (1983).

[131] P. M. Lenahan and P. V. Dressendorfer, "Effect of Bias on Radiation-Induced Paramagnetic Defects at the Silicon-Silicon Dioxide Interface," Appl. Phys. Lett. 41, 542 (1982).

[132] Y. Nishi, "Electron Spin resonance in SiO_2 Grown on Silicon," Japan. J. Appl. Phys. 5, 333 (1966).

[133] Y. Nishi, "Study of Silicon-Silicon Dioxide Structure by Electron Spin Resonance I," Japan. J. Appl. Phys. 10, 52 (1971).

[134] P. J. Caplan, E. H. Poindexter, B. E. Deal, and R. R. Razouk, "ESR Centers, Interface States, and Oxide Fixed Charge in Thermally Oxidized Silicon Wafers," J. Appl. Phys. 50, 5847 (1979).

[135] E. H. Poindexter, P. J. Caplan, B. E. Deal, R. R. Razouk, "Interface States and Electron Spin Resonance Centers in Thermally Oxidized (111) and (100) Silicon Wafers," J. Appl. Phys. 52, 879 (1981).

[136] G. J. Gerardi, E. H. Poindexter, P. J. Caplan, and N. M. Johnson, "Interface Traps and P_b Centers in Oxidized (100) Silicon Wafers," Appl. Phys. Lett. 49, 348 (1986).

[137] A. H. Edwards, "Theory of Defects in the MOS System," in The Physics and Chemistry of SiO_2 and the Si/SiO_2 Interface, C. R. Helms and B. F. Deal, editors (Plenum, New York), p. 271 (1988).

[138] K. L. Brower, "Electron Paramagnetic Resonance Studies of $Si-SiO_2$ Interface Defects," Semiconductor Science and Technology 4, 970 (1989).

[139] J. M. Benedetto, H. E. Boesch, Jr., F. B. McLean, and J. P. Mize, "Hole Removal in Thin-Gate MOSFETs by Tunneling," IEEE Trans. Nucl. Sci. NS-32, 3916 (1985).

[140] D. M. Fleetwood, P. S. Winokur, R. A. Reber, Jr., T. L. Meisenheimer, J. R. Schwank, M. R. Shaneyfelt, and L. C. Riewe, "Effects of Oxide Traps, Interface Traps, and "Border Traps" on Metal-Oxide-Semiconductor Devices," J. Appl. Phys. 73, 5058 (May 1993).

[141] D. M. Fleetwood, M. R. Shaneyfelt, and J. R. Schwank, "Simple Method to Estimate Oxide-Trap, Interface-Trap, and Border-Trap Charge Densities in Metal-Oxide-Semiconductor Transistors," Appl. Phys. Lett. 64, 1965 (1994).

[142] R. E. Paulsen, R. R. Siergiej, M. L. French, and M. H. White, "Observation of Near-Interfacial Oxide Traps With the Charge-Pumping Technique," IEEE Electron Dev. Lett. EDL-13, 627 (1992).

[143] M. J. Uren, S. Collins, and M. J. Kirton, "Observation of Slow States in Conductance Measurements on Si MOS Capacitors," Appl. Phys. Lett. 54, 1448 (1990).

[144] J. J. Simone, G. Blasquez, and G. Barbottin, "1/*f* Noise in MOSFETs," in Instabilities in Silicon Devices: Silicon Passivation and Related Instabilities, vol. 2, Amsterdam, Elsevier, 1989, pp. 639-657.

[145] D. M. Fleetwood and J. H. Scofield, "Evidence That Similar Point Defects Cause 1/*f* Noise and Radiation-Induced Hole Trapping in MOS Transistors," Phys. Rev. Lett. 64, 579 (1990).

[146] T. L. Meisenheimer and D. M. Fleetwood, "Effect of Radiation-Induced Charge on 1/*f* Noise in MOS Devices," IEEE Trans. Nucl. Sci. NS-37, 1696 (1990).

[147] P. J. Restle, "Individual Oxide Traps as Probes Into Submicron Devices," Appl. Phys. Lett. 53, 1862 (1988).

[148] M. J. Kirton and M. J. Uren, "Noise in Solid-State Microstructures; A New Perspective on Individual Defects, Interface States, and Low-Frequency (1/*f*) Noise," Advances in Physics 38, 367 (1989).

[149] C. T. Sah and F. H. Hielscher, "Evidence of the Surface Origin of the 1/*f* Noise," Phys. Rev. Lett. 17, 956 (1966).

[150] E. H. Nicollian and J. R. Brews, MOS Physics and Technology, New York, Wiley, 1982, pp. 775-798.

[151] D. M. Fleetwood, P. S. Winokur, L. C. Riewe, and R. L. Pease, "An Improved Standard Total Dose Test for CMOS Space Electronics," IEEE Trans. Nucl. Sci. NS-36, 1963 (1989).

[152] J. R. Schwank and W. R. Dawes, Jr., "Irradiated Silicon Gate MOS Device Bias Annealing," IEEE Trans. Nucl. Sci. NS-30, 4100 (1983).

[153] J. R. Schwank, P. S. Winokur, W. R. Dawes, Jr., and F. W. Sexton, "Implications for Rebound for IC Radiation Hardness," Government Microcircuit Applications Conference Digest of Papers, Las Vegas, NV, 1984, pp. 438-442.

[154] F. W. Sexton and J. R. Schwank, "Correlation of Radiation Effects in Transistors and Integrated Circuits," IEEE Trans. Nucl. Sci. NS-32, 3975 (1985).

[155] S. C. Sun and J. D. Plummer, "Electron Mobility in Inversion and Accumulation Layers on Thermally Oxidized Silicon Surfaces," IEEE Trans. Electron Dev. ED-27, 1497 (1980).

[156] F. B. McLean, "Time-Dependent Degradation of MOSFET Channel Mobility Following Pulsed Irradiation," IEEE Trans. Nucl. Sci. NS-36, 1772 (1989).

[157] D. Zupac, K. F. Galloway, P. Khosropour, S. R. Anderson, R. D. Schrimpf, and P. Calvel, "Separation of Effects of Oxide-Trapped Charge and Interface-Trap Charge on Mobility in Irradiated Power MOSFETs," IEEE Trans. Nucl. Sci. NS-40, 1307 (1993).

[158] MIL-STD 883D Test Method 1019.4, issued January 1992 by the Defense Electronics Support Center, Dayton, Ohio.

[159] P. S. Winokur, M. R. Shaneyfelt, T. L. Meisenheimer, and D. M. Fleetwood, "Advanced Qualification Techniques," Radiation: Effects on Components and Systems (RADECS) 93, Saint Malo, France (accepted for publication).

[160] D. M. Fleetwood, P. S. Winokur, C. E. Barnes, and D. C. Shaw, "Accounting for Time-Dependent Effects on CMOS Total-Dose Response in Space Environments," Radiat. Phys. Chem. 43, 129 (1994).

[161] P. S. Winokur, F. W. Sexton, D. M. Fleetwood, D. M. Terry, M. R. Shaneyfelt, P. V. Dressendorfer, and J. R. Schwank, "Implementing QML for Radiation Hardness Assurance," IEEE Trans. Nucl. Sci. NS-37, 1794 (1990).

[162] P. V. Dressendorfer, "Radiation Effects on MOS Devices and Circuits," in Ionizing Radiation Effects in MOS Devices and Circuits, edited by T. P. Ma and Paul V. Dressendorfer, John Wiley & Sons, New York, pp. 256-332, 1989.

[163] K. Naruke, M. Yoshida, K. Maeguchi, and H. Tango, "Radiation-Induced Interface States of Poly-Si gate MOS Capacitors Using Low Temperature Gate Oxidation," IEEE Trans. Nucl. Sci. NS-30, 4054 (1983).

[164] N. S. Saks, M. G. Ancona, and J. A. Modolo, "Radiation Effects in MOS Capacitors With Very Thin Oxides at 80 K," IEEE Trans. Nucl. Sci. NS-31, 1249 (1984).

[165] H. E. Boesch, Jr., "Interface-State Generation in Thick SiO_2 Layers," IEEE Trans. Nucl. Sci. NS-29, 1446 (1982).

[166] H. E. Boesch, Jr. and F. B. McLean, "Hole Transport and Trapping in Field Oxides," IEEE Trans. Nucl. Sci. NS-32, 3940 (1985).

[167] T. R. Oldham, A. J. Lelis, H. E. Boesch, J. M. Benedetto, F. B. McLean, and J. M. McGarrity, "Post-Irradiation Effects in Field-Oxide Isolation Structures," IEEE Trans. Nucl. Sci. NS-34, 1184 (1987).

[168] T. P. Ma, "Process-Induced Radiation Effects," in Ionizing Radiation Effects in MOS Devices and Circuits, edited by T. P. Ma and Paul V. Dressendorfer, John Wiley & Sons, New York, pp. 401-442, 1989.

[169] P. A. Miller, D. M. Fleetwood, and W. K. Schubert, "Damage Due to Electron, Ion, and X-Ray Lithography," J. Appl. Phys. 69, 488 (1991).

[170] R. A. Kjar and J. Peel, "Radiation-Induced Leakage Current in n-Channel SOS Transistors," IEEE Trans. Nucl. Sci. NS-21, 2081 (1974).

[171] L. S. Napoli, R. K. Smeltzer, J. L. Yeh, and W. F. Heagerty, "CMOS/SOS 4K RAMs Hardened to 100 krads(Si)," IEEE Trans. Nucl. Sci. NS-29, 1707 (1982).

[172] S. S. Tsao, D. M. Fleetwood, and H. T. Weaver, "Radiation-Tolerant, Sidewall-Hardened SOI/MOS Transistors," IEEE Trans. Nucl. Sci. NS-34, 1686 (1987).

[173] D. M. Fleetwood, S. S. Tsao, and P. S. Winokur, "Total-Dose Hardness Assurance Issues for SOI MOSFETs," IEEE Trans. Nucl. Sci. NS-35, 1361 (1988).

[174] B.-Y. Mao, C.-E. Chen, M. Matloubian, L. R. Hite, G. Pollack, H. L. Hughes, and K. Maley, "Total Dose Characterization of CMOS Devices in Oxygen Implanted Silicon-on-Insulator," IEEE Trans. Nucl. Sci. NS-33, 1702 (1986).

[175] H. E. Boesch, Jr. and T. L. Taylor, "Time-Dependent Radiation-Induced Charge Effects in Wafer-Bonded SOI Buried Oxides," IEEE Trans. Nucl. Sci. NS-39, 2103 (1992).

[176] H. E. Boesch, Jr., T. L. Taylor, L. R. Hite, and W. E. Bailey, "Time-Dependent Hole and Electron Trapping Effects in SIMOX Buried Oxides," IEEE Trans. Nucl. Sci. NS-37, 1982 (1992).

[177] C. A. Pennise and H. E. Boesch, Jr., "Determination of the Charge-Trapping Characteristics of Buried Oxides Using a 10-keV X-Ray Source," IEEE Trans. Nucl. Sci. NS-37, 1990 (1990).

[178] H. E. Boesch, Jr., T. L. Taylor, and G. A. Brown, "Charge Buildup at High Dose and Low Fields in SIMOX Buried Oxides," IEEE Trans. Nucl. Sci. NS-38, 1234 (1991).

[179] C. A. Pennise and H. E. Boesch, Jr., "Thermal Annealing of Trapped Holes in SIMOX Buried Oxides," IEEE Trans. Nucl. Sci. NS-38, 1240 (1991).

[180] R. E. Stahlbush, G. J. Campisi, J. B. McKitterick, W. P. Maszara, P. Roitman, and G. A. Brown, "Electron and Hole Trapping in Irradiated SIMOX, ZMR, and BESOI Buried Oxides," IEEE Trans. Nucl. Sci. NS-39, 2086 (1992).

[181] C. A. Pennise, H. E. Boesch, Jr., G. Goetz, and J. B. McKitterick, "Radiation-Induced Charge Effects in Buried Oxides with Different Processing Treatments," IEEE Trans. Nucl. Sci. NS-40, 1765 (1993).

[182] J. B. McKitterick, A. Caviglia, and W. P. Maszara, "Total Dose Hardness of Bonded SOI Wafers," IEEE Trans. Nucl. Sci. NS-39, 2098 (1992).

[183] M. E. Zvanut, R. E. Stahlbush, W. E. Carlos, H. L. Hughes, R. K. Lawrence, R. Hevey, and G. A. Brown, "SIMOX With Epitaxial Silicon: Point Defects and Positive Charge," IEEE Trans. Nucl. Sci. NS-38, 1253 (1991).

[184] R. A. B. Devine, J.-L. Leray, and J. Margail, "Ultraviolet Radiation Induced Defect Creation in Buried SiO_2 Layers," Appl. Phys. Lett. 59, 2275 (1991).

[185] J. F. Conley, P. M. Lenahan, and P. M. Roitman, "Electron Spin Resonance of SIMOX Oxides: Evidence for Structural Change and a Deep Electron Trap," Appl. Phys. Lett. 60, 2889 (1992).

[186] A. Stesmans and K. Vanheusden, "Depth Profiling of Oxygen Vacancy Defect Generation in Buried SiO_2," Material Research Society Symposium Proceedings 284, 299 (1993).

[187] A. Stesmans, R. A. B. Devine, A. G. Revesz, and H. L. Hughes, "Irradiation-Induced EPR Active Defects in SIMOX Structures," IEEE Trans. Nucl. Sci. NS-37, 2008 (1990).

[188] J. F. Conley, P. M. Lenahan, and P. Roitman, "Evidence for a Deep Electron Trap and Charge Compensation in Separation by Implanted Oxygen Oxides," IEEE Trans. Nucl. Sci. NS-39, 2114 (1992).

[189] W. L. Warren, D. M. Fleetwood, M. R. Shaneyfelt, J. R. Schwank, and P. S. Winokur, "Excess-Si Related Defect Centers in Buried SiO_2 Thin Films," Appl. Phys. Lett. 62, 3330 (1993).

[190] W. L. Warren, J. R. Schwank, M. R. Shaneyfelt, D. M. Fleetwood, and P. S. Winokur, "Hydrogen Interactions with Delocalized Spin Centers in Buried SiO_2 Thin Films " Appl. Phys. Lett. 62, 1661 (1993).

[191] W. L. Warren, D. M. Fleetwood, J. R. Schwank, M. R. Shaneyfelt, P. S. Winokur, R. A. B. Devine, and W. P. Maszara, "Shallow Oxygen-Related Donors in Bonded and Etchback Silicon on Insulator Structures," Appl. Phys. Lett. 64, 508 (1994).

[192] A. Stesmans, "Shallow Donors in Buried Oxide Silicon-on-Insulator Structures Revealed by γ-Irradiation-Induced Electron Spin Resonance Activation," Solid State Communications 78, 321 (1991).

[193] T. Hori, H. Iwasaki, and K. Tsuji, "Electrical and Physical Properties of Ultrathin Reoxidized Nitrided Oxides Prepared by Rapid Thermal Processing," IEEE Trans. Electron Dev. ED-36, 340 (1989).

[194] L. Manchanda, G. R. Weber, Y. O. Kim, L. C. Feldman, N. Moryia, B. E. Weir, R. C. Kistler, M. L. Green, and D. Brasen, "A New Method to Fabricate Thin Oxynitride/Oxide Gate Dielectric for Deep Submicron Devices," Microelectronic Engineering 22, 69 (1993).

[195] T. Hori, Y. Naito, H. Iwasaki, and H. Esaki, "Interface States and Fixed Charges in Nanometer-Range Thin Nitrided Oxides Prepared by Rapid Thermal Annealing," IEEE Electron Device Letters EDL-7, 669 (1986).

[196] H. Fukuda, T. Arakawa, and S. Ohno, "Thin-Gate SiO_2 Films Formed by *in situ* Multiple Rapid Thermal Processing," IEEE Trans. Electron Dev. ED-39, 127 (1992).

[197] T. Hori, "Inversion Layer Mobility under High Normal Field in Nitrided-Oxide MOSFETs," IEEE Trans. Electron Dev. ED-37, 2058 (1990).

[198] T. Hori, S. Akamatsu, Y. Odake, "Deep-Submicrometer CMOS Technology with Reoxidized or Annealed Nitrided-Oxide Gate Dielectrics Prepared by Rapid Thermal Processing," IEEE Trans. Electron Dev. ED-36, 118 (1992).

[199] G. L. Dunn and P. W. Wyatt, "Reoxidized Nitrided Oxide for Radiation-Hardened MOS Devices," IEEE Trans. Nucl. Sci. NS-36, 2161 (1989).

[200] N. Bhat and J. Vasi, "Interface-State Generation under Radiation and High-Field Stressing in Reoxidized Nitrided Oxide MOS Capacitors," IEEE Trans. Nucl. Sci. NS-39, 2230 (1992).

[201] G. J. Dunn and S. A. Scott, "Channel Hot-Carrier Stressing of Reoxidized Nitrided Silicon Dioxide," IEEE Trans. Electron Dev. ED-37, 1719 (1990).

[202] M. A. Schmidt, F. L. Terry, B. P. Mathur, and S. D. Senturia, "Inversion Layer Mobility of MOSFETs with Nitrided Oxide Gate Dielectrics," IEEE Trans. Electron Dev. ED-35, 1627 (1988).

[203] T. Kusaka, A. Hiraiwa, and K. Mukai, "Mobility Degradation of Nitrided Oxide MISFETs," J. Electrochem. Soc. 135, 166 (1988).

[204] P. Letourneau, A. Harb, M. Dutoit, and J. Solo de Zaldivar, "Effect of Nitrogen Profile on Electrical Characteristics of Ultrathin SiO_2 Films Nitrided by RTP," Microelectronic Engineering 15, 483 (1991).

[205] H. E. Boesch, Jr. and G. J. Dunn, "Hole Transport in SiO_2 and Reoxidized Nitrided SiO_2 Gate Insulators at Low Temperatures," IEEE Trans. Nucl. Sci. NS-38, 1083 (1991).

[206] J. T. Yount, P. M. Lenahan, and G. J. Dunn, "Electron Spin Resonance Study of Radiation-Induced Point Defects in Nitrided and Reoxidized Nitrided Oxides," IEEE Trans. Nucl. Sci. NS-39, 2211 (1992).

[207] J. T. Wallmark and S. M. Marcus, "Minimum Size and Maximum Packing Density of Nonredundant Semiconductor Devices," Proceedings of the IRE, 286 (1962).

[208] D. Binder, E. C. Smith, and A. B. Holman, "Satellite Anomalies from Galactic Cosmic Rays," IEEE Trans. Nucl. Sci. NS-22, 2675 (1975).

[209] L. C. Northcliffe and R. F. Schilling, "Range and Stopping Power Tables for Heavy Ions," Nucl. Data Tables A7, 233 (1970).

[210] J. F. Ziegler, "Handbook of Stopping Cross-Sections fore Energetic Ions in All Elements," from the series "The Stopping and Ranges of Ions in Matter," vol. 5, ed. J. F. Ziegler, Pergamon Press (New York, 1980).

[211] J. F. Ziegler, J. P. Biersak, and U. Littmark, "Stopping and Range of Ions in Solids," vol. 1, Pergamon Press (New York, 1985).

[212] T. R. Weatherford, "Single Event Upset in GaAs Integrated Circuits," North Carolina State University, Ph. D. thesis.

[213] C. M. Hsieh, P. C. Murley, and R. R. O'Brien, "A Field Funneling Effect on the Collection of Alpha-Particle-Generated Carriers in Silicon Devices," IEEE Electron Dev. Lett. EDL-2, 103 (1981).

[214] C. M. Hsieh, P. C. Murley, and R. R. O'Brien, "Dynamics of Charge Collection From Alpha-Particle Tracks in Integrated Circuits," Proceedings of the IEEE International Reliability Physics Symposium, p.38, Orlando, Florida, April 7, 1981.

[215] F. B. McLean and T. R. Oldham, "Charge Funneling in N- and P-Type Si Substrates," IEEE Trans. Nucl. Sci. NS-29, 2018 (1982).

[216] C. M. Hsieh, P. C. Murley, and R. R. O'Brien, "Collection of Charge From Alpha-Particle Tracks in Silicon Devices," IEEE Trans. Electron Dev. ED-30, 686 (1983).

[217] M. A. Hopkins and J. R. Srour, "Charge Collection Measurements on GaAs Devices Fabricated on Semi-Insulating Substrates," IEEE Trans. Nucl. Sci. NS-31, 1116 (1984).

[218] T. R. Oldham and F. B. McLean, "Charge Collection Measurements for Heavy Ions Incident on n- and p-Type Silicon," IEEE Trans. Nucl. Sci. NS-30, 4493 (1983).

[219] M. A. Hopkins and J. R. Srour, "Measurements of Alpha-Particle-Induced Charge in GaAs Devices," IEEE Trans. Nucl. Sci. NS-30, 4457 (1983).

[220] L. D. Flesner, "Gate Charge Collection and Induced Drain Current in GaAs FETs," IEEE Trans. Nucl. Sci. NS-32, 4110 (1985).

[221] A. Campbell, A. Knudson, D. McMorrow, W. Anderson, J. Roussos, S. Espy, S. Buchner, K. Kang, D. Kerns, and S. Kerns, "Ion Induced Charge Collection in GaAs MESFETs," IEEE Trans. Nucl. Sci. NS-36, 2292 (1990).

[222] A. R. Knudson, A. B. Campbell, D. McMorrow, S. Buchner, K. Kang, T. Weatherford, V. Srinivas, G. A. Swartzlander Jr., and Y. J. Chen, "Pulsed Laser-Induced Charge Collection in GaAs MESFETs," IEEE Trans. Nucl. Sci. NS-37, 1909 (1990).

[223] S. Buchner, K. Kang, D. W. Tu, A. R. Knudson, A. B. Campbell, D. McMorrow, V. Srinivas, and Y. J. Chen, "Charge Collection in GaAs MESFETs and MODFETs," IEEE Trans. Nucl. Sci. NS-38, 1370 (1991).

[224] T. R. Weatherford, D. McMorrow, W. R. Curtice, A. B. Campbell, and A. R. Knudson, "Examination of the SEU Sensitivity of GaAs MESFETs via 2-D Computer Simulation and Picosecond Charge Collection Experiments," 1993 IEEE International Reliability Physics Symposium Proceedings, p. 357, (1993).

[225] D. McMorrow, J. S. Melinger, A. R. Knudson, A. B. Campbell, T. Weatherford, and L. H. Tran, "Picosecond Charge-Collection Dynamics in GaAs MESFETs," IEEE Trans. Nucl. Sci. NS-39, 1657 (1992).

[226] D. McMorrow, A. R. Knudson, and A. B. Campbell, "Fast Charge Collection in GaAs MESFETs," IEEE Trans. Nucl. Sci. NS-37, 1902 (1990).

[227] W. T. Anderson, A. R. Knudson, F. A. Buot, H. L. Grubin, J. P. Kreskovsky, and A. B. Campbell, "Experimental and Theoretical Study of Alpha Particle Induced Charge Collection in GaAs FETs," IEEE Trans. Nucl. Sci. NS-34, 1326 (1987).

[228] B. Hughlock, T. Williams, A. Johnston, and R. Plaag, "Ion Induced Charge Collection in GaAs MESFETs and Its Effect on SEU Vulnerability," IEEE Trans. Nucl. Sci. NS-38, 1442 (1991).

[229] Y. Umemoto, N. Matsunaga, and K. Mitsusada, "A Bipolar Mechanism for Alpha-Particle Induced Soft Errors in GaAs Integrated Circuits," IEEE Trans. Electron Dev. ED-36, 864 (1989).

[230] J. R. Hauser, S. E. Diehl-Nagle, A. R. Knudson, and A. B. Campbell, "Ion Track Shunt Effects in Multi-Junction Structures," IEEE Trans. Nucl. Sci. NS-32, 4115 (1985).

[231] A. R. Knudson, A. B. Campbell, J. R. Hauser, M. Jessee, W. J. Stapor, and P. Shapiro, "Charge Transport by the Ion Shunt Effect," IEEE Trans. Nucl. Sci. NS-33, 1560 (1986).

[232] J. R. Schwank, F. W. Sexton, T. R. Weatherford, D. McMorrow, and A. R. Knudson, "Charge Collection in GaAs MESFETs Fabricated on Semi-Insulating Substrates," IEEE Electron Dev. Lett. (submitted for publication).

[233] C. Loge, D. Burnett, T. McNelly, K. Baker, A. Borman, D. Dreier, V. Soorholtz, "Soft Error Rate and Stored Charge Requirements in Advanced High Density SRAM," 1993 International Electron Device Meeting, pp. 73-82.

[234] J. T. Blandford, Jr., A. E. Waskiewicz, and J. C. Pickel, "Cosmic Ray Induced Permanent Damage in MNOS EAROMs," IEEE Trans. Nucl. Sci. NS-31, 1568 (1984).

[235] J. C. Pickel, J. T. Blandford, Jr., A. E. Waskiewicz, and V. H. Strahan, Jr., "Heavy Ion Induced Permanent Damage in MNOS Gate Insulators," IEEE Trans. Nucl. Sci. NS-32, 4176 (1985).

[236] T. F. Wrobel, "On Heavy Ion Induced Hard-Errors in Dielectric Structures," IEEE Trans. Nucl. Sci. NS-34, 1262 (1987).

[237] T. F. Wrobel and D. E. Beutler, "Solutions to Heavy Ion Induced Avalanche Burnout in Power Devices," IEEE Trans. Nucl. Sci. NS-39, 1636 (1992).

[238] T. A. Fischer, "Heavy-Ion-Induced, Gate-Rupture in Power MOSFETs," IEEE Trans. Nucl. Sci. NS-34, 1786 (1987).

[239] J. H. Hohl and K. F. Galloway, "Analytical Model for Single-Event Burnout of Power MOSFETs," IEEE Trans. Nucl. Sci. NS-34, 1275 (1987).

[240] A. E. Waskiewicz, J. W. Groninger, V. H. Strahan, and D. M. Long, "Burnout of Power MOS Transistors with Heavy Ions of Californium-252," IEEE Trans. Nucl. Sci. NS-33, 1710 (1986).

[241] J. L. Titus, G. H. Johnston, R. D. Schrimpf, and K. F. Galloway, "Single-Event Burnout of Power Bipolar Junction Transistors," IEEE Trans. Nucl. Sci. NS-38, 1315 (1991).

[242] T. F. Wrobel, F. N. Coppage, G. L. Hash, and A. J. Smith, "Current-Induced Avalanche in Epitaxial Structures," IEEE Trans. Nucl. Sci. NS-32, 3991 (1985).

[243] G. H. Johnson, R. D. Schrimpf, and K. F. Galloway, "Temperature Dependence of Single-Event Burnout in N-Channel Power MOSFETs," IEEE Trans. Nucl. Sci. NS-39, 1605 (1992).

[244] P. Calvel, C. Peyrotte, A. Baiget, and E. G. Stassinopoulos, "Comparison of Experimental Measurements of Power MOSFET SEBs in Dynamic and Static Modes," IEEE Trans. Nucl. Sci. NS-38, 1310 (1991).

[245] J. R. Brews, M. Allenspach, R. D. Shrimpf, and K. F. Galloway, "A Conceptual Model of Single-Event Gate-Rupture in Power MOSFETs," IEEE Trans. Nucl. Sci. NS-40, 1959 (1993).

DATE
FILMED
7/29/94
END