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# PROGRESS ON THE EMITTER WRAP-THROUGH SILICON SOLAR CELL

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**ABSTRACT:** The Emitter Wrap-Through (EWT) solar cell is a back-contacted solar cell with a carrier-collection junction ("emitter") on the front surface. Elimination of grids from the front surface allows for higher performance by eliminating grid-obscuration losses and reducing series resistance, while keeping an emitter on the front surface maintains high collection efficiency in solar-grade materials with modest diffusion lengths. The EWT cell uses laser-drilled vias to wrap the emitter diffusion on the front surface to interdigitated contacts on the back surface. We report on progress towards demonstration of two concepts for the EWT cell. The first EWT concept uses a fabrication sequence based on heavily diffused grooves and plated metallizations, and the second EWT concept uses a single furnace step and screen-printed metallizations. We also report on demonstration of double-sided carrier collection in the EWT cell.

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# INTRODUCTION



We recently presented a new concept for a back-contacted silicon solar cell with a carrier-collection junction ("emitter") on the front surface [1]. This concept (Emitter Wrap Through -- EWT) wraps the emitter on the front surface through laser-drilled vias to interdigitated current-collection grids on the back surface. The primary advantage of a back-contacted cell is elimination of the grid on the front surface, which increases cell performance through elimination of grid obscuration and reduction in series resistance. There are additional advantages for a back-contacted cell in terms of module performance, assembly, and aesthetics [1]. Unlike other back-contact cell designs, the carrier-collection junction is on the front surface in the EWT cell; the front-surface emitter helps maintain a high internal collection efficiency in solar-grade silicon materials with modest diffusion lengths. The EWT cell can also easily include a carrier-collection junction on the back surface so that photogenerated carriers in the bulk are collected at both surfaces; such a "double-junction" cell is particularly appropriate for materials with diffusion lengths less than the device width (e.g., multicrystalline silicon solar cells). Our previous modeling calculations for an EWT solar cell with solar-grade silicon found that the double-junction structure is capable of increasing the cell efficiency by around 1% absolute compared to a front-junction cell [1]. These calculations used conservative material parameters associated with solar-grade silicon, and also found that efficiencies of 18 and 21% are possible with multi- and monocrystalline 100-$cm^2$ EWT solar cells, respectively [1].

The concept that we previously presented for the EWT cell uses a cell fabrication process that is very similar to a buried-contact cell process; i.e., the grids and contacts on the back surface consist of interdigitated grooves that, along with the vias, are heavily diffused with an appropriate dopant ($n^{++}$ and $p^{++}$) and filled with plated metals [1]. We believe the buried-contact process to be quite attractive for an EWT cell because bifacially contacted, buried-contact cells have demonstrated high performance, are in pilot production at several locations, and are believed to be cost competitive with commercial processes

based on screen-printed metallizations [2]. Nevertheless, there are two potential problems with our prior EWT concept, which we now refer to as the Buried-Contact EWT (BC-EWT) cell. First, the BC-EWT cell requires several high-temperature furnace steps for the $n^+$ emitter diffusion, the $n^{++}$ groove and via diffusion, and the $p^{++}$ groove diffusion. There are significant interactions between these furnace steps that complicate the fabrication sequence and may degrade the bulk lifetime, which is a particular concern with solar-grade silicon materials. Second, buried-contact cells are still only in limited production. Hence, the BC-EWT cell could not be quickly adopted for commercial production. There are also issues concerning the production costs and environmental acceptability (particularly regarding the plating chemicals) of buried-contact cell fabrication.

We are developing a variation of our original EWT cell that uses a single $n^+$ diffusion and that can use screen-printed metallizations. We refer to this variation as the Screen-printed EWT cell (SEWT). Because the SEWT concept uses fabrication technologies that are already commonly used in commercial production, we believe the SEWT cell can be easily adapted for commercial production. The SEWT process is also simpler than the BC-EWT process, which should lead to a lower production cost. Solar-grade silicon should work well with the SEWT process because the SEWT cell uses only a single furnace step above 800°C. However, the process simplification of the SEWT cell is obtained at some reduction in potential performance (about 1% absolute) compared to the BC-EWT cell.

In this paper, we first describe our new SEWT cell concept. Next, we present estimates of the potential performance for the new cell concept. We then describe progress towards demonstration of both BC-EWT and SEWT cells. Finally, we describe demonstration of double-sided carrier collection in an EWT cell.

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## DESCRIPTION OF THE SEWT CELL

Figure 1 presents a schematic illustration of the SEWT cell. Note that the SEWT cell has an $n^+$ emitter on both surfaces. The $n^+$ diffusion on the back surface is required for making the n-type contact, but is also desirable for improved internal collection efficiency in materials with short diffusion lengths. The fabrication sequence for a SEWT cell starts with drilling an array of holes in the p-type silicon substrate with a laser. After cleaning of the substrate and etching of the holes, a phosphorus diffusion is performed such that an $n^+$ diffusion is formed on both surfaces and inside the holes. The $n^+$ diffusion in the holes provides the electrical conduction path between the front- and back-surface diffusions; hence, we refer to these holes as "vias".

The cell is completed with application of the grids on the back surface. First, Ag is screen printed on the back surface and fired for the n-type contact and grid. This grid is aligned over the vias. Next, an AlAg paste is screen printed in a grid pattern that is interdigitated with the previous n-type grid. Hence, each screen-printed metal requires an alignment, which is a potential complication for manufacturing. The aluminum from the AlAg paste forms a $p^+$ layer that penetrates the $n^+$ diffusion during firing, which allows the AlAg grid to electrically contact the p-type substrate. If necessary, an alkaline etch may be used at this point to electrically isolate the $n^+$ and $p^+$ junctions on the back surface. Researchers at Hitachi report using a similar sequence without the laser-drilled vias to fabricate double-junction cells with a triode structure [3]. They reported obtaining an efficiency of 16.8% for a 100-$cm^2$ multicrystalline silicon solar cell. Because the SEWT cell adds only a single step (laser-drilled vias) to typical commercial cell fabrication sequences, and because the researchers at Hitachi have already demonstrated many elements of the SEWT cell, we believe the SEWT cell could be easily adapted for commercial production.

The SEWT cell has a lower *potential* performance compared to the BC-EWT cell due to two factors. First, the single $n^+$ diffusion in the SEWT cell is a compromise for good blue response and low series resistance. In particular, commercial silicon cells with screen-printed metallizations use a phosphorus diffusion profile with a high surface concentration in order to compensate for the poor contact resistance of screen-printed silver metalizations. This non-optimal diffusion profile in commercial silicon cells results in a 10% reduction of

performance due to poor blue response compared to high-efficiency laboratory cells [4]. The BC-EWT cell has separate diffusions for the illuminated region and for the metal-contacted region, so the diffusions in these regions can be separately optimized for good blue response and low resistance, respectively. Note that performance compromises for the SEWT cell can be significantly reduced with an additional heavy diffusion of the back surface and vias, or with a short selective etch of the front diffusion; such a SEWT cell would then have a high sheet resistance in the illuminated region for good blue response and have a low sheet resistance in the metal-contacted and via regions for low resistance.

The second factor limiting the potential performance of SEWT cells compared to BC-EWT cells is the series resistance associated with conduction through the vias. The via resistance is negligible in the BC-EWT cell because the vias are heavily diffused (around 10 Ω/□) and are filled with plated metal. The vias in the SEWT cell have a higher sheet resistance and probably less metal compared to the BC-EWT cell, with the net result that the SEWT cell may require as many as 4X more vias than the BC-EWT cell for an acceptable series resistance. Note that the difference in via resistance would be negligible if the vias can be appreciably filled with the screen-printed metal in the SEWT cell. We estimate that the potential performance of the SEWT cell is about 1% absolute less than the BC-EWT cell due to the above two factors, which corresponds to projected efficiencies around 17 and 20% for 100-cm$^2$ SEWT cells using solar-grade multicrystalline and single-crystal silicon substrates, respectively.

## EXPERIMENTAL RESULTS

We are developing a SEWT cell using photolithographic processes and evaporated metallization to demonstrate the concept. We refer to this cell as the Photolithographic EWT cell (PhEWT). We are also continuing investigation of the BC-EWT cell. We are using electroplated silver rather than electroless plated copper for our BC-EWT cell due to available equipment in our laboratory, although commercial cells would probably use electroless plated copper. Our BC-EWT and PhEWT cell sequences are presented in Tables 1 and 2.

The BC-EWT sequence is much longer and more complicated than the PhEWT cell sequence. The BC-EWT cell requires LPCVD $Si_3N_4$, three aligned laser-scribe steps, three diffusions ($n^+$, $n^{++}$, and $p^{++}$), and several $SiO_2$ CVD and densification steps due to the interactions between the $n^+$, $n^{++}$, and $p^{++}$ diffusions. These deleterious interactions are manifested in the completed cells as either incorrectly doped grooves (i.e., the p-type groove is doped n-type by the $n^{++}$ diffusion), or by plating over the front surface. However, we believe that use of a deposited borosilicate glass for the boron diffusion source would eliminate many of the diffusion interactions, possibly eliminate several furnace steps, and would considerably simplify the BC-EWT process sequence. Deposited borosilicate and phosphosilicate glass have been successfully used as diffusion sources for high-efficiency, back-contacted silicon concentrator cells [5].

The PhEWT cell uses processes that are very similar to our one-sun and concentrator baseline cells [6,7]. The only additional process required for the PhEWT cell is performing photolithography on wafers with holes. We found that a low-tack tape is useful to prevent photoresist bleeding through the wafer and contaminating the front surface during application of photoresist on the back surface. The holes can also be a source of photolithographic defects if the hole diameter approaches the dimensions of the photolithographic pattern, so that the vias should not be etched too long. The vias can also be a source of shunts in the completed cells if the vias are not sufficiently etched; the vias must be etched to remove damage from the laser-scribe process. Hence, optimization of the via etch is a critical step. The PhEWT cell must also be scribed from the wafer for testing, which is unlike our baseline cells where we use a patterned emitter diffusion to isolate the cells on the wafer.

Table 3 presents results for our best cells of each type to date. The relatively low performance of our EWT cells is primarily due to low FF and $V_{oc}$. We recently determined that the low $V_{oc}$ in the PhEWT cell is primarily due to an extrinsic factor (perimeter recombination) related to separating the cell from the wafer. We have also observed shunt and excess recombination currents (dark-IV currents with diode factor $n>1$) associated with the vias and with the interdigitated back-contact structure.

## DISCUSSION

One of the most interesting features of the PhEWT and BC-EWT cells is the double-junction structure that offers the possibility for enhanced collection efficiency from the bulk. Our previous calculations indicated that the double-junction structure can enhance the efficiency by nearly 1% absolute compared to a conventional front-junction cell; these calculations used material parameters appropriate for solar-grade silicon [1]. The region over the n-type grid in the PhEWT cell has an $n^+pn^+$ structure (Figure 1), so that carrier collection from the p-type bulk can occur from both $n^+$ surfaces.

We performed a 1060-nm laser-beam induced current (LBIC) scan of a PhEWT cell (Figure 2). The enhanced carrier collection on the right-hand-side (RHS) of the plot is over the n-type contact with the double-junction region. The lower response on the left-hand-side of the plot is over the p-type contact; this region of the PhEWT cell has a carrier-collection junction only on the front surface. The large spot in the top RHS is the via; there is enhanced carrier collection around the via because the via is diffused. (The diameter of the laser spot was larger than the via diameter, so the LBIC scan did not show a reduced response in the center of the via.) This particular cell has a diffusion length around half the device width, so the contrast between the two regions is large. The plot clearly indicates enhanced internal collection efficiency due to the double-junction structure over the n-type contact.

## CONCLUSIONS

The EWT silicon cell is a back-contacted cell with a carrier-collection junction on the front surface. This cell structure allows for a high efficiency by eliminating grid obscuration while maintaining high internal collection efficiency. The EWT cell may also be fabricated with a double-junction structure and with low-cost processes. We described two EWT cell concepts based on plated and screen-printed metallizations, and reported progress towards demonstrating these concepts.

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Table 1. Process sequence for BC-EWT cells.

Texture etch front surface.
Phosphorus emitter diffusion (100 Ω/□).
$Si_3N_4$ deposition by LPCVD (100 nm).
CVD $SiO_2$ on back surface (>500 nm).
Groove p-type grid.
KOH etch grooves.
CVD $SiO_2$ on front surface (>500 nm).
$B_2H_6$ boron diffusion (approximately 50 Ω/□).
CVD oxide (600 nm) on back surface.
Densify and drive-in boron (1000°C , 60 minutes).
Groove and drill n-type grid.
KOH etch grooves and vias.
$PH_3$ phosphorus diffusion to approximately 10 Ω/□.
Deglaze grooves and tune nitride to ARC (35 minute HF etch).
Electroless nickel plate grooves.
Sinter in forming gas, 500°C.
Electroplate silver.
Forming gas anneal, 400°C.
Scribe and test.

Table 2. Process sequence for PhEWT cells.

Laser-scribe vias and separation grooves.
Etch grooves and vias.
CVD $SiO_2$ on back surface (300 nm).
Texture etch front surface.
Pattern oxide on back surface for $p^+$ contact.
$POCl_3$ diffusion (around 60 Ω/□).
Pattern oxide on back surface for metal.
Evaporate and liftoff AlTiPdAg metalization.
Forming gas anneal, 400°C .
Scribe and test.

Table 3. Summary of best EWT cells demonstrated to date. The BC-EWT and PhEWT cells were fabricated on 2-Ωcm FZ and 0.4-Ωcm FZ silicon wafers, respectively.

| Type | Area $cm^2$ | $V_{oc}$ volts | $J_{sc}$ $mA/cm^2$ | FF | Eff. % |
|---|---|---|---|---|---|
| BC-EWT | 36 | 0.554 | 32.5 | 0.487 | 8.76 |
| PhEWT | 4 | 0.614 | 37.2 | 0.676 | 15.4 |

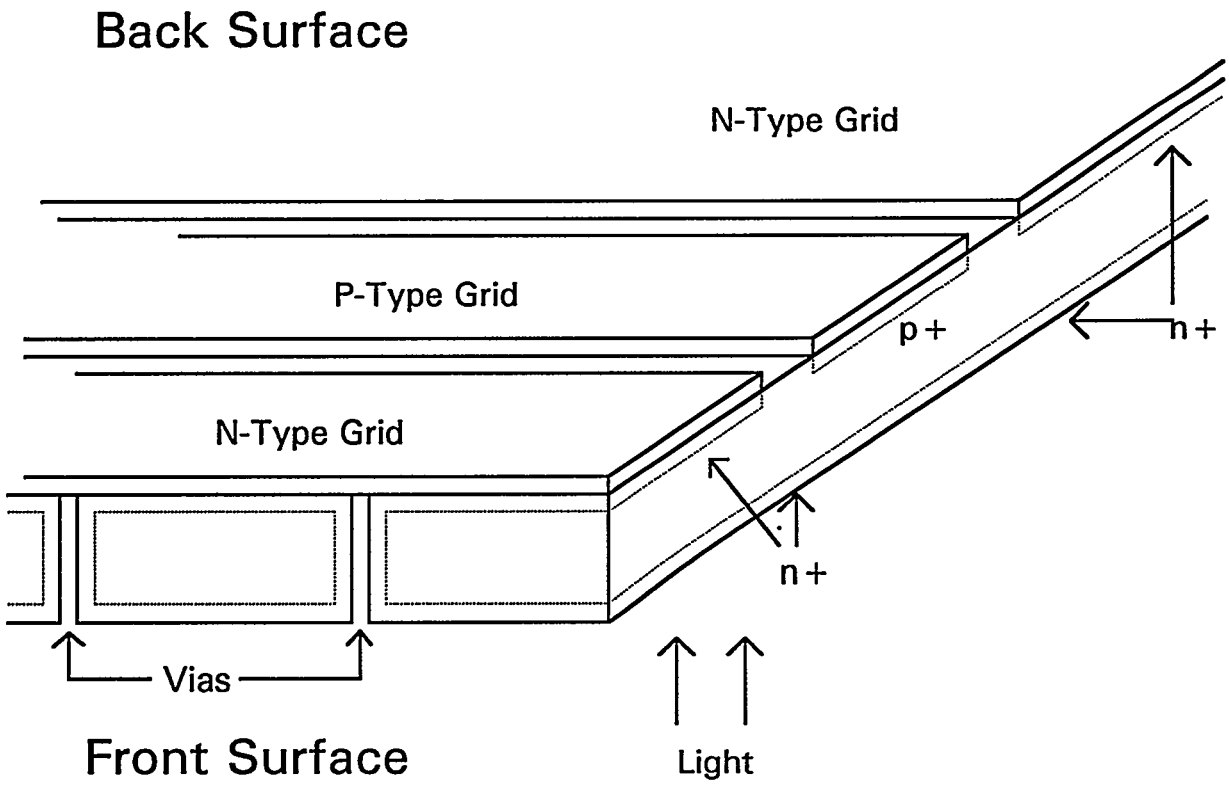
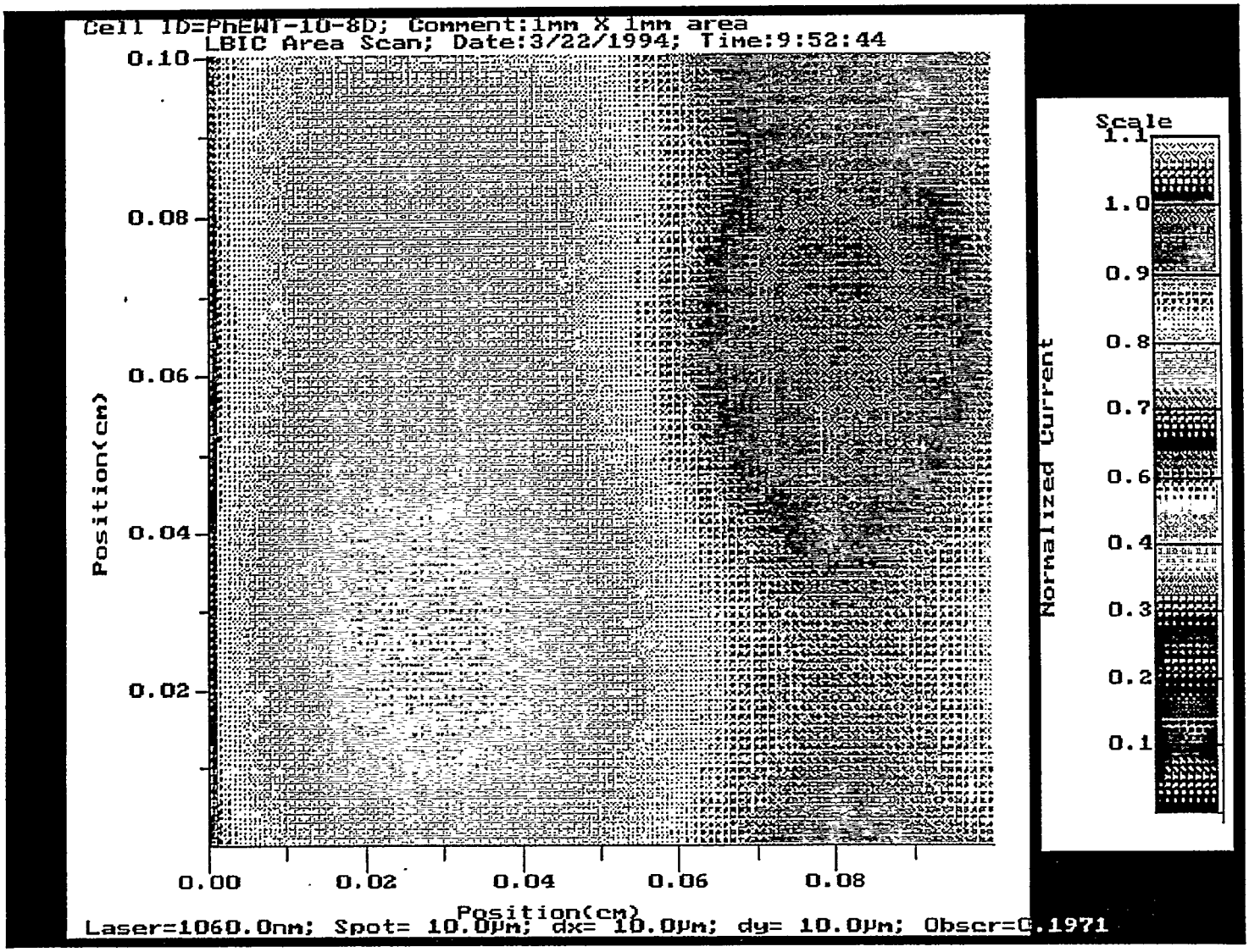



Figure 1. Schematic illustration of SEWT cell. The bottom surface is shown facing up in the diagram in order to illustrate the interdigitated grid on the back surface. Approximately 50% of the cell has an $n^+pn^+$ structure.

Figure 2. 2-dimensional LBIC scan of a PHEWT cell at 1060 nm. The right-hand-side of the plot is over an n-type contact and the left-hand-side of the plot is over the p-type contact. Similar LBIC scans at 670 and 820 nm show no features other than the vias, which demonstrates that the contrast in the 1060-nm scan is due to variations in the internal collection efficiency.


Cell ID=PhEWT-10-8D; Comment:1mm X 1mm area
LBIC Area Scan; Date:3/22/1994; Time:9:52:44
0.10
0.08
0.06
0.04
0.02
Position(cm)
0.00
0.02
0.04
0.06
0.08
Position(cm)
Scale
1.1
1.0
0.9
0.8
0.7
0.6
0.4
0.3
0.2
0.1
Normalized Current
Laser=1060.0nm; Spot= 10.0µm; dx= 10.0µm; dy= 10.0µm; Obscr=0.1971