NREL/TP-411-4840 • UC Category: 271 • DE92001244

NREL/TP--411-4840

DE92 001244

Research on Stable, High-Efficiency Amorphous Silicon Multijunction Modules

Annual Subcontract Report 1 January 1991 - 31 December 1991

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National Renewable Energy Laboratory
(formerly the Solar Energy Research Institute)
1617 Cole Boulevard
Golden, Colorado 80401-3393
A Division of Midwest Research Institute
Operated for the U.S. Department of Energy
under Contract No. DE-AC02-83CH10093

Prepared under Subcontract No. ZM-1-19033-2

April 1992

On September 16, 1991 the Solar Energy Institute was designated a national laboratory, and its name was changed to the National Renewable Energy Laboratory.

Printed in the United States of America
Available from:
National Technical Information Service
U.S. Department of Commerce
5285 Port Royal Road
Springfield, VA 22161

Price: Microfiche A01
Printed Copy A05

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PREFACE

This Annual Technical Progress Report covers the work performed by United Solar Systems Corp. for the period 1 January 1991 to 31 December 1991 under DOE/SERI Subcontract Number ZM-1-19033-2. The following personnel participated in the research program:

A. Banerjee, E. Chen, R. Clough, T. Glatfelter, S. Guha (Principal Investigator), G. Hammond, M. Hopson, N. Jackett, M. Lycette, J. Noch, T. Palmer, A. Pawlikiewicz, I. Rosenstein, R. Ross, D. Wolf, Xixiang Xu, J. Yang, and K. Younan.

We would like to thank V. Trudeau for preparation of this report.

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EXECUTIVE SUMMARY

OBJECTIVES

The principal objective of the program is to conduct research on semiconductor materials and non-semiconductor materials to enhance the performance of multi-bandgap, multijunction, large-area amorphous silicon-based alloy modules. The goal for 1991 is to demonstrate stabilized module efficiency of 8% for multijunction panel of area greater than 900 cm^2.

APPROACH

Double-junction and triple-junction cells are made on Ag/ZnO back reflector deposited on stainless steel substrates. a-SiGe alloy is used for the *i*-layer in the bottom cell; the other cells use a-Si alloy. After evaporation of antireflection coating, silver grids and bus bars are put on the top surface, and the panel is encapsulated in an EVA/Tefzel structure to make a one-square-foot monolithic module.

STATUS/ACCOMPLISHMENTS

- Uniform deposition of back reflector a-Si alloy layers and transparent conducting oxide was achieved over one-square-foot area. The uniformity was checked by making an array of 16 x 5 subcells of 7.4 cm^2 area over the entire surface. The variation in subcell short-circuit current density was within ± 5%.

- High quality a-SiGe alloys were deposited over large areas, and single-junction cells were fabricated with an output of 3.35 mW/cm^2 under global AM1.5 illumination with a 630 nm red cut-on filter. These cells were used as the bottom cell of double-junction and triple-junction structures, and small-area (0.25 cm^2) initial efficiencies of 11% for double-junction and 10% for triple-junction cells were achieved. The triple-junction cells are being further optimized.

- A new method was developed by which the performance of single-junction cells after long-term, one-sun exposure at 50°C can be predicted by exposing cells to short-term intense light at different temperatures. Using this method, we found that single-junction cells show the highest stabilized efficiency when the thickness of the intrinsic layer is about 2000 Å. The method was also used to investigate the stability of single-junction a-SiGe alloy cells.

- Our numerical model for solar cells was used to explain the light-induced degradation behavior of single-junction cells. The experimental data on thick cells, both in the undegraded and degraded states, could be explained by assuming that the only effect of prolonged light illumination is an increase in the gap state density.

- We have fabricated a series of double-junction and triple-junction modules in which the grid loss is about 4%. The following table summarizes results of three double-junction and two-triple-junction fully encapsulated modules as measured under USSC Spire simulator.

Table I. Initial performance of multijunction modules.

Sample No.	Aperture Area	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	η (%)
588	919.3	1.60	9.52	65	9.90
597	918.1	1.60	8.80	68	9.57
602	919.9	1.60	8.82	68	9.60
598	912.0	2.45	5.84	67	9.59
603	905.4	2.45	5.34	70	9.15

The same modules, however, show 15% to 18% lower efficiencies when measured under NREL Spire simulator. The major discrepancy is in the fill factor and short-circuit current density. The discrepancy in the measurements is now being investigated.

The highest aperture-area efficiency of our modules as measured at NREL is 8.35% for triple-junction and 8.2% for double-junction structure. NREL measurements have an accuracy of $\pm 10\%$, and, assuming the higher limit, the module efficiency could be 9.2%. We see a typical degradation of 15% of our modules after 600 h of one-sun light soaking. The stabilized efficiency is thus projected to be 7.8%, which is within 3% of our 1991 goal.

SECTION 1
INTRODUCTION

The research program is directed toward advancing our understanding of amorphous silicon alloys and other relevant non-semiconductor materials for use in large-area multijunction modules. An important thrust of the program is on performance of modules after long-time light exposure; therefore, study of light-induced degradation forms an important part of the program. The final goal of the program is to demonstrate a stable, aperture-area efficiency of 12% for a two-terminal, multi-bandgap, multijunction module of aperture area of at least 900 cm^2 by the end of 1993.

The program is divided into three tasks. Task 1, semiconductor materials research, is directed toward depositing, optimizing, and characterizing of suitable amorphous silicon alloy materials and cell structures over 900 cm^2 area. Task 2, non-semiconductor materials research, involves investigating suitable back reflectors and antireflection coatings and also encapsulants for the modules. Task 3, module research, is directed toward fabricating modules involving grid patterning, cell isolation and interconnect, and encapsulation.

In this report, we outline the progress made toward the program goal in the different task areas. In Section 2, we discuss the experimental results on characteristics of a-Si and a-SiGe alloy cells using a large-area deposition chamber capable of deposition over 1 sq. ft. area. Results on back reflectors and antireflection coatings are also discussed. Small-area (0.25 cm^2) subcell initial efficiency of 11% has been achieved using Ag/ZnO back reflector. The cells use a dual-bandgap, double-junction structure. Optimization of the triple-junction cells is not yet complete, and a cell efficiency of 10% has been achieved. Results on uniformity over the large area are also presented. In Section 3, the module design procedure is outlined. The losses associated with grid lines, cell isolation, and encapsulation are evaluated and optimized. With our current grid design and encapsulation procedure, the difference between active-area subcell efficiency and module aperture-area

efficiency is about 10%. In Section 3, we also discuss the performance of double- and triple-junction modules fabricated by us. We find a significant difference in the values of efficiency as measured at USSC and NREL. Possible causes for this discrepancy are discussed. In Section 4, we discuss accelerated light-soaking results in cells. A new method has been developed to obtain cell performance after prolonged one-sun light soaking using high-intensity short-time illumination at different temperatures.

SECTION 2
LARGE-AREA SEMICONDUCTOR AND NON-SEMICONDUCTOR DEPOSITION

2.1 Selection of Feedstock Materials

During the period under review, the emphasis has been toward the optimization of single-junction and dual-junction a-Si:H alloy cells using a large-area batch deposition system. The initial goal was to translate into large area the results obtained in the small-area deposition reactor under the previous subcontract [1]. The deposition conditions and the cell structures are therefore similar to what were reported earlier. The dual-junction configuration employs a-Si:H *i*-layer for the top and a-SiGe:H *i*-layer for the bottom cells. We have also done some preliminary work on triple-junction cells using a-SiGe:H *i*-layer in the bottom cell only. The schematic of a dual-junction cell structure is shown in Fig. 1. All the semiconductor layers have been deposited in the large-area IIB machine (described below) by the conventional rf glow-discharge method. We have used microcrystalline *p* layers in order to obtain both higher V_{oc} and higher blue response.

The feedstock materials (gases) selected for depositing the films in the IIB machine are the same as those used in an earlier SERI subcontract [1]. The gases are silane, disilane, hydrogen, and silicon tetrafluoride for the intrinsic layers. Phosphine and boron trifluoride are used for the doped layers. Germane is used for the a-SiGe:H narrow-bandgap intrinsic layers. The relevant information regarding the feedstock gases, including purity, are given in Table II.

Table II. Impurity content in the process gases.

GAS	IMPURITY (ppm)			
	O_2	N_2	CO/CO_2	H_2O
Silane	< 1	< 5	< 2	< 1
Disilane	< 1	< 5	< 2	-
Germane	< 1	< 2	< 2	-
Silicon Tetrafluoride	< 4	< 4	< 2	-
Phosphine	< 1	< 1	< 2	< 1
Boron Trifluoride			99.5% pure	

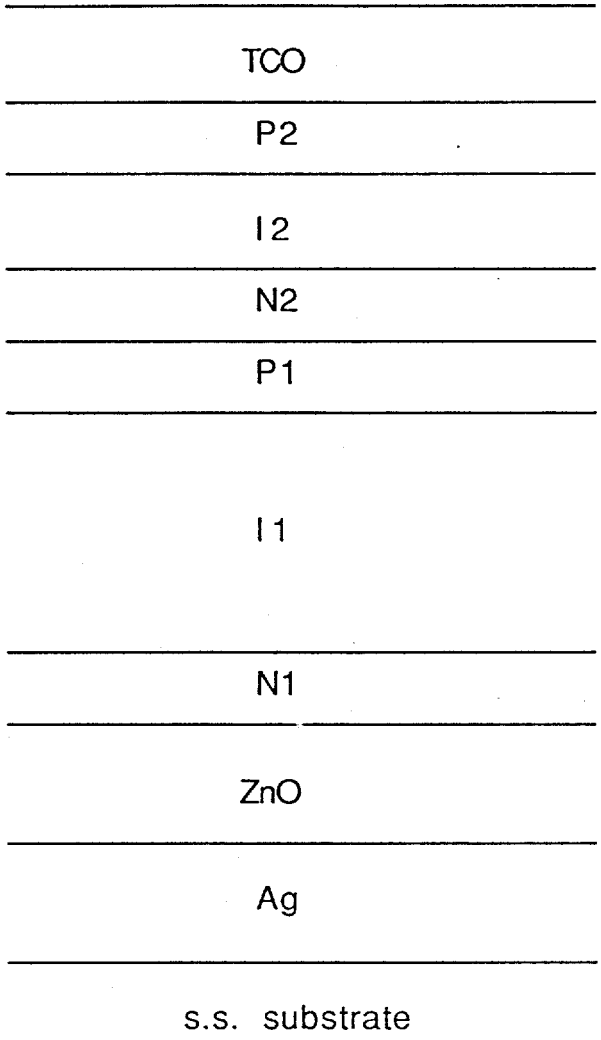


Fig. 1. Schematic of dual-junction cell structure.

The structural, electrical and optical properties of the semiconductor layers are similar to those deposited in small-area deposition systems and reported in an earlier SERI subcontract [1]. The optical gap of the a-SiGe alloy can be varied by changing the germanium content in the film and for a Ge-content of about 40%, the optical gap as measured using Tauc plot is 1.44 eV (Fig. 2). The sub-bandgap absorption of the film as measured using photothermal deflection spectroscopy is shown in Fig. 3. The slope of the Urbach edge is 47 meV, and the absorption coefficient at 1 eV is ~ 10 cm^{-1}. The conductivity activation energy of the film (Fig. 4) is about 0.7 eV, which shows that the Fermi level is close to the mid-gap. The results are comparable to those achieved using the small-area machine [1].

2.2 Large-Area a-Si:H and a-SiGe:H Deposition System

A multichamber system "IIB" with gate valves isolating the *p, i, n* chambers has been used for the large-area device research. The system is computer-controlled and has the capability of fabricating 1 sq. ft. devices. Two types of substrate sizes with corresponding substrate holders have been used. One incorporates a large frame that holds a substrate for the 1 sq. ft. device work. The second type uses a substrate holder that holds six 2" x 2" substrates, the positions of which are dispersed over an area of 1 sq. ft.

Back Reflector

The results presented in this report have been obtained using Ag/ZnO back reflectors deposited on stainless steel substrates. During the initial part of the project, the ZnO and Ag films were deposited on 2" x 2" substrates in two different batch deposition machines. In the latter part, a sputtering system was constructed for the preparation of large-area Ag/ZnO back reflectors. Further description of the back reflector studies is given in Section 2.3.

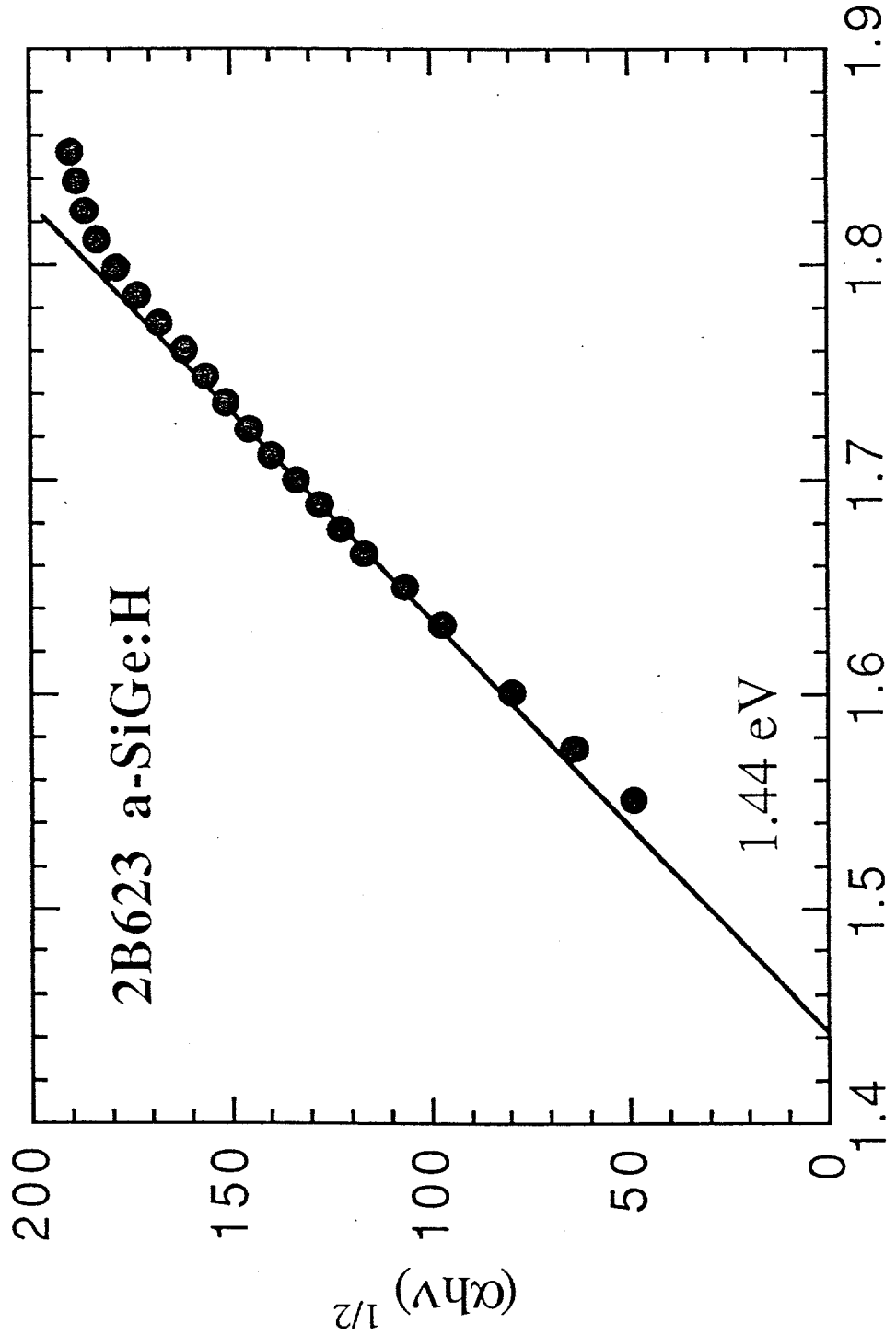


Fig. 2. Tauc plot of absorption coefficient of a-SiGe:H alloy.

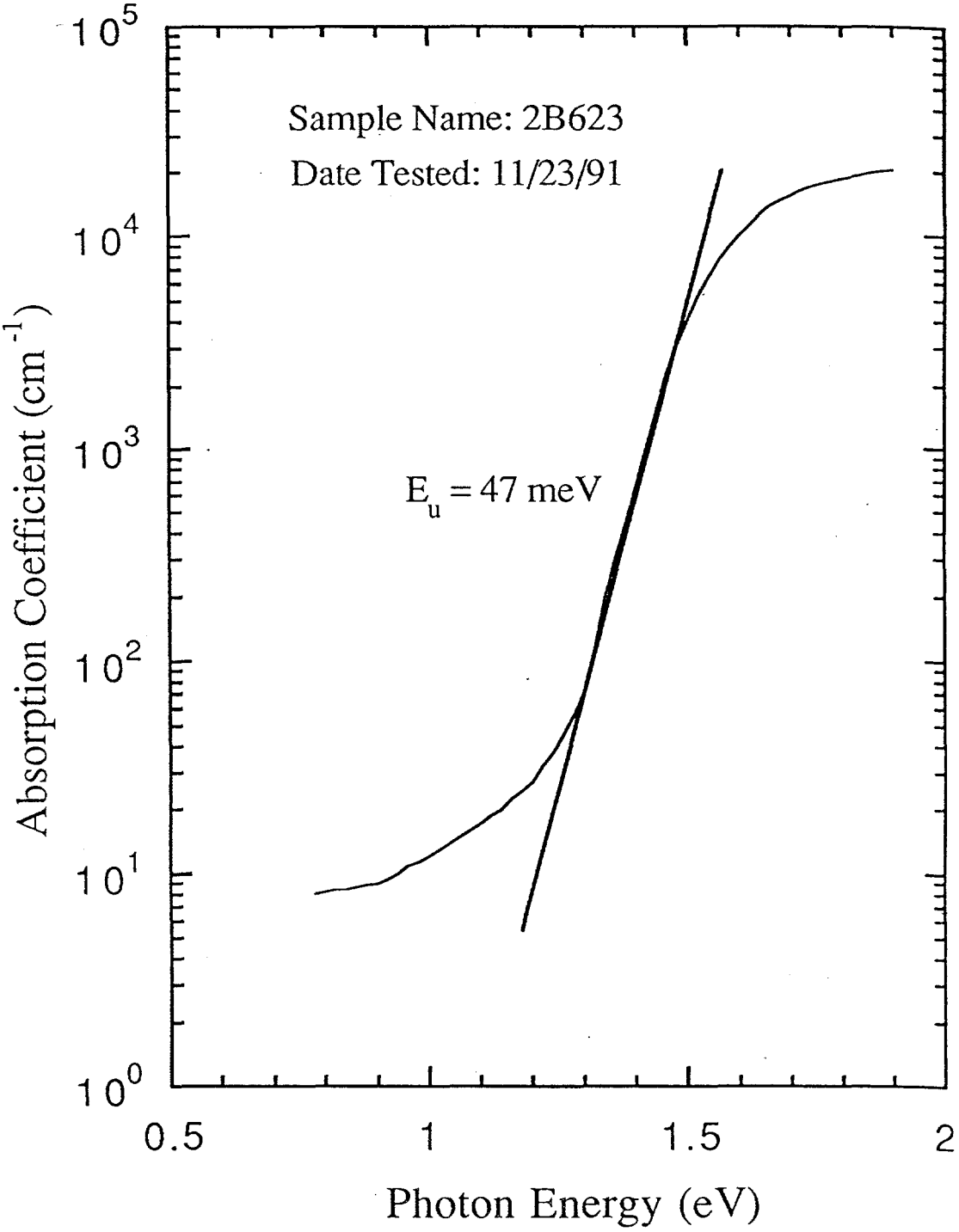


Fig. 3. Sub-bandgap absorption of the sample shown in Fig. 2.

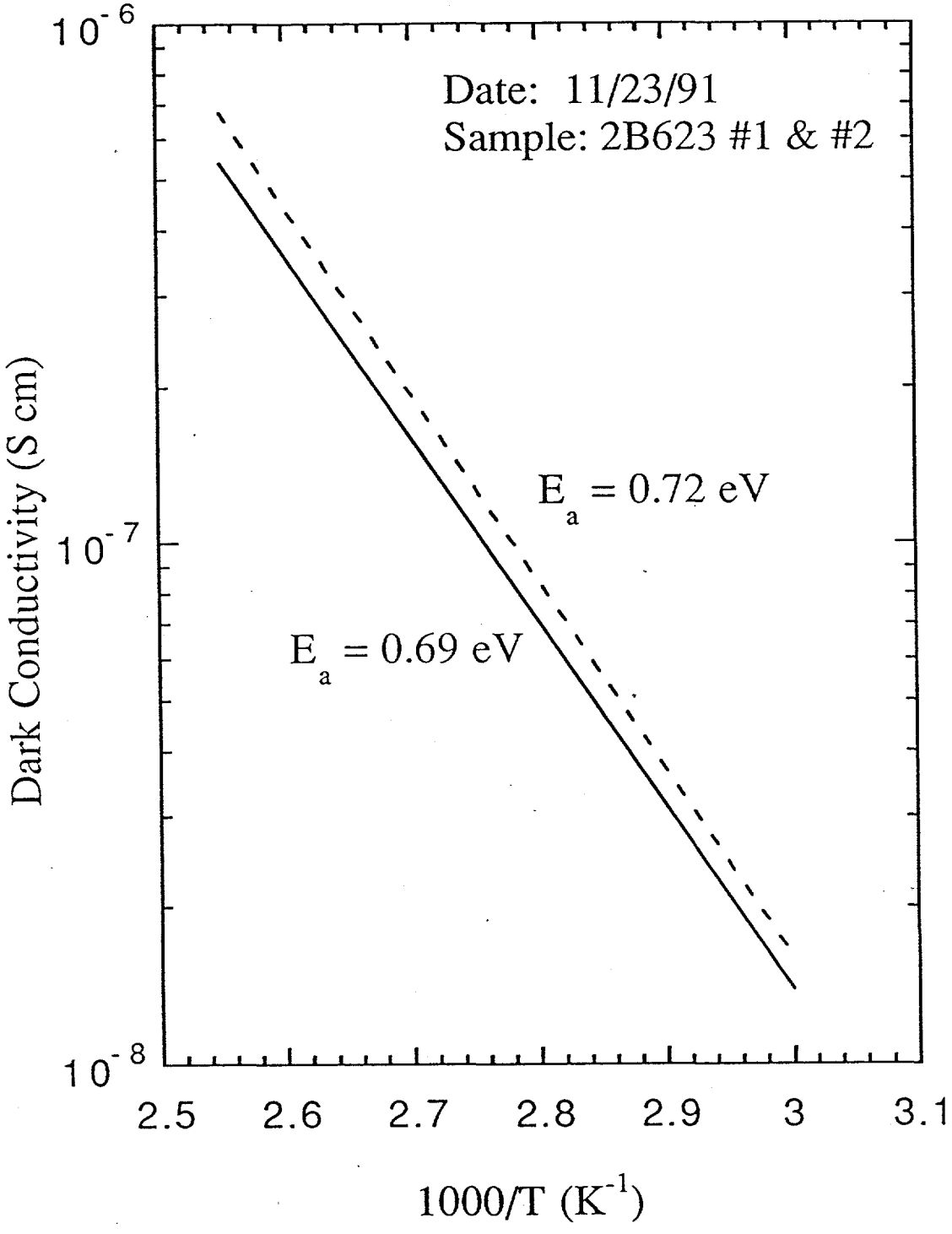


Fig. 4. Conductivity activation energy of the sample shown in Fig. 2.

Results on 2″ x 2″ Substrates

The J-V characteristics of a single-junction *n-i-p* a-Si:H cell as measured under global AM1.5 illumination are shown in Fig. 5. The active device area is 0.25 cm^2. The V_{oc} and FF of the cell are 0.915 V and 0.636, respectively. The J_{sc} of the cell has been obtained from the *Q* curve, and as shown in Fig. 6 the value is 16.57 mA/cm^2. Thus, the initial cell efficiency is 9.64% assuming the quantum efficiency measurement is correct.

The J-V characteristics and *Q* curve of a single-junction a-SiGe:H cell are shown in Figs. 7 and 8, respectively. The values of V_{oc}, J_{sc}, FF, and initial efficiency are 0.732 V, 20.16 mA/cm^2, 0.606, and 8.94%, respectively. The J-V characteristics of the same cell under a 630 nm red cut-on filter are shown in Fig. 9. The value of power, P_{max}, at the maximum power point is 3.35 mW/cm^2. A linear bandgap profiling was used for the intrinsic layer of this cell structure, and the bandgap of the a-SiGe:H film at the minimum bandgap point is ~ 1.4 eV.

The results of a double-junction, dual-bandgap cell are shown in Figs. 10 and 11, respectively. The cell structure consists of an a-SiGe:H bottom cell and an a-Si:H top cell. The bottom cell parameters are as in the cell of Fig. 9, and the intrinsic layer of the top cell has a bandgap of 1.8 eV. The values of V_{oc}, J_{sc}, FF, and efficiency are 1.639 V, 9.76 mA/cm^2, 0.69, and 11.04%, respectively. The *Q* curve shown in Fig. 11 shows that the top and bottom cells are pretty well matched. The top cell exhibits a value of J_{sc} equal to 9.83 mA/cm^2 and the bottom cell 9.93 mA/cm^2.

The J-V characteristics and *Q* curves of a triple cell are shown in Figs. 12 and 13, respectively. The cell architecture consists of an a-SiGe:H bottom cell as in the cell of Fig. 9 and similar bandgap (1.7 to 1.8 eV) a-Si:H middle and top cells. The values of V_{oc}, J_{sc}, FF, and initial efficiency are 2.334 V, 6.54 mA/cm^2, 0.656, and 10.02%, respectively. The component values of J_{sc} of the bottom, middle, and top cells are 7.28, 6.58, and 6.73 mA/cm^2, respectively. The deposition parameters for the triple cells are being optimized in order to enhance the device efficiency.

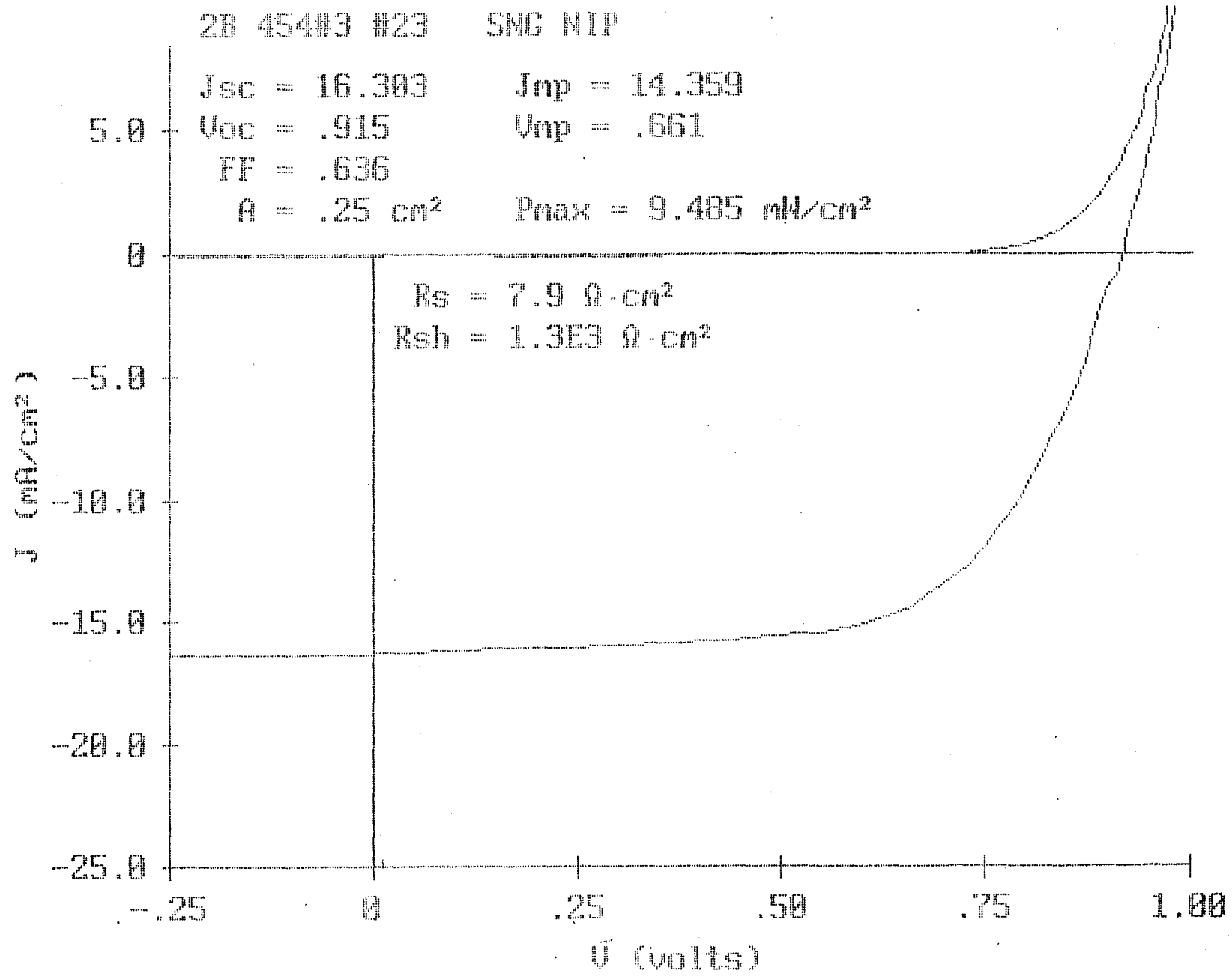


Fig. 5. J-V characteristics of a single-junction n-i-p a-Si:H cell.

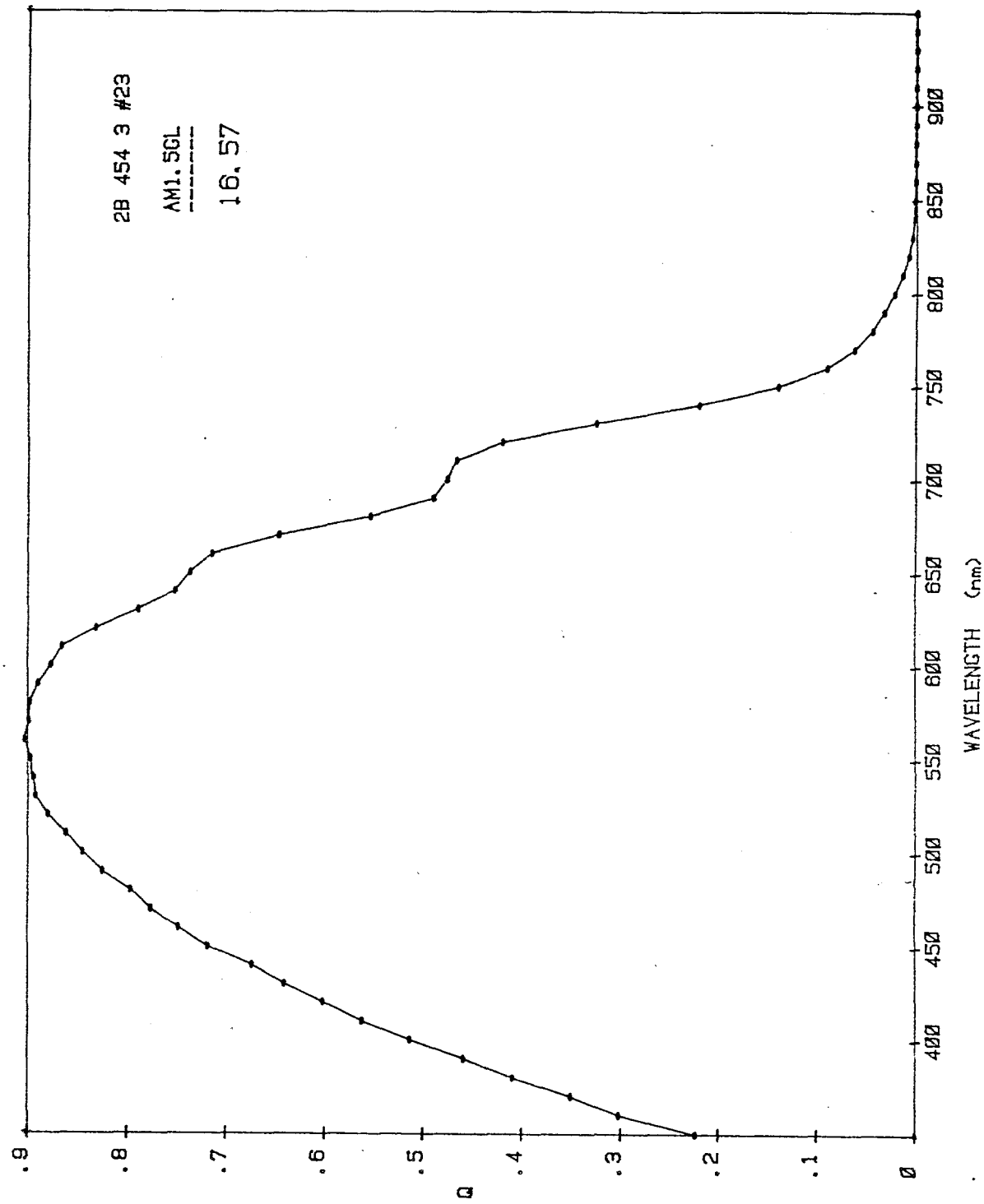


Fig. 6. Quantum efficiency characteristics of the cell shown in Fig. 5.

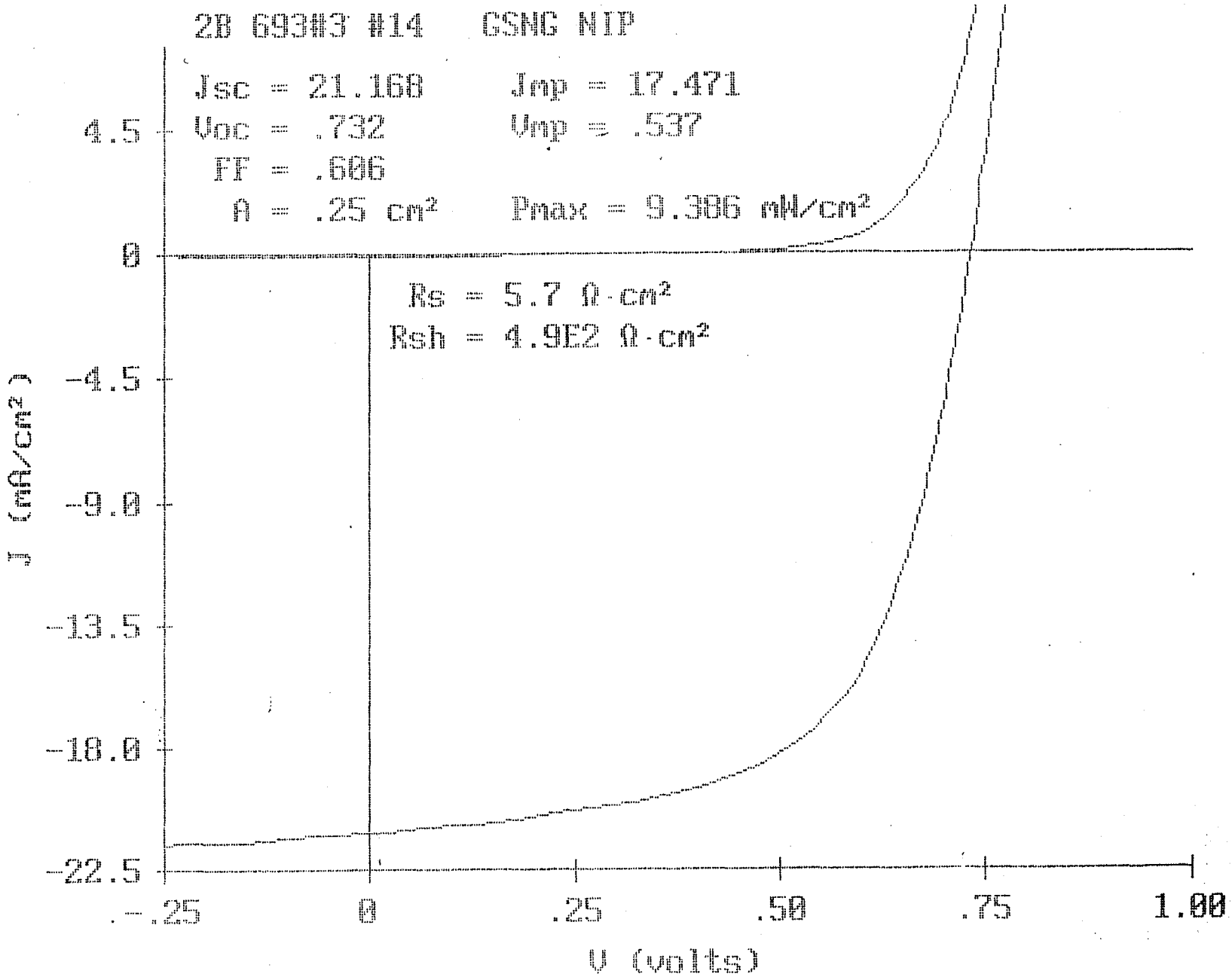


Fig. 7. J-V characteristics of a single-junction n-i-p a-SiGe:H cell.

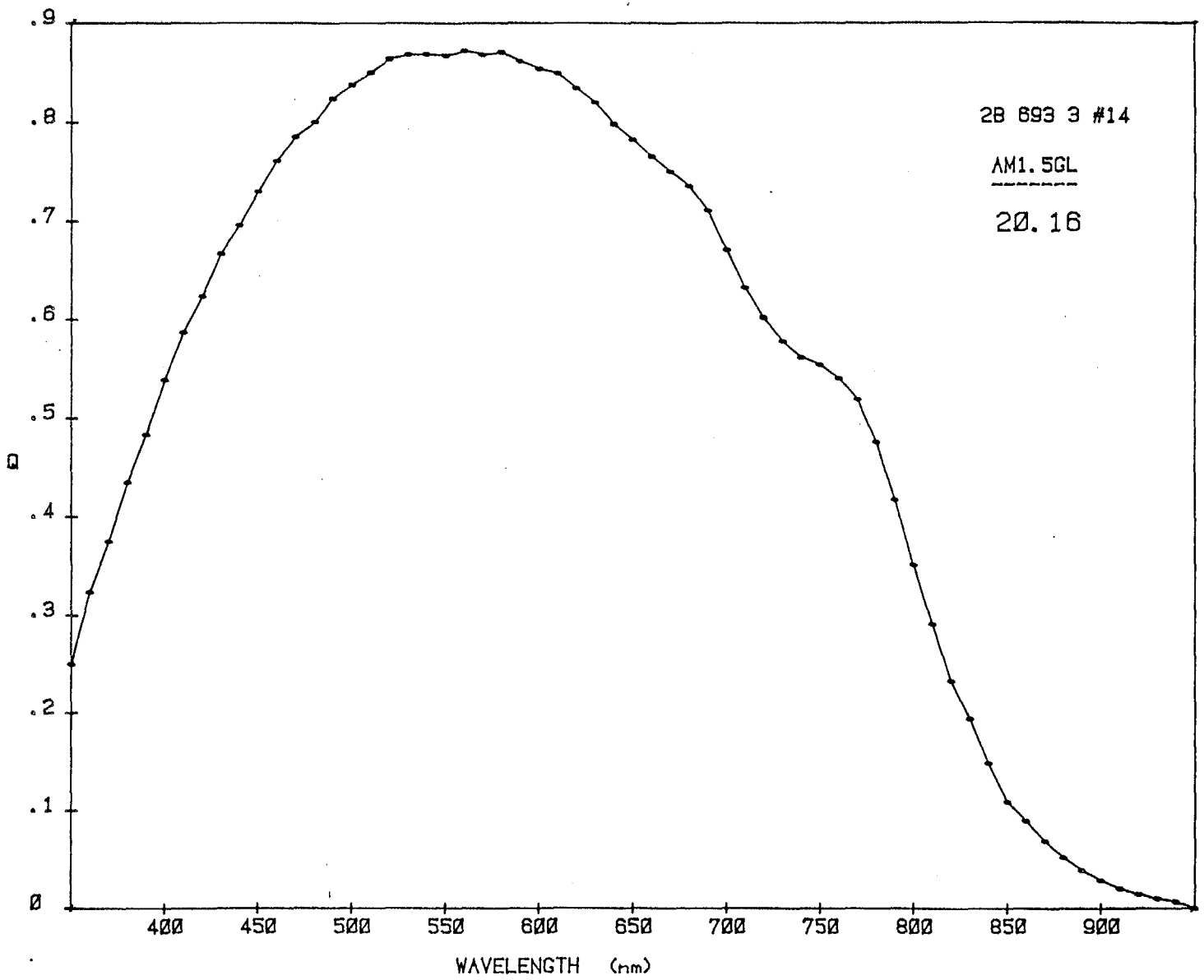


Fig. 8. Quantum efficiency characteristics of the cell shown in Fig. 7.

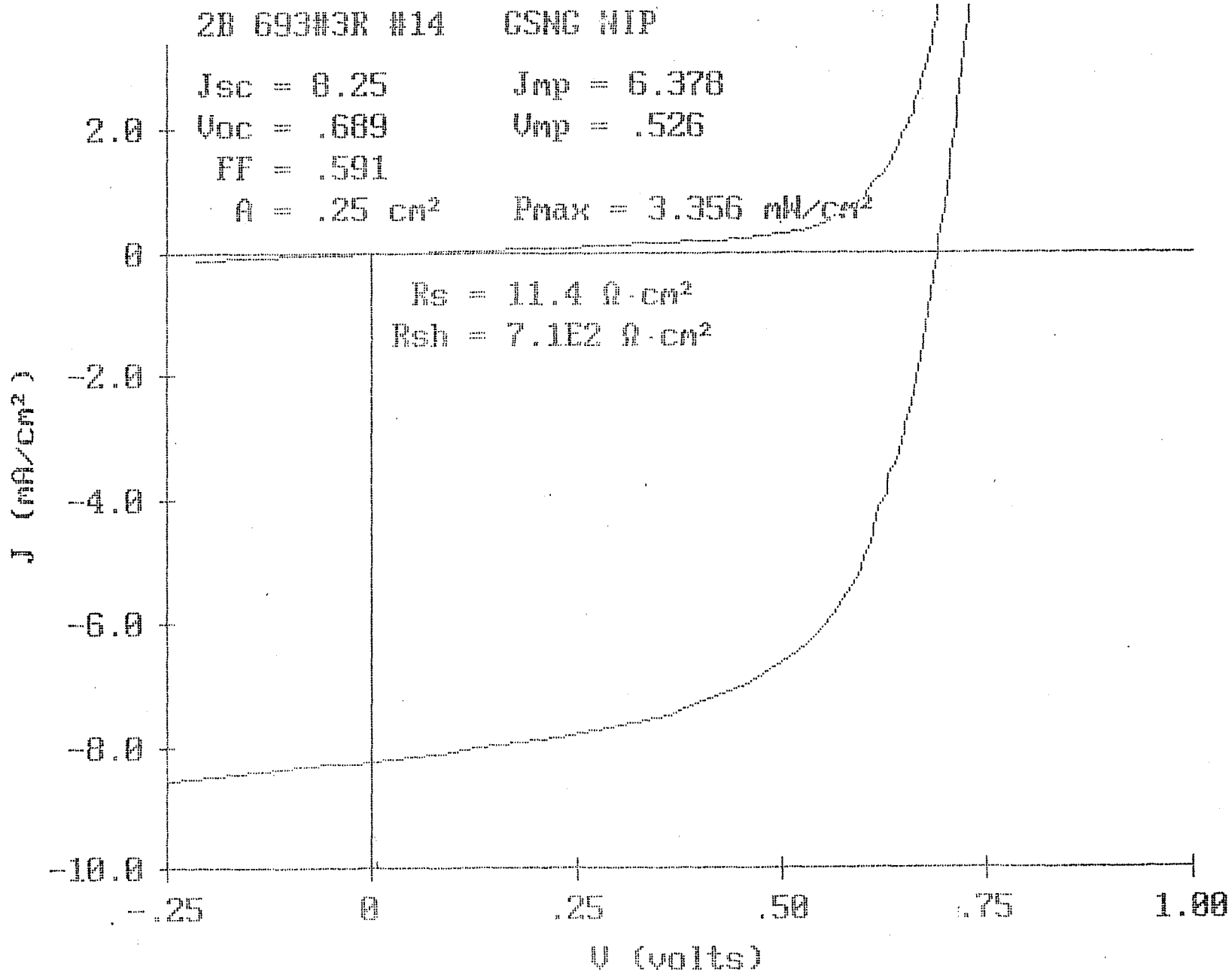


Fig. 9. J-V characteristics of the cell shown in Fig. 7 as measured with a 630 nm cut-on red filter.

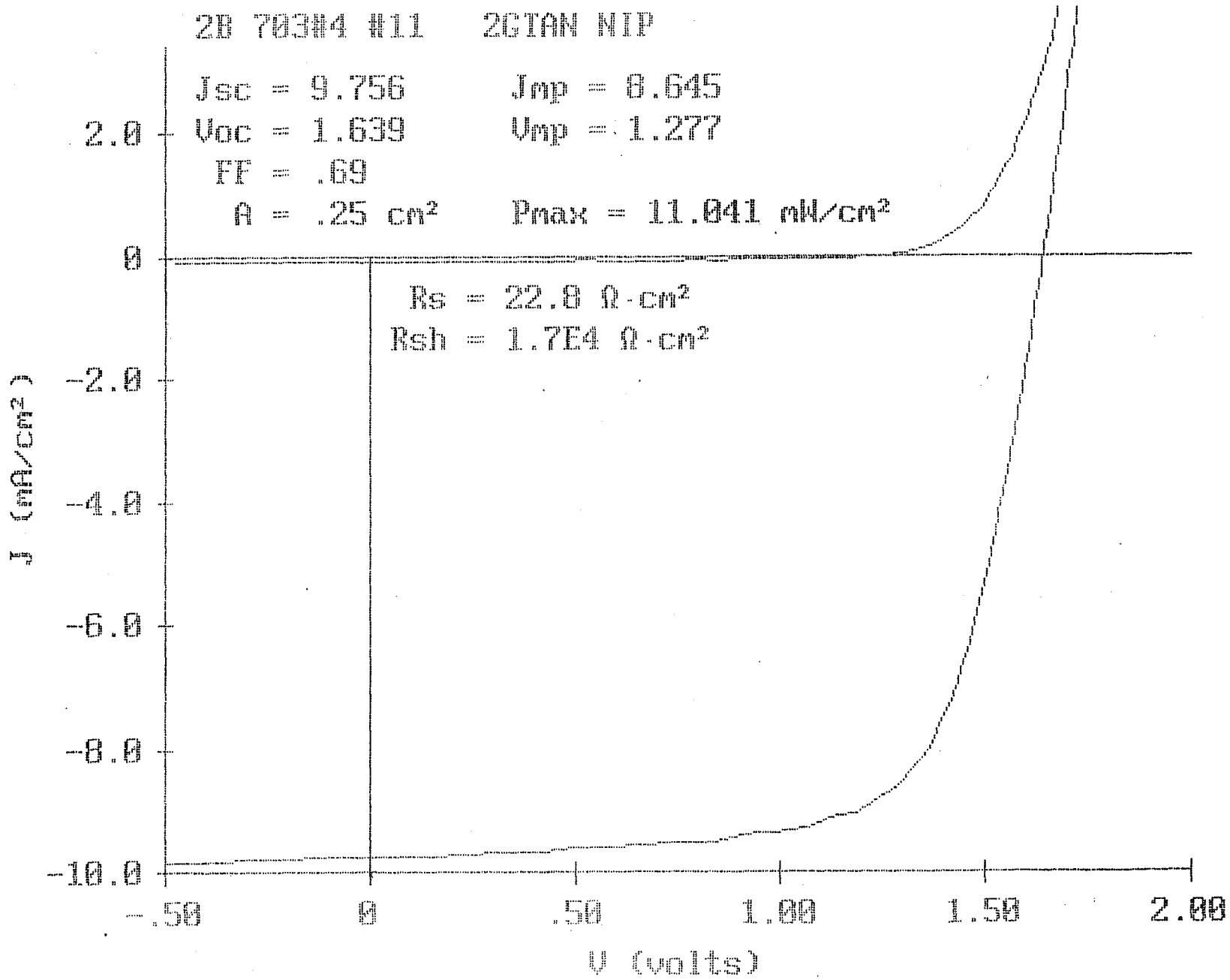


Fig. 10. J-V characteristics of a double-junction, dual-bandgap cell.

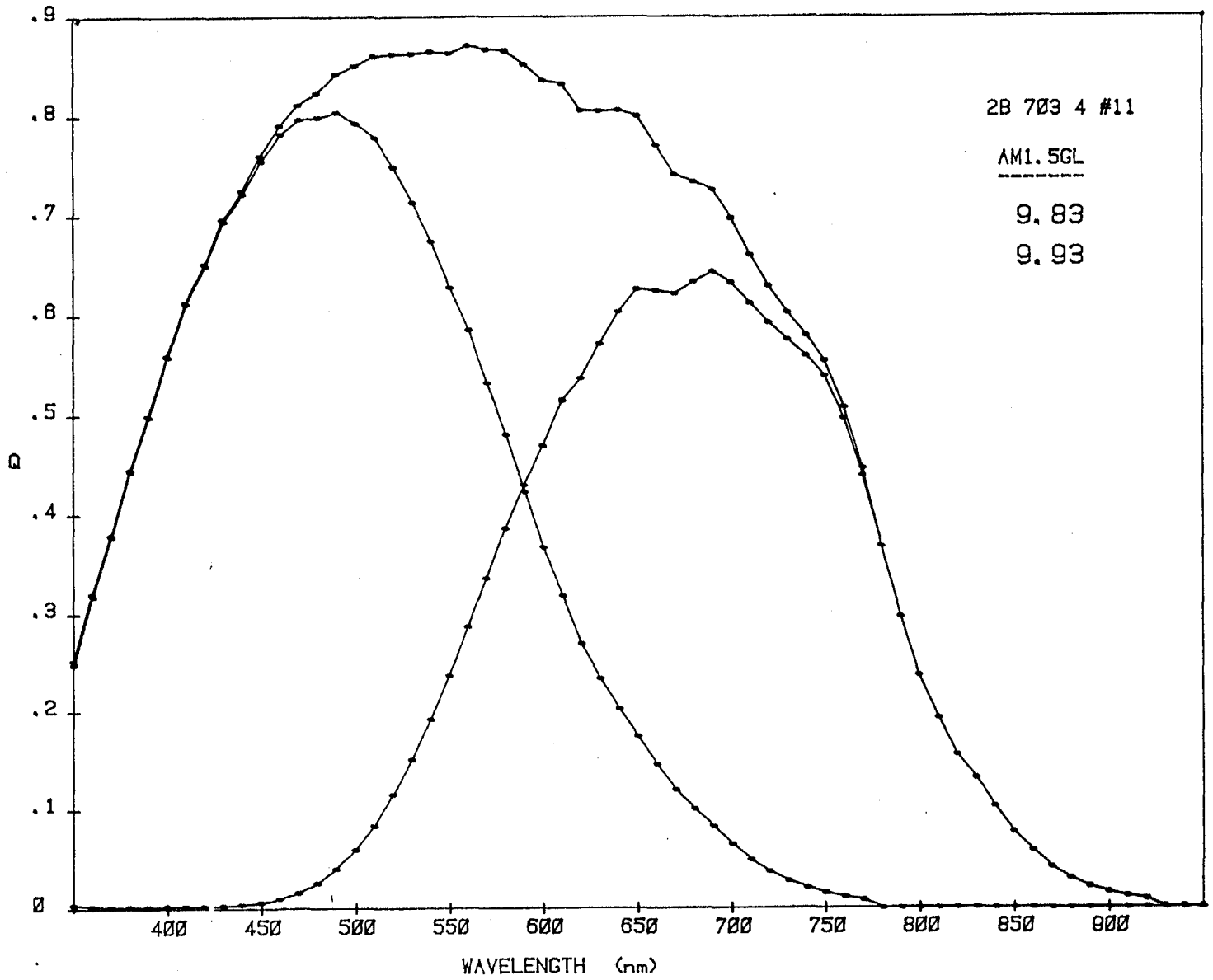


Fig. 11. Quantum efficiency characteristics of the cell shown in Fig. 10.

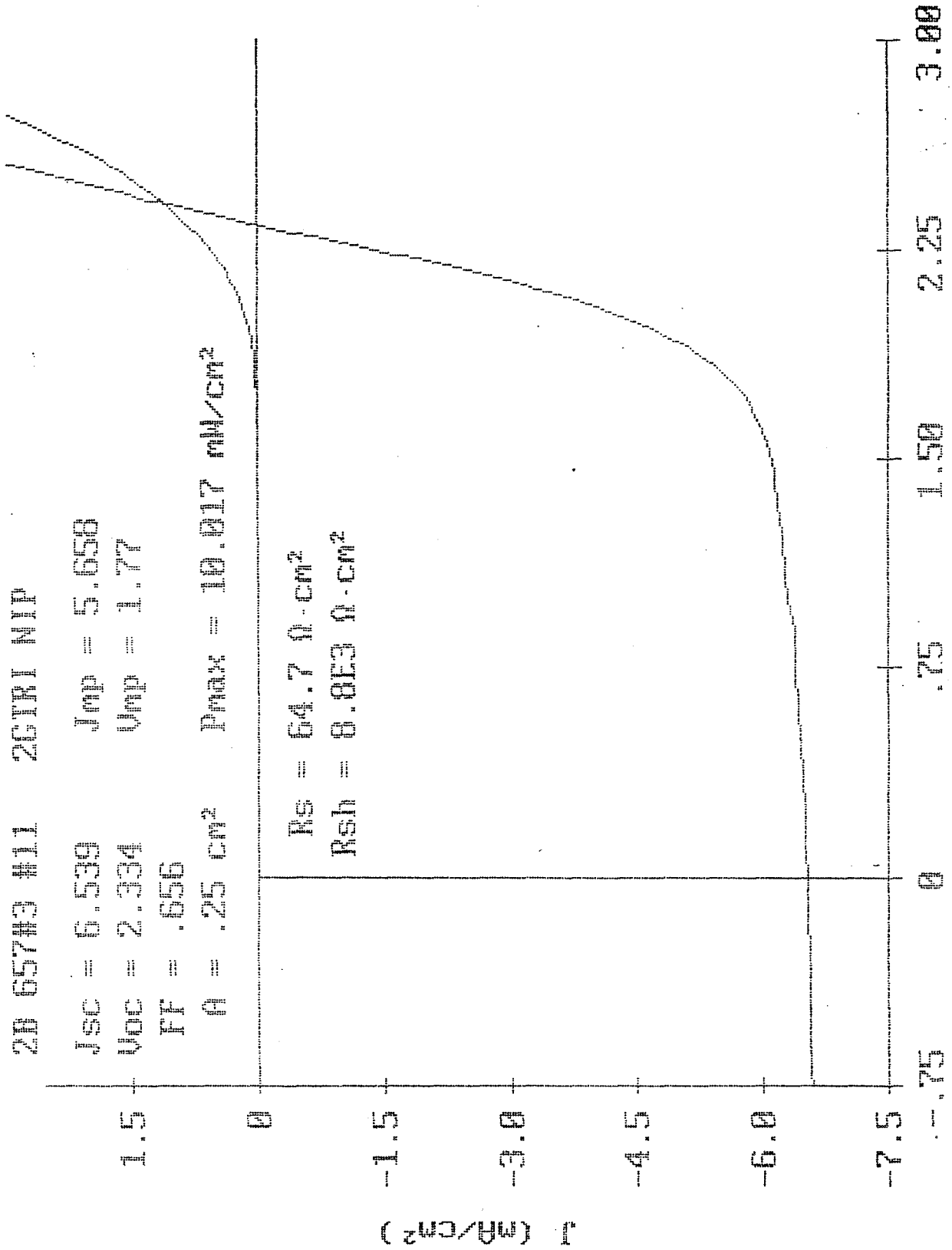


Fig. 12. J-V characteristics of a triple-junction, dual-bandgap cell.

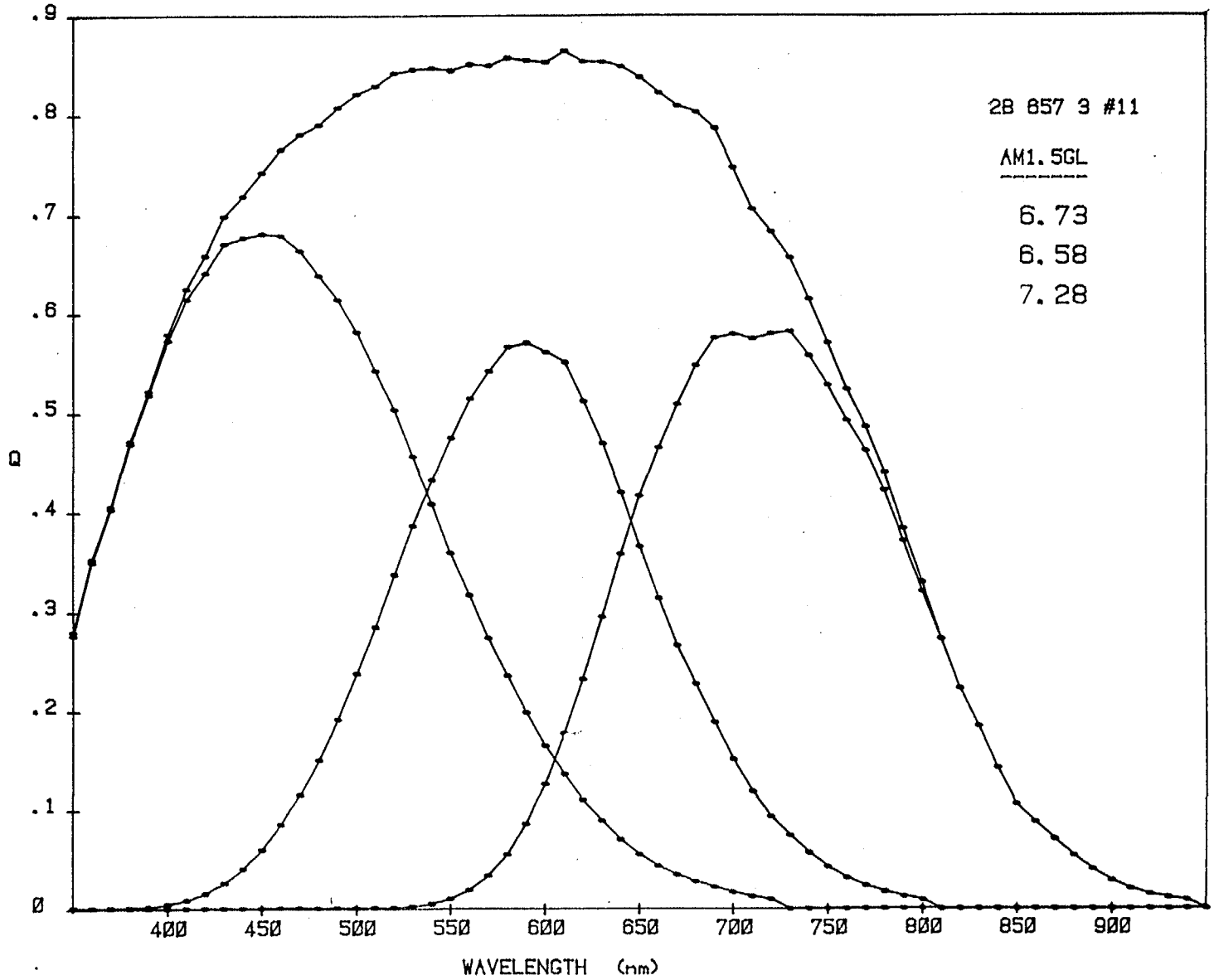


Fig. 13. Quantum efficiency characteristics of the cell shown in Fig. 12.

Results on Large-Area Substrates

The large-area substrates were processed in two different ways. In the first approach, the 1 sq. ft. device was delineated into smaller subcells, each of area 7.36 cm^2, in an array of 16 x 5 (total of 80 subcells) by etching the ITO suitably. This pattern allowed the evaluation of individual subcells for uniformity studies. In the second method, the 1 sq. ft. device was gridded and wired in order to fabricate a monolithic module. The results of a single-junction a-Si:H *n-i-p* cell which has been patterned into the 16 x 5 subcell array are shown in Fig. 14.

The subcell results are summarized in Table III which shows the performance of the best cell, five best cells, ten best cells, and all cells whose fill factor is greater than or equal to 0.45. This criterion was chosen to determine the occurrence of shunts and shorts in large-area cells. The right-hand column gives the average device performance of all working subcells over the 1 sq. ft. area. The difference between the average efficiency and the highest efficiency is less than 10%, which testifies to the uniformity of the deposition of all the different layers (back reflector, *n, i, p* and TCO).

Table III. Initial subcell results on single-junction a-Si:H *n-i-p* cell deposited on 900 cm^2 area.

	Best Cell	Best Five	Best Ten	FF ≥ 0.45
V_{oc} (V)	0.92	0.92	0.92	0.92
J_{sc} (mA/cm^2)	15.25	15.39	15.31	15.05
η (%)	8.84	8.78	8.70	8.12
FF	0.63	0.62	0.62	0.59

PHASE II B/NIP/2B517LA

Dev.#		Best #61	Best 10	Best 5	FF ≥ 0.45
76	0.93 V	0.92 V	0.92 V	0.92 V	0.92V
39	16.36 mA	15.25 mA	15.31 mA	15.39 mA	15.05 mA
61	8.84 mW	8.84 mW	8.70 mW	8.78 mW	8.12 mW
49	0.63 ff	0.63 ff	0.62 ff	0.62 ff	0.59 ff

Efficiency

Best 10 cells = 8.70%
Best 5 cells = 8.78%
FF ≥ 0.45 = 8.12%
Best cell = 8.84%

Yield = 93.8%
for cells with
FF ≥ 0.45

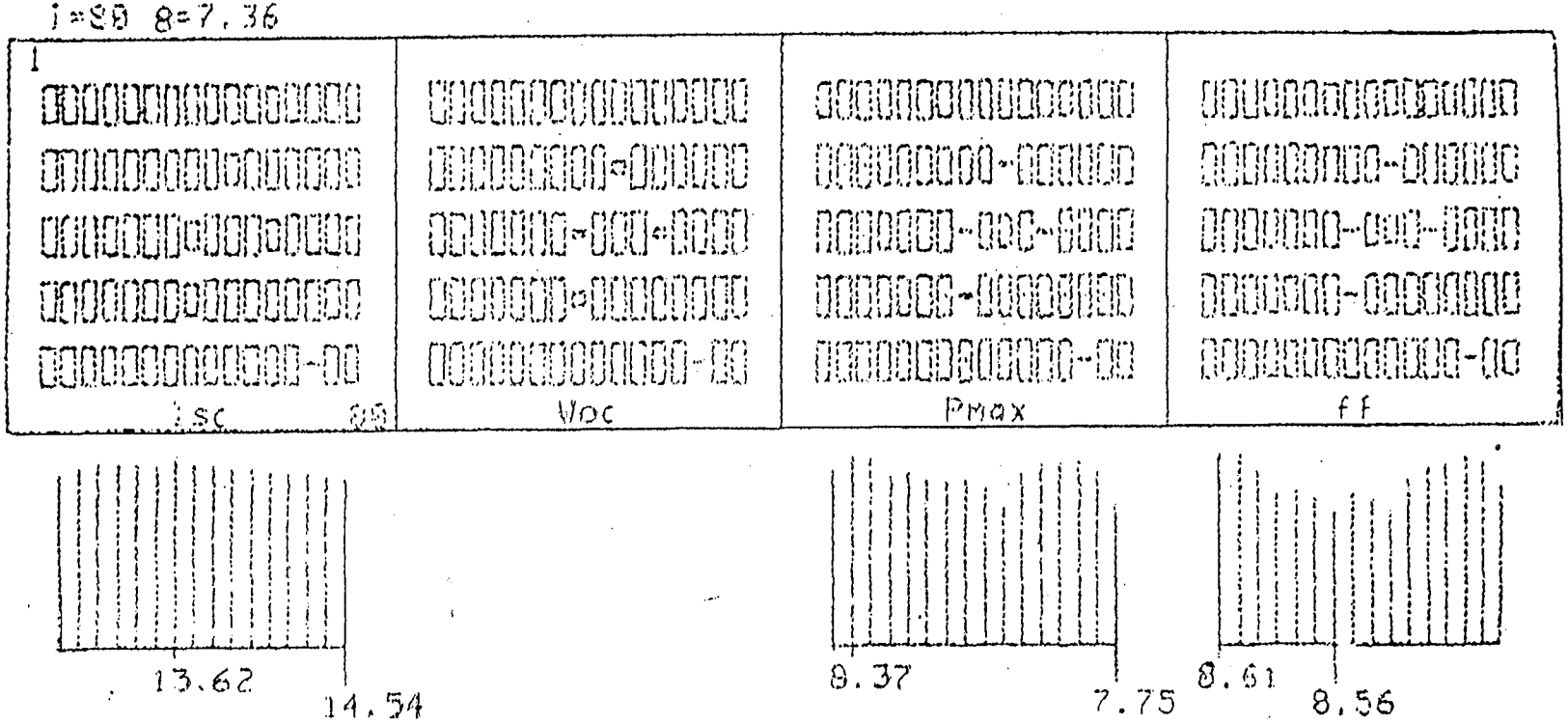


Fig. 14. Performance of single-junction subcells on 1 sq. ft. substrate.

Light-Induced Stability

Preliminary light-induced degradation investigations have been carried out on both dual-bandgap, double- and triple-junction cells. Some of the results of the double- and triple-junction cells made in the IIB machine are summarized in Tables IV and V, respectively. The cell architecture is the same as described earlier, i.e., a-Si:H/a-SiGe:H for the double-junction and a-Si:H/a-Si:H/a-SiGe:H for the triple-junction structures. Table IV shows the degradation behavior of three different double-junction cells made with different top cell and bottom cell thicknesses. The relative thicknesses are described by the relative deposition times of the top and bottom cells. The results show that the stabilized efficiency after ~ 500-hour exposure is close to 8%. The triple-junction cell stability result shown in Table V shows that the extent of degradation is less than that in the double-junction cells. It is expected that with further optimization of the double- and triple-junction cells, the initial efficiency would be higher and the corresponding stabilized efficiency will be well over 8%. For example, using an average degradation value of ~ 18% for the double-junction cells in Table IV, the cell whose characteristics are shown in Fig. 10 would stabilize at ~ 9.0%.

Table IV. Efficiency of dual-bandgap, double-junction cells of active area 0.25 cm^2 after one-sun exposure at 50°C for various times.

Sample No.	493	494	519
Top cell deposition time (min)	12	8	10.5
Bottom cell deposition time (min)	20	12	16
Efficiency (%)	9.90 (0 hr)	9.37 (0 hr)	9.73 (0 hr)
	8.48 (96 hr)	8.03 (96 hr)	8.52 (50 hr)
	7.90 (496 hr)	7.66 (498 hr)	8.10 (520 hr)

Table V. Stability of dual-bandgap, triple-junction cell of active area 0.25 cm^2 after one-sun exposure at 50°C.

Sample No.	582
Top cell deposition time (min)	4.5
Middle cell deposition time (min)	20
Bottom cell deposition time (min)	20
Efficiency (%)	9.14 (0 hr)
	7.73 (360 hr)

As mentioned earlier, the triple-junction cells are not yet optimized, and that explains why both the initial and final efficiencies of these cells are lower than those of double-junction devices.

2.3 Non-Semiconductor Materials and Deposition

We have used stainless steel substrates for all the work. The back reflector material used for the devices is Ag/ZnO, which was deposited using a dc magnetron sputtering machine specially constructed for this program. The machine can use up to three sputtering targets, and the substrate can be moved back and forth to ensure uniform deposition over 1 sq. ft. area. The thickness uniformity is better than ±10%.

Typical deposition parameters for the ZnO and Ag films are pressure ~ 1-10 milli-Torr and substrate temperature ~ 100-400°C. The top transparent conducting contact (Indium Tin Oxide) has been prepared by reactive evaporation. The substrate temperature is ~ 175-225°C. The thin ITO layer also acts as the antireflection coating. The optical absorption of this layer is < 2%, and the sheet resistance is ~ 75-100 ohm/square. The uniformity of the combined back reflector, semiconductor layers, and TCO coating over a 1 sq. ft. area can be evaluated from the 1 sq. ft. device performance shown in Table III where we find that the difference between the best device efficiency and the average efficiency is less than 10%.

SECTION 3
MODULE DESIGN AND CHARACTERIZATION

3.1 Grid Design Calculations

The first step in the module design was to develop a model to calculate the optimal grid coverage for either a series-connected or monolithic-type module. This model solves for a minimum in the power loss equation. This equation is comprised of two terms. The first term involves the addition of all shadowing losses. These are the finger loss, bus loss, etch-line loss, and bus-to-finger connector loss. The second term involves the functional dependencies of all the electrical losses. The total electrical loss will depend primarily on six variables. These variables are the length and width of the grid fingers, the distance from the tip of each finger to the etch line, the distance between fingers, and the conductivity of the ITO and metalization. This may be seen schematically in Fig. 15.

An exact solution to this problem for a module by some numerical method was not achieved. The approach we did choose was to find an exact solution to a unit cell that has all the relevant variables associated with it as seen in Fig. 15. The maximum area that could be solved readily is about 10 cm^2. The exact method used to solve this smaller area problem ($< 10\ cm^2$) has been described in a previous SERI subcontractor's semiannual report [2]. Briefly, this program calculates potential profiles across the device by dividing the device in small mathematical elements. These elements may be either ITO elements or grid elements at any position depending on the geometry of the device. Each element mathematically becomes a single-node equation. The program then alters the operating voltages in order to minimize the residual currents in each node. Once the residual currents of each element become sufficiently small, we may calculate the power output and evaluate the electrical loss of this geometry.

We varied each parameter (L_{grid}, L_{edge}, W_{grid}, W_{ITO}, P_{grid}, P_{ITO}) independently to evaluate the effect a change in that parameter had on the unit cell power output. What we were then left with was the unit cell power loss versus these six independent variables.

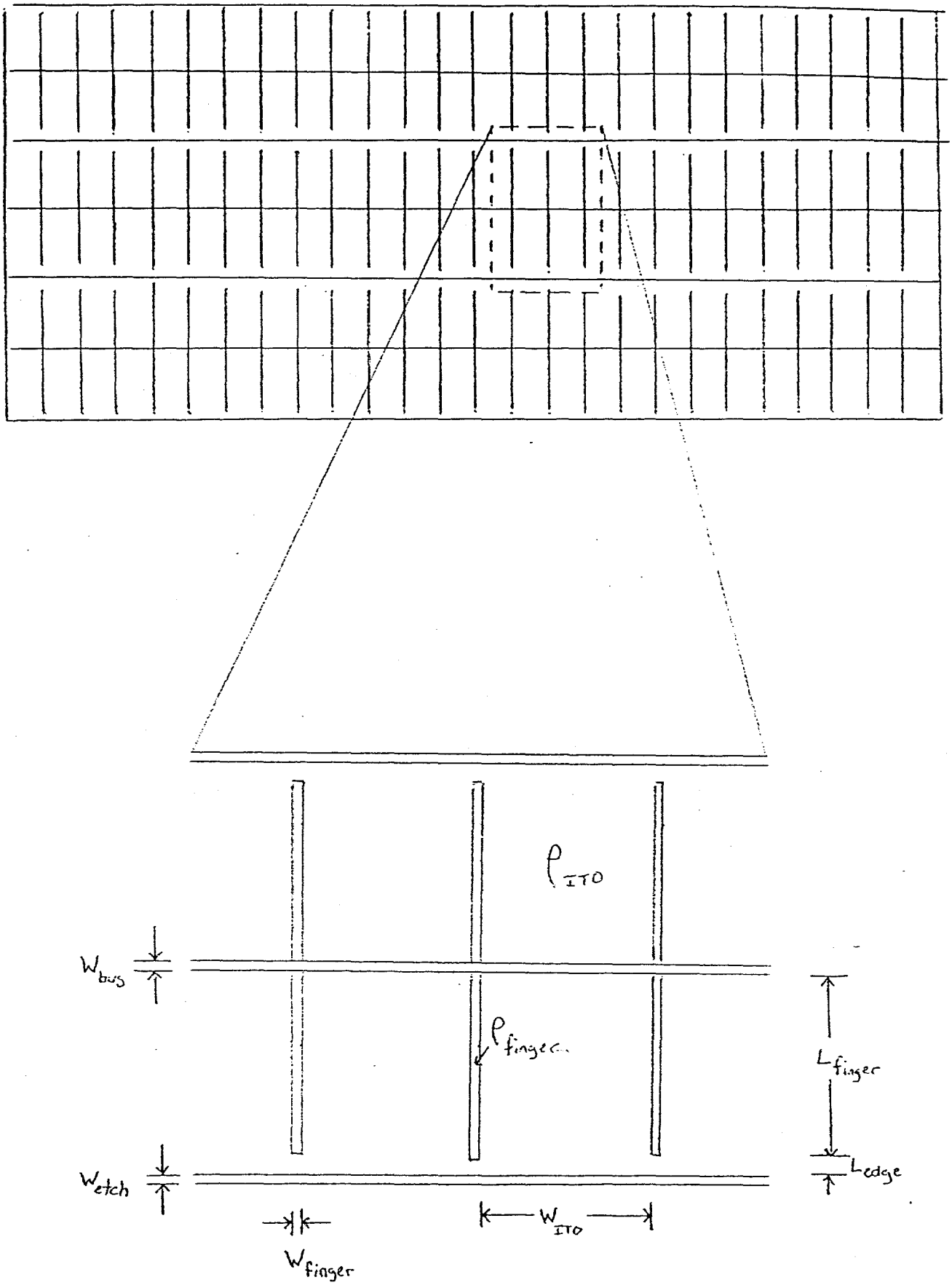


Fig. 15. Schematic of the unit cell and the associated variables used in the grid design optimization.

3.2 Loss Analysis

The next step was to empirically find the functional form in which these parameters described the power loss. Several functional forms were tested using an error minimization routine that matched the losses that were calculated using the empirical formula with those calculated from the exact solution. The functional form that matched best was the product of power law functions of each parameter such as m_1 x, γ_1 where γ_1 is the power for parameter one (e.g., L_{grid}), m_1 is the coefficient for parameter one, and x is the actual distance in cm. The reason for this approach was that the exact solution for each unit cell requires several hours to calculate and the functional form milliseconds. We may therefore try many more cases using this method.

Once we have obtained all the coefficients and powers for each parameter, we plug this formulation in for the electrical losses and add the shadowing losses. These losses are then minimized using an error minimization routine to find the physical dimensions of the module. We have assumed that parameters such as interstrip etch thickness and bus bar widths are fixed by present technology and total module dimensions by definition.

In Fig. 16 we show a plot of the total power loss, shadowing plus electrical, for a 1 ft^2 monolithic module versus the number of bus bars and the finger spacing. The ITO and grid resistance in this case were 250 ohm and 0.02 ohm, respectively. The minimum total power loss was 7.6% using 8 bus bars and 0.84 cm finger spacing. The two components of loss (shadowing and electrical) for this module case are broken down in Figs. 17 and 18. Note from Fig. 17 that the shadow loss rises quickly as the finger spacing is reduced, and the shadow loss rises slowly with an increase in the number of bus bars. In Fig. 18 we have the opposite trends, i.e., the electrical loss increases with increasing finger spacing and decreased number of bus bars. At the minimum in total loss, the shadow loss comprises approximately 2/3 of the total and the electrical loss 1/3.

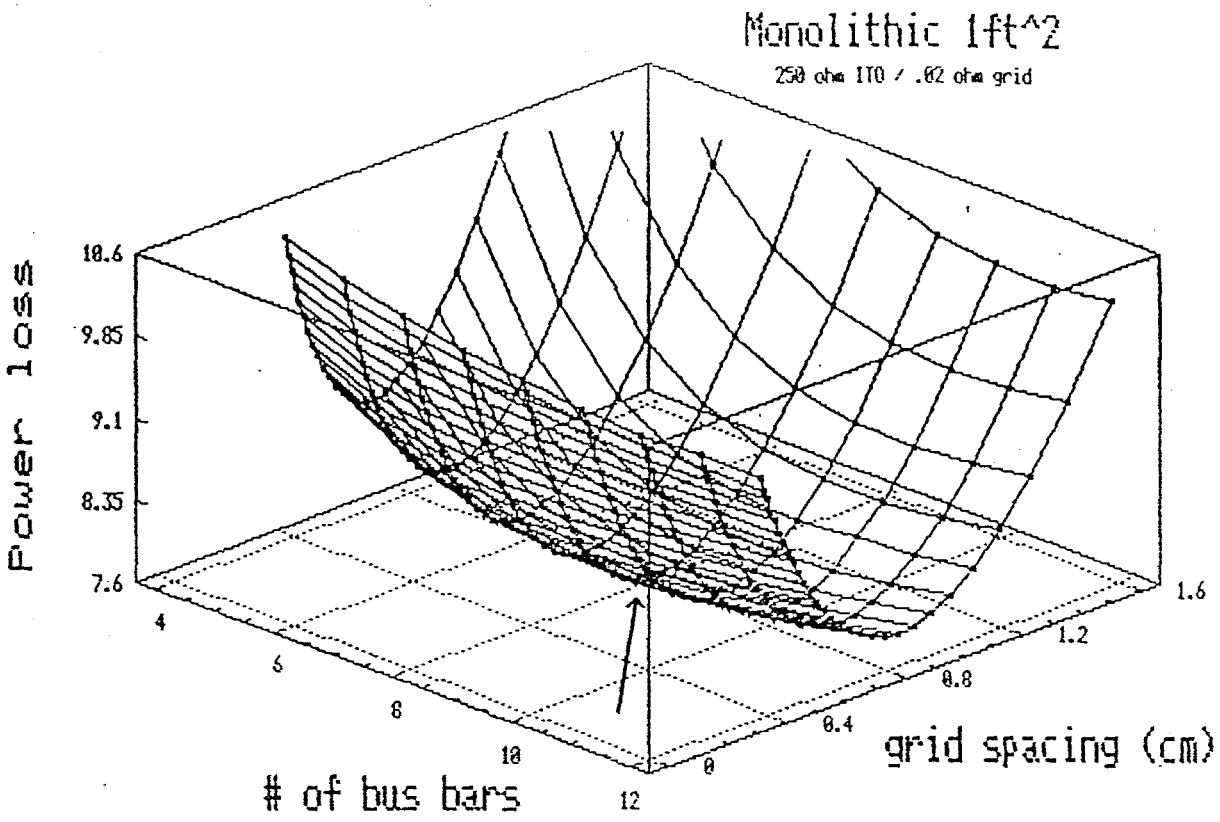


Fig. 16. Total power loss, electrical plus shadowing, for a 1 ft^2 monolithic-type module versus number of bus bars and finger spacing.

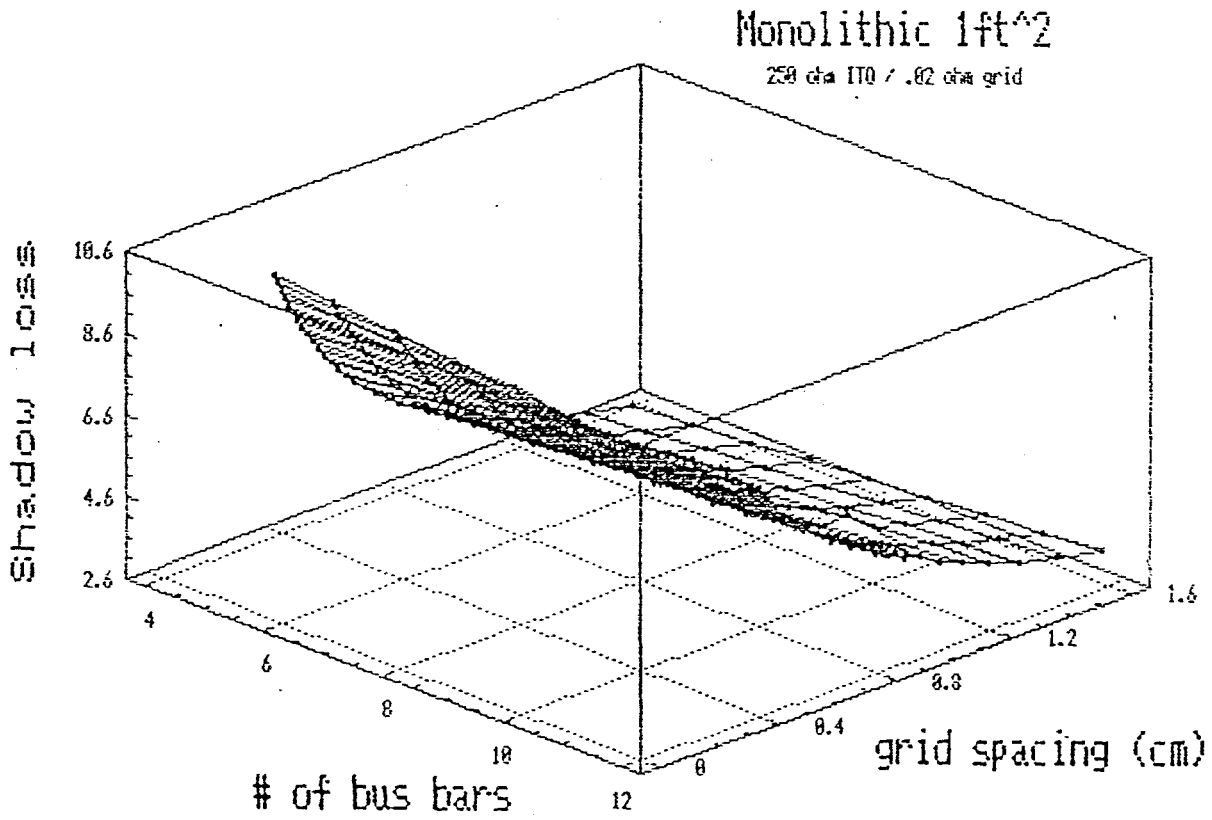


Fig. 17. Shadow loss component of the total power loss function in Fig. 16.

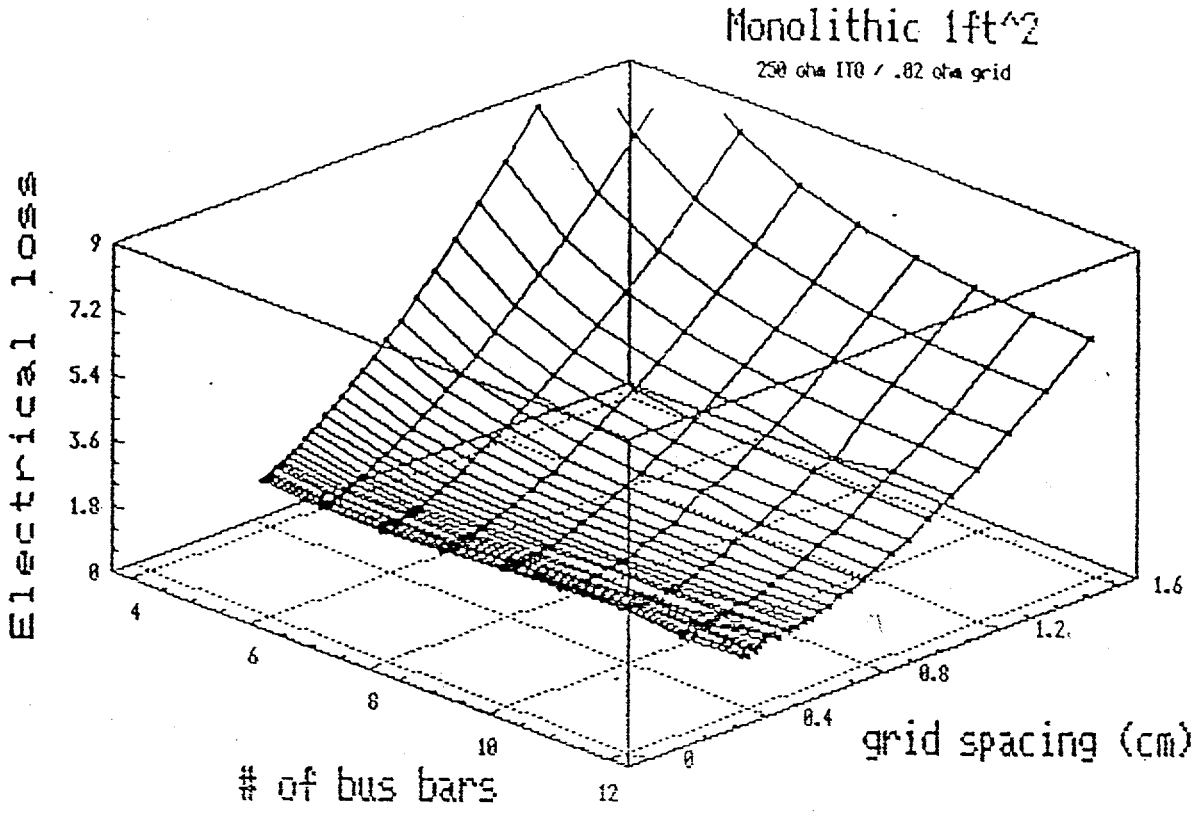


Fig. 18. Electrical loss component of the total loss power function in Fig. 16.

A summary of power loss minimum for the two module cases, monolithic and series connected, for several values of ITO and grid sheet resistance are tabulated in Table VI. There are several points of interest in this table. First, there is about a 1% power loss difference between the two types of modules for one value of ITO and grid resistance due to the strip interconnect distance in the series-connected module. There is also an approximately 0.5% difference in power loss for every 50 ohm reduction in ITO resistance. There was a relationship assumed between grid resistance and grid width. The grid width for a grid resistance of 0.02 ohm was about 0.35 mm, while the grid width for a 0.2 ohm grid resistance was about 0.15 mm. It was decided to optimize the grid pattern for an ITO resistance of 100 ohm/square and a grid resistance of 0.028 ohm/square and 0.25 mm grid width. This module will give a total power loss of 6.6% for the series-connected case and 5.7% for the monolithic case.

Table VI. Summary of power loss minimum for the monolithic-type and series-connected module.

Resistances (ohm per square)		Power Loss (%)	
		Series Connected	Monolithic
ITO	Grid		
50	0.02	6.4	5.5
50	0.2	5.3	4.5
100	0.02	7.3	6.3
150	0.02	7.9	6.8
250	0.02	8.7	7.6
250	0.2	7.2	6.3
100	0.028	6.6	5.7

3.3 Encapsulation

Specifications for a superstrate encapsulant structure are extremely demanding. All these materials must have very high transmission throughout the visible spectrum, be extremely ultraviolet resistant, have low water-permeability coefficients, and must be resistant to embrittlement and cracking for at least a twenty-year period. They must also have good adhesion properties, under extreme temperature and humidity conditions, to the underlying solar cell as well as to the other materials in the stack. They must be economical, easy to apply into large, uniform areas, and provide good coverage over all surface irregularities.

To meet these requirements, we use a multilayer structure of EVA and Tefzel. The EVA has high transmission, excellent adhesion properties, as well as being economically viable. The Tefzel, along with high transmission properties, has one of the lowest water permeability coefficients of any plastic and excellent ultraviolet protection for all the underlying layers.

These layers are applied onto the solar cell by laying them flat to the surface and curing under vacuum to remove any air trapped between layers. The curing temperatures that provide maximum properties are between 130 and 160°C.

Figure 19 shows the quantum efficiency of a cell before and after encapsulation. It can be seen that most of the difference is in the deep blue due to absorption and in the central region due to an increase in reflection resulting from the encapsulant altering the antireflection properties of the AR coating. Figure 20 shows the quantum efficiency of the cells shown in Fig. 19, normalized by their reflection. The difference in the two curves is approximately equal to the spectral absorption of the encapsulation materials.

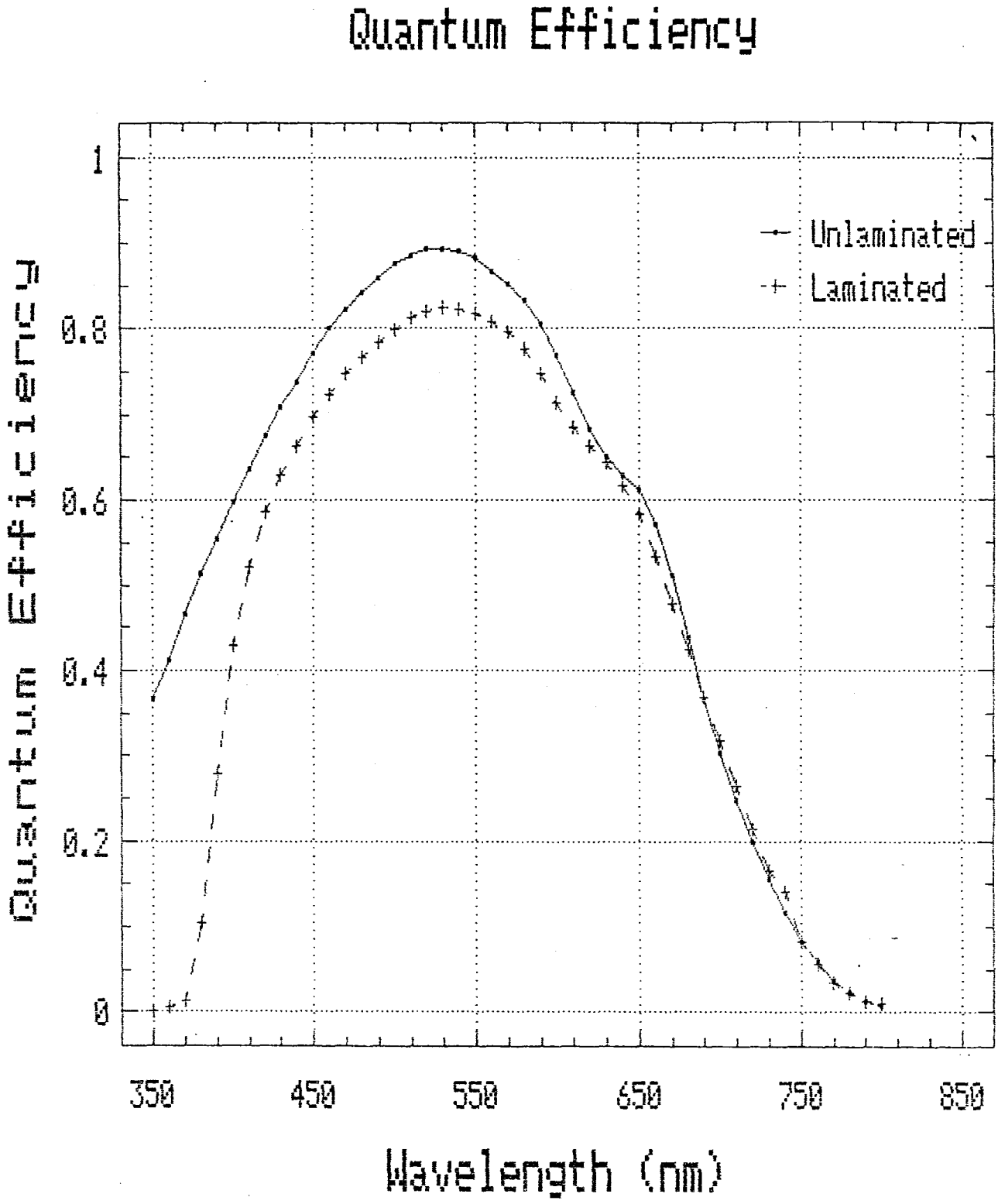


Fig. 19. Quantum efficiency of a single-junction a-Si:H device before and after lamination.

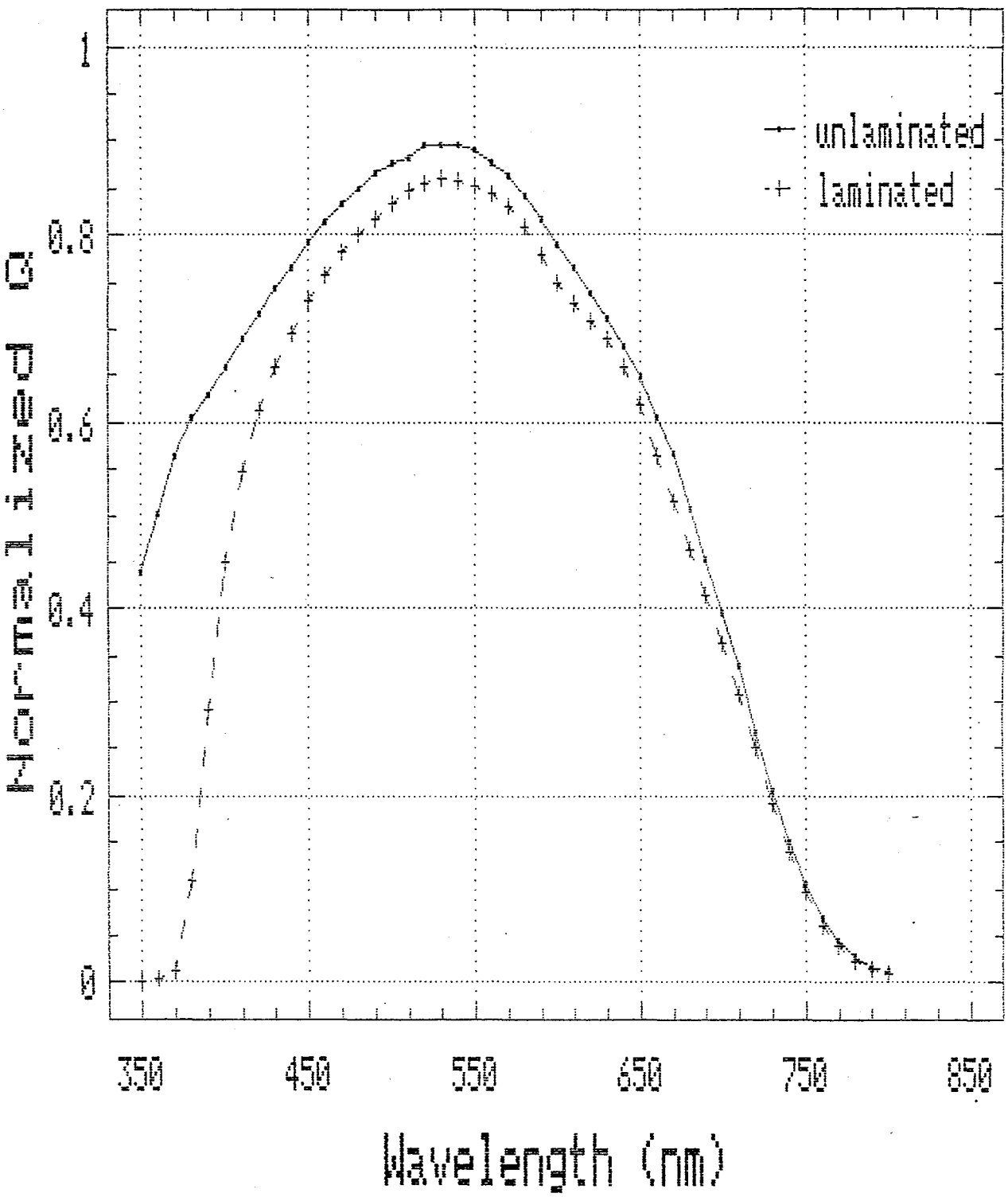


Fig. 20. Quantum efficiency shown in Fig. 19 normalized by one minus the front surface reflection (Q/(1-R)).

3.4 Interconnect Schemes

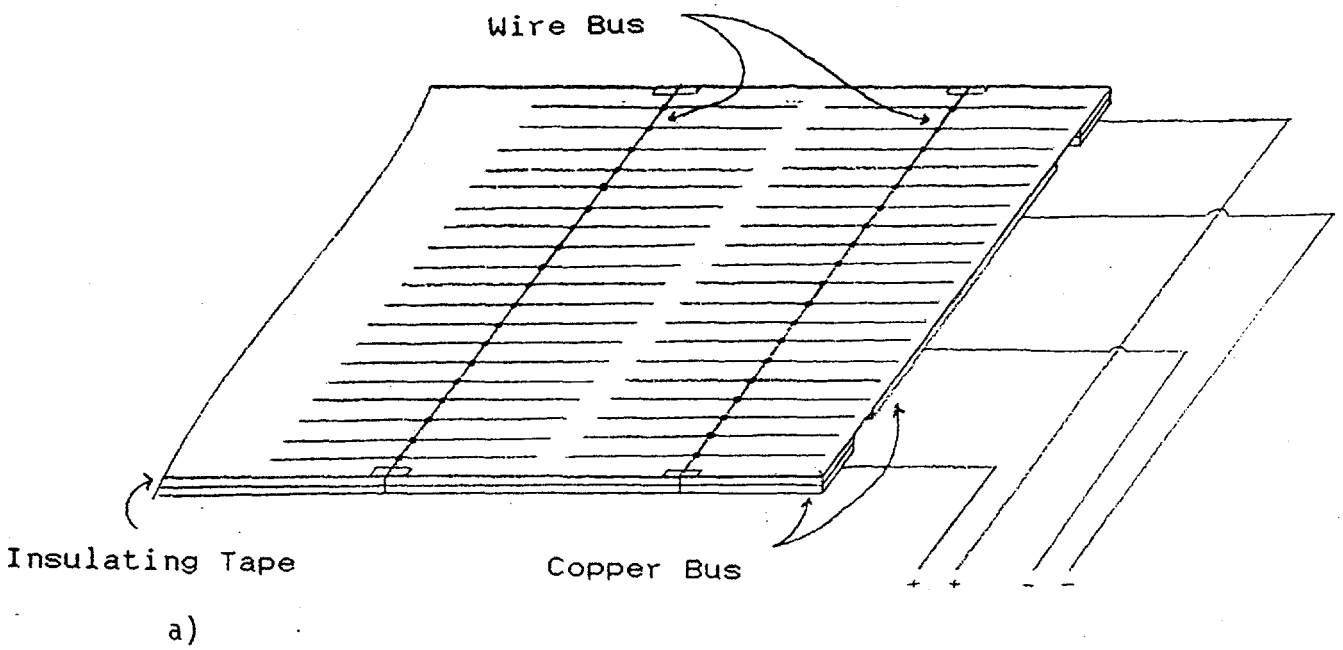
Figures 21a and 21b show the present interconnect scheme for the monolithic-type module and the series-connected module, respectively. After the BR/a-Si/ITO deposition, the module aperture area is then defined by ITO isolation with an etchant. In the case of the series-connected module, the strips are also isolated (to prevent ITO to ground contact when slabbing strips) using this etchant. The edge isolation line is 0.060″, while the strip isolation line is 0.030″. The isolation resistance is about 5 kohm. Next, the fingers are applied using a silver epoxy, screen printed onto the ITO surface, and cured. These lines are 250 μm wide by 4.7 cm with a conductivity of approximately 0.02 ohm/sq. The wire bus (26 AWG) is connected to each finger with silver epoxy and cured. The approximate diameter of each connecting dot is 2 mm.

The module, in the series-connected case, is next slabbed into six strips. Interconnection between strips is made by spot welding 1/8″ copper foil to ground, and the foil is soldered to wire bus bar of the neighboring strip. All isolation of copper and wire bus from ground is done with a 0.005″ polyester tape. In the monolithic-type module, wire bus bars are connected to 3/8″ copper foil. Modules are finally encapsulated in an EVA/Tefzel structure.

In Table VII we show the loss analysis for the present module design. The major loss mechanisms are shadowing losses due to fingers, wire bus bars and connecting dots, electrical losses due to ITO, fingers and wire bus bars, interconnect resistance and inactive interconnect areas, and encapsulation transmission.

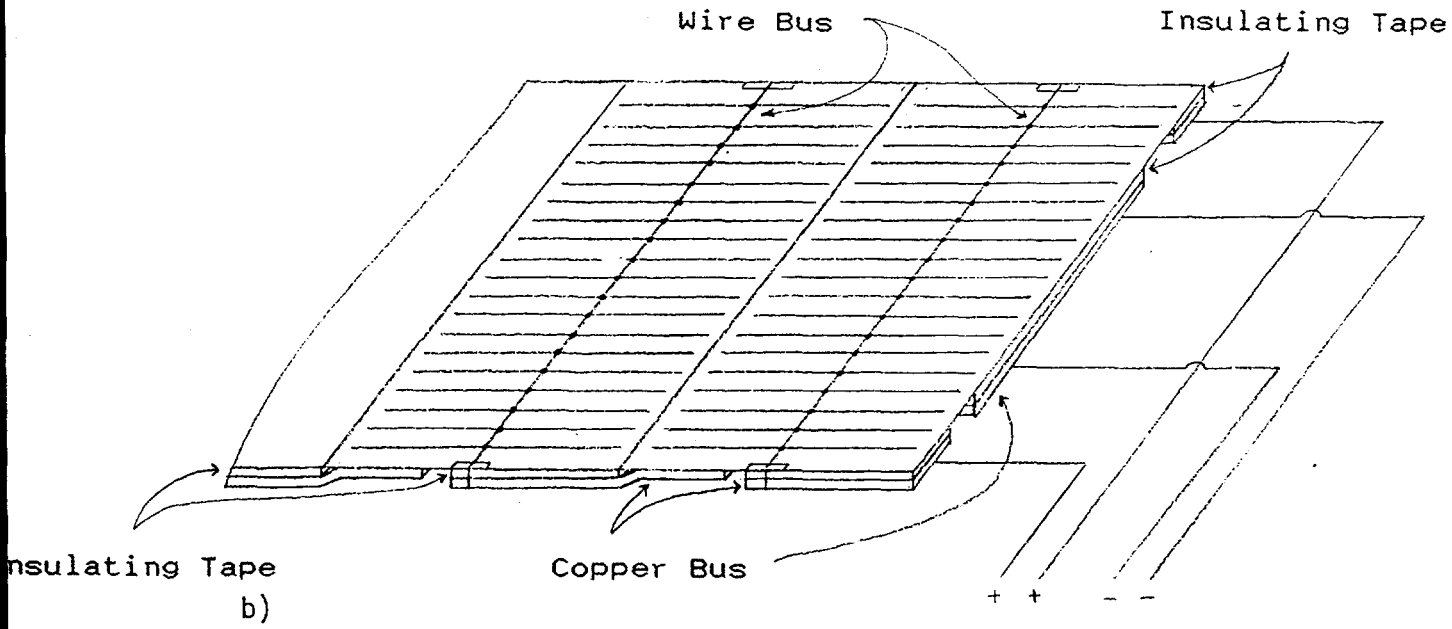
To experimentally determine the module losses, we measured the active area efficiency (overgridded to minimize electrical losses) for a small area cell and compared that to the aperture area efficiency of a completed module. The active area efficiency was determined to be 7.98%, while the module had an aperture area efficiency of 7.10%. This represents an 11% decrease from the active area efficiency, which is in good agreement with the total losses for the monolithic type module shown in Table VII.

MONOLITHIC



a)

SERIES CONNECTED



b)

Fig. 21. Schematic of the interconnect scheme for the a) monolithic-type module and b) series-connected module.

Table VII. Module loss analysis of the monolithic-type and series-connected type modules.

Loss Mechanism	Monolithic Type (%)	Series Type (%)
Encapsulation[1]	3.0	3.0
Electrical[2]	2.7	2.8
ITO + Fingers	1.9	2.0
Wire Bus	0.8	0.8
Shadow	4.4	5.2
Fingers	3.8	3.8
Wire Bus	0.6	0.6
Interconnect	---	0.8
Total	10.1	11.0

[1] Determined by solar simulator measurements. Encapsulation loss as determined by Q.E. measurements is 7%. The source of the difference is being investigated.

[2] Calculated.

3.5 Characterization

To evaluate module efficiency, we use a Spire pulsed solar simulator, model Spi-Sun 240. This solar simulator is calibrated using a SERI calibrated AM1.5 global reference cell. The solar simulator is adjusted to the reference cell AM1.5 global calibration number and corrected for spectral mismatch between the Spire simulator, AM1.5 global, the reference cell spectral response, and the cumulative response of the individual junctions of the multijunction module. The quantum efficiency of the module is determined from the subcell quantum efficiency measurements.

3.6 Module Measurements

We have fabricated numerous double- and triple-junction one square foot modules (> 900 cm^2) that incorporate the a-Si:H and a-SiGe:H materials described earlier. Table VIII shows the results of five double-junction and five triple-junction modules, all having an initial efficiency of 9.15% or greater. These modules were evaluated under a Spire Spi-Sun 240 solar simulator.

The highest initial efficiency module was a double-junction module measuring 9.9% with a current density of 9.5 mA/cm^2 open-circuit voltage of 1.6 volts and 65% fill factor. This module utilized a-SiGe:H in bottom-junction, which was described earlier. The highest initial efficiency triple-junction module measured 9.6% with a current density of 5.8 mA/cm^2 open-circuit voltage of 2.45 volts and 67% fill factor. This module utilized a-Si:H in the top- and middle-junctions and a-SiGe:H in the bottom-junction as described previously. All of the modules listed in Table VIII were monolithic modules (i.e., no series-connected components) as shown in Fig. 21a.

Table VIII. Initial module performance measured by USSC Spire solar simulator.

Sample	Structure	Aperture Area (cm^2)	V_{oc} (volts)	J_{sc} (mA/cm^2)	FF (%)	η* (%)
588	a-Si/a-SiGe	919.3	1.60	9.52	65	9.90
597	a-Si/a-SiGe	918.1	1.60	8.80	68	9.57
602	a-Si/a-SiGe	919.9	1.60	8.82	68	9.60
616	a-Si/a-SiGe	921.1	1.60	8.81	67	9.44
626	a-Si/a-SiGe	918.1	1.60	8.99	68	9.78
598	a-Si/a-Si/a-SiGe	912.0	2.45	5.84	67	9.59
603	a-Si/a-Si/a-SiGe	905.4	2.45	5.34	70	9.15
619	a-Si/a-Si/a-SiGe	921.1	2.45	5.89	66	9.52
621	a-Si/a-Si/a-SiGe	916.9	2.45	5.84	66	9.44
629	a-Si/a-Si/a-SiGe	920.5	2.40	5.80	67	9.32

* Aperture Area Efficiency

Table IX lists three double- and two triple-junction modules measured at both USSC and NREL laboratories. The discrepancy between the two laboratories in measured efficiency is very large, ranging from 10% to 22%. This difference has appreciable contribution from both the fill factor and short-circuit current. The difference in short-circuit current measurements range from 0% to 10%, while the fill factor discrepancy is 12% to 16%.

Table IX. Initial module performance measured by NREL Spire and USSC Spire solar simulators.

Sample	Structure	Aperture Area (cm^2)	V_{oc} (V)	I_{sc} (A)	J_{sc} (mA/ cm^2)	FF (%)	η* (%)	Spire Simulator
588	a-Si/a-SiGe	921	1.64	7.88	8.55	58	8.20	NREL
		919.3	1.60		9.52	65	9.90	USSC
597	a-Si/a-SiGe	918	1.65	7.33	7.98	60	7.87	NREL
		918.1	1.60		8.80	68	9.57	USSC
602	a-Si/a-SiGe	918	1.64	7.46	8.13	60	8.01	NREL
		919.9	1.60		8.82	68	9.60	USSC
598	a-Si/a-Si/a-SiGe	915	2.52	5.03	5.50	58	8.09	NREL
		912.0	2.45		5.84	67	9.59	USSC
603	a-Si/a-Si/a-SiGe	900	2.51	4.81	5.34	62	8.35	NREL
		905.4	2.45		5.34	70	9.15	USSC

* Aperture Area Efficiency

We have performed a detailed spectral analysis in an attempt to resolve the differences in the two sets of measurements. The short-circuit current of any device under a standard spectrum is given by

$$I_{comp,std} = \frac{I_{comp,src}}{I_{ref,src}} \times \frac{I_{ref,std}}{M} \quad (1)$$

where $I_{comp,std}$ and $I_{comp,src}$ is the current of the component-junction under the standard and source spectra, respectively; $I_{ref,std}$ and $I_{ref,src}$ is the current of the reference cell under the standard and source spectra, respectively; and M is the spectral mismatch between the reference cell and component-junction. If the source (i.e., simulator) is set up such that $I_{ref,std} = I_{ref,src}$ (which was the case for each set of measurements), then the ratio of component-junction current under the simulator to the component-junction current under the standard spectrum, namely, $I_{comp,src}/I_{comp,std}$, is simply the spectral mismatch M.

These ratios give a reasonably accurate estimation of how each component-junction responds to the solar simulator with respect to the standard spectrum. Table X lists these ratios for all component-junctions for several representative double- and triple-junction cells. A current ratio less than unity represents a spectral deficiency for that component-junction, and a current ratio greater than one represents excess spectral irradiance. (Note that these calculations were not performed on the actual modules because the measurement of quantum efficiency on a module would be very difficult. However, because these ratios are not very sensitive to slight variations in quantum efficiencies, the use of representative small-area devices is still valid.)

The short-circuit current of the double-junction modules will be proportional to the top cell ratios under either simulator, because these are well known to be top-junction limited under these simulators. It is therefore concluded that the discrepancy between the two sets of current measurements is not resolvable by any differences in the two simulator spectral irradiances.

The fill factor of these multijunction modules, as related to simulator spectral content, will primarily be a function of top- to bottom-junction current matching condition under these spectra. The shift in spectral content is defined as the bottom-junction ratio

divided by the top-junction ratio. Table X lists these ratios. A shift ratio greater than unity indicates a red-rich simulator spectrum with respect to the standard spectrum, while a shift ratio less than unity indicates a blue-rich simulator spectrum with respect to the standard spectrum. It can be seen from these shift ratios that both simulators (USSC and NREL) are equally red rich. It must therefore be concluded that the differences in the module fill factors also have no relationship to the differences in spectral content of the simulators.

Table X. Current ratios of component cells under source and standard spectra for various double- and triple-junction cells.

		USSC SPIRE			
Module	Type	Top	Middle	Bottom	Shift Bottom Ratio / Top Ratio
2B 613	2G Double	0.981	N/A	1.158	1.180
2B 611	2G Double	0.983	N/A	1.172	1.192
2B 609	2G Double	0.983	N/A	1.151	1.171
2B 605	2G Triple	0.971	0.995	1.225	1.262
2B 600	2G Triple	0.974	0.996	1.212	1.244
		NREL SPIRE			
Module	Type	Top	Middle	Bottom	Shift Bottom Ratio / Top Ratio
2B 613	2G Double	0.956	N/A	1.104	1.155
2B 611	2G Double	0.954	N/A	1.110	1.164
2B 609	2G Double	0.953	N/A	1.105	1.159
2B 605	2G Triple	0.925	1.013	1.116	1.206
2B 600	2G Triple	0.921	1.015	1.114	1.209

It must be concluded that the spectral distribution of the USSC and NREL Spire solar simulators is not a major source of efficiency measurement differences between the two laboratories. It is also not believed to be differences in reference cell calibrations, since both reference cells have been calibrated from the same primary reference cell. It must therefore be presumed that the primary source of the differences lie in the electronic measurement itself. Because both simulators are pulsed solar simulators, there are many possible sources of discrepancies. Steps are now under way to resolve these large discrepancies presented here.

3.7 Future Directions

It is important at this point to discuss what improvements are needed to obtain stabilized module efficiencies of 10% and beyond. The highest module efficiency measured at NREL on our triple-junction panel is 8.35%. NREL measurements have an accuracy of ±10%, and assuming the upper limit, the module efficiency is 9.2%. If we take a 15% degradation, the projected stabilized efficiency is 7.8%. How do we improve this efficiency further?

As mentioned in Section 2, one of the major thrusts of the Phase I program was to translate into large area what was already achieved using the small-area deposition machine. The highest small-area double-junction efficiency obtained using the IIB machine is 11%. This is 18% lower than the efficiency of 13% obtained using the small-area deposition machine. With suitable adjustment of deposition parameters and cell architecture as outlined in Section 4, we can lower the light-induced degradation from 15% to 12%. One can also expect another 5% reduction in the losses as one goes from cell efficiency to panel efficiency by obtaining better uniformity of deposition and smaller shadow losses. Incorporation of all these improvements in our panel should lead to 10% stabilized panel efficiency.

To get beyond this efficiency, one needs a breakthrough in the quality of the narrow bandgap alloy and in material stability. Many interesting studies are being carried out all over the world to address these issues. Improvement of stability can come from materials with better microstructure. A better microstructure may improve the quality of a-SiGe

alloys as well. The role of hydrogen in improving material quality is also being carefully assessed. We are hopeful that progress will be made in the near future, and this will have an immediate impact on the module efficiency.

3.8 Module Cost

The manufacturing cost of the modules consists of direct and indirect material cost, labor cost, and also overhead cost due to managerial personnel, facilities, utilities, and depreciation of the production equipment. At Energy Conversion Devices, Inc., detailed analysis [3] has been done to estimate the fully-loaded production cost using roll-to-roll deposition technology with a triple-junction cell structure. For a production facility of 20 MW annual capacity, the cost is about 70 to 80 cents per peak watt out of which 52% is due to materials, 12% due to labor and the rest due to depreciation and other overheads. One of the fundamental advantages of the continuous roll-to-roll deposition system is the ease of scaleup, and significant economy of scale advantage can be obtained by going for higher capacity.

SECTION 4
ACCELERATED STAEBLER-WRONSKI TESTING

4.1 Introduction

As we strive to reduce the gap between initial active area efficiency and the stabilized final total area efficiency, we must focus on reducing Staebler-Wronski (S-W) degradation. Despite considerable effort expended on this subject, the S-W effect remains the highest single derating factor when projecting final module output from the initial active area efficiency of the solar cell. Whether attempting to understand the physical mechanisms or engineering an optimal material or design, one of the biggest obstacles to evaluating the magnitude of this effect is the very large amount of time it takes to determine the maximum degradation under normal outdoor conditions.

The use of indoor simulated light at an intensity of one sun decreases the time required by only about a factor of five. This still leaves an evaluation period of at least several months. This is far too long of a period to perform any reasonable studies. In view of these facts, many laboratories have now resorted to some kind of accelerated testing [4-6]. This typically involves intensity levels well in excess of one sun and temperature ranges far exceeding those experienced under field conditions.

4.2 Experimental Setup

To achieve this accelerated testing and reasonable turn-around time on S-W results, we have designed and built a completely automated data acquisition system capable of such testing (see Fig. 22 for schematic). This apparatus enables us to light soak a given sample with an intensity range of dark to 100 times AM1.5 under ELH spectrum at any temperature between 15 and 225°C. We have incorporated a fast shutter to provide light soaking intervals resolved to tenths of seconds. There are also three separate temperature plates, each operating at an independent temperature. Any one of these plates may be engaged at any time to make intimate contact to the back of the stainless steel substrate. The interchange of any two plates of different temperature (e.g., 100°C to 25°C) and the

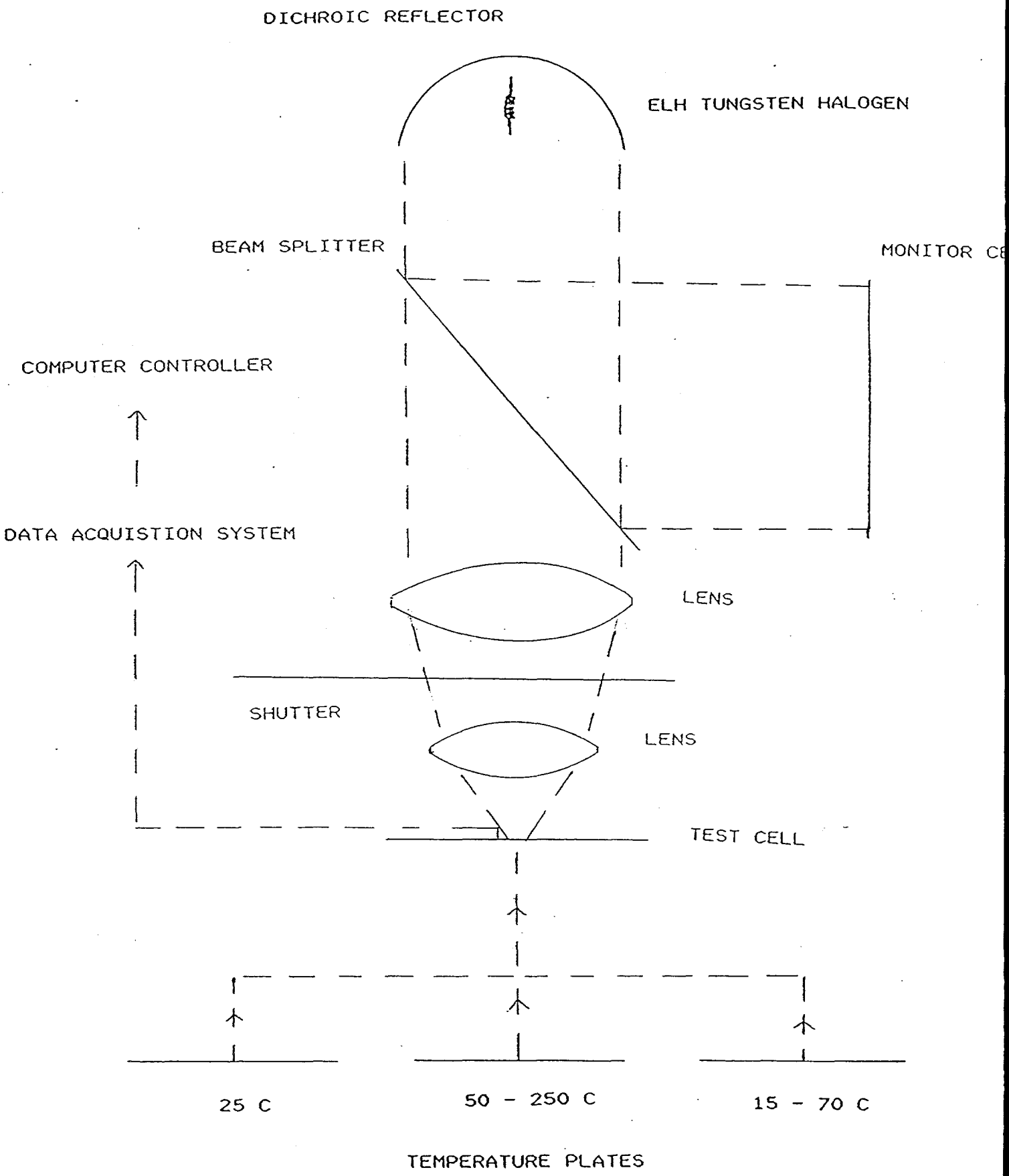


Fig. 22. Schematic of the accelerated Staebler-Wronski tester.

stabilization of device temperature to within 5°C is typically 4-7 seconds (in 1-3 seconds the device is within 10°C of equilibrium).

We are also able to measure the current-voltage characteristics of the device in situ. This is achieved by simply engaging the correct temperature plate, adjusting the ELH lamp to the desired intensity, and measuring the I-V characteristics. This allows us to determine the exact effect the light and/or temperature soaking has on the device. We are then able to determine the rates of degradation and/or annealing at any time between the initial measurement and the final saturation. (It is important to comment at this point that we believe that for optimization of single-junction cell devices, which will be used for the middle and bottom of a multijunction device, the reddish spectrum of the ELH is more appropriate than that of a Xenon source.)

4.3 Theory

In order to obtain stability data under normal operating conditions (one sun or less at temperatures of 50°C or less), we need a kinetics model that accurately describes the device stability. The model used to approximate the degradation of these devices as a function of intensity, temperature, and time was taken from a published model and modified to more accurately describe our data. The rate equation for light induced degradation (LID) and thermal induced anneal (TIA) is [7]

$$\frac{dN(E)}{dt} = \exp\left(\frac{-A_d(E)}{KT}\right) G^{x_1}\left(\frac{C_1(G)}{N(E)} + \frac{C_2(G)}{N(E)^2}\right)\left(N_g(E,G) - N(E)\right) - k\exp\left(\frac{-A_a(E)}{KT}\right) N(E)^{x_2} \qquad (2)$$

where G is the generation rate, N(E) is the number of metastable defects at energy E, N_g (E, G) is the maximum possible number of metastable states at energy E, which is a function of G, and X_1, X_2, $C_1(G)$, $C_2(G)$ are coefficients to be determined for each sample. The first is the LID term with a distributed activation energy $A_d(E)$, and the second term is the TIA term with a distributed activation energy $A_a(E)$. To convert solar cell power output to number of metastable defects, N, a standard collection length formula was used [8]. Fig. 23 shows, for a typical set of parameters, the relationship between normalized efficiency and normalized N for various thicknesses.

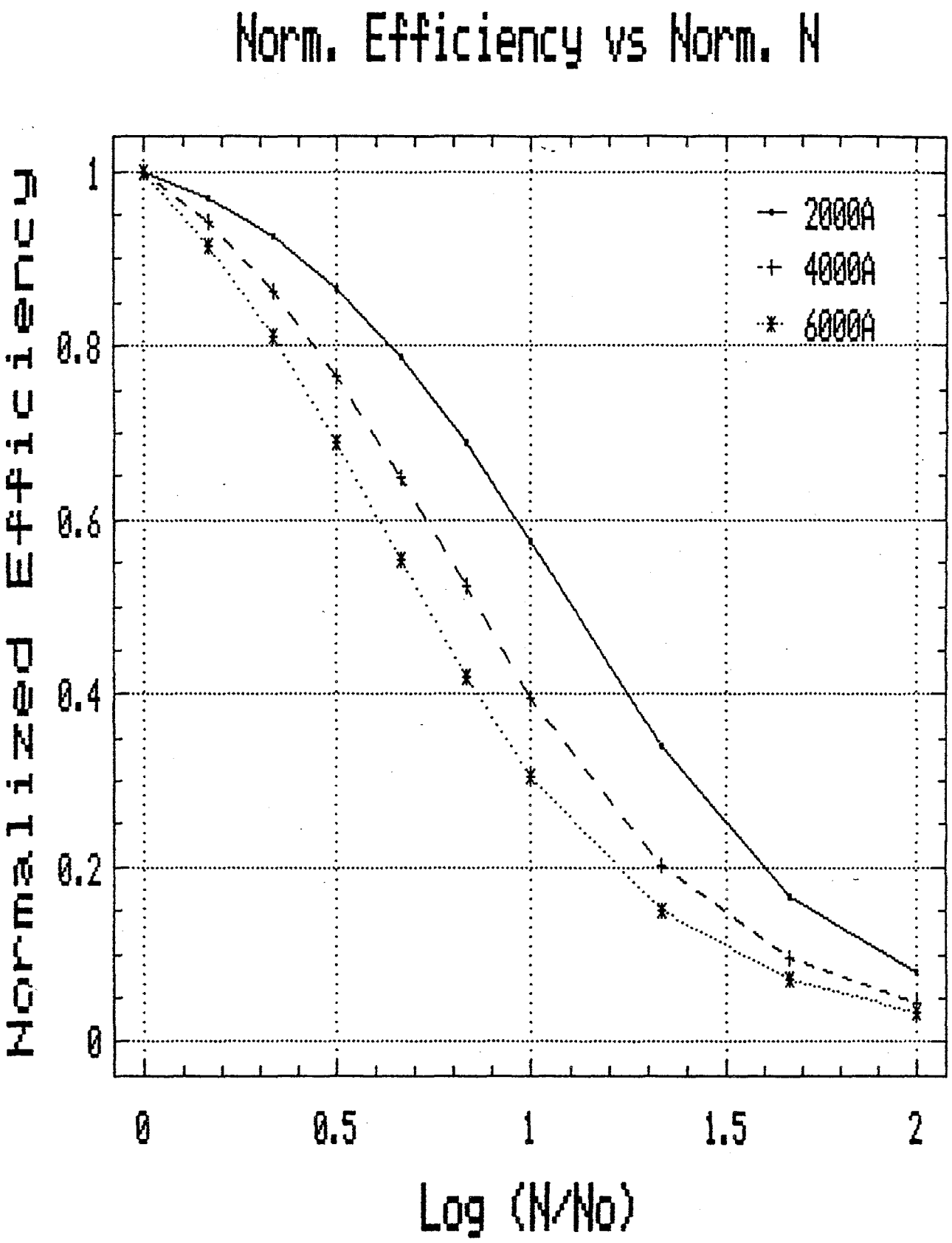


Fig. 23. Plot of normalized efficiency versus normalized N calculated for three different thicknesses.

The typical curve fitting parameters from Eq. 2 are listed in Table XI. It should be noted that not all of these parameters are strictly determined independent of one another. The intensity dependence of the constants C_1 and C_2 were determined empirically to be linear with intensity. The final saturation density N_{sat} is not determined absolutely (e.g., 2 x 10^{17}) but with respect to the initial density N_0; therefore, these ratios are given in Table XI. The activation energies for LID and TIA are approximately 0.12 and 0.9 eV, respectively. The distributed activation energies were incorporated to provide a much improved data fit for the time regions around the onset of saturation at the various temperatures. This onset was much too gradual to be explained by a single activation energy. The distribution for both activation energies as well as N and N_0 were assumed to be gaussian in shape.

Table XI. Typical curve fitting parameters for an a-Si:H single-junction cell used in Eq. 2 in text.

Activation Energy for TIA	0.9 ± 0.1 eV
Activation Energy for LID	0.15 ± .03 eV
N_{sat} / N_0	10 - 20
X_1	2
X_2	8 - 10
C_1 (m,b)	0.01, 0.08
C_2 (m,b)	0.03, 0.01

4.4 High Intensity/Temperature Studies

In Figs. 24a and 24b we show the energy distribution of the metastable defects versus time and temperature at an intensity of 55 suns. Note that at lower energies the saturated density rises to a value lower than $N_g(E)$. $N_g(E)$ is the maximum number of defects that can be generated at energy E. At the higher temperatures this difference becomes larger as well as shifting to higher energies. Note also that a central energy is not specified since the shape of the degradation curve is only dependent on the relative energy distribution.

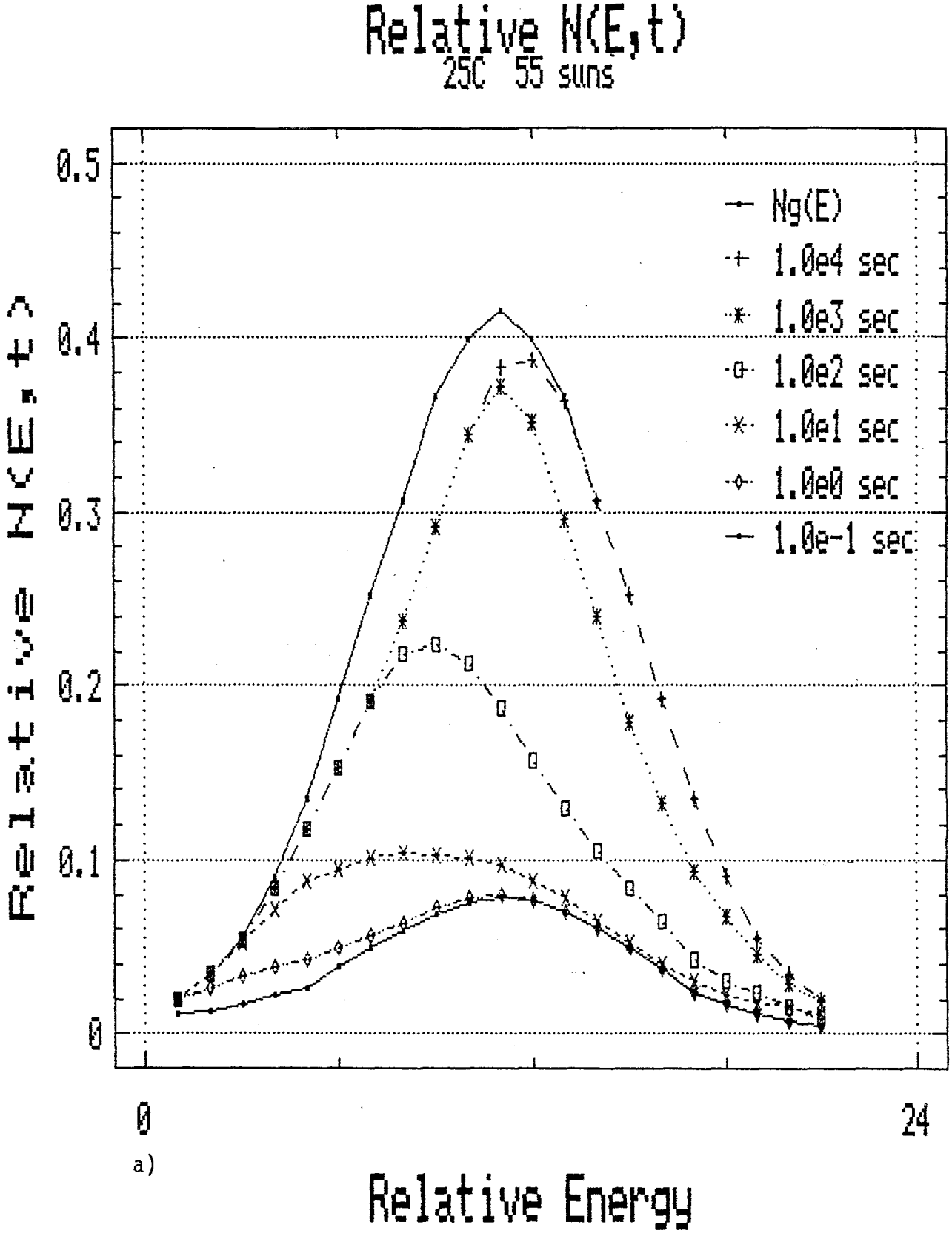


Fig. 24a. Relative N(E,t) for a device illuminated at 55 suns and a temperature of 25°C.

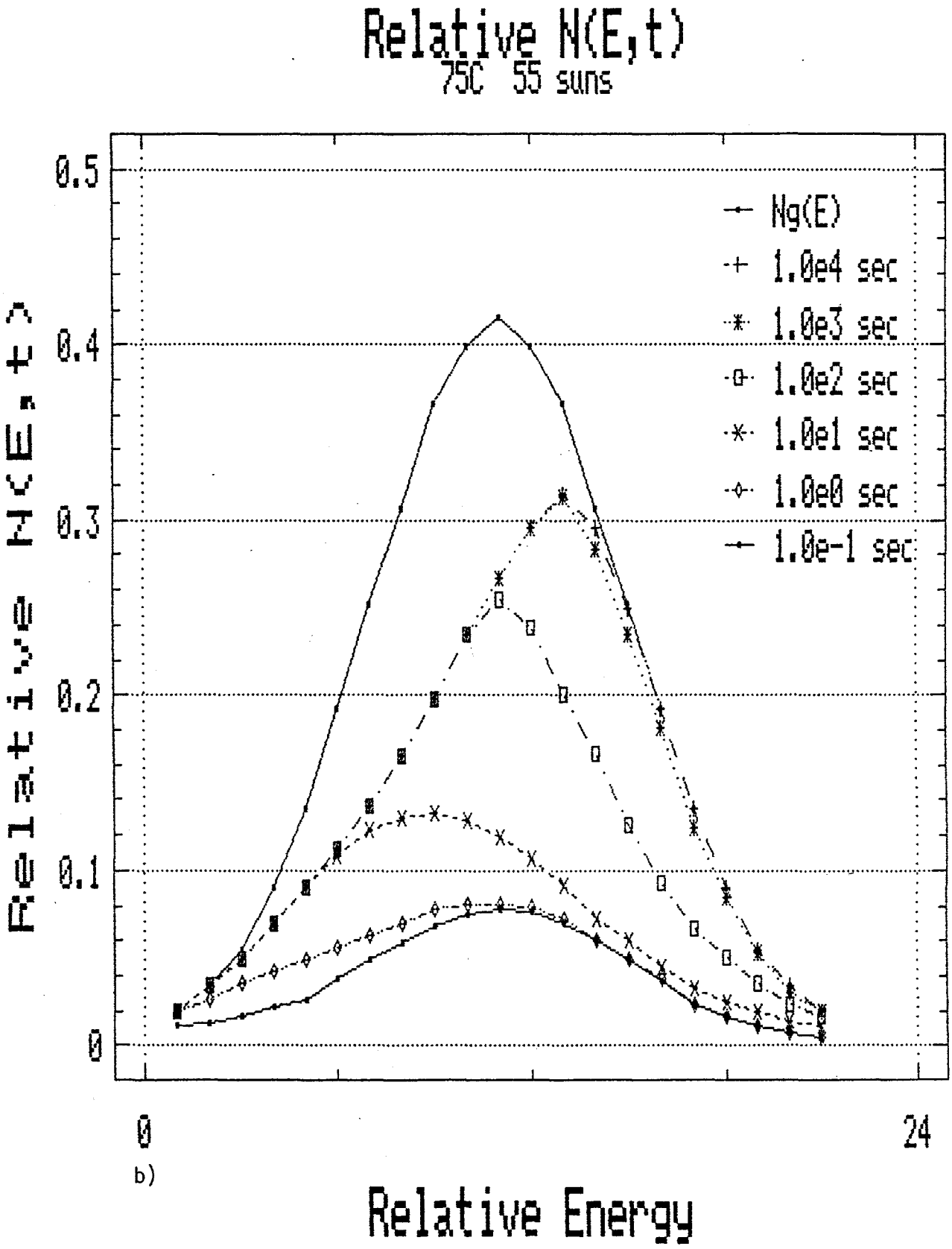


Fig. 24b. Relative N(E,t) for a device illuminated at 55 suns and a temperature of 75°C.

Figure 25 shows that the final saturation at any given intensity is independent of the initial starting density N_o (in Eq. 2 N(E) at an arbitrary time zero). This figure shows the stability characteristics of a device degraded at 50 suns that was annealed to different levels but saturating to the same value. This data has been normalized in Fig. 26 to demonstrate the error in considering the normalized degradation. It can be seen here that the device history can play an important role in this quantity, thereby leading to possible erroneous conclusions. This will certainly depend on the light exposure and thermal history of the device such as AM1 characterization time and the time exposed to elevated temperatures after a-Si deposition such as during TCO and metalization deposition processes. We therefore would like to emphasize absolute efficiency in analyzing data.

4.5. Extrapolated One-Sun Studies

In order to arrive at the stability characteristics under normal operating conditions, we must first measure the device at various levels of high intensity light and a range of temperatures that will include the normal device operating temperatures. Once this has been evaluated, we may fit the model to this data by varying the coefficients to minimize the rms error. Using the coefficients obtained from the high intensity data, we then change only the intensity and temperature to evaluate the extrapolated one-sun conditions.

Figure 27 shows an example of a test procedure run on an a-Si single-junction cell. This device, which has an *i*-layer thickness of 4000 Å, was degraded at intensities ranging from 7 to 82 suns and temperatures from 25 to 75°C. In this example, the data at 52x, 65x and 82x at 25 and 75°C (six curves) was curve fit by the model to determine the coefficients for this particular sample. In between each degradation cycle, the cell was annealed at 175°C for 10^4 sec. Figures 28, 29, and 30 show the exactness of the curve fitting using Eq. 2. The rms error for this data fit was about .04 mW per point (0.6% per point), which is typical. Once the coefficients were obtained, we simply changed the intensity and temperature (while keeping all coefficients constant) to evaluate the ability of Eq. 2 to extrapolate the high intensity degradation to lower intensities at various temperatures. Figures 31, 32, and 33 compare the calculated (extrapolated) data to the actual measure data at the given intensities and temperatures. Figure 34 shows the one sun extrapolated and measured data for another sample.

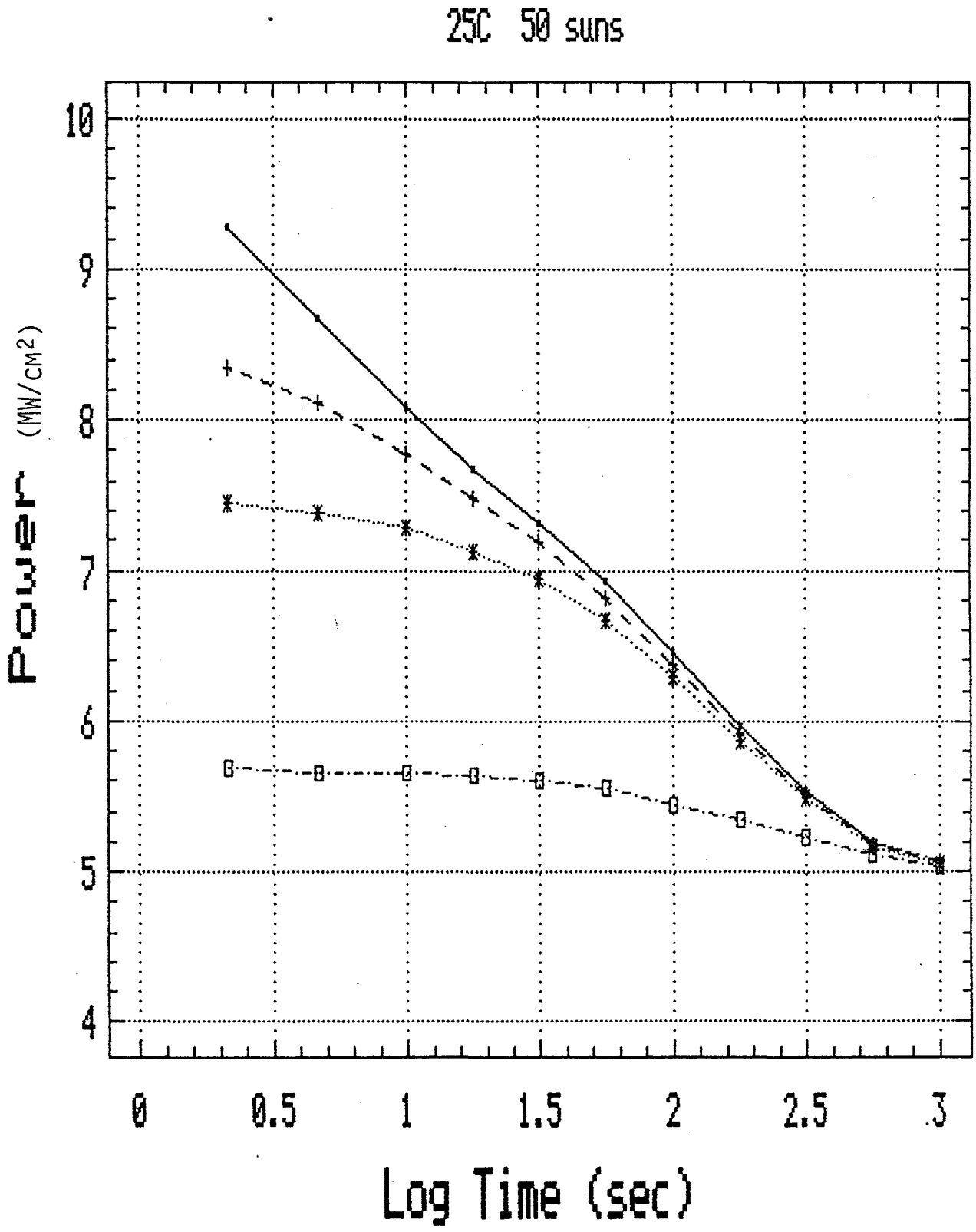


Fig. 25. Power versus time for an a-Si:H device illuminated at 50 suns and a temperature of 25°C for various levels of recovery.

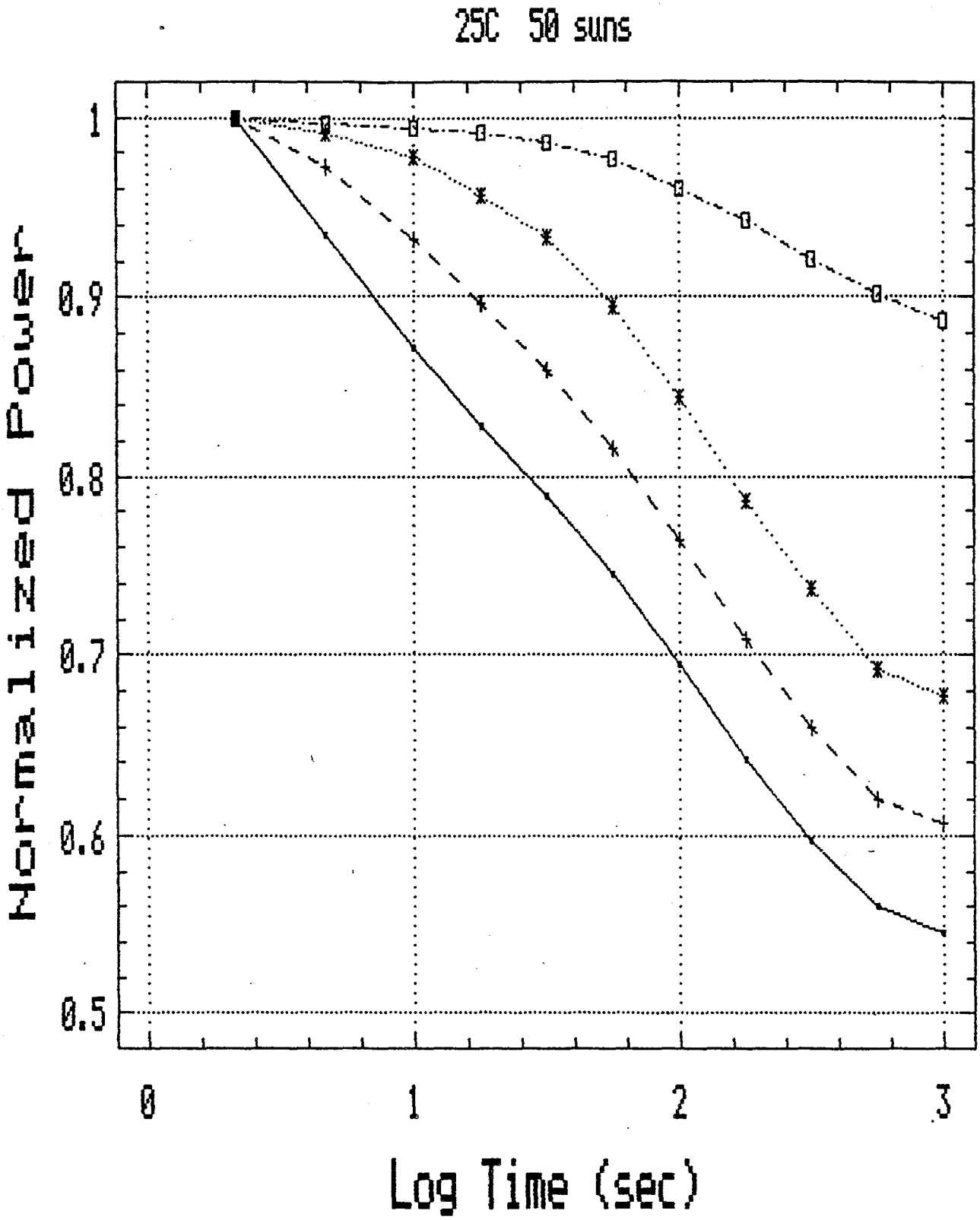


Fig. 26. Normalized initial power versus time for curves from Fig. 25.

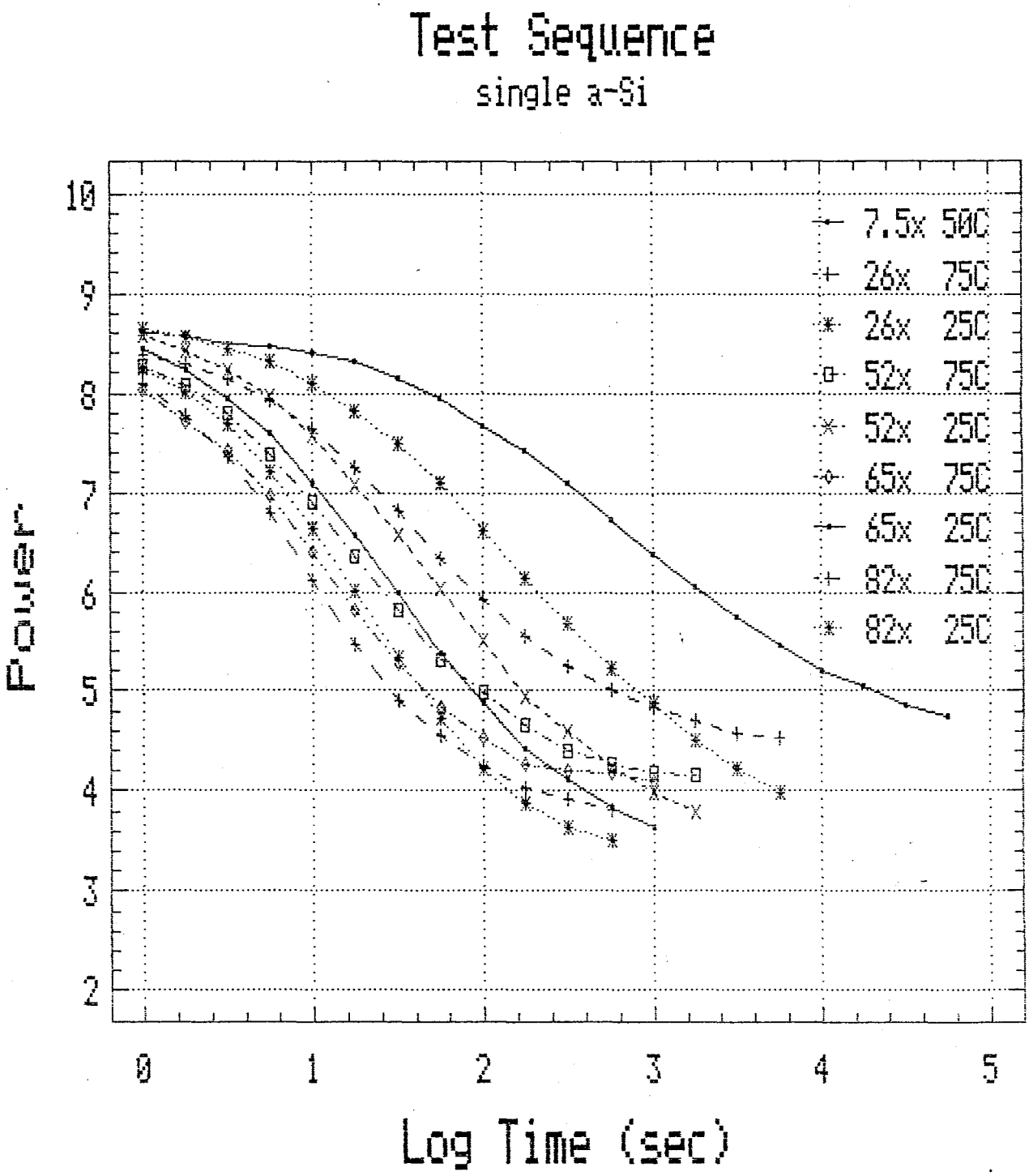


Fig. 27. Test sequence performed on an a-Si:H single-junction cell at various intensities and temperatures.

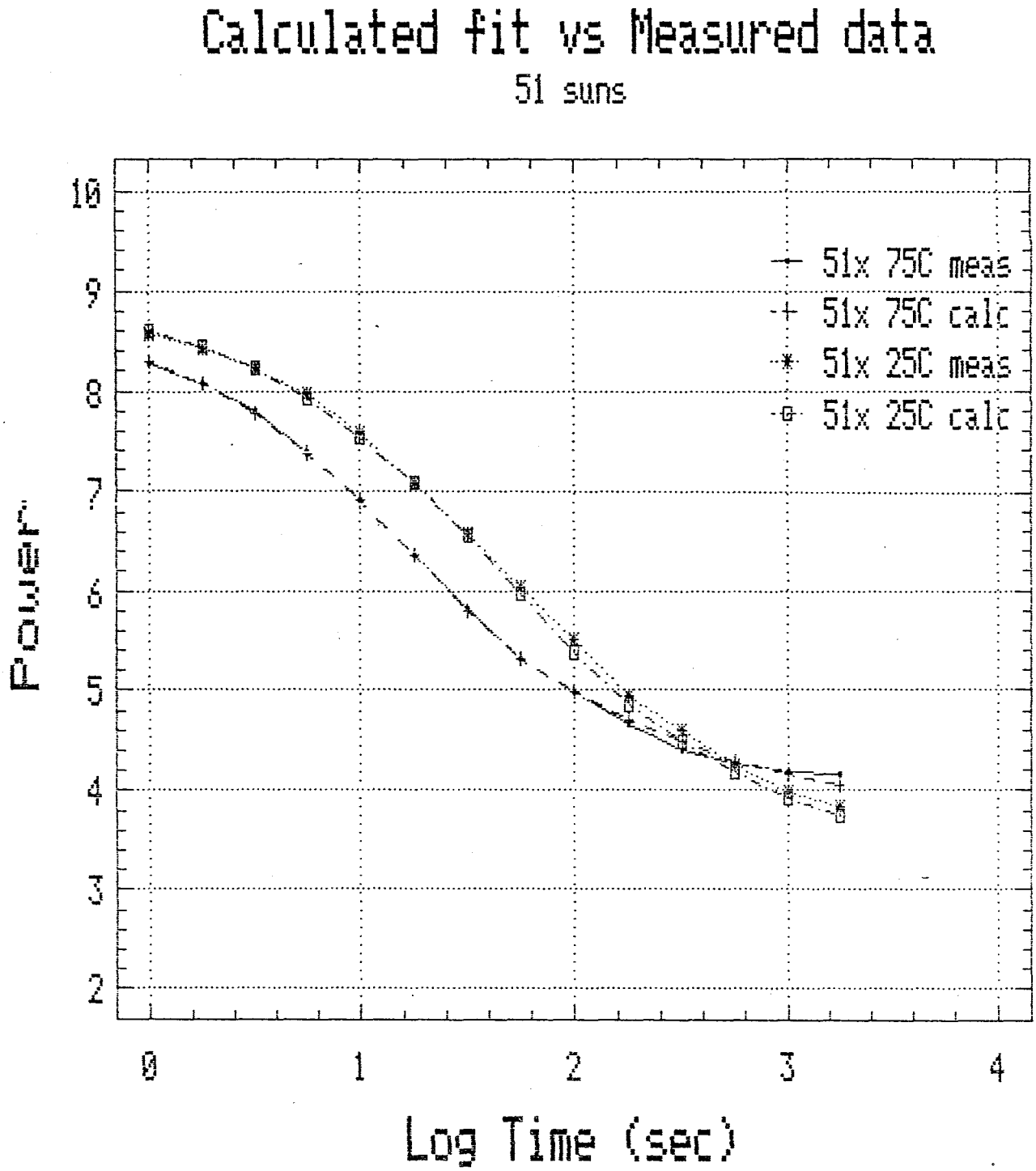


Fig. 28. Evaluation of the exactness of curve fitting from Eq. 2 for a device illuminated at 51 suns and 25 and 75°C.

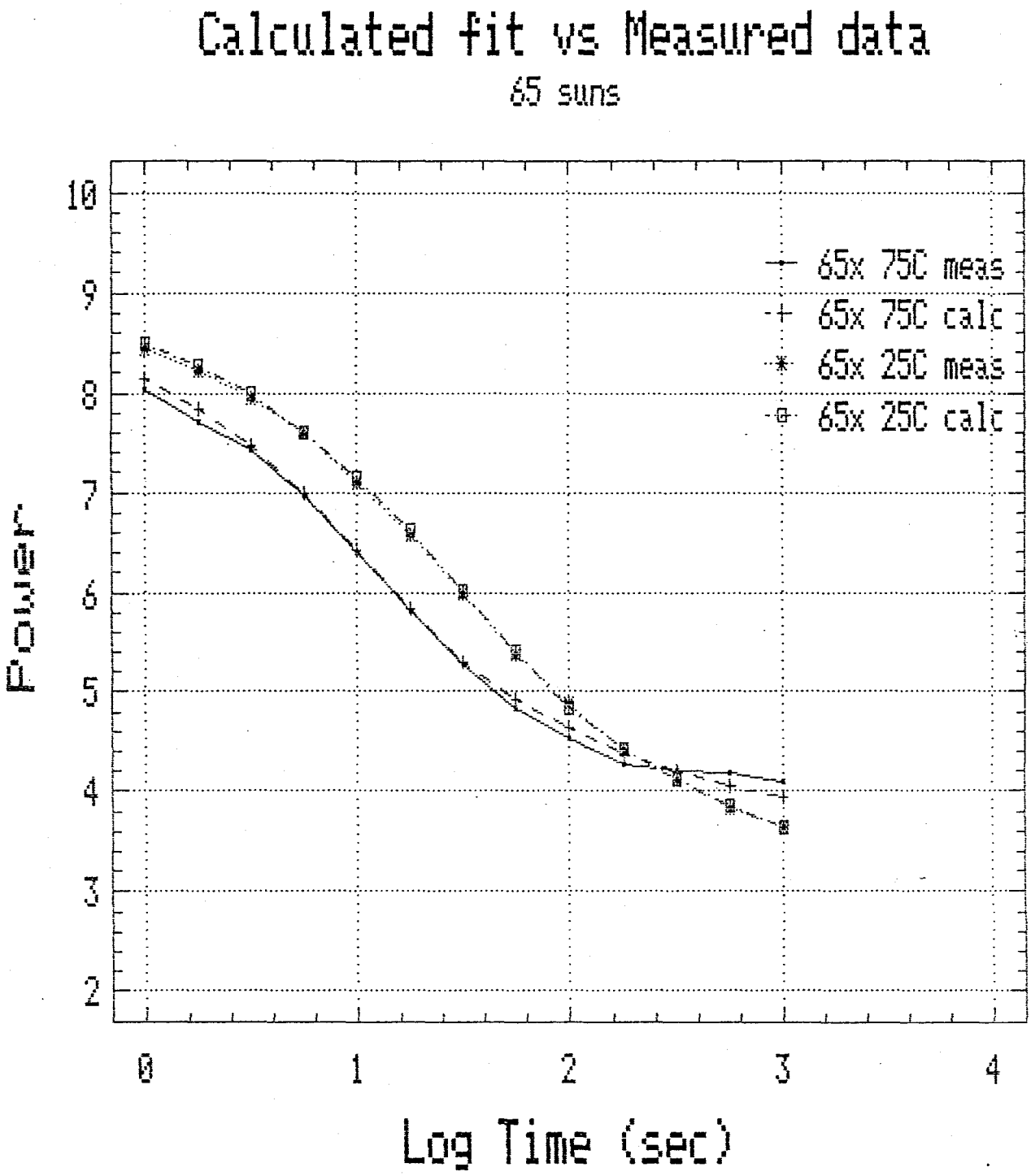


Fig. 29. Evaluation of the exactness of curve fitting from Eq. 2 for a device illuminated at 65 suns and 25 and 75°C.

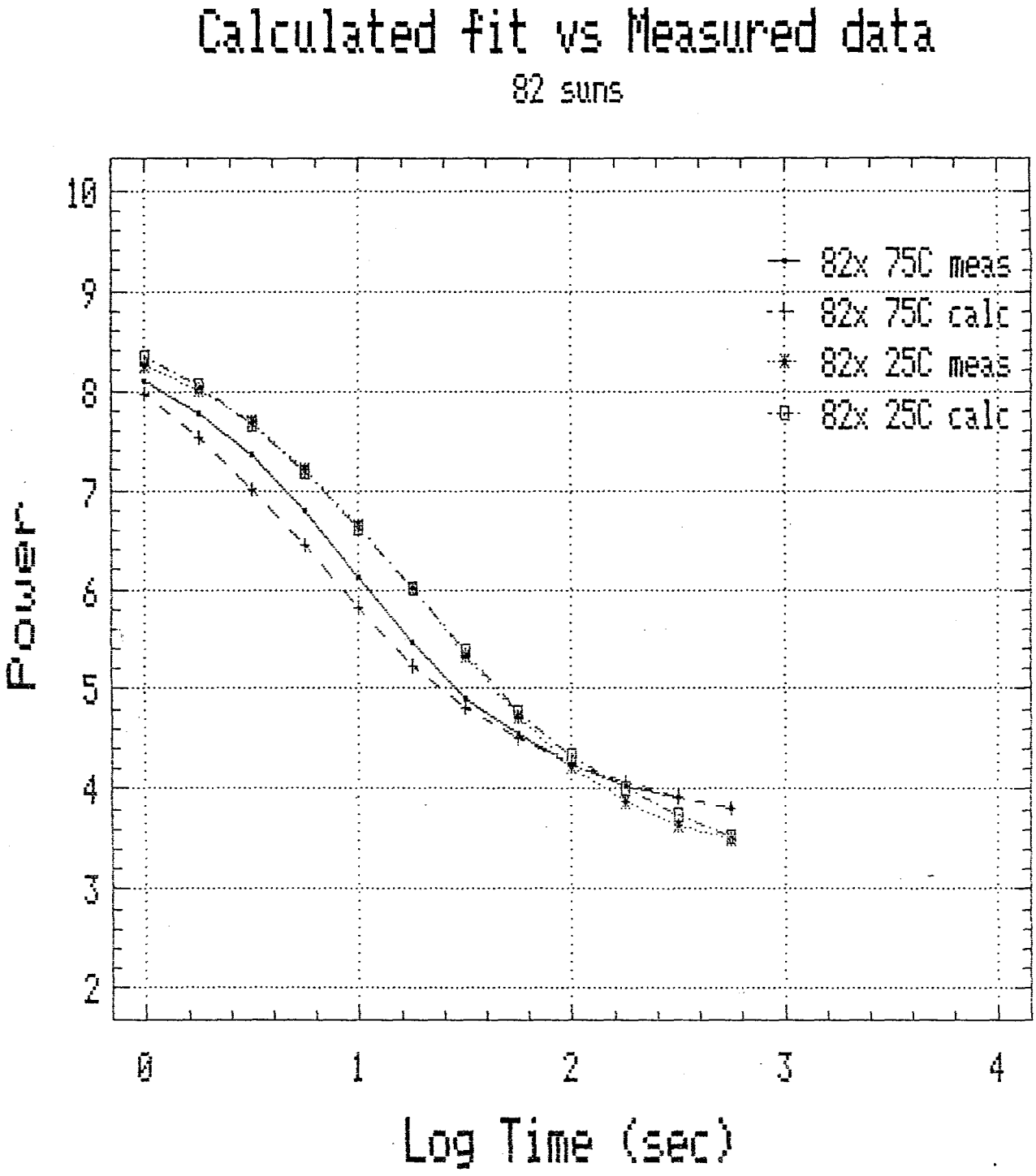


Fig. 30. Evaluation of the exactness of curve fitting from Eq. 2 for a device illuminated at 82 suns and 25 and 75°C.

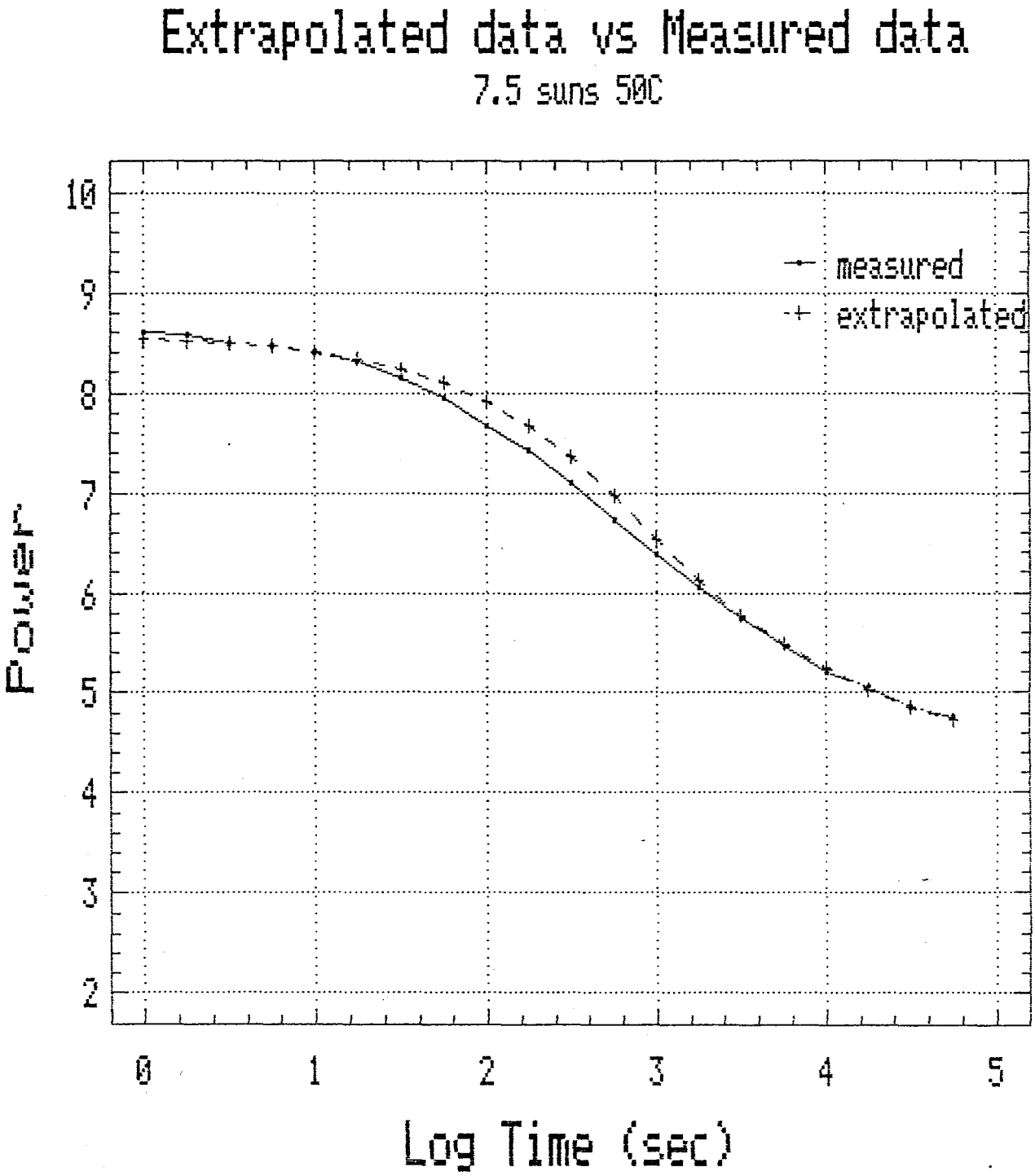


Fig. 31. Comparison of extrapolated data determined from coefficients derived from data in Figs. 28-30 by Eq. 2 and measured data at 7.5 suns and 50°C.

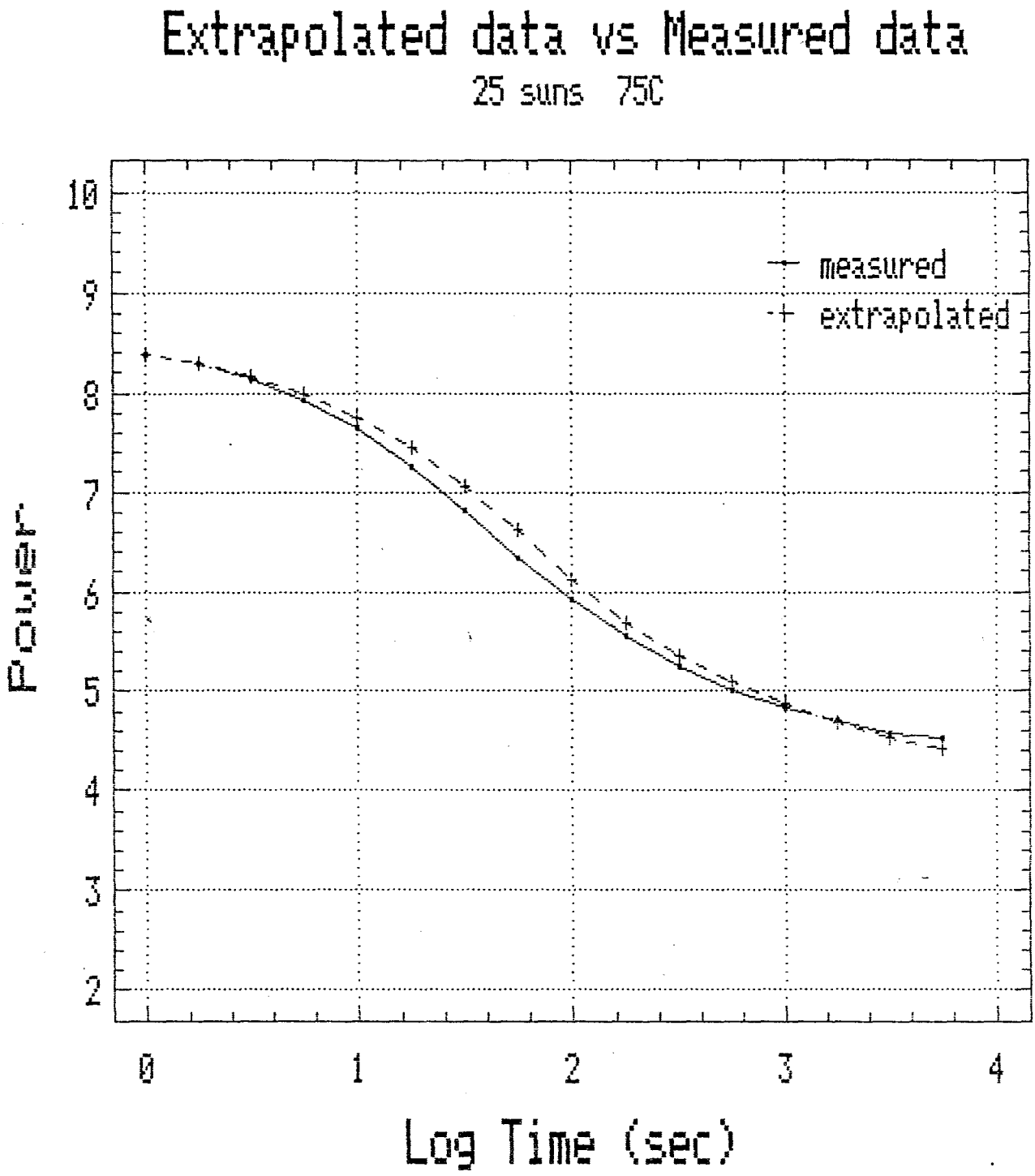


Fig. 32. Comparison of extrapolated data determined from coefficients derived from data in Figs. 28-30 by Eq. 2 and measured data at 25 suns and 75°C.

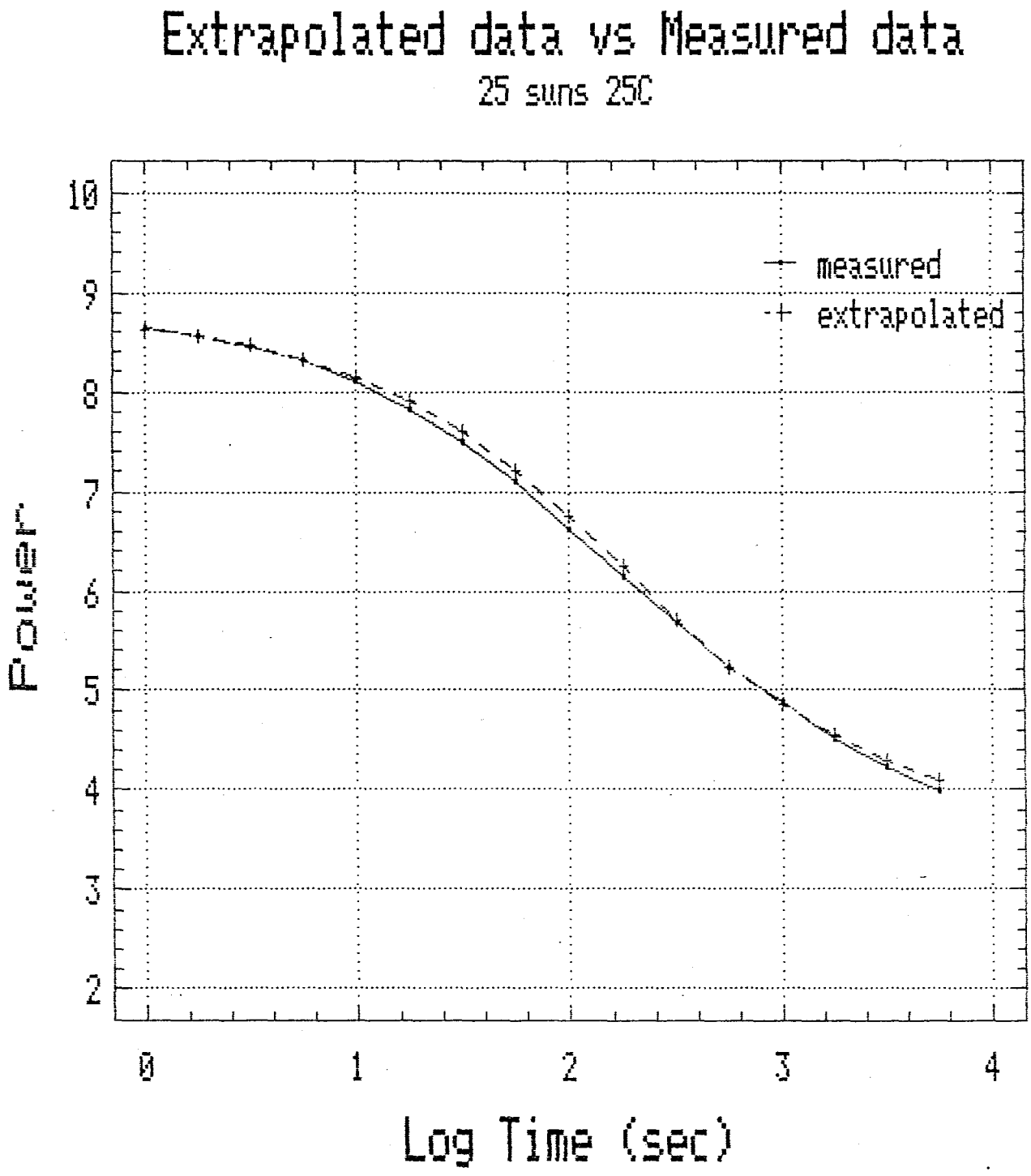


Fig. 33. Comparison of extrapolated data determined from coefficients derived from data in Figs. 28-30 by Eq. 2 and measured data at 25 suns and 25°C.

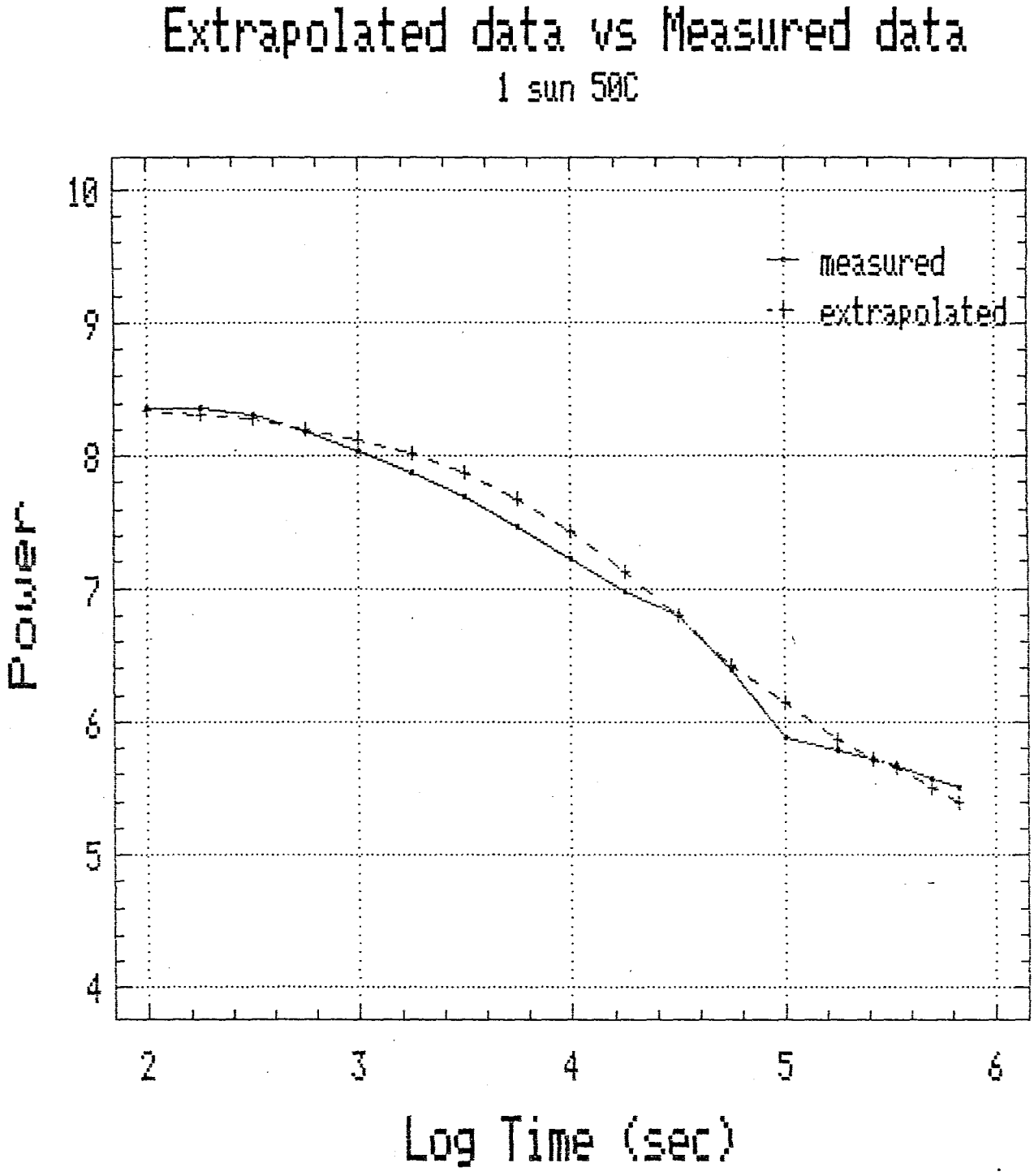


Fig. 34. Comparison of extrapolated data determined from coefficients derived from high intensity data by Eq. 2 and measured data at one sun and 50°C.

We have completed several one-sun (extrapolated) studies. The first two involve determining the role of device thickness on stabilized power for devices on specular stainless steel and specular Ag/ZnO back reflector. These two sets of samples were prepared with *i*-layer thicknesses ranging from 850 Å to 5100 Å (deposited at a rate of 85 Å/min). Then for each sample, the one sun 50°C results were extrapolated from the high intensity measurements.

In the stainless steel case, we find that the optimal thickness changes from about 4200 Å for the initial efficiency to about 3000 Å for the final stabilized efficiency (Figs. 35 and 36). For the back reflector case, we find a very dramatic change in optimal thickness from nearly 5100 Å to just 2100 Å (Figs. 37 and 38). It is quite amazing to find a sample of 850 Å thickness to have a higher stabilized power than that of a 5100 Å device.

It can be concluded that most of the shift in final efficiency peak from 3000 Å for the stainless steel to 2100 Å for the back reflector is seen in the features of the initial efficiency curves (Figs. 36 and 38). As the thickness of the device is increased from 850 Å, we see a much quicker rise in power in the back reflector case. Although there is some variation, the normalized change in efficiencies is similar for the stainless steel and back reflector cases for a given thickness.

It is also interesting to note the difference between the two cases in the one-sun degradation curves (Figs. 35 and 37). In the back reflector case, we see that we have a considerably quicker saturation time than for the stainless steel case, especially for the thicker samples. This is a result of the considerably higher current densities seen in the back reflector case (17 mA/cm^2 compared to 13 mA/cm^2). This allows a higher defect creation rate and more rapid approach toward its saturation density.

The conditions of the degradation for these results were one-sun illumination at a cell temperature of 50°C under open-circuit operating conditions. A more realistic operating condition when considering the operation of a double-junction device would be an illumination intensity of 1/2 sun under maximum power operation. If we assume that the total recombination is proportional to (1 - Imax/Isc), where Imax is the current at the maximum power operating voltage, the effective recombination under 1/2-sun loaded conditions would be 1/2 * (1 - I_{max}/I_{sc}). The ratio of I_{max}/I_{sc} is approximately 3/4, thus

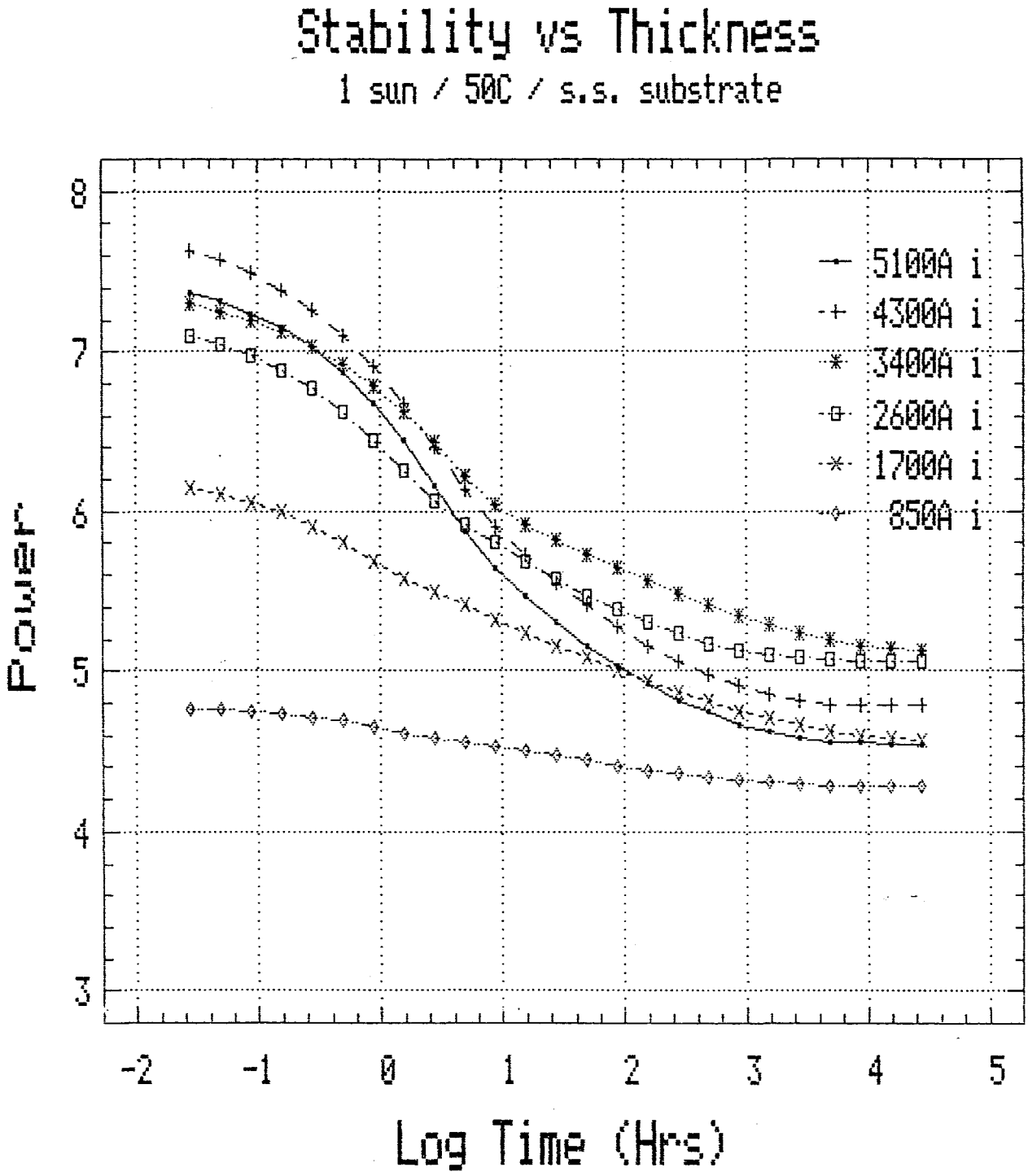


Fig. 35. Extrapolated power versus time for various thicknesses of a-Si:H single-junction cells deposited on bare stainless steel substrates for one sun and 50°C conditions.

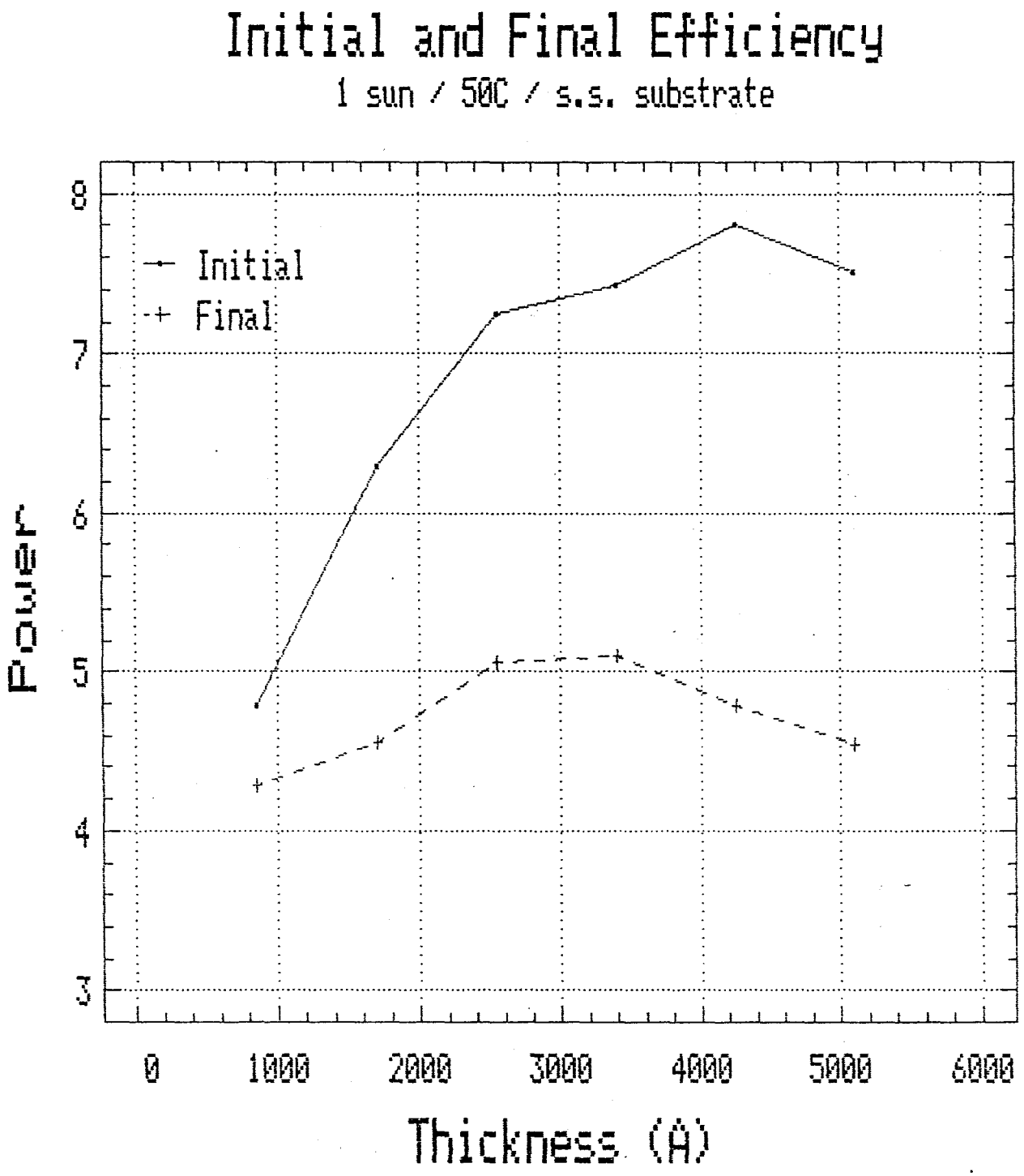


Fig. 36. Initial and final efficiencies for the extrapolated one sun data shown in Fig. 35.

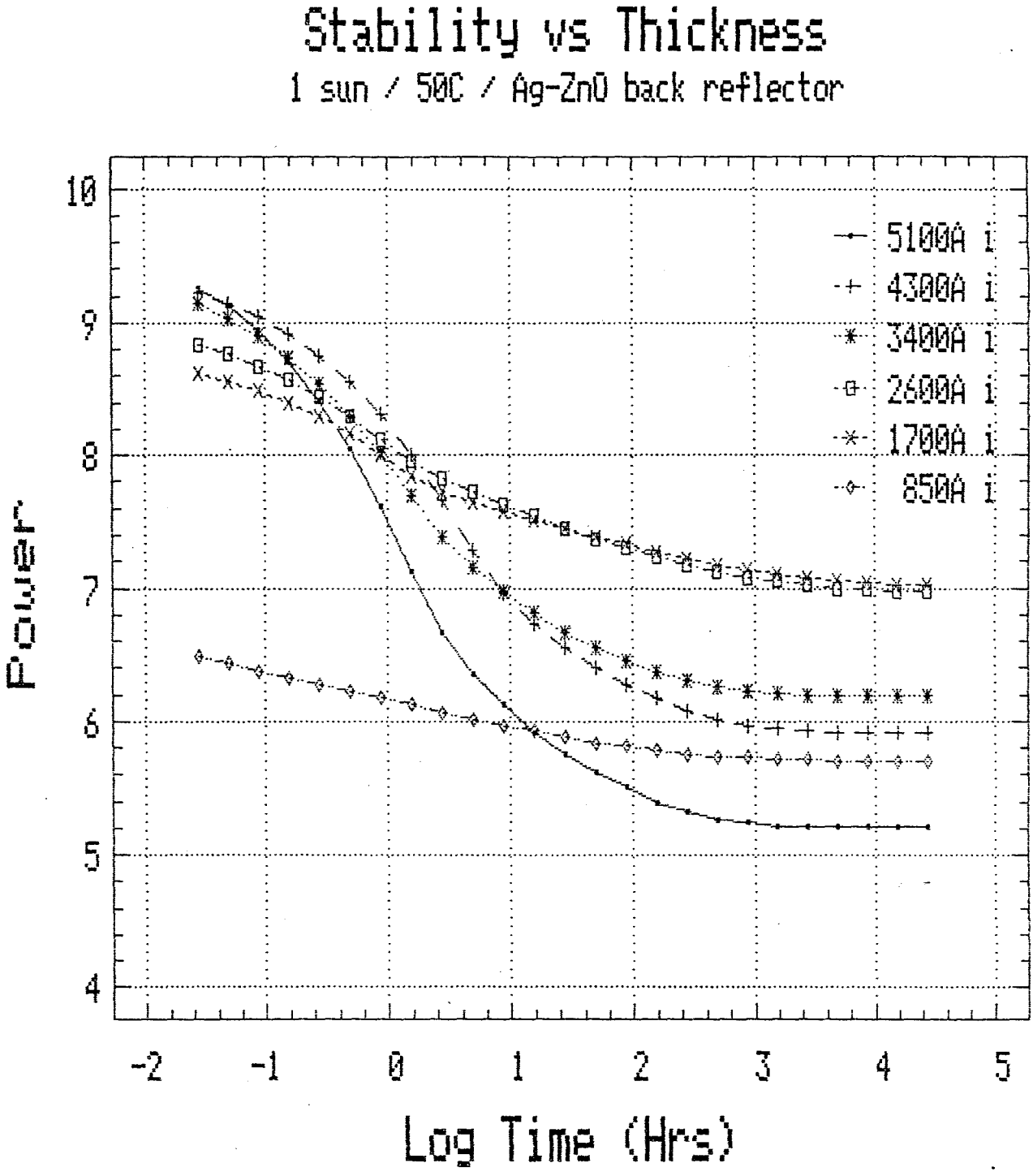


Fig. 37. Extrapolated power versus time for various thicknesses of a-Si:H single-junction cells deposited on specular Ag/ZnO back reflectors for one sun and 50°C.

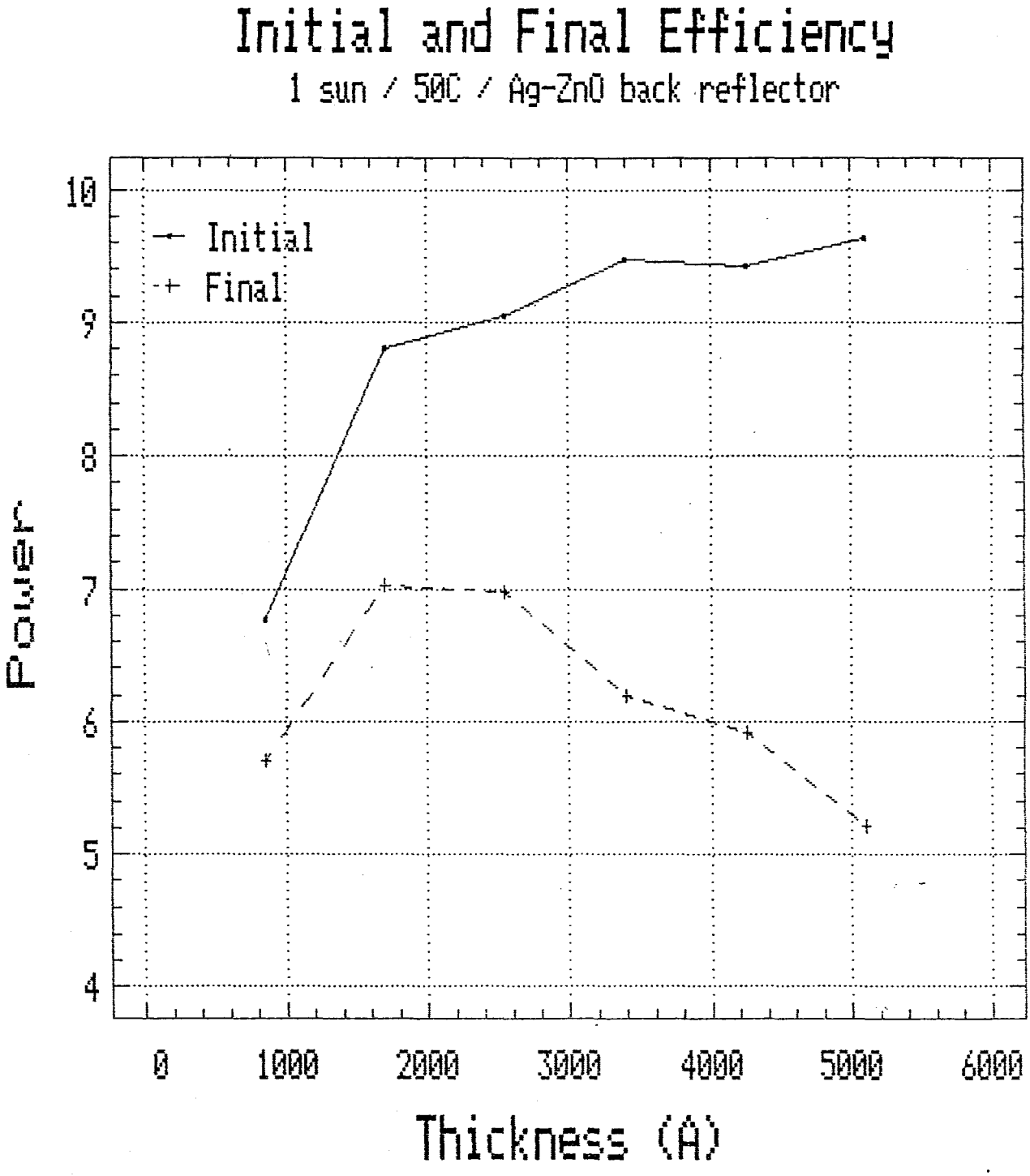


Fig. 38. Initial and final efficiencies for the extrapolated one sun data shown in Fig. 37.

making the recombination proportional to 0.125 one-sun generation for this 1/2-sun loaded condition.

Figure 39 shows a graph of the power versus a-Si/BR intrinsic thickness for the initial state as well as the 1-sun open condition and 1/2-sun loaded condition. We observe from this figure that the optimal thickness shifts slightly from the 1-sun open condition to the 1/2-sun loaded condition. In the 1-sun open condition, the optimal thickness is approximately 2000 Å, whereas the 1/2-sun loaded condition is optimal around 2500 Å. This shift in thickness is a result of the thicker cell's stabilized power being much more responsive to the lower degradation rates. This lower light-induced degradation rate allows the thermal annealing longer times and equilibrating the degradation and annealing at a higher efficiency.

Figure 40 shows the effect deposition temperature has on S-W. All the a-Si single-junction cell devices in this study were approximately 4300 Å and deposited on bare stainless steel. We find the optimal temperature of these devices is the same before and after light soaking, that is, 300°C. Moreover, the final efficiency of cells deposited at 350°C is no better than that of cells deposited at 250°C or 300°C.

We have also evaluated the stability of a set of a-SiGe devices incorporating various levels of Ge content. Figure 41 shows the initial, 1-sun open and 1/2-sun loaded conditions versus the bandgap of the intrinsic layer. The 1.75 eV sample contains no Ge. All of these devices were of equal thickness of about 3000 Å and deposited on bare stainless steel substrates. The stabilized efficiency declines as the Ge content is increased. It is important to point out that over the entire composition of Ge investigated, saturation in cell efficiency was observed.

Figure 42 also shows the stability of a set of a-SiGe devices incorporating various levels of Ge content. In this study, however, the intrinsic layers of each device (except the 1.75 eV sample, which has no Ge) were graded from 1.75 eV (no Ge) at the n^+/i interface to the minimum bandgap (x-axis coordinate) at the p^+/i interface. As in Fig. 41, we see a steady decline in stabilized power as we lower the bandgap except that below 1.5 eV we see a sharp decrease in this final power. This bandgap regime was not investigated for the constant bandgap structures (note the difference in the bandgap scale in the two figures). This sudden drop below 1.5 eV is a considerable effect and warrants further investigation.

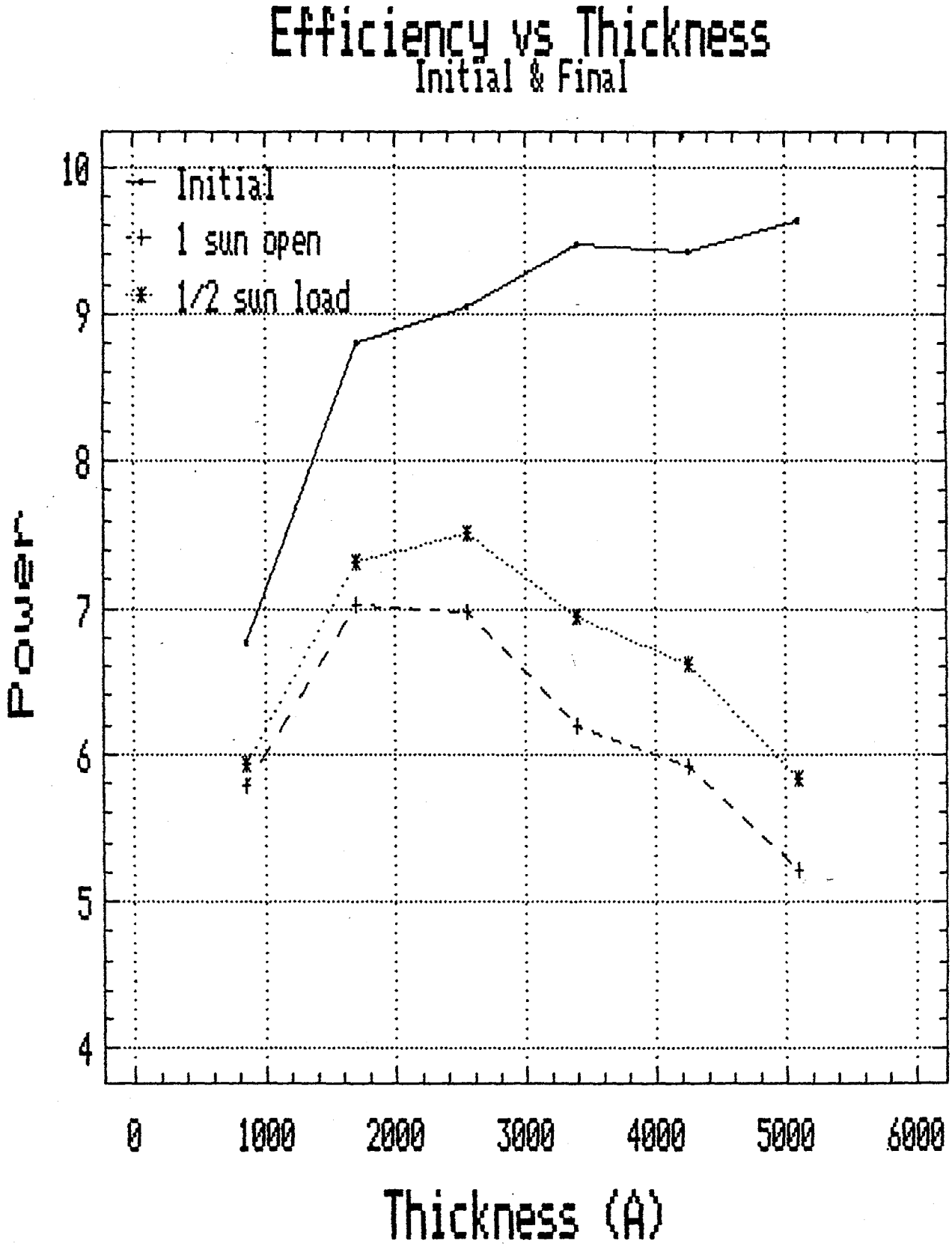


Fig. 39. Initial and final (1 sun open and 1/2 sun loaded) efficiencies for single-junction a-Si/BR devices with various intrinsic layer thicknesses.

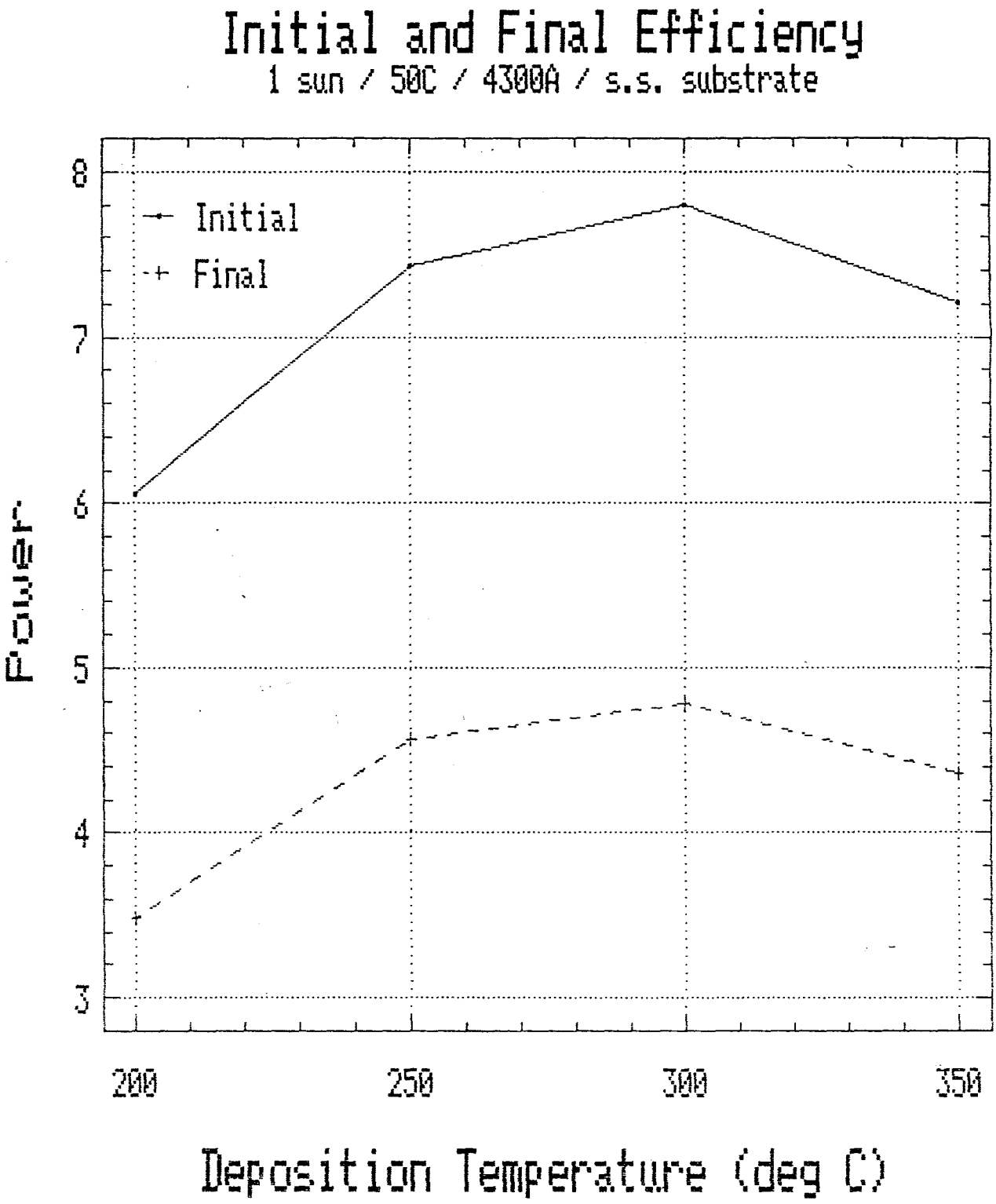


Fig. 40. Initial and final efficiencies for the extrapolated one sun data of a-Si:H single-junction cells deposited at various temperatures at a thickness of 4300 angstroms.

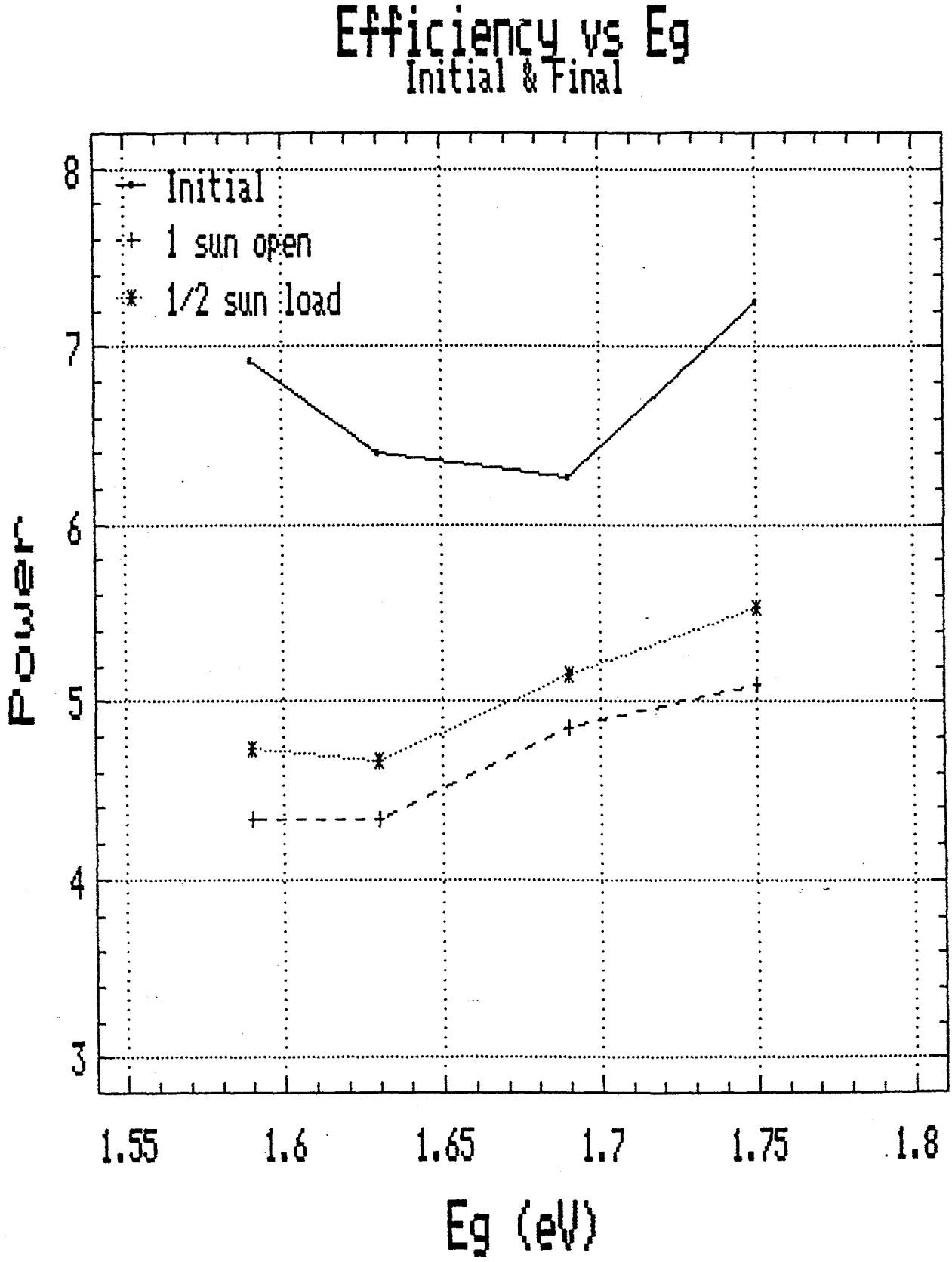


Fig. 41. Initial and final efficiencies for a-Si and a-SiGe single-junction cells deposited on ss with various bandgaps.

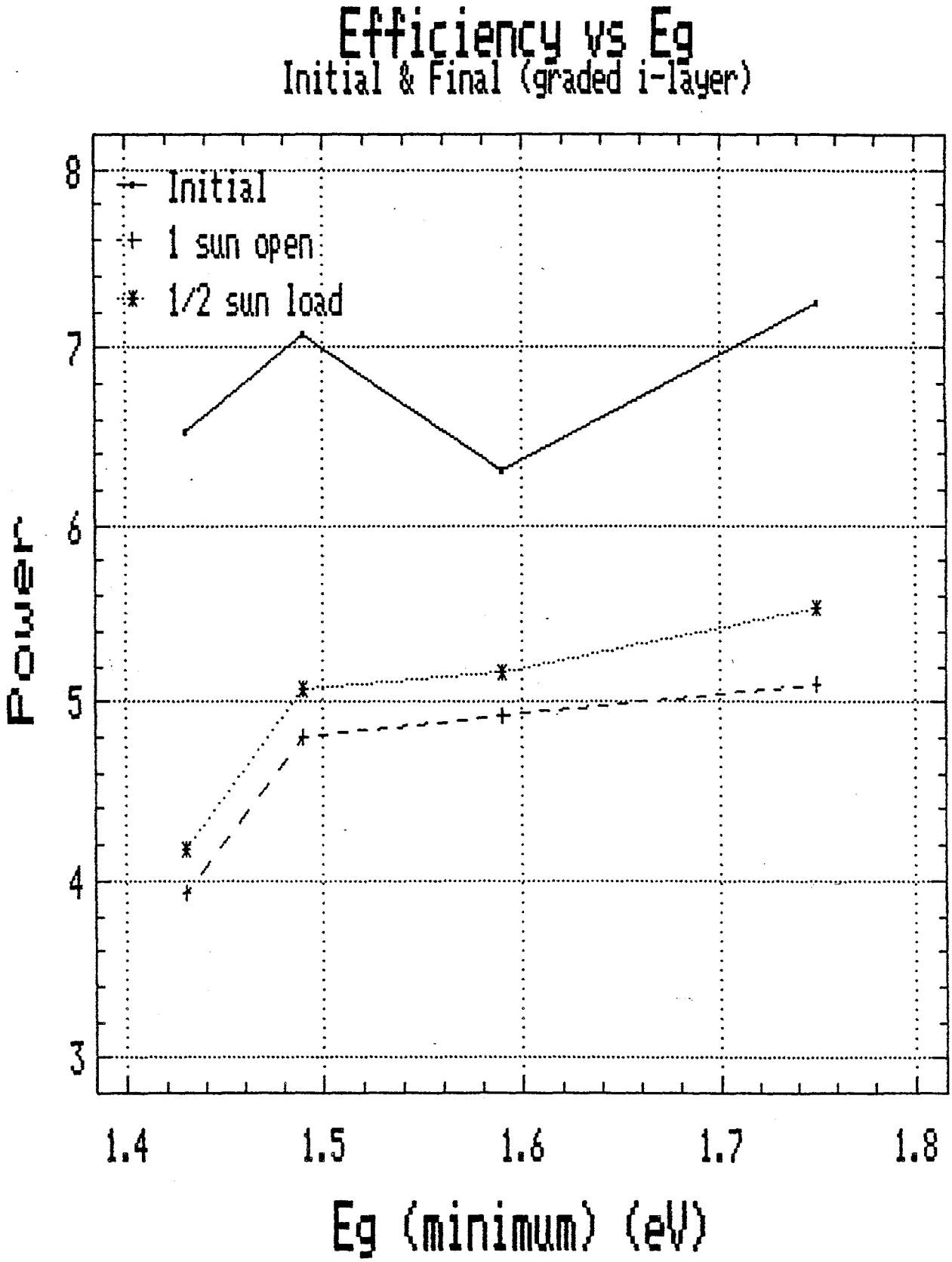


Fig. 42. Initial and final efficiencies for a-Si and a-SiGe devices deposited on ss with graded i-layer with various bandgaps.

Figure 43 shows the initial, 1-sun open and 1/2-sun loaded conditions versus the bandgap of the intrinsic layer for devices built on Ag/textured ZnO back reflectors. The 1.75 eV sample contains no Germanium. All of these devices were of equal thickness of about 3000 Å. The stabilized efficiency declines as the Ge content is increased in a similar manner to the no-BR case.

Figure 44 also shows the stability of a set of a-SiGe devices incorporating various levels of Ge content. In this study, however, the intrinsic layers of each device (except the 1.75 eV sample, which has no Ge) were graded from 1.75 eV (no Ge) at the n^+/i interface to the minimum bandgap (x-axis coordinate) at the p^+/i interface. As in the no-BR case, we see a sharp decline in stabilized power as we lower the bandgap below 1.5 eV.

Using our numerical model [9] for a-Si alloy cells, we have shown [10] that the degradation behavior for single-junction cells can be explained on the basis of change of gap state density alone. The results were presented in the semi-annual report [11].

The results obtained from accelerated light-soaking shed some interesting light on the design considerations for stable multijunction cells. The optimum temperature range for the top cell deposition is obtained from Fig. 40. Comparison of Fig. 43 and 44 shows the importance of bandgap profiling for obtaining higher stabilized efficiency; the optimum bandgap at the minimum for the highest stability is also defined. These results will be used in Phase II to obtain higher stable efficiency in multijunction cells.

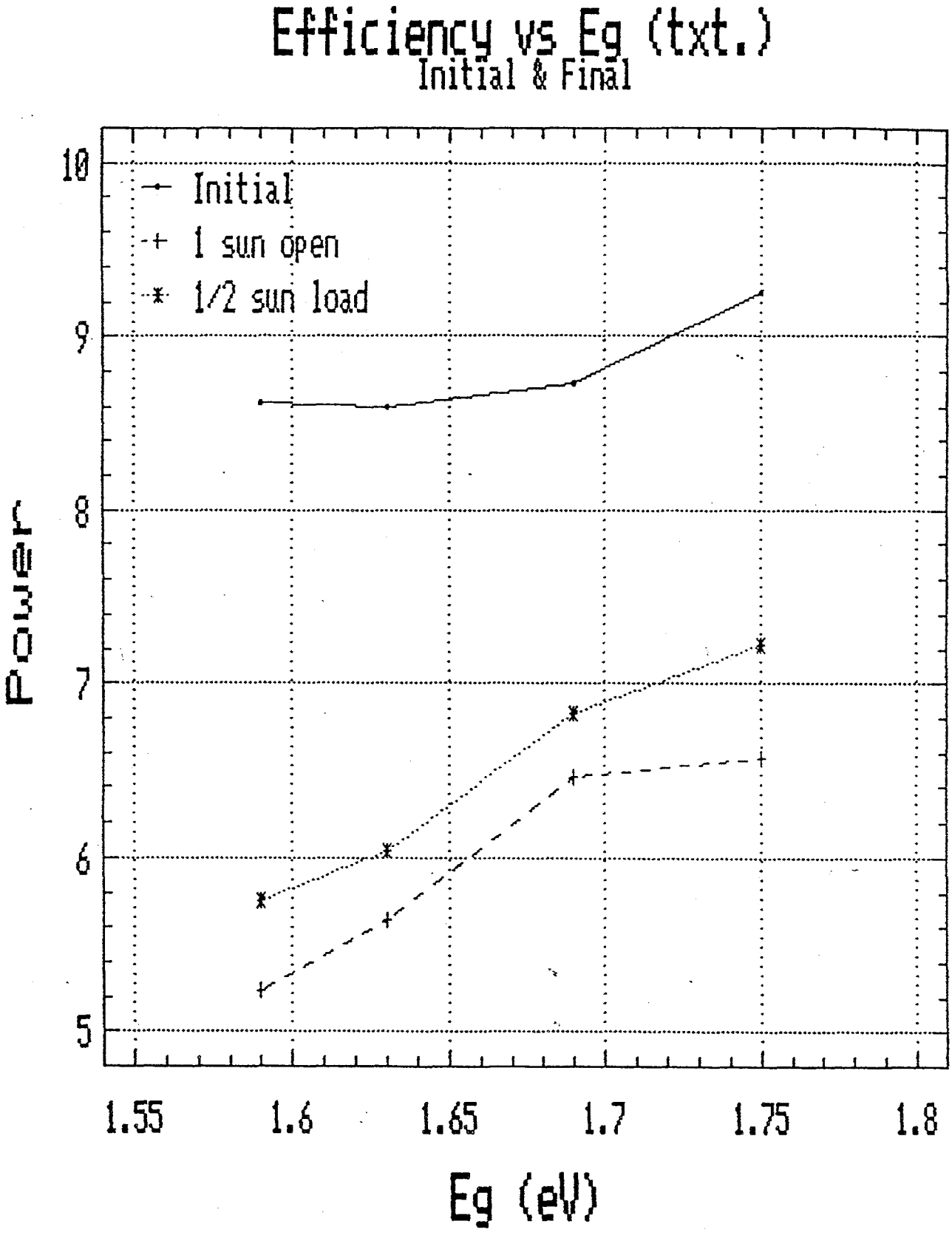


Fig. 43. Initial and final efficiencies for single-junction a-Si and a-SiGe devices deposited on Ag/ZnO back reflector with various bandgaps.

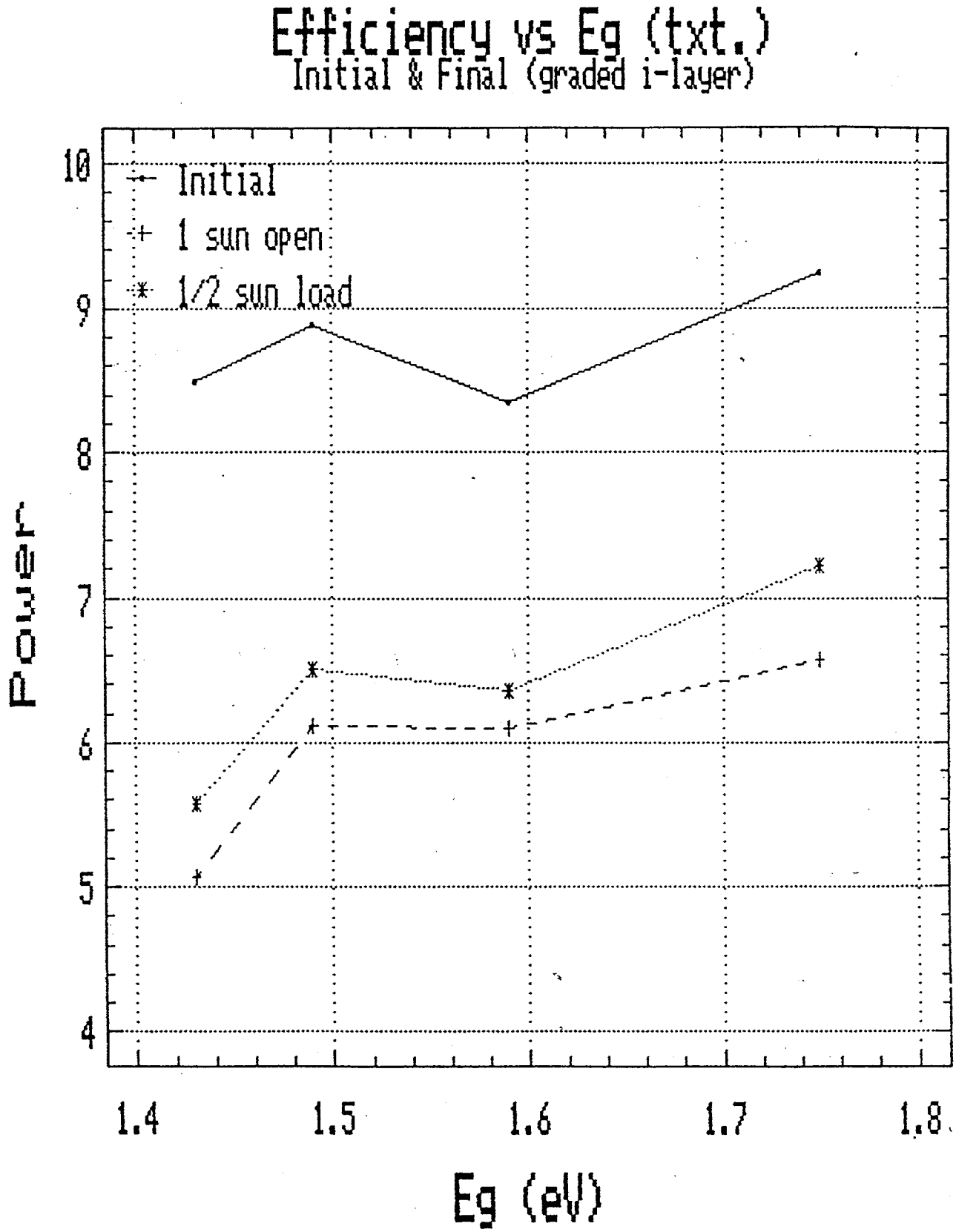


Fig. 44. Initial and final efficiencies for single-junction a-Si and a-SiGe devices deposited on Ag/ZnO back reflector with graded i-layer with various bandgaps.

REFERENCES

1. SERI Annual Report (March 1987-February 1988), Subcontract No. ZB-7-06003-4 (SERI/STR-211-3373).

2. SERI Semi-Annual Report (March-August 1988), Subcontract No. ZB-7-06003-4.

3. Energy Conversion Devices, Inc. Internal Report, 1990 (unpublished).

4. H. R. Park, J. Z. Liu and S. Wagner, Appl. Phys. Lett. 55, 2658 (1989).

5. L. Yang, L. Chen and A. Catalano, in Amorphous Silicon Materials and Solar Cells (Ed. B. L. Stafford), AIP Conf. Proc. 234, p. 275, 1991.

6. M. Grimbergen, L. E. Benatar, A. Fahrenbruch, A. Lopez-Otero, D. Redfield and R. H. Bube, in Ref. 5, p. 138.

7. C. S. Hong and H. L. Hwang, J. Appl. Phys. 62, 1989 (1987).

8. Z. E. Smith, S. Wagner and B. W. Faughnam, Appl. Phys. Lett. 46, 1079 (1985).

9. A. Pawlikiewicz and S. Guha, IEEE ED-37, 403 (1990).

10. A. Banerjee, S. Guha, A. Pawlikiewicz, D. Wolf and J. Yang, in Ref. 5, p. 268.

11. NREL Semi-Annual Report (January-June 1991), Subcontract No. ZM-1-19033-2.

Document Control Page	1. NREL Report No. NREL/TP-411-4840	2. NTIS Accession No. DE92001244	3. Recipient's Accession No.

4. Title and Subtitle

Research on Stable, High-Efficiency Amorphous Silicon Multijunction Modules

5. Publication Date

April 1992

6.

7. Author(s)

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8. Performing Organization Rept. No.

9. Performing Organization Name and Address

United Solar Systems Corporation
1100 West Maple Road
Troy, Michigan 48084

10. Project/Task/Work Unit No.

PV241101

11. Contract (C) or Grant (G) No.

(C) ZM-1-19033-2

(G)

12. Sponsoring Organization Name and Address

National Renewable Energy Laboratory
1617 Cole Blvd.
Golden, CO 80401-3393

13. Type of Report & Period Covered

Technical Report
1 January 1991 - 31 December 1991

14.

15. Supplementary Notes

NREL technical monitor: W. Luft

16. Abstract (Limit: 200 words)

This report describes the progress made during Phase 1 of research and development program to obtain high-efficiency amorphous silicon alloy multijunction modules. Using a large-area deposition system, double- and triple-junction cells were made on stainless steel substrates of over 1 ft^2 area with Ag and ZnO predeposited back reflector. Modules of over 1 ft^2 were produced with between 9.2% and 9.9% initial aperture-area efficiencies as measured under a USSC Spire solar simulator. Efficiencies as measured under the NREL Spire solar simulator were found to be typically 15% to 18% lower. The causes for this discrepancy are now being investigated. The modules show about 15% degradation after 600 hours of one-sun illumination at 50°C. To optimize devices for higher stabilized efficiency, a new method was developed by which the performance of single-junction cells after long-term, one-sun exposure at 50°C can be predicted by exposing cells to short-term intense light at different temperatures. This method is being used to optimize the component cells of the multijunction structure to obtain the highest light-degraded efficiency.

17. Document Analysis

a. Descriptors

high efficiency ; amorphous silicon ; multijunction ; modules ; photovoltaics ; solar cells

b. Identifiers/Open-Ended Terms

c. UC Categories

271

18. Availability Statement

National Technical Information Service
U.S. Department of Commerce
5285 Port Royal Road
Springfield, VA 22161

19. No. of Pages

85

20. Price

A05