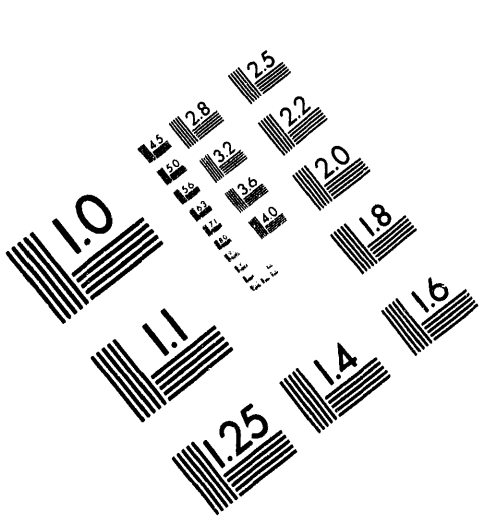

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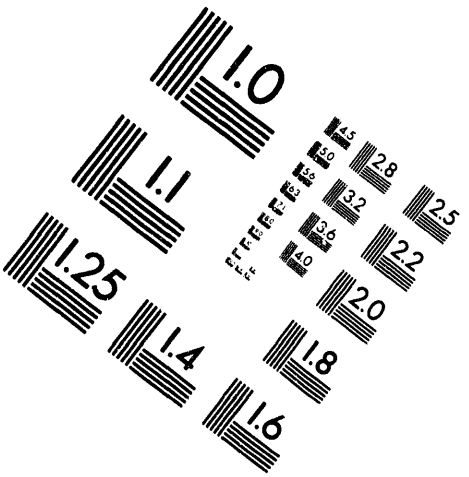

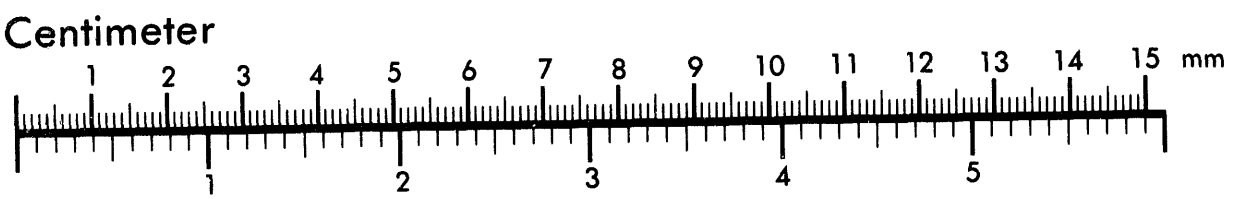

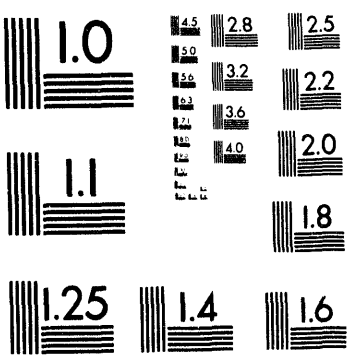

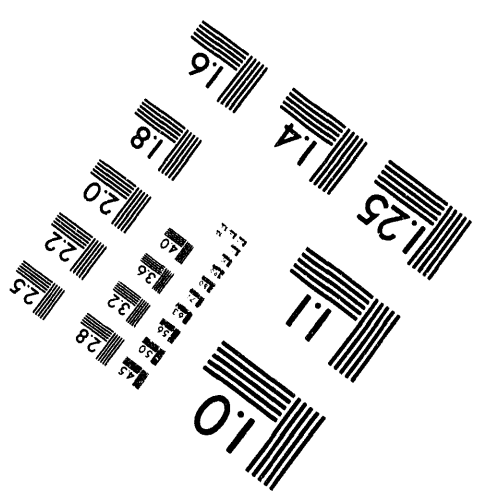

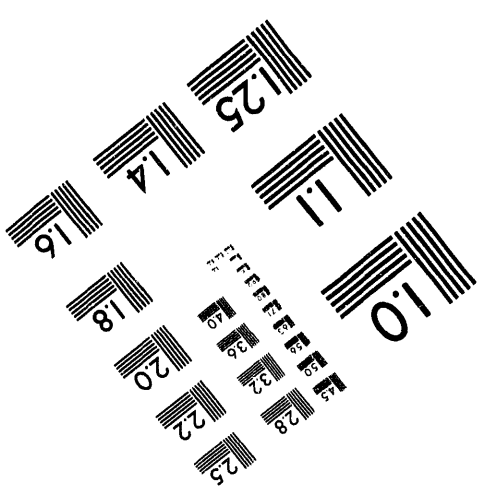

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ROLE OF BURN-IN DURING QUALIFICATION TESTING*

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ABSTRACT

Significantly different radiation responses have been observed for both transistors and ICs with and without preirradiation burn-in. The hardness assurance implications of these results and possible changes to the MIL-STDs will be presented.

I. INTRODUCTION

To qualify an IC for a weapon or space application, it is necessary to screen devices for both reliability and radiation hardness. Some types of reliability tests are considered non-destructive and are performed on all deliverables. For instance, burn-in (biased-elevated-temperature anneal) is routinely performed on all deliverables to reduce the possibility of "infant" mortality in ICs. On the other hand, to reduce costs and to provide rapid feedback on process control, radiation testing is often performed on devices which have not been subjected to reliability screens. In fact, in the Qualified Manufacturer's List (QML) methodology, process control and radiation testing relies heavily on statistically oriented wafer-level radiation testing where biased-elevated temperature anneals are impractical. Thus, devices in a fielded system are often subjected to biased-elevated-temperature anneals that devices used for radiation qualification are not subjected to. If these anneals affect the radiation response, then radiation testing that omits these anneals may not provide an accurate measure of the radiation hardness of fielded parts.

In this paper, we examine the effects of biased-elevated-temperature anneals from 25 to 150°C on the radiation response of transistors and ICs. The implications of these results on hardness assurance testing are discussed.

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II. EXPERIMENTAL DETAILS

Transistors (gate- and field-oxide) were characterized for the total threshold-voltage shift, ΔV_{th}, and the threshold-voltage shifts due to interface-trap, ΔV_{it}, and oxide-trap charge, ΔV_{ot}, using the dual-transistor I-V method [1]. In addition, capacitors were also characterized using thermally-stimulated-current (TSC) and standard (1 MHz) high-frequency C-V measurements. ICs were characterized for changes in timing and leakage current parameters and functionality.

Delidded devices were irradiated using a 10-keV x-ray source at a dose rate of 167 rad(SiO_2)/s (within the dose-rate range specified by MIL-STD 883D, Method 1019.4). To evaluate the effects of biased elevated-temperature anneals on the radiation response, devices were evaluated with and without a 150°C, 1-week biased anneal.

For this summary, data is presented only for transistors and ICs manufactured in Sandia's CMOS IIIA technology [2]. This technology uses radiation-hardened process techniques for both the gate and field oxide. In addition, TSC measurements were performed on capacitors with two flavors of hardened field oxides (noted here as HFOA and HFOB) manufactured at Sandia. HFOB is similar in nature to the hardened field oxide used in the CMOS IIIA technology. In the full paper, results will be presented for devices manufactured by other suppliers.

III. RESULTS

The effects of burn-in on the radiation response of gate- and field-oxide transistors from the same wafer is illustrated in Figure 1. This figure is a plot of the threshold-voltage shift as a function of dose for n-channel gate-oxide transistors irradiated without a preirradiation burn-in and for transistors subjected to a 150°C, 1-week burn-in prior to irradiation. The gate-to-source bias during both burn-in and irradiation was 5 V. The open symbols give the threshold-voltage shifts after a 600-s postirradiation room temperature biased anneal. The figure in the inset is the threshold-voltage shift for

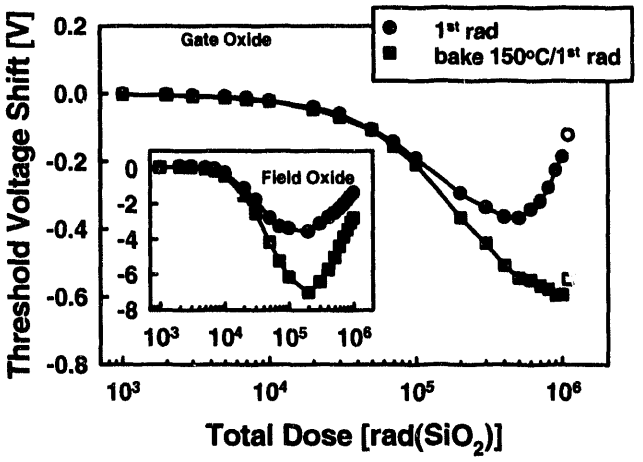

Figure 1: Threshold-voltage shift versus total dose for gate and field (insert) oxide transistors irradiated with (squares) and without (circles) a preirradiation 150°C burn-in.

field-oxide transistors with and without burn-in. The radiation response is qualitatively similar for both the gate-and field-oxide transistors. Transistors that were subjected to a preirradiation burn-in show a much larger decrease in threshold voltage than the transistors without a burn-in. At approximately 400 krad(SiO_2), the threshold voltage for the non-burned-in gate-oxide transistors begins to turnaround. After irradiating to 1 Mrad(SiO_2), the threshold-voltage shift for the gate-oxide transistors without a burn-in is approximately three times less in magnitude than the threshold-voltage shift of the transistors with a preirradiation burn-in.

The large turnaround in threshold voltage for the gate-oxide transistors irradiated without burn-in suggests a larger increase in interface traps in the non-burned in case than the burned-in case [3]. This is

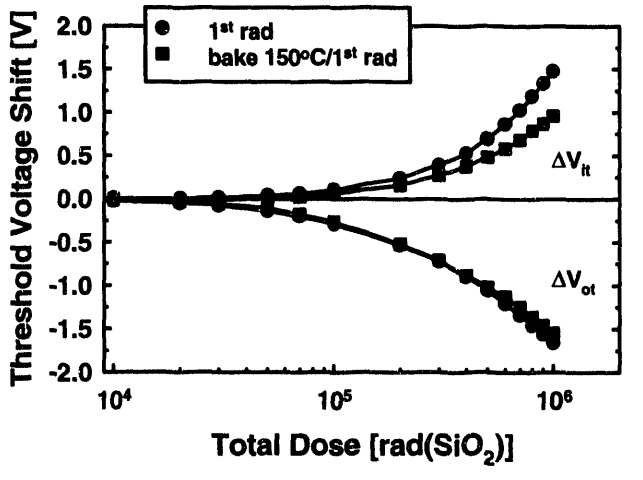

Figure 2: Threshold-voltage shifts due to interface-trap and oxide-trap charge for the gate-oxide transistor data of Figure 1.

confirmed in Figure 2 where the threshold-voltage shifts due to interface and oxide-trap charge for gate-oxide transistors are plotted for the data of Figure 1. Within experimental uncertainty, there is no difference in oxide-trap charge buildup, but the interface-trap charge buildup is larger by approximately 0.5 V at 1 Mrad(SiO_2) for the transistors without a preirradiation burn-in. Thus, for these devices the major cause of the turnaround in threshold voltage during irradiation for the transistors without a preirradiation burn-in, as well as the larger negative threshold-voltage shift for the transistors with a preirradiation burn-in, is due to differences in interface-trap buildup. The conclusion we draw is that burn-in appears to suppress the radiation-induced buildup of interface traps.

The difference in interface-trap buildup for the transistors with and without a preirradiation burn-in should lead to differences in the amount of degradation in timing parameters for an IC with and without burn-in [4,5]. Note that the dominant failure mechanism in space environments for ICs built in CMOS technologies with large interface-trap buildup is usually related to changes in "timing" parameters [4,5]. This is illustrated in Figure 3 where the change in address-enabled read-access time (T_{ac}) for 16k SRAMs is plotted versus irradiation. The burn-in and irradiations were performed with the ICs written in a checkerboard pattern. The access time for the ICs was measured with the memory written with a 1's pattern. The power supply voltage, V_{DD}, during burn-in, irradiation, and measurement was 5 V. Access times were also measured with a 0's pattern written into the memory, with qualitatively similar results. The data of Figure 3 are the average read-access times for several SRAMs. The read-access time for a given SRAM is the average read-access time for 8000 memory locations (all the locations written with 0's during the irradiation). Note that the increase in access time is about a factor of two higher after irradiating to 1 Mrad(SiO_2) for the ICs without a preirradiation burn-in. This is consistent with a larger buildup of interface traps for these devices as suggested by the transistor data (Figure 2). In addition, these data would suggest performing qualification using non-burned SRAMs for this technology would significantly overestimate the timing degradation in a space environment, as we will discuss in more detail later.

The data of Figure 3 is the average over several SRAMs. The same trends were also observed for the variation in read-access time for the individual memory

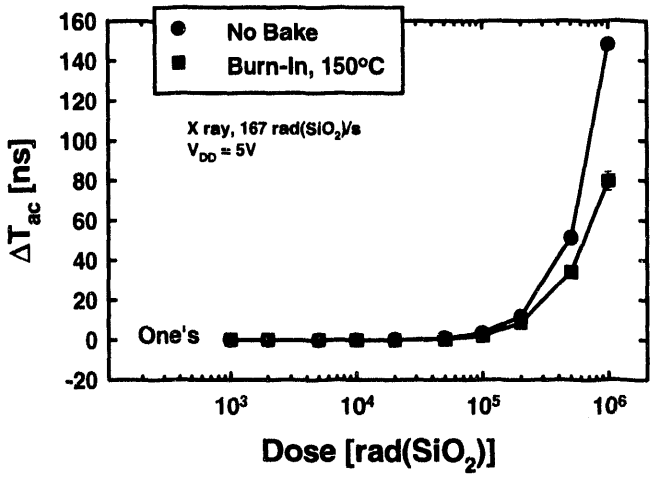

Figure 3: Change in address-enabled read-access time for 16k SRAMs irradiated with (squares) and without (circles) a preirradiation 150°C burn-in.

cells within an SRAM, as would be expected. Figure 4 is the distribution in the radiation-induced change in read-access times for 8000 memory cells from a single SRAM. For the SRAMs irradiated without a preirradiation burn-in the change in the read-access time peaks at 82.9 ns with a standard deviation of 3.4 ns. For the SRAMs irradiated with a preirradiation burn-in, the change in the read-access time peaks at 148 ns with a standard deviation of 8.0 ns. Thus, the radiation-induced change in read-access time for SRAMs irradiated with a preirradiation burn-in is approximately 44% lower than the change in read-access time for SRAMs irradiated without a preirradiation burn-in. In addition, the standard deviation in the change in read-access time for SRAMs irradiated without a preirradiation burn-in is almost 2.5 times more than that for ICs irradiated with a preirradiation burn-in. Hence, the burn-in reduces the variation in the radiation-induced change in read-access time to each memory location.

Another IC parameter that was affected by the preirradiation burn-in was the "standby" power supply leakage current, I_{DD}. However, "as we might expect," the ICs that were irradiated with a preirradiation burn-in had the largest increases in I_{DD}. The leakage current is caused primarily by large negative threshold-voltage shifts of both n-channel gate-oxide transistors and parasitic field-oxide transistors [2,6]. As the threshold voltages tend toward depletion, there is a significant increase in I_{DD}. The maximum value for I_{DD} for ICs irradiated with a preirradiation burn-in was an order of magnitude greater than the maximum value for I_{DD} for ICs irradiated without a preirradiation burn-in. Thus, as we discuss later, qualification testing of ICs, from this technology, that are to be use in environments were I_{DD} currents dominate the radiation response must be done on burned-in ICs to prevent underestimating the "standby" power supply leakage current of the ICs. IC leakage current data will be presented in the full paper.

To provide insight into the mechanisms responsible for the reduced interface-trap buildup in devices irradiated with a preirradiation burn-in, thermally-stimulated-current and capacitance-voltage measurements were performed on field-oxide capacitor structures. Previous TSC experiments on gate-oxide capacitors had shown that after a typical TSC measurement (in which the temperature is ramped from 25 to 350°C with a constant gate bias) that the flatband voltage measured (using C-V techniques) after TSC is performed on an irradiated capacitor is identical to the flatband voltage preirradiation [7]. This is an indication that, for these gate oxides, all radiation-induced charge has been annealed out during the TSC measurement. TSC measurements were taken on two flavors of hardened-field-oxide capacitors, referred to as HFOA and HFOB. The field oxide for the HFOB capacitors is similar to that used in the CMOS IIIA process. Results of the measurements are presented in Figure 5 where the flatband voltage is plotted following various irradiations and TSC runs. The squares are pre flatband voltages. The triangles are flatband voltages measured after a TSC run (25 to 350°C). The circles are flatband voltages measured after irradiation. Details of the irradiation and anneal conditions in Figure 5 will be presented in the full paper. Note that, for both types of hardened-field oxides, the flatband voltage measured after a TSC measurement does not always return to the

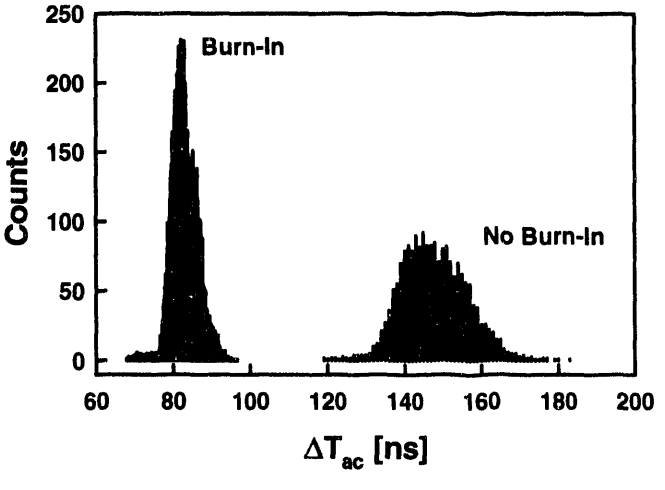

Figure 4: Distribution of the change in read-access time for ICs irradiated with and without a preirradiation burn-in.

preirradiation value. This indicates that there are large instabilities in these hardened-field oxide capacitors. Whether or not these instabilities are a source of the differences observed for devices irradiated with and without a preirradiation burn-in is not yet known. These instabilities may explain the differences observed in IC leakage currents between the non-burned-in and burned-in ICs. These results suggest that other technologies using hardened-field oxides may also show similar radiation responses before and after burn-in to those shown above. In the full paper, we will discuss other possible mechanisms for the reduced interface-trap buildup for burn-in devices. For example, we will relate our results to the enhanced interface-trap buildup (caused by hydrogen gas) observed by Kohler et. al [9].

IV. HARDNESS ASSURANCE IMPLICATIONS

Based on the above results, for some technologies, whether or not a device is burned-in before irradiation may have a significant impact on the response during irradiation. For a low-dose-rate environment (e.g. space), IC degradation can be governed primarily by increases in the number of interface traps which lead to degradation in timing parameters [4,5]. From Figures 2 and 3, the ICs irradiated with a preirradiation burn-in have approximately one-half the increase in read-access time than for ICs irradiated without a preirradiation burn-in. Thus, performing radiation qualification using non-burned-in devices from this technology may significantly overestimate the timing degradation in a space environment. This may cause the unnecessary rejection of ICs that may be suitable for actual system use, leading to increased system cost. In contrast, performing radiation qualification using non-burned-in devices, from technologies whose radiation response is dominated by leakage current, may significantly underestimate the leakage current degradation of ICs in the use environment. For example in high-dose-rate environments, at short times after irradiation IC response is governed primarily by increases in IC leakage current. As will be shown in the full paper, devices that pass radiation qualification may fail their intended use.

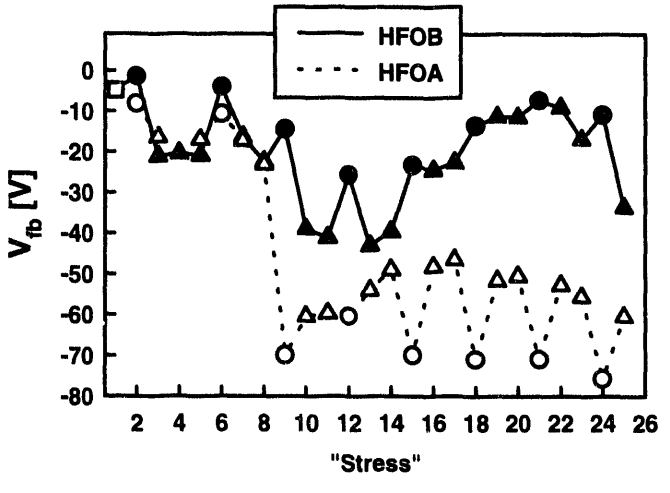

Figure 5: Flatband voltages following a number of different irradiation (circles) and TSC measurement (triangles) conditions.

The present MIL-STD-883D test guideline does not specify the need to burn-in devices prior to radiation testing. These results suggest that, for some technologies, radiation qualification may need to be performed on devices that have been subjected to all elevated-temperature anneals required by system specifications.

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