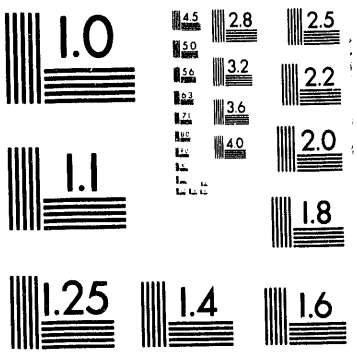
1.0
1.1
1.25
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2.0
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1 of 1

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Application of the Modified Voltage-Dividing Potentiometer to Overlay Metrology in a CMOS/Bulk Process†

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ABSTRACT

The measurement of layer-to-layer feature overlay will, in the foreseeable future, continue to be a critical metrological requirement for the semiconductor industry. Meeting the image placement metrology demands of accuracy, precision, and measurement speed favors the use of electrical test structures. In this paper, a two-dimensional, modified voltage-dividing potentiometer is applied to a short-loop VLSI process to measure image placement. The contributions of feature placement on the reticle and overlay on the wafer to the overall measurement are analyzed and separated. Additional sources of uncertainty are identified, and methods developed to monitor and reduce them are described.

Introduction

The projected requirements for the placement of features by lithography systems for coming generations of VLSI processing require metrological tools having *precision* and *accuracy* on the order of several nanometers. Earlier work [1,2] described improvements to the voltage-dividing potentiometer test structure and test methodology [3,4] for this application. The precision of measurements made using the modified voltage-dividing potentiometer test structure (seen in Figure 1) was demonstrated to be better than 20 nm (3σ) precision for a chrome-on-glass mask. This result represented a substantial improvement over earlier capabilities. The goal of the current work is a) to apply this metrological technique to CMOS process tools and b) to refine the test structure design and associated measurement method to meet the metrological requirements of future lithographic processes.

In this paper, we identify extensions to this test structure that are intended to improve its overall precision for identifying and eliminating unintended process-related anomalies that can manifest as registration errors. These apparent registration errors, which include the actual, physical placement of the lines on the reticles and subsequent effect on the measurement of level-to-level registration, can be large compared to the actual registration error of an advanced stepper. In this paper, the term *net mask pattern mismatch* or simply *pattern mismatch* refers to the placement of features on the reticles by the primary pattern generator; the term *registration* refers to the layer-to-layer alignment of a set of corresponding features on two photomask layers by the

stepper to a predetermined reference coordinate.

A second issue addressed is the effect of the local variation of the linewidth on the measured registration. Initial models have suggested that this can cause an error in the determination of registration. The newest designs provide for the measurement and elimination of this effect.

Modified Voltage-Dividing Potentiometer Test Structure

The modified voltage-dividing potentiometer[†] provides improved performance when compared to previous potentiometer techniques by two enhancements: the systematic error in the length of the bridge due to the presence of voltage taps, δL, is measured and eliminated, and the taps that make up the potentiometer are placed closely to minimize random error. δL is given by

$$\delta L = L_1\left(\frac{V_4 - V_3}{n V_4}\right)$$

where V_3, V_4, and L_1 are defined as shown in Figure 1 and n is the number of "dummy tap" pairs in segment 3 of Figure 1. The overlay x is thus given by

$$x = \left(\frac{V_1 - V_2}{V_1 + V_2}\right)\left(\frac{L - \delta L}{2}\right)$$

where V_1, V_2, and L are defined as shown in Figure 1. Note that if any of the taps are defined

[†] A full discussion of the basic test structure and measurement technique may be found in reference [1].

in different layers or different process steps, such as was done for the current work, a δL must be determined for each type of voltage tap.

Test Structure Design

A set of test structures was designed to be compatible with 2-μm CMOS design rules. Previous work [1] has shown that the linewidths in the test structure are not factors which affect the performance of this measurement technique.

Primary Design

The basic test structure used in this work is a compact double-mask (voltage taps *and* bridges formed by the second mask step) seen in Figure 2. This test structure utilizes a single potentiometer bridge, as had been reported previously [1], but it includes the voltage taps needed to incorporate three built-in design offsets (i.e., the spacing of the center tap from the design midpoint between the end taps). The built-in offsets chosen for this experiment were -0.5, 0.0, and -0.5 μm.

Secondary Design

Additional design modifications were made to extend the usefulness of the test structure as well as to reduce or eliminate several second-order effects. These structures were configured in such

a way as to include a van der Pauw resistor and elements of a linewidth bridge. These elements allow the measurement of the electrical linewidth of the actual alignment bridge as seen in Figure 2.

Layout

Five test structures were arranged on a 14- by 14-mm exposure field such that the principal diagonals of each exposure field were spanned. Each field was stepped at 73 sites on a 150-mm wafer. This allowed for the feature placement and linewidth to be determined along several directions across the diameter of the entire wafer. Additional structures were also placed in the test chip, including registration targets for the stepper and traditional optical alignment test structures.

Sample Preparation and Electrical Testing

Two 5X reticles were produced from the test structure design. The first level is a bright field reticle and defines the basic bridge resistor. The second level is a dark field reticle and defines the locations of the center taps.

A 300-nm-thick n-type (implanted with phosphorous, 5×10^{15} cm^{-3}, at 130 keV) polysilicon film was deposited on an insulating film on the test wafers. The first-level reticle was stepped across the wafers using a g-line stepper with a 0.42-NA lens into a positive photoresist layer. After

development, the polysilicon was plasma-etched using Cl_2/He/HBr chemistry. The process was basically repeated with the second-level reticle which was registered relative to the alignment targets on the first level and stepped at each site on the wafer to reveal the complete test structure features.

The wafers were tested using a parametric test system. The measured sheet resistance was approximately 50 Ω/□. General procedures for testing the structure were similar to those found in [1]. In order to eliminate data from defective test structures or measurements, two exclusion criteria were employed. First, any data with a measured offset greater than 10 μm were excluded. Second, any data that did not meet the following self-consistency check were removed: the measured resistance of a bridge pair was compared with the sum of the resistances of the individual bridges. If these sums were substantially different (>1 Ω), the data was presumed to be corrupt. From the data on the remaining test structures, the offsets x were calculated.

Overlay Error, Pattern Mismatch Error, and Registration Error

Figure 3 shows schematically the patterning of each of two masks with four square features. To simplify the discussion, features 1 and 2 on each of the two masks are assumed to be correctly located relative to the coordinate systems defined by the respective masks' alignment marks in the lower left and the upper right of the exposure fields. Similarly the optics of the aligner tool are assumed to image without distortion. Feature 3 on the first mask is misplaced to the left by two units. Feature 4 on the second mask is misplaced to the right by one unit. The features on

the first mask represent the end-tap pairs of four potentiometers, and those on the second mask represent their complementary center taps.

Figure 4 shows a die site on a substrate having four composite features, representing testable potentiometers, defined sequentially by the two mask levels. Each of the four composite patterns in each die site on the substrate have generally different local overlay errors, which are spatially dependent measures of the losses of the fidelity of the composite patterns, at each location within the die site. The losses result from two independent mechanisms whose effects are additive.

The first mechanism is the net projected feature fidelity loss, or *pattern mismatch error*, sustained exclusively as a result of the drawn feature misplacement on each of the two separate mask levels. At any fixed point within each die site the portion of the overlay error attributable to pattern mismatch is the same at every die site on the substrate. The second contribution to overlay error within a die site is the effect of net mask misregistration and/or alignment error, or *registration error*. Unlike the effect of pattern mismatch error, registration error is generally different at different die sites on the substrate but is constant within a given die site. The following discusses both pattern mismatch and registration errors in terms of measurements of overlay error at each composite pattern location within each die site.

It is convenient first to define patterning mismatch by considering the "best possible" overlay of the two sets of features as illustrated in Figure 5. Whereas no two complementary components within the hypothetical die site exactly register on the substrate shown in Figure 5, the relative

alignment of the two masks is such that the sum of the squares of the four overlay errors is minimized. This condition of best possible registration is affected when the first moments of the two sets of individual projected images about some point are equal. Such a condition is defined here to be zero registration error. The four vector patterning mismatches are then defined to be the contributions to the respective overlay errors that prevail when zero registration error is attained, as shown in Figure 5. Finally, overlay error is defined to be the vector sum of registration error and pattern mismatch error.

Overlay Error Measurement Algorithm for Extraction of Registration Error and Pattern Mismatch Error

Consistent with the previous definitions, measurement of overlay error extracted from a particular potentiometer is an estimate of the sum of registration error and the pattern mismatch error for that potentiometer. Ideally, measured overlay error is the net difference between the center-tap end-tap locations, adjusted for any design offset.

Typically, residual errors originating in the tester and patterning imperfections are superposed on the measurements. The dominant source observed is generally the processing-induced imperfections in the film materials and in their patterning.

One objective of the current work is to separate the contributions to measured overlay which are

produced by pattern mismatch, registration errors, and residual errors. The approach used fits the individually measured overlays, extracted from the same three potentiometers replicated on a selection of die sites, to a model which superposes registration error to intrasite, location-dependent, pattern mismatch error.

Specifically, if die site i, of a total of N_s sites, sustains registration error M_i, and the actual net patterning mismatch for potentiometer j, of a total of N_p potentiometers per die site is P_j, then the overlay error, O_{ij}, is $M_i + P_j$. However, due to the random errors introduced above, the *measured* overlay error O'_{ij} will generally differ from the *actual* overlay error, O_{ij}. In order to estimate the desired values of M_i and P_j, the conventional practice of minimizing the sum of the squares $\Sigma\Sigma(O'_{ij} - O_{ij})^2$ with respect to M_i and P_j results in the generation of $N_s + N_p$ simultaneous linear equations. However, of these, only $N_s + N_p - 1$ are independent. A necessary additional relationship is obtained by the previous definition of zero registration error when the overlay is minimized at each die site, i.e., $\Sigma P_j = 0$. Use of this last relationship effectively renders the determinant of the coefficients M_i and P_j of the simultaneous linear equations non-singular, enabling them to be determined.

Example of Extraction of Overlay, Pattern Mismatch, and Registration Errors

The pattern mismatch and registration error extraction algorithm described above was applied to measurements of overlay error from 27 die sites having three potentiometers in each of two

directions identified here as "vertical" and "horizontal."

Table 1. Initial Measured Values of Overlay

		Overlay Error Measurement Statistics (nm)					
		Horizontal			Vertical		
		x1	x2	x3	x1	x2	x3
Drawn		-500	0	500	-500	0	500
Measured	Mean	-473	30	545	-408	81	586
	STD	79	71	69	60	113	75

Table 1 lists the initial means and standard deviations of the two sets of 81 overlay error values of x1, x2, and x3, seen in Figure 2, for the vertical and horizontal potentiometers measured by the parametric testing system. For both sets, the means reflect the drawn offsets of -500 nm, 0, and +500 nm of the x1, x2, and x3 potentiometers, respectively. However, there exists substantial scatter in the initial measurement data which reflects the scatter in the registration errors at the 27 die sites. The results which follow show how this scatter is resolved by separating the measurement data into contributions deriving from pattern mismatch and registrations errors, respectively, by using the algorithm described in the previous section.

Table 2. Average Extracted Registrations

		Registration Error Measurement Statistics (nm)	
		Horizontal	Vertical
Drawn (mean)		0	0
Measured	Mean	34	87
	STD	43	41

Table 2 shows the mean and standard deviations of the registrations extracted from the initial vertical and horizontal measurement data sets. The magnitude of the extracted mean for registration is somewhat arbitrary and is a function of the method used to determine "perfect" registration. Other definitions of "perfect" registration result in a change in the mean value by a constant; however, the standard deviations of the registrations remain unchanged.

Table 3. Resultant Pattern Mismatch Errors

	Net Mask Patterning Mismatch Statistics (nm)					
	Horizontal			Vertical		
	x1	x2	x3	x1	x2	x3
Drawn	-500	0	500	-500	0	500
Extracted Mean	-507	-4	511	-494	-6	500

Table 3 shows results from pattern mismatch errors. These errors were determined to be less than or equal to 11 nm when compared to the design values, for the 16 samples tested. This value is in general agreement with results previously reported for determining pattern mismatch errors by directly electrical testing of photomasks [1]. The values represent an upper limit on the quality of the photomask and any errors introduced by the fabrication process, test structure design, and the measurement method.

Conclusions

For the first time, the modified voltage-dividing potentiometer methodology has been applied to the separation of on-wafer overlay error measurements into contributions from pattern mismatch

error and registration error. The test structures were fabricated using commercial materials and tools. Although the raw data exhibited relatively high scatter, possibly due to the film's being polysilicon of relatively high sheet resistance, a straightforward algorithm for identification of patterning mismatch and registration errors provided values of the mean and the standard deviation of the registration error for the 27 die sites which were tested. These values were nominally within the aligner-tool manufacturer's specifications, suggesting that the measurement technique contributed little if any error to the measurement data.

Furthermore, the values derived for the mask patterning mismatch substantially validate the measurement technique for estimating the mask patterning mismatch errors. When these are compared with the drawn values, the agreement is less than or equal to 11 nm in all cases. This number bounds errors contributed by the mask patterning, the on-wafer pattern replication, and the measurement technique itself.

As device geometries become smaller, overlay budgets will also correspondingly shrink. Pattern mismatch and level-to-level registration, as well as the metrology associated with measurement of these parameters, will be of increased importance in manufacturing advanced semiconductor products.

Acknowledgments

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Figure Captions:

Figure 1: The modified voltage-dividing potentiometer test structure.

Figure 2: The two-dimensional, two-layer modified voltage-dividing potentiometer test structure.

Figure 3: Features on two masks *as drawn* by the primary pattern generator

Figure 4: The relative placement of the features shown in Figure 3 *with non-zero* registration error.

Figure 5: The relative placement of the features shown in Figure 3 *with zero* registration error.

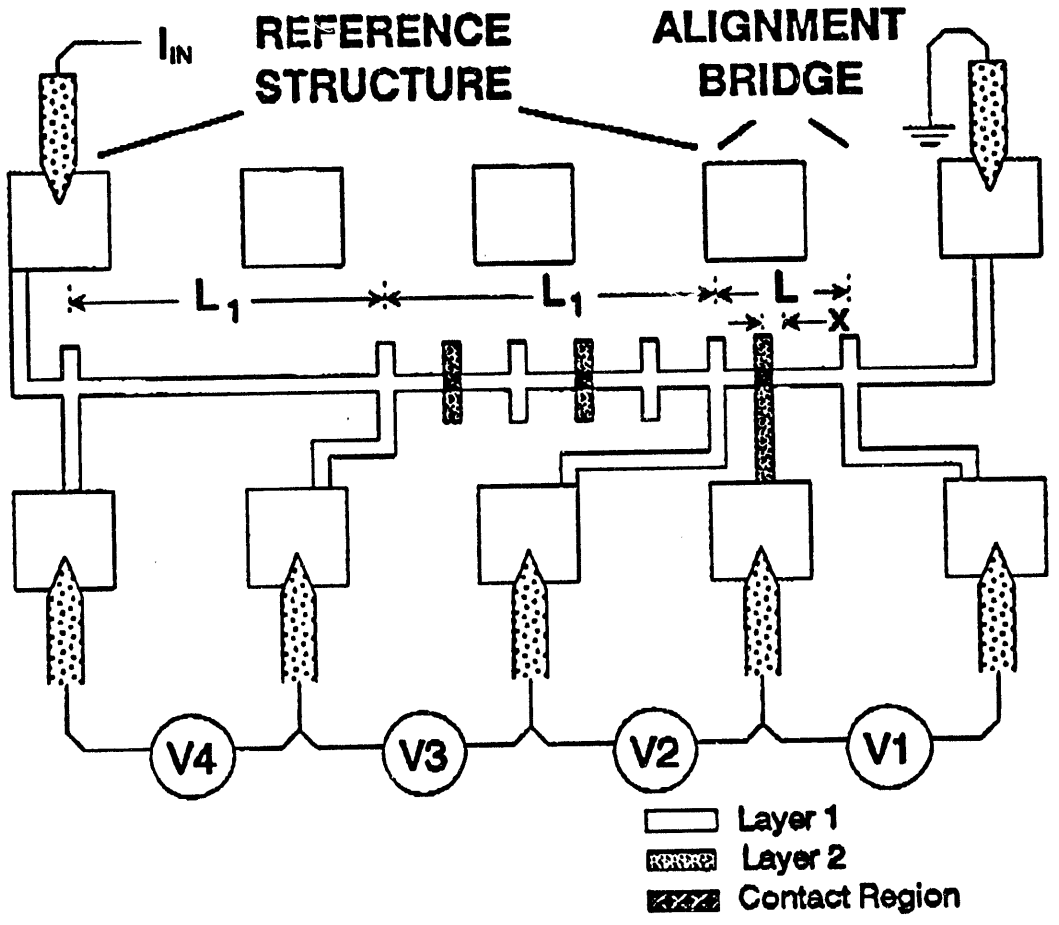
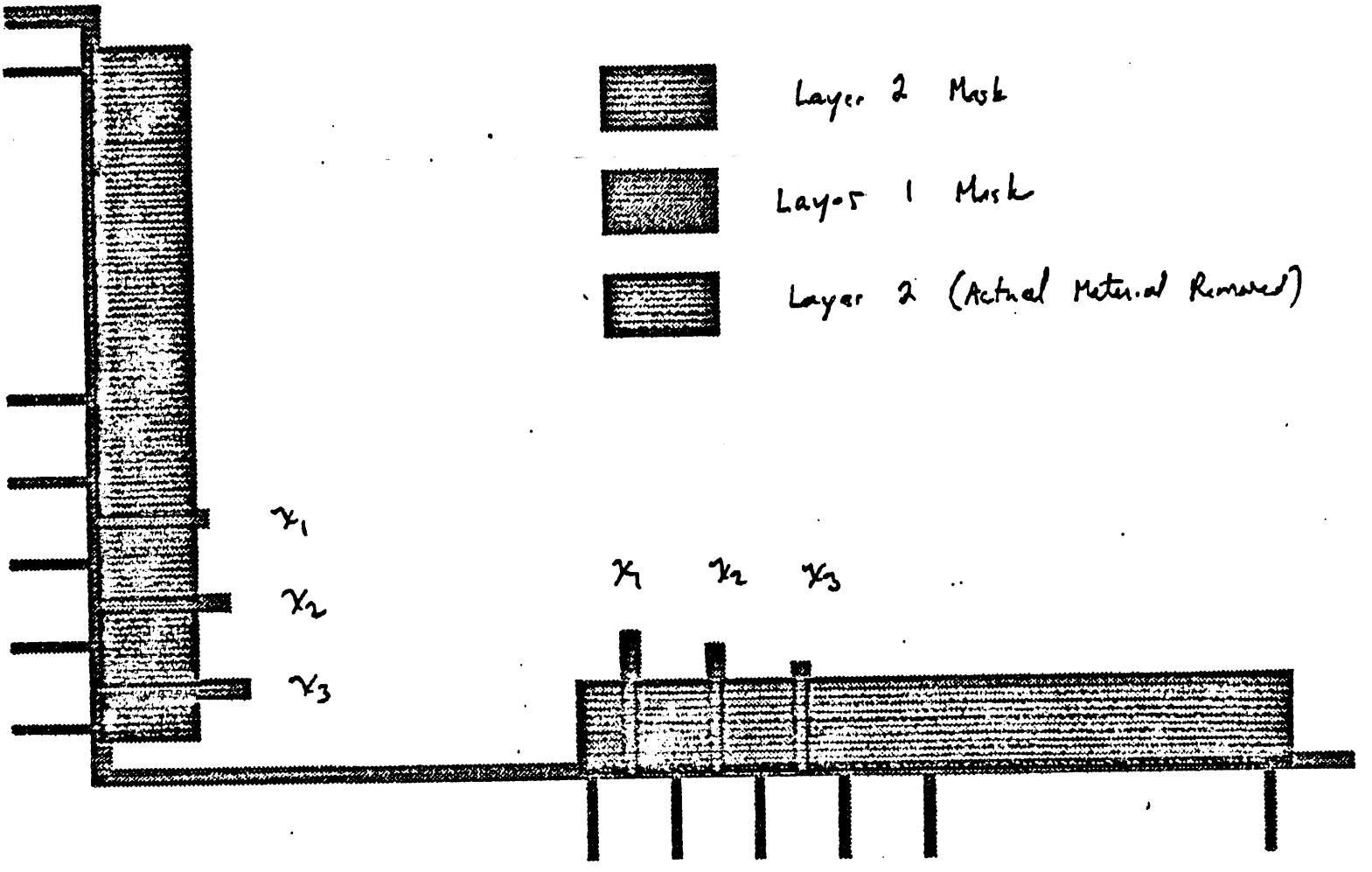

I_{IN}
REFERENCE STRUCTURE
ALIGNMENT BRIDGE
L_1
L_1
L
X
V4
V3
V2
V1
Layer 1
Layer 2
Contact Region

Figure 1



~~Figure transmissive two layer test structure~~

Fig 2

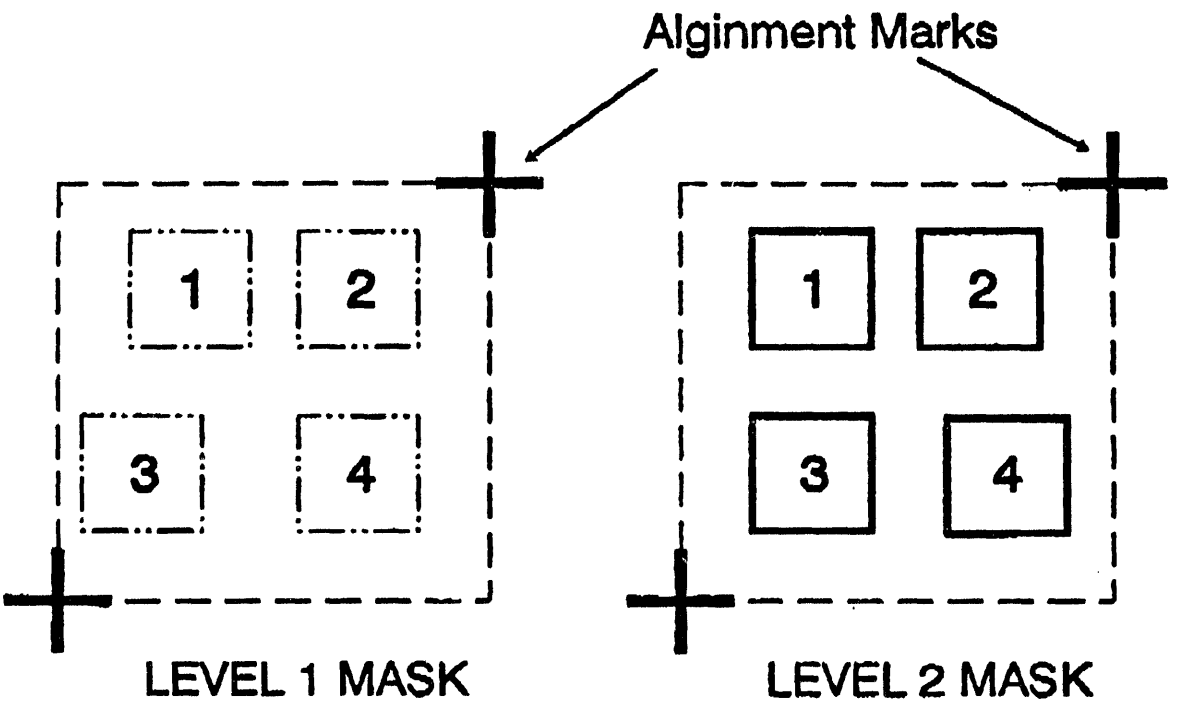


Figure 3

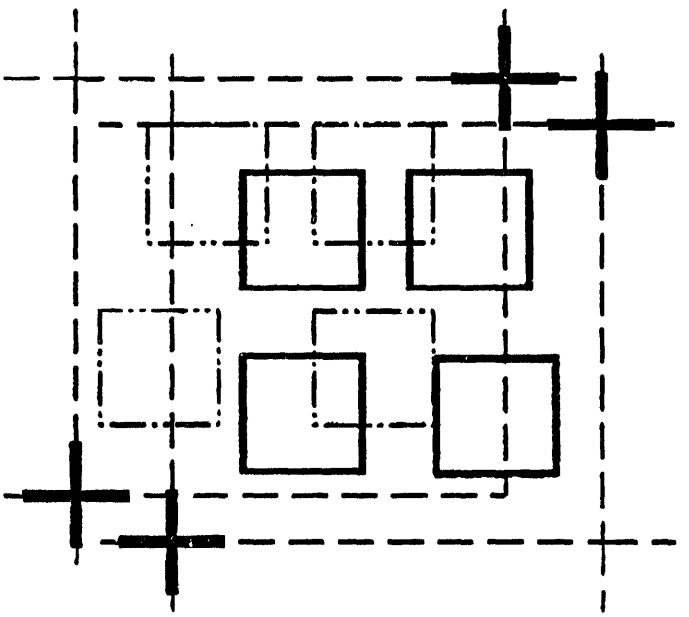


Figure 4

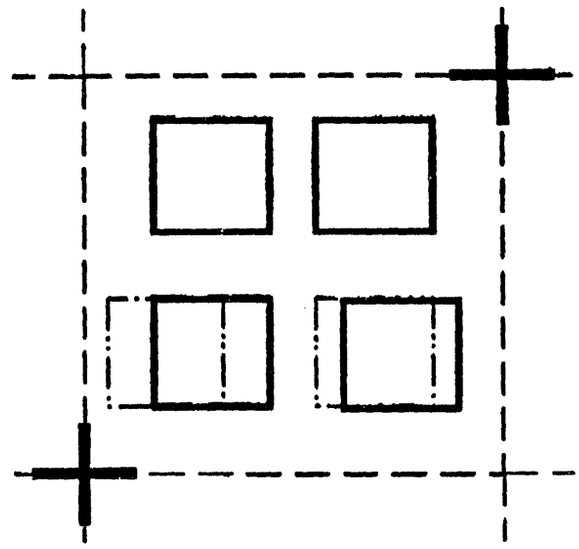


Figure 5

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