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Innovative Sputtering Techniques for CIS and CdTe Submodule Fabrication

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FOREWORD

This document serves as an interim technical progress report for the National Renewable Energy Laboratory (NREL) program YG-1-11070-1, "Innovative Sputtering Techniques for CIS and CdTe Submodule Fabrication," for the Phase 1 period of the contract initiating on 1 September, 1991 and ending on 30 August 1992. This effort was designed to study innovative deposition techniques, such as the rotating cylindrical magnetron sputtering system and electrodeposition for large-area, low-cost copper-indium-diselenide (CIS) and cadmium-telluride (CdTe) devices. Technical Monitor of this project is Dr. Harin Ullal, NREL.

Contract YG-1-11070-1 was performed at Martin Marietta Astronautics Group in Denver, CO, by the R&T Mechanical Group in Central Technical Operations. The primary subtier contractor for this effort was International Solar Electric Technology, Inc (ISET) from Inglewood, CA. ISET is a small, disadvantaged business who are experts in the field of CIS and CdTe thin-film devices. Team Members include:

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1.0 INTRODUCTION

A key issue for photovoltaics (PV), both in terrestrial and future space applications, is producibility, particularly for applications utilizing a large quantity of PV. Among the concerns for fabrication of polycrystalline thin-film photovoltaics, such as copper-indium-diselenide (CIS) and cadmium-telluride (CdTe), are production volume, which translates directly related to cost, and minimization of waste. Both rotating cylindrical magnetron (C-Mag™) sputtering and electrodeposition have tremendous potential for the fabrication of polycrystalline thin-film photovoltaics due to scaleability, efficient utilization of source materials and inherently higher deposition rates. In the case of sputtering, the unique geometry of the C-Mag™ facilitates innovative cosputtering and reactive sputtering that could lead to greater throughput, reduced health and safety risks, and ultimately lower fabrication cost. Electrodeposited films appear to be adherent and compatible with low-cost fabrication techniques.

This NREL program entitled "Innovative Sputtering Techniques for CIS and CdTe Submodule Fabrication," is organized in two phases. Phase 1, which this report covers, began at ATP on 1 Sept, 1991, and continued until 30 August, 1992. This phase involves the initial film and device fabrication using the two techniques mentioned above. Devices were tested by both internal facilities, as well as at NREL and ISET. Phase 2 involves the device optimization with a goal of 8% efficient cells and a 930 cm^2 (1 ft^2) monolithically-integrated module. As of this writing, devices with 8.4% and 6.3% efficiencies for CIS and CdTe have already been fabricated, and Phase 2 has been initiated.

2.0 POLYCRYSTALLINE THIN-FILM DEVICES

Both CIS and CdTe were chosen for this investigation. In both cases, a single heterojunction design was selected and are discussed below.

2.1 COPPER-INDIUM-DISELENIDE (CIS)

A schematic of the substrate CIS device structure selected for this investigation is shown in Figure 2.1-1. In all cases, 2.4 mm (0.093 in.) thick soda lime glass was used as a substrate. The back contact, Mo, was sputtered to a thickness of 1 μm. CIS, the absorber layer, was fabricated by selenization of copper (Cu) and indium (In) stacks using either the ISET two-stage selenization or the Se-vapor selenization developed at NREL. Final thickness of the CIS film was 2 μm. CdS, the n-type window layer, was deposited by a solution-growth method to a thickness of 1000 Å - 2000 Å. Finally, zinc oxide (ZnO), the transparent conductive oxide (TCO), was deposited by MOCVD. Nominal thickness was approximately 1 μm — 2 μm.

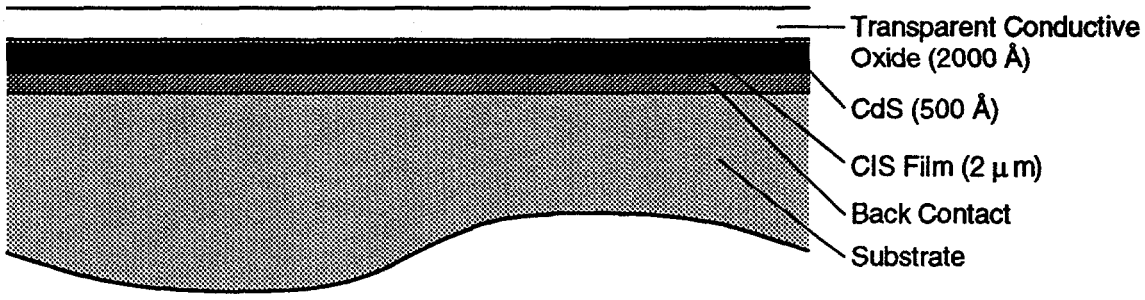

Figure 2.1-1 Schematic of the Heterojunction Structure of CIS Devices Used in this Investigation.

2.2 CADMIUM-TELLURIDE (CdTe)

A superstrate structure was selected for the CdTe devices in this investigation (Fig. 2.2–1). Soda lime glass 2.4 mm (0.093 in.) thick was used in this investigation as the superstrate. Two different types of TCO were studied, namely indium-tin-oxide (ITO) and tin-oxide

(SnO_2). Both conventional and haze tin-oxide were studied in order to improve the CdTe microstructure during electrodeposition. Thickness of the ITO ranged from 1000Å to 1500Å, while the SnO thickness was 2000 Å. A solution-grown CdS film with nominal 1500Å thickness was deposited on top of the TCO to serve as the n-type window layer. Next, a 1-2 μm thick CdTe film was electrodeposited on top of the glass/TCO/CdS stack. Finally, for these test devices, gold (Au) was evaporated onto the CdTe to serve as a back contact. Alternative back contacts are currently under investigations.

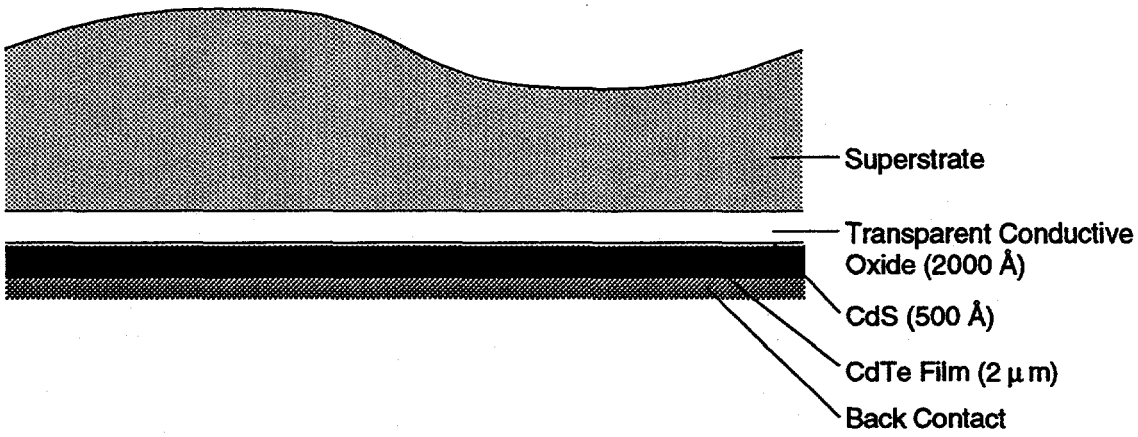

Figure 2.2-1 Schematic of the Heterojunction Structure of CdTe Devices Used in this Investigation.

The following sections discuss the deposition processes in detail, as well as the analysis of CIS and CdTe films and cells fabricated in this investigation.

3.0 THIN-FILM DEPOSITION TECHNOLOGY

A key issue for the commercialization potential of polycrystalline thin-film photovoltaics is low-cost, large-area deposition techniques with potential for large-volume production. Many deposition techniques, such as evaporation, produce high-quality devices but do not exhibit high compositional uniformity over large areas. Other techniques, such as screen printing, can result in large-volume production but has not exhibited high-efficiency devices.

Of the myriad of thin-film technologies available, two appear to be the most promising in terms of deposition efficiency, large-area film uniformity, and potential for high-volume manufacturing. Magnetron sputtering offers proven large-area deposition with good film uniformity. Furthermore, magnetron sputtering is commonly used to produce architectural glass using continuous in-line processing in excess of 1.9 million m^2 (20 million ft^2) per year. Electrodeposition, the second technique, offers the advantages of very low-cost capital investment, as well as the potential for large-area deposition. Furthermore, electrodeposition can produce films of uniform thickness and composition and lends itself easily to *in situ* intelligent processing technologies.

Both of these techniques have been used, with some success, in the fabrication of both CIS and CdTe devices. However, some work must be done on making sputtering and electrodeposition commercially viable for photovoltaic module fabrication. Discussion of the progress on these techniques is discussed below.

3.1 MAGNETRON SPUTTERING

As mentioned above, magnetron sputtering is a thin-film deposition technique with tremendous promise for fabricating CIS and CdTe in a production environment. In particular, planar magnetron sputtering systems have been used to coat optical coatings on glass for architectural applications to sizes in excess of 9.3 m^2 (100 ft^2). Difficulties arise when using planar magnetrons over large area which can impede its use in large-volume CIS and CdTe fabrication. Below, the fundamentals of direct current (DC) magnetron sputtering are discussed, including the potential difficulties with this technique for fabricating polycrystalline thin-film PV. Next, a variant of the planar magnetron new to photovoltaic device fabrication will be described, namely the rotating cylindrical magnetron,

which offers solutions to all of these problems faced by planar sputtering technology. Finally, the rotating cylindrical magnetron sputtering system used in these investigations will be described and data system characterization will be presented.

3.1.1 Planar Magnetron Sputtering

Planar magnetron sputtering is a common technique developed in the late 1950's which is used to deposit very large areas of materials with moderate-to-high melting temperatures. Both elemental and alloyed targets are used, and oxide film formation can be accommodated by planar sputtering in reactive environments, such as oxygen gas.

A schematic of a typical planar magnetron is shown in Figure 3.1.1-1 [Ref 1]. In this orientation, a target material serves as a cathode while the substrate to be deposited serves as an anode. Magnets are placed in such a manner as to define a closed path where magnetic field lines are parallel to the cathode surface. In operation, a voltage is applied across the anode and cathode which reside in a vacuum. Primary electrons are accelerated by the force generated from the **E X B** of the fields, but are constrained adjacent to the cathode by the closed path, or "racetrack", formed by the magnetic field. These electrons, in turn, ionize the working gas, typically argon (Ar), near the cathode and a discharge plasma is generated. However, the Ar ions, constrained in the racetrack and traveling in the opposite direction, are attracted to the cathode and bombard the target material. Bombardment of the target ejects material which then condenses onto the substrate passing parallel to the target.

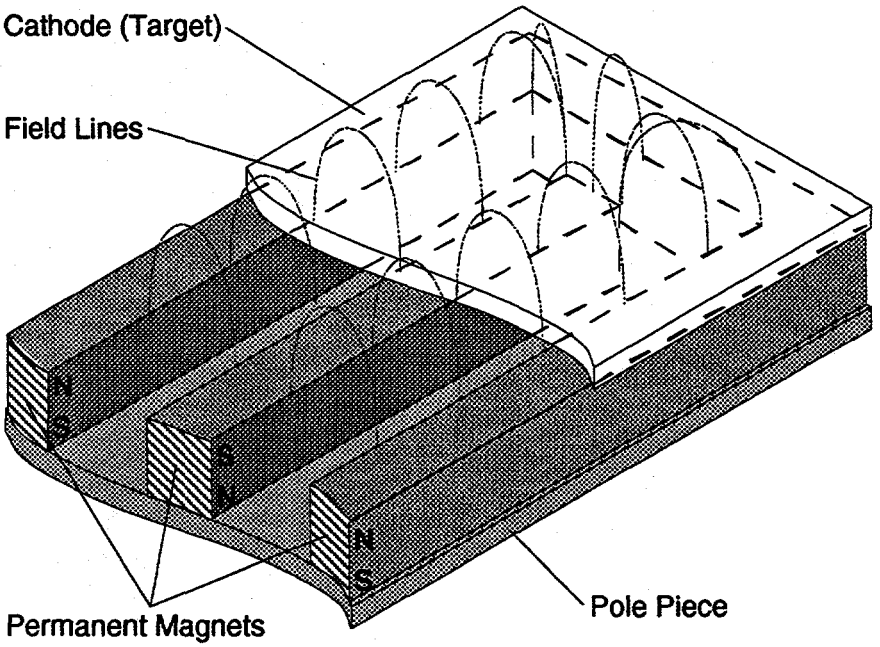

Figure 3.1.1-1 Schematic of a Planar Magnetron Showing Placement and Orientation of the Magnets and the Formation of the "Racetrack"

Several issues arise when working with planar magnetrons. First, because the closed magnetic field loop, or racetrack, is necessary for operation of the magnetron, it is by design that the magnetic field is nonuniform and that preferential erosion of the target occurs. This erosion, commonly referred to as "racetrack erosion" (Fig. 3.1.1-2), can result in significant removal of material in the racetrack. After a period of time, racetrack erosion results in destroying a target with only 25% of the material utilized in the deposition process. While these targets can be recycled, racetrack erosion results in significant downtime to allow for target replacement, which in a production environment, leads to significant reduction in production rates.

Another issue which becomes significant in polycrystalline thin-film PV is sputtering rates. Similar to downtime in continuous in-line processing, deposition rates can limit the maximum throughput of a system. Solutions to this type of limitation typically involve multiple magnetrons which adds to the complexity and cost of an in-line system. Planar magnetrons, by their design, have the cathode (or target) continuously in the presence of the plasma generated adjacent to it. Consequently, cooling of the target often consists of flowing water around the magnets and across the back of the target (or a backing plate bonded to the target).

Two concerns arise related to target cooling. First, if the water comes in direct contact with the target back, it is possible that water leaks could occur during normal operations, particularly when target materials reach the end of their service life. Second, it is difficult to cool the target effectively, particularly in areas near the magnet assembly. At best, inefficient cooling of the sputtering target limits the cathode power, which in turn, limits the ultimate deposition rate for the system. At worst, inability to

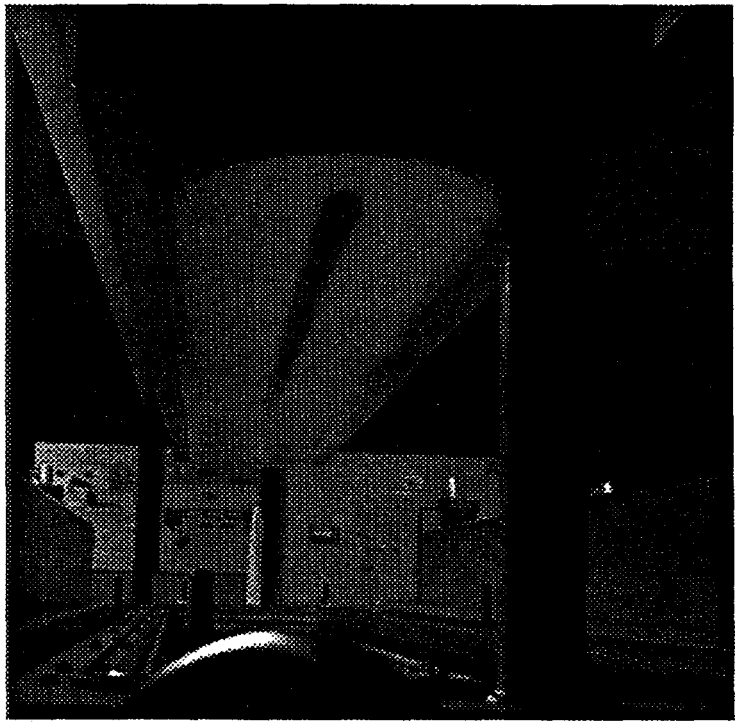

Figure 3.1.1-2 Photograph of a Planar Magnetron Showing the Emergence of a "Racetrack Erosion" Pattern.

cool the target sufficiently limits the types of materials that can be sputtered because of potential target melting.

3.1.2 Rotating Cylindrical Magnetron Sputtering

A unique solution to the problems described above is to make the target move with respect to the magnet assemblies. Such a solution is the rotating cylindrical magnetron as shown schematically in Figure 3.1.2-1. In this geometry, the targets are cylindrical and hollow to accommodate both cooling water and magnets. High-temperature seals at both ends of the target allow it to be rotated about its primary axis by a DC drive motor. High-strength iron-neodinium-boron (Fe–Nd–B) permanent magnets, which are used to define the racetrack, are held in place near the surface of the target parallel to, but offset from, the target's primary axis. Consequently, the magnetic field is concentrated at one side of the target where the substrate passes beneath (Fig. 3.1.2-2).

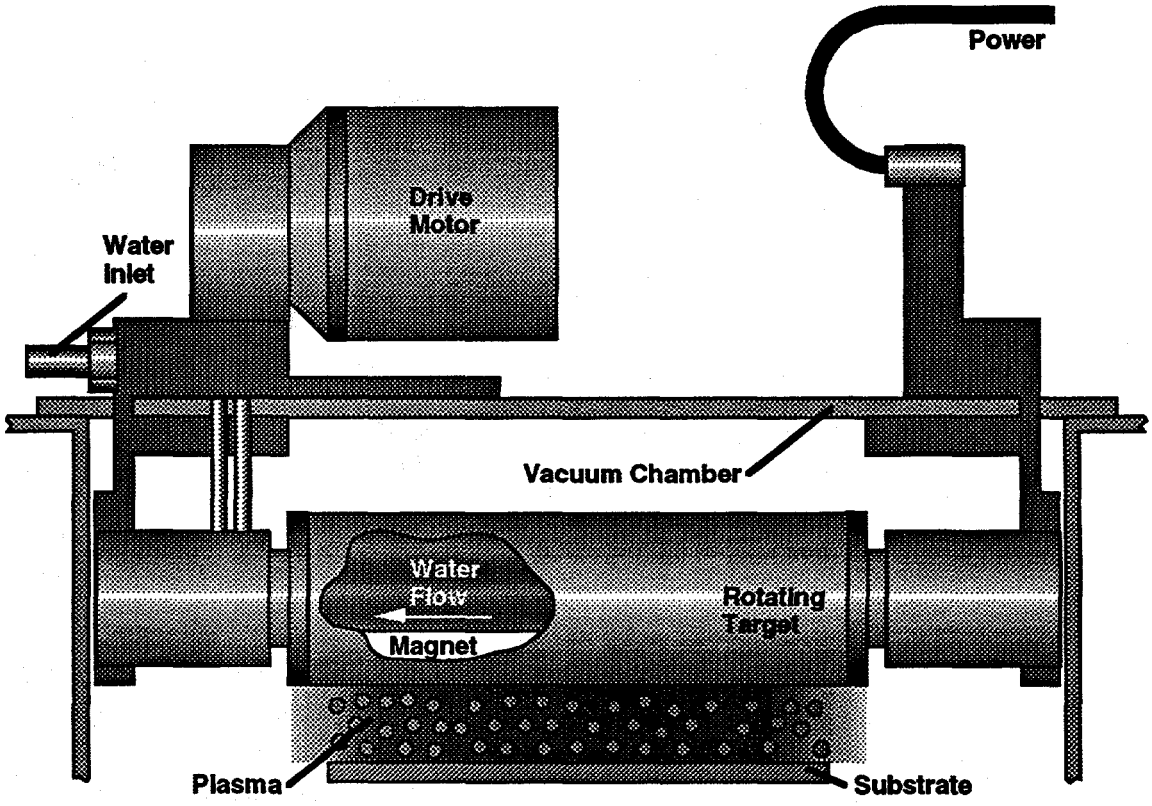

Figure 3.1.2-1 Schematic of a Rotating Cylindrical Magnetron

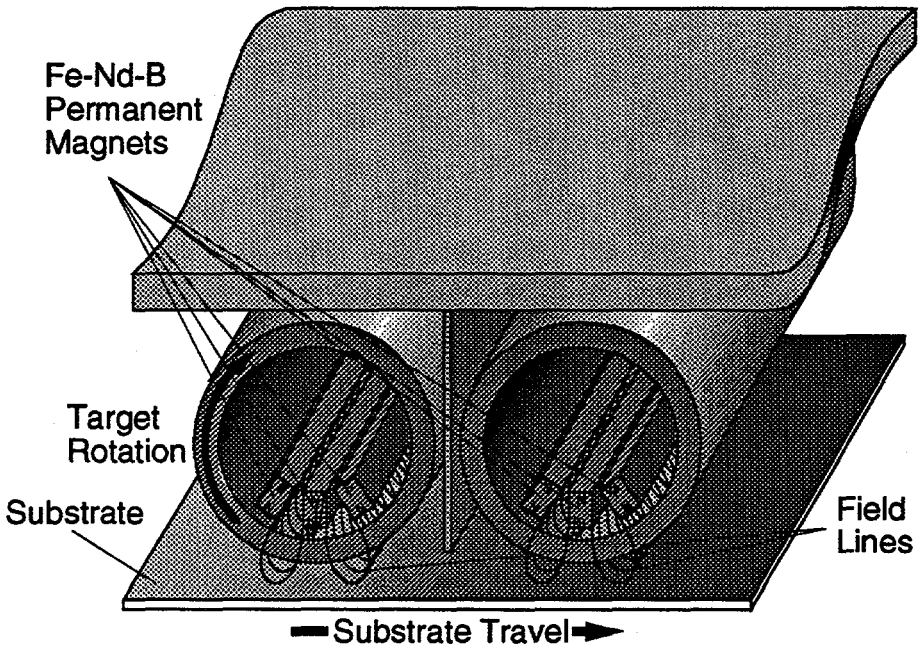

Figure 3.1.2-2 Schematic of a Rotating Cylindrical Magnetron Indicating the Location of the Racetrack

Nonuniform target erosion is solved by this configuration. First, because the target rotates through the racetrack, no preferential erosion appears short of the material outside of the racetrack turnarounds (Fig. 3.1.2-3). Target utilization for rotating cylindrical magnetron targets can be as high as 80% to 95% before replacement is required [Refs 2,3]. Thus, it is possible to develop large-volume continuous in-line sputtering systems for CIS and CdTe which do not require frequent maintenance for target replacement.

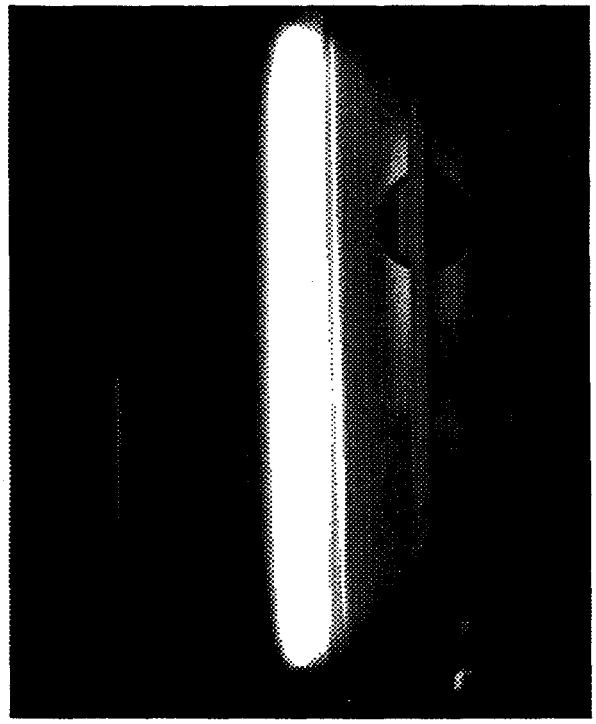

Figure 3.1.2-3 Photograph C-Mag Plasma During Sputtering.

Target temperature, which limits the ultimate deposition rate, is also addressed by

this design. By rotating through the racetrack, a given part of the target is not continuously in the presence of the plasma. When not in the plasma, water which flows through the target can cool the target more efficiently. Materials such as indium (In) and selenium (Se), which are low melting temperature materials but are essential for CIS devices, can now be sputtered at much higher deposition rates than possible with planar magnetrons. Difficult-to-fabricate and/or expensive materials can be fabricated into targets around stainless-steel backing sleeves with impressive results.

3.1.3 Martin Marietta C-Mag™ Sputtering Facility

Martin Marietta has developed a rotating cylindrical magnetron sputtering facility utilizing the AIRCO Dual 940 Modular C-Mag™ cathode as shown in Figure 3.1.3-1. This unit consists of two cathodes (targets) which are rotated by a common DC drive mechanism. Each target is powered and cooled independently which allows for dissimilar materials to be sputtered.

A photograph of the Martin Marietta C-Mag™ sputtering system used in this investigation is shown in Figure 3.1.3-2. Cathodes are mounted onto a swinging door which facilitates easy access for cleaning and maintenance. Two 10 kW Advanced Energy DC power supplies are used for sputtering. Access to the chamber is also possible from either end of the chamber (a load lock for improved throughput is already designed and planned for installation in the near future). A mechanical pump serves to rough out the chamber, while a turbo pump was selected for clean high vacuum down to 10^{-7} Torr. A liquid nitrogen Meissner trap is installed to minimize contamination of the turbopump by heavy metal vapor (Cd, Se) which could be potential hazardous. Substrates can be heated and maintained in excess of 400°C by calrod heaters. A

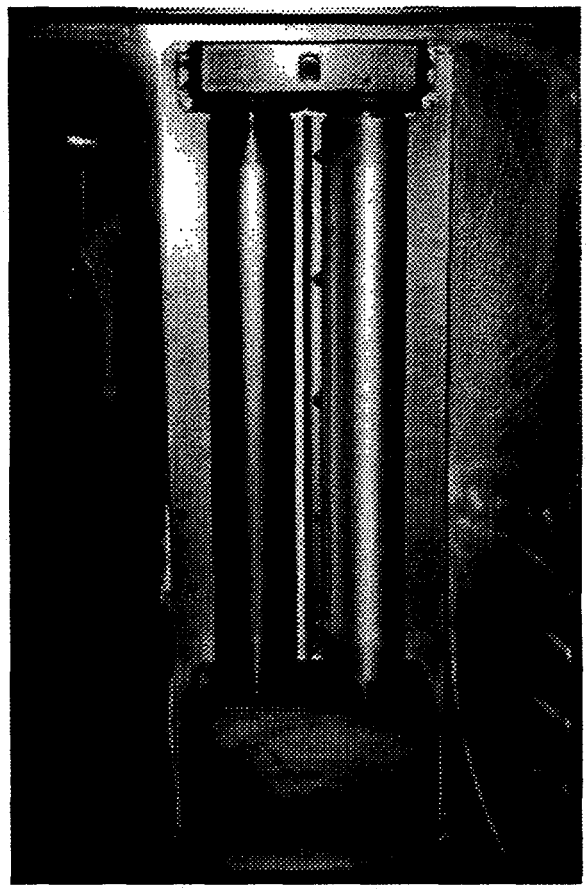

Figure 3.1.3-1 Photograph of AIRCO Modular 940 Dual Rotating Cylindrical Magnetron

12-1/2 Ton chiller circulates 70°C glycol solution through the cathodes and through channels on the chamber to maintain temperature.

Constant substrate speed is maintained by a high-speed stepper motor with gear reduction. All aspects of the sputtering operation, including cathode power and substrate speed/direction, are controlled by an IBM PS/2 microcomputer.

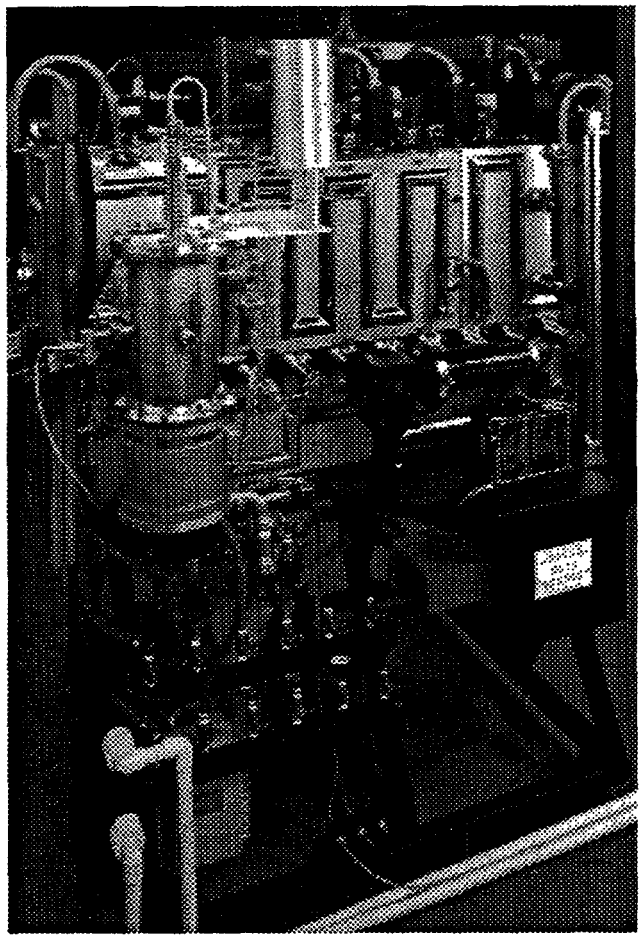

Figure 3.1.3-2 Photograph of Martin Marietta's Rotating Cylindrical Magnetron Sputtering System

3.2 ELECTRODEPOSITION

Electrodeposition is another thin-film deposition technique with promise of large-area, large volume production. Some work has been done on electrodeposition of thin films for PV [14,15]. In principal, the codeposition of two metals is the same as the deposition of a single metal, whereby the passage of a high current density in a bath of the mixed metallic salts will result in a deposit of the two metals (Fig. 3.2-1). Unfortunately, deposits obtained under high current density are porous, nonadherent, and in most cases compositionally inhomogeneous. To codeposit two metals effectively, conditions must be optimized for depositing the less-noble metal without employing an excessive current density.

In the case of CdTe electrodeposition, tellurium (Te) is the more noble component with a standard rest potential of 0.551 V (all electrochemical potentials discussed in this proposal are referenced to a standard hydrogen electrode, or SHE) and cadmium is the less noble component with a rest potential of (–) 0.403 V. Both cadmium and tellurium will deposit with an applied potential less than (–) 0.403 V. However, the free energy gain associated with CdTe compound formation causes a shift in the cadmium potential from (–) 0.403 V at the CdTe/Cd phase boundary to 0.143 V at the CdTe/Te phase boundary. Without this

shift in potential, Cd and Te could not be easily codeposited from a simple salt bath. Therefore, the potential of the solution/film interface has to be maintained between (–) 0.403 V to 0.143 V (SHE) to deposit stoichiometric and near-stoichiometric CdTe.

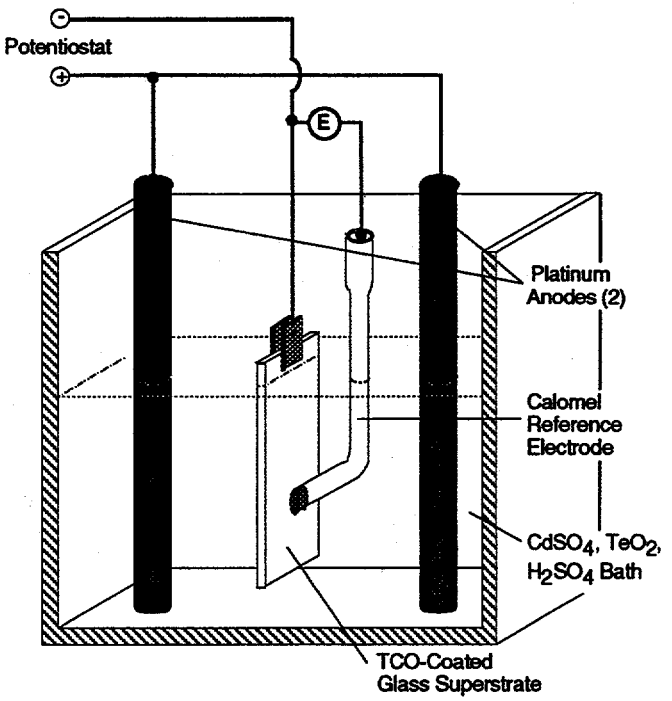

Figure 3.2-1 Schematic of the Electrodeposition Process

CdTe was electrodeposited onto CdS/ITO/glass substrates using both constant potential and constant current control from a PAR 273 Potentiostat/Galvanostat. Deposits of CdTe produced using constant current and constant voltage from a purified 0.5 M $CdSO_4$ solution saturated with TeO_2 at 85°C and pH 2.2 are characterized in Figure 3.2-2. Current increases rapidly for applied voltages below approximately (–) 0.69 V (vs. SCE) due to the sole deposition of pure Cd. Above approximately (–) 0.2 V, the current decreases as the deposit becomes Te rich and CdTe is no longer deposited.

In constant current/potential CdTe electrodeposition, the deposition rate and quality is limited by diffusion of tellurium to the cathode surface (i.e., the concentration of $HTeO_2^+$ at the surface drops to zero). Assuming cadmium is present in sufficient concentration and that the chemical reaction of CdTe is not rate limiting, then the limiting current for CdTe deposition is controlled by the diffusion of tellurium to the surface.

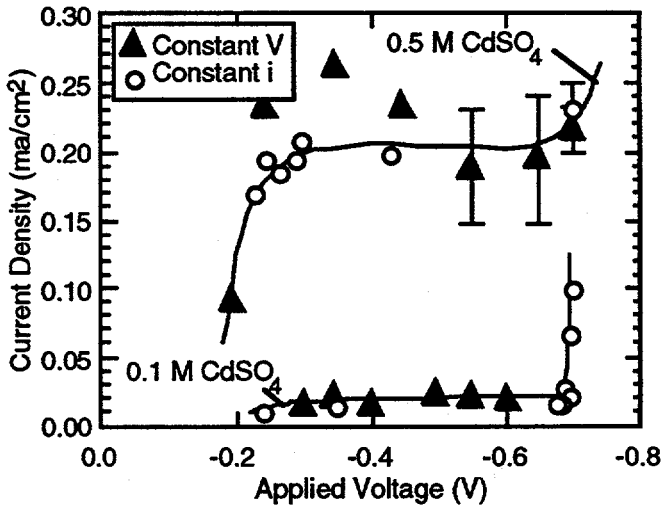

Figure 3.2-2 Current Density versus Applied Cathode Voltage for Both Constant Current and Constant Potentials

3.3 CHEMICAL IMMERSION DEPOSITION OF CdS

Cadmium sulfide (CdS) is used in both the CIS and CdTe cell configuration as the n-type window layer. Thin films of CdS are commonly prepared by vacuum evaporation, sputtering, and spray pyrolysis although another inexpensive method for preparing thin films of CdS is by a chemical solution growth technique. In this method, CdS can be prepared by decomposition of thiourea (or thioacetamide) in an alkaline solution of cadmium salts where the salt can be $CdSO_4$, $Cd(NO_3)_2$, or $CdCl_2$. Substrates are immersed in a pH-adjusted salt solution at temperatures less than 90°C, and upon the addition of thiourea, CdS indiscriminately deposits on properly activated surfaces. Under Martin Marietta Internal Research and Development (IR&D) D-17R, techniques for depositing thin films of CdS were developed. Distribution/stability diagrams were also prepared for $CdCl_2$ in NH_4Cl and $CdCl_2$ in NH_4OH in order to characterize and optimize the mechanism(s) for film growth.

4.0 CIS FILMS AND DEVICES

Films and devices for CIS devices were manufactured using the Martin Marietta C-Mag sputtering facility for the Mo back contact, as well as the Cu and In films associated with the CIS absorber layer. Film thickness uniformity was studied by optical density measurements. In addition, two types of selenization were studied, namely the two-stage ISET H_2Se selenization and the Se-vapor selenization technique developed at NREL. Finally, CdS was solution grown and ZnO transparent conductive oxide was deposited by MOCVD. Details of these techniques are given below.

4.1 THIN-FILM DEPOSITION/CHARACTERIZATION

Because the substrate moves with respect to the cathode, conventional deposition rates have little meaning. Instead, a dynamic deposition rate (DDR) is used to supplant static deposition rates. The DDR in $Åmm^2/J$ is defined in the following manner [Refs 2,3]:

$$DDR = \frac{d \bullet C \bullet S}{P \bullet n} \tag{4.1}$$

where
- d ≡ Thickness of the film (Å)
- C ≡ Racetrack length (mm)
- S ≡ Palate speed (mm/s)
- P ≡ Applied cathode power (W), and
- n ≡ Number of passes.

For the 50.8 cm (20 in.) Modular 940 Dual C-Mag used in the Martin Marietta system, C = 940 mm. As is the case with static deposition rates, DDR values vary with material and other processing parameters such as operating pressure.

4.1.1 Film Uniformity of the C-Mag Facility

Film uniformity with the C-Mag sputtering system over a 30.5 cm x 30.5 cm (12 in. x 12 in.) was studied by depositing 400 Å of copper which corresponded to an optical density of 1.0. Variations of the optical density over the surface is shown in Figure 4.1.1-1. Maximum variation in the optical density was 3.6% which was due to nonuniformity of substrate palate speed. Subsequent tests conducted at Martin Marietta under another program

identified palate weight as a key issue with substrate speed variations and a titanium palate is being fabricated to eliminate this issue.

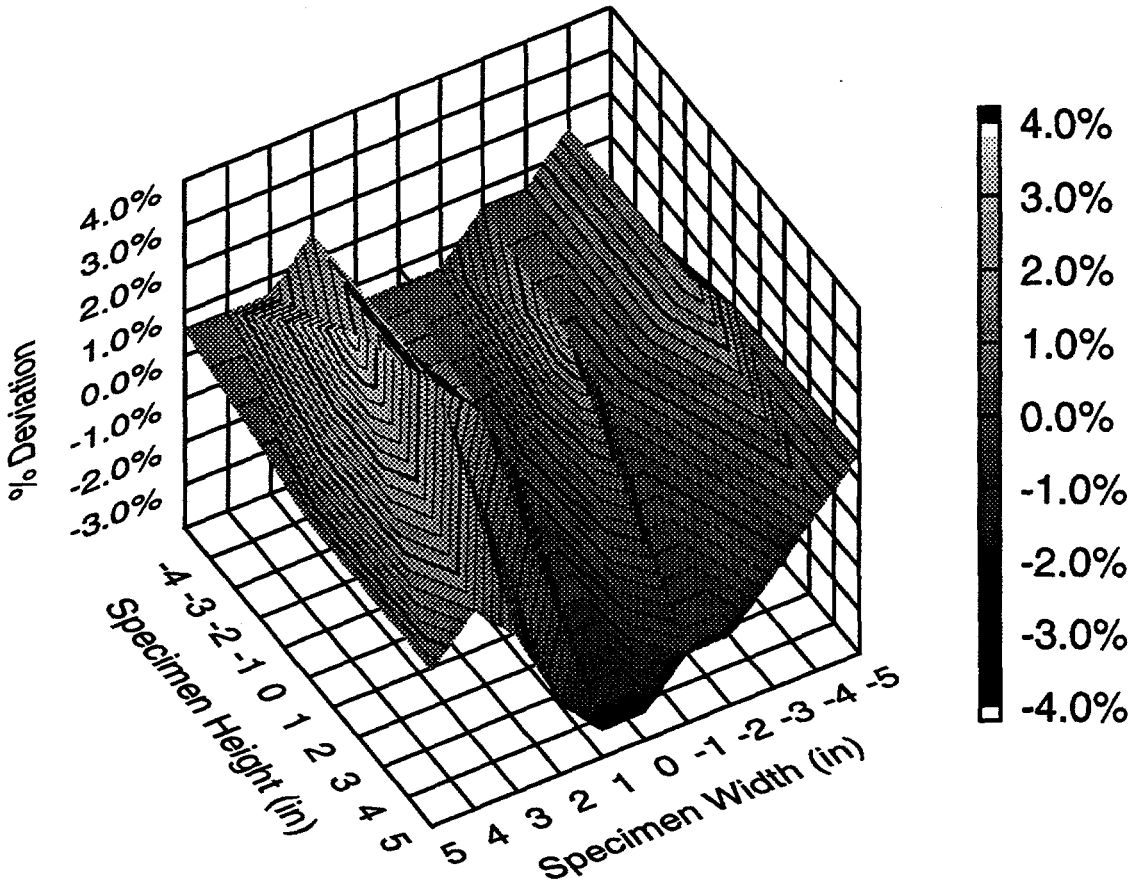

Figure 4.1.1-1 Optical Uniformity of a 400Å Copper Film Sputtered by the Martin Marietta C-Mag Sputtering System.

C-Mag sputtering techniques developed under Martin Marietta IR&D D-17R, Photovoltaic Technologies, including substrate preparation, were applied to the Mo, Cu, and In films for the fabrication of CIS devices. Each is described below.

4.1.2 Substrate Preparation

After cut to the desired size, 2.4 mm (0.093 in.) thick soda lime glass substrates were hand-washed in mild soap in deionized water and dried with lint-free cloths. Substrates were then wiped with lens tissue soaked with isopropal alcohol (IPA). Once cleaned, substrates were mounted onto the substrate palate via clamps and subjected to a drag wipe prior to deposition.

After substrates were mounted to the palate, the C-Mag coating chamber was closed and evacuated to at least 1 x 10^{-6} Torr by a 1000 liter turbopump/Meissner trap combination. Substrates were then preheated to a minimum of 120°C for improved adhesion.

4.1.3 C-Mag Target Fabrication

For preliminary tests conducted by Martin Marietta on an ILS1600 in-line system at AIRCO's facility in Concorde, CA, indium targets were available in-house; however, no Mo and Cu targets were available. Stainless-steel backing tubes for the ILS1600 C-Mag were coated with Mo and Cu by plasma spray techniques at Martin Marietta Laboratories in Baltimore, MD to a thickness of 4000Å, which was deemed sufficient for these early tests.

Several types of C-Mag targets were studied to reduce material costs. In the case of materials whose structural integrity would be insufficient to withstand the operational parameters of the C-Mag, such as indium and selenium, targets were cast around a stainless steel backing tube which contained the mounting threads, seal mating surfaces, and the virtual leak bleed slots of a target (Fig. 4.1.3-1). In each case, target material purity was a minimum of 99.99%. Porosity of these cast targets were an issue; fabrication parameters were altered to obtain a high-density target. Despite this lower-cost option, targets of In and Se cost in excess of $4,000 each.

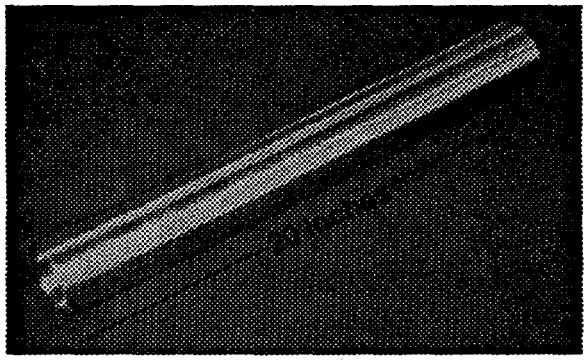

Figure 4.1.3-1 Photograph of Stainless Steel Backing Tube Used in C-Mag Targets.

Targets of 99.95% molybdenum and 99.99% copper were cast into a solid billet and machined to tolerances cited by AIRCO for their targets. Other configurations for targets, including electrodeposited materials and mechanically-bonded foils, were not used to eliminate potential contamination and delamination issues.

4.1.4 C-Mag Sputtered Molybdenum Films

Initial Mo films were deposited on the ILS1600 system. Substrates were loaded into the process chamber and the surface was cleaned by glow discharge. Mo films from the ILS

system were deposited at room temperature in multiple passes at 2 kW DC cathode power with an operating pressure of 1-2 millitorr. Deposition rates were determined from witness slides marked with parallel lines by a permanent markers. Once the films were deposited, the slides were ultrasonically cleaned in IPA which removed the film above the ink, as well as the ink. A DekTak IIA profilometer was used to measure thicknesses over an average of several Mo lines. Rate slides, which were not subjected to the rigorous ultrasonic cleaning as were the actual substrates, demonstrated high compressive stresses in the Mo films which was attributed to the low operating pressure. Tape tests of Mo films on the actual substrates demonstrated little adhesion between the Mo/glass interface. Furthermore, films exhibited high resistivity (110 mΩ — 140 mΩ) which was probably attributed to the plasma sprayed targets used on the ILS system. Using a cathode power of 2 kW, a DDR of 2,365 Åmm^2/J was obtained.

When the Martin Marietta C-Mag system was on-line, experience obtained from the ILS system was used to establish baseline parameters. To enhance the life of the target, cathode power was ramped from ignition (typically occurring at 20W or less) up to 100% of the predetermined 2 kW sputtering over two or more minutes. Although no glow discharge was available on the C-Mag system, it was believed that proper preheating of the substrate, as well as a higher operating pressure, would eliminate the adhesion problems observed earlier. Consequently, prepared substrates were heated to a minimum of 120°C, and to ensure a clean target surface, the Mo cathode was ignited for presputtering while the target was covered by the air-actuated cathode shutters (Fig. 4.1.4-1). Between the shutters, a gas manifold was installed to ensure uniform gas distribution throughout the entire length of the target. Operating pressure for the Mo deposition was set at 7.5 millitorr by adjusting the throttle valve on the turbopump to control vacuum conductance.

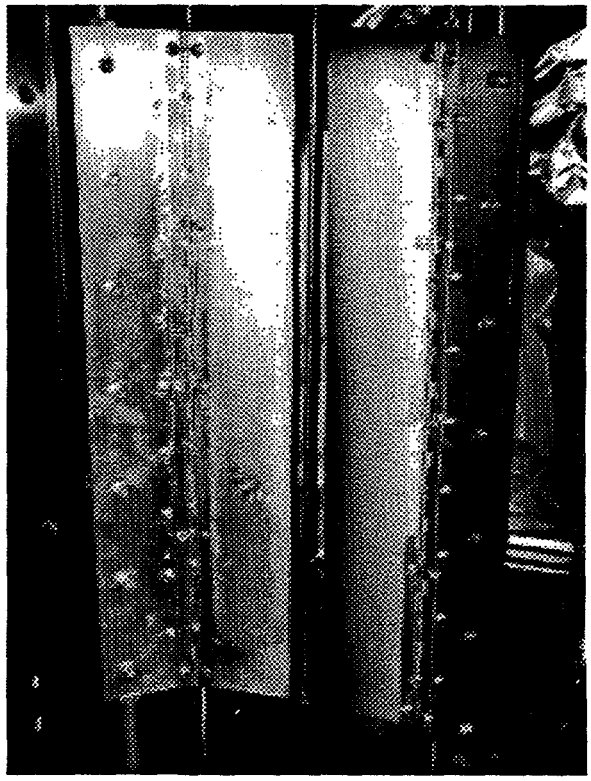

Figure 4.1.4-1 Photograph of Stainless Steel Shutters Used in Presputtering of Targets.

Results from the Martin Marietta C-Mag sputtering systems were significantly better than that of the earlier ILS1600 tests. First, the higher operating pressure of 7.5 millitorr and substrate preheating resulted in significantly higher film adhesion. Tape tests using Kapton tape burnished onto the film resulted in the removal of adhesive from the tape. No pinholes on the surface of the film were observed from transmission optical microscope studies. Also, the higher purity of the cast Mo target (99.95%) resulted in a much lower resistivity film (30 mΩ — 40 mΩ). At these higher pressures, the calculated DDR for Mo had dropped to 1,716 Åmm^2/J at 10.08 cm/m substrate speed and an actual DC power of 1,980 W. With these parameters, four (4) passes are required to obtain the desired 1 μm film.

4.1.5 C-Mag Sputtered CIS from Selenization of Cu and In

Early experiments with C-Mag facilities at AIRCO in Concorde, CA also involved Cu and In films deposited on the Mo-coated 2.4 mm (0.093 in.) thick soda-lime glass. As was the case for the Mo films, an operating pressure between 1 and 2 millitorr was used during deposition. A DDR of 4411 Åmm^2/J was obtained for the plasma-sprayed Cu target. Because thickness of the In films could not be measured by the DekTek profilometer due to its softness, existing values at AIRCO of 9500 Åmm^2/J were used.

To achieve the 0.95:1 Cu:In ratio goal for the ISET two-stage selenization process, film thicknesses of 2000Å and 4650Å for Cu and In respectively were deposited onto Mo-coated glass. One issue which was identified during the In deposition was discoloration of the In target. After several runs, the In target displayed a dark surface which significantly affected the stability of the plasma. In several cases, the plasma was quenched and required reignition during the deposition run.

These films were selenized by the ISET two-stage process using standard processing parameters identified elsewhere [6]. In all cases, the high stress observed in the ILS-deposited Mo films caused a dramatic delamination of the CIS/Mo stack during selenization (Fig. 4.1.5-1). Consequently, a second series of tests were conducted by depositing Cu and In, using identical processing parameters as before, onto previously prepared Mo-coated glass from ISET which had proven reliable in the two-stage process. Films from these tests were selenized as before, but no delamination was observed. Conductivity of these films was sufficiently high to make subsequent devices short out. Furthermore, contamination by Na and Cl were found (Fig. 4.1.5-2) by AES at the film surface when

compared to similar behavior from a standard planar sputtered CIS film from ISET (Fig. 4.1.5-3). Cu concentration of the C-Mag film was higher than the planar film as expected by the film resistance measurements. Furthermore, the O content of the surface was significantly higher in the C-Mag films which can be attributed to the plasma-sprayed targets used in this investigation. After etching 20 nm through the surface, the composition of this film proved to be nearly identical to the ISET film.

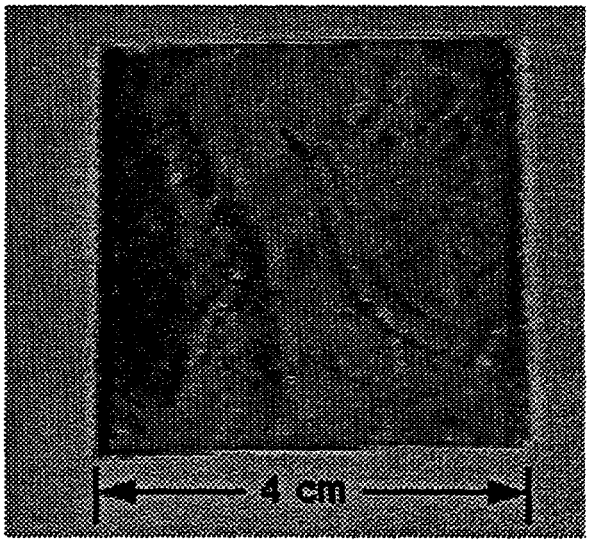

Figure 4.1.5-1 Photograph of Delaminated CIS/Mo Stack Due to High Stress in the Mo Film.

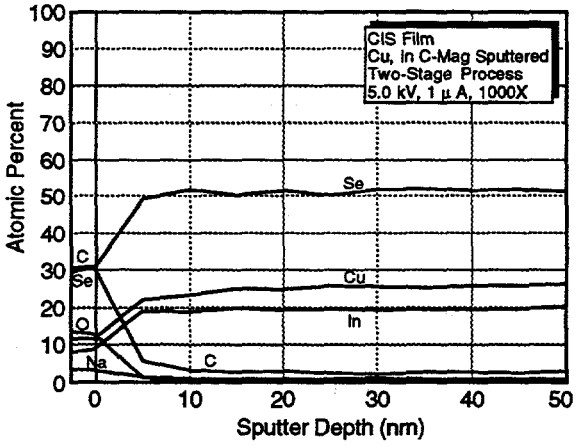

Figure 4.1.5-2 AES Depth Profile of C-Mag CIS Film Indicating Na, Cl, and O Contamination in the Films.

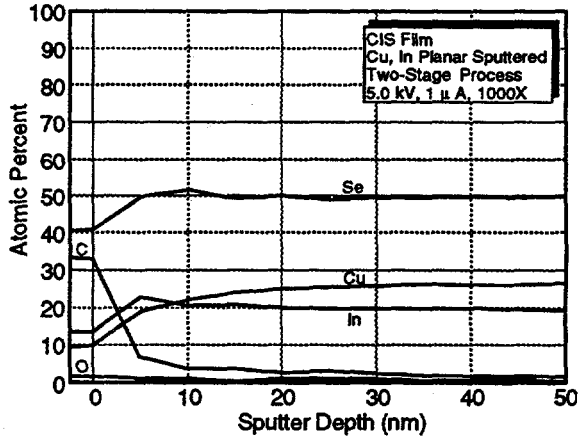

Figure 4.1.5-3 AES Depth Profile of a Reference Planar CIS Film.

Once the Martin Marietta C-Mag facility was available, Cu and In films were deposited onto highly-adhesive Mo-coated glass. Cu films were deposited at 8.2 mT to 8.6 mT operating pressure at different substrate speeds. DDR values for this test are shown in Table 4.1.5-1. DDR values, which should be relatively constant, varied by 20% which indicated that substrate drive may be nonlinear. This speed nonuniformity is the subject of a present investigation under another Martin Marietta program.

Table 4.1.5-1 DDR Values for Copper Films Deposited by the Martin Marietta C-Mag Sputtering System

Pressure mT	d (Å)	S (cm/m)	P (W)	Passes n	DDR (Åmm²/J)
8.60	2,002	70.44	1,970	4	2,804
8.20	486	88.05	1,960	1	3,420

Depositing indium films by the Martin Marietta C-Mag system was far more difficult, however. Original tests conducted at 2 kW appeared to deposit material at a significant rate, but an apparent flaw at the In/backing tube interface caused a momentary separation of the In after several thermal cycles. Subsequently, a portion of bottom part of the target melted as shown in Figure 4.1.5-4. Consultation with the vendor indicated that the interface bonding during fabrication of the target is still an issue and agreed to manufacture another target. Meanwhile, the integrity of the target interface was sufficient to allow operation of the In sputtering at powers not exceeding 1 kW. Based on these limitations, DDR values as high as 8,416 were obtained (Table 4.1.5-2).

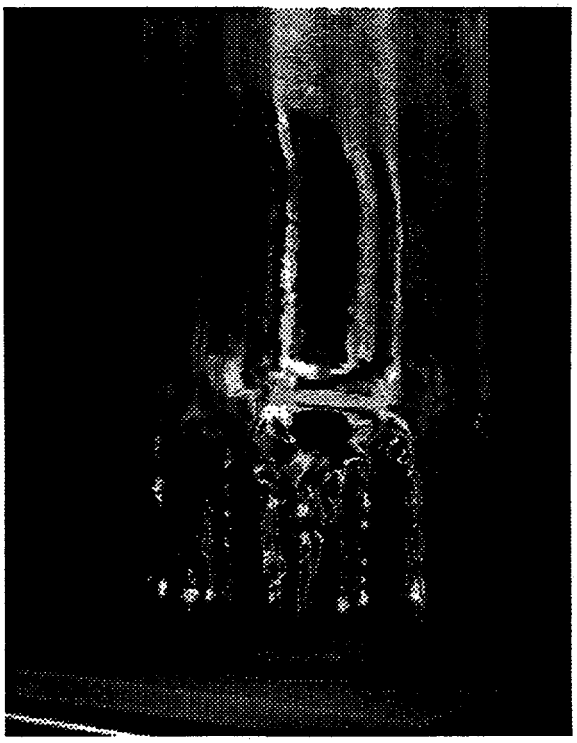

Figure 4.1.5-4 Photograph of the C-Mag Indium Target Indicating Significant Melting Near the Racetrack Turnaround Area.

Table 4.1.5-2 DDR Values for Indium Films Deposited by the Martin Marietta C-Mag Sputtering System

Pressure mT	d (Å)	S (cm/m)	P (W)	Passes n	DDR (Åmm²/J)
7.50	2,304	10.0	480	1	7,520
7.50	5,318	10.0	990	1	8,416

Once confidence in the C-Mag was achieved, glass/Mo/Cu/In stacks were prepared with target Cu:In ratios of 0.85, 0.90, and 0.95. Initial processing parameters were based on the obtained DDRs and the assumption that films were nearly fully dense.

However, all films obtained by ISET two-stage processing exhibited very high electrical conductivity and localized nonuniformites. In some cases, blistering of the CIS surface was also observed (Fig. 4.1.5-5). Subsequent composition measurements of these films indicated that films were significantly copper -rich (Table 4.1.5-3).

Indium film density measurements demonstrated that In films were only 62%—65% fully dense which was partially due to the sputtering process and also due to the 74% full density of the target itself (Table 4.1.5-4). As a result, the subsequent In target will have both an improved interface integrity as well as higher density. All subsequent Cu/In stacks for selenization took account of the low In target and film density.

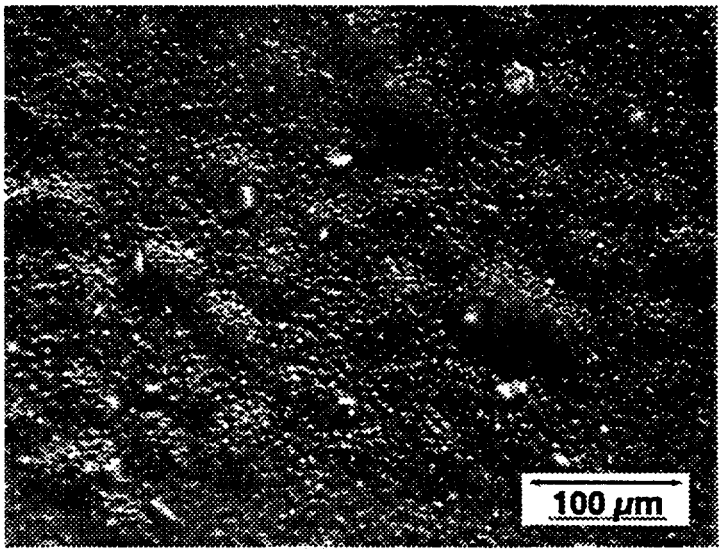

Figure 4.1.5-5 Darkfield View of Selenized Cu/In Stacks Showing Blistering of the CIS Surface.

Table 4.1.5-3 Composition Data Based on Weight Percent Measurements

Run #1	Power (W)	Speed (cm/min)	wt. %	% of Coating	Atomic Weight	Actual Moles	Desired Ratio	Desired Moles	Variation (%)
Cu	2000	18.00	0.063	14.93%	63.546	0.00235	1.00	0.00235	100.00%
In	1000	2.38	0.069	16.35%	114.820	0.00142	1.05	0.00247	173.66%
Mo	2000	10.08	0.290	68.72%	95.940	0.00716	—	—	—

Run #2	Power (W)	Speed (cm/min)	wt. %	% of Coating	Atomic Weight	Actual Moles	Desired Ratio	Desired Moles	Variation (%)
Cu	2000	18.00	0.001	14.29%	63.546	0.00225	1.00	0.00225	100.00%
In	500	4.70	0.001	14.29%	114.820	0.00124	1.05	0.00237	190.20%
Mo	2000	10.08	0.005	71.43%	95.940	0.00745	—	—	—

Run #3	Power (W)	Speed (cm/min)	wt. %	% of Coating	Atomic Weight	Actual Moles	Desired Ratio	Desired Moles	Variation (%)
Cu	2000	18.00	0.036	15.86%	63.546	0.00250	1.00	0.00250	100.00%
In	500	2.35	0.061	26.87%	114.820	0.00234	1.05	0.00263	112.25%
Mo	2000	10.08	0.130	57.27%	95.940	0.00597	—	—	—

Table 4.1.5-4 Verification of the Low Density of the Indium Films

Glass & Indium Mass (mg)	Glass Mass Alone (mg)	Indium Mass (mg)	Film Area (cm^2)	Film Thickness (μ m)	Indium Volume (cm^3)	Film Density (g/cm^3)	Indium Density (g/cm^3)	Indium Target Density (g/cm^3)	Film Density Compared to Full Density (%)	Film Density Compared to Target Density (%)
190.05	178.71	11.35	4.83	5.0	$2.41x10^{-3}$	4.70	7.31	74.0	64.3	86.9
188.44	178.54	9.90	4.32	5.0	$2.16x10^{-3}$	4.58	7.31	74.0	62.7	84.7
189.88	178.29	11.58	4.88	5.0	$2.44x10^{-3}$	4.74	7.31	74.0	64.9	87.7

4.1.5.1 Two-Stage H_2Se Selenization — Once compositional variations due to In target/film density were identified and addressed, glass/Mo/Cu/In stacks were selenized at ISET by the two-stage process which involved a 400°C, 30 minute heat treatment in a H_2Se atmosphere. Once again, films appear to be Cu-rich, although the films themselves were measured to be In rich. A variation of the stack geometry involved glass/Mo/In/CuIn where the CuIn cosputtered stack was used to guard against In loss which would result in a Cu-rich film. These films exhibited good resistivity and were subsequently identified for further fabrication of devices.

4.1.5.2 Se-Vapor Selenization — In order to assess the effects of H_2Se upon the interfacial integrity of the CIS devices, some films were selenized using the Se-vapor selenization techniques developed by NREL [Ref 5]. A variety of configurations were tested, including glass/Mo/Cu/In, glass/Mo/In/Cu, glass/Mo/In/Cu/In/Cu, and glass/Mo/In/CuIn (Table 4.1.5.2-1). As was the case in the H_2Se case, In loss was evident. Consequently, the best results were obtained when glass/Mo/Cu/In stacks were annealed in an Ar atmosphere at 130°C for 30 minutes to promote alloying of the Cu and In. Cu/In sandwiches tried later in the evaluation appeared to be extremely copper lean, making it extremely difficult to manufacture devices with sufficient adhesion for analysis. However, films with adequate adhesion and reasonable film conductivity were also used in device fabrication.

Poor adhesion at the Mo-CIS interface and discoloration of the Mo films exposed by removal of CIS layer was quantified by X-ray diffraction on specimen C-147. As shown in Figure 4.1.5.2-1, selenization of the underlying Mo films was observed by the appearance of Mo_3Se_4 and $Mo_{15}Se_{19}$ phases. In addition, a $Mo_4Se_{5.33}$ high-temperature phase was observed as well, but it is not yet known if this phase is present at the surface or in the bulk of the film. Glancing incidence diffractometry will be used in subsequent investigations to identify the nature of this film, as well as stress analysis of the Mo films [Ref 6].

Table 4.1.5.2-1 Results from Se-Vapor Selenization Experiments

Run #	Stack Configuration	Target Cu/In Ratio	Pre-selenization Conditions	NREL EPMA composition @ 10 kV (20 kV)	Comments
C121	Mo/Cu/In	0.85	None	25.26/25.66/49.08 (25.54/24.83/49.64)	Adhesion OK, Mo surface strongly discolored
C122	Mo/Cu/In	0.9	100°C anneal (vacuum)	27.78/23.94/48.29 (27.49/24.48/49.03)	Good adhesion
C124	Mo/Cu/In	0.95	100°C anneal (vacuum), 200°C anneal (vacuum)	25.69/25.22/49.09 (26.38/24.15/49.46)	Poor adhesion, Mo surface strongly discolored
C127	Mo/Cu/In	0.85	130°C anneal (argon), 200°C anneal (vacuum)	23.03/26.91/50.05 (23.57/25.8/50.63)	Good adhesion, 6% (active) device fabricated
C128	Mo/In/Cu	0.95	100°C anneal (vacuum)	31.42/21.95/46.63 (31.64/20.67/47.69)	Poor adhesion, Mo surface strong yellow color
C129	Mo/In/Cu	0.95	100°C anneal (vacuum), 200°C anneal (vacuum)	31.08/22.17/46.75 (30.74/21.33/47.93)	Adhesion OK, Mo surface faint yellow color
C134	Mo/In/CuIn	0.95	100°C anneal (vacuum), 200°C anneal (vacuum)	18.08/30.34/51.58 (19.37/28.75/51.88)	Adhesion OK, Mo surface faint yellow color, highly resistive film
C136	Mo/In/CuIn	0.95	100°C anneal (vacuum), 200°C anneal (vacuum)	18.58/30.26/51.17 (18.51/29.00/52.50)	Adhesion OK, Mo surface faint yellow color, highly resistive film
C137	Mo/In/Cu/In	0.85	100°C anneal (vacuum)	29.03/23.33/47.64 (29.21/22.37/48.41)	Poor adhesion
C138	Mo/In/Cu/In	0.95	100°C anneal (vacuum), 200°C anneal (vacuum)	not available	Very poor adhesion

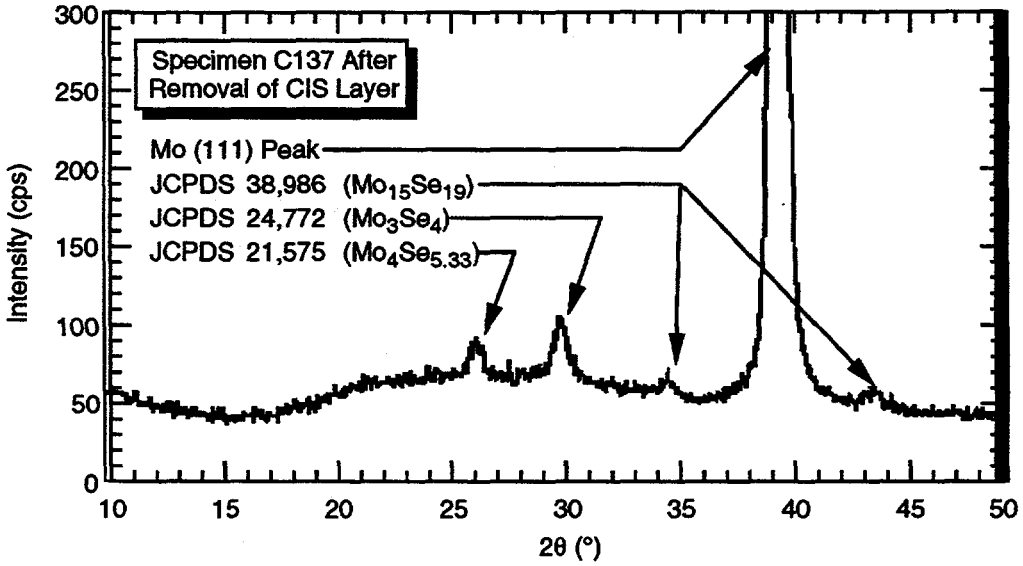

Figure 4.1.5.2-1 X-Ray Analysis of Mo Film Beneath Poorly-Adhering CIS Layer on Specimen C137 Indicating Selenization of Mo Back Contact.

4.1.5.3 Compositional Variation Issues — In addition to the target density issue, it was noted that Cu/In stacks varied in composition from run to run, as well as from position on the palate. Furthermore, the In target was observed to darken in a similar fashion to the In target at AIRCO. Samples from the target surface were analyzed by both SEM and AES to determine the variation in deposition rate. As shown in Figure 4.1.5.3-1, alternating dark and light bands appear on the surface of the target. A closer look (Fig. 4.1.5.3-2) indicates the preferential erosion of the In target into needle-like growth. An analysis of the tip of one of these areas (Fig. 4.1.5.3-3) indicates the presence of Cu from low-angle sputtering from the other targets. This poisoning of the In target has been eliminated by modifications of the C-Mag cathode structure.

4.1.6 Solution-Grown CdS

In this heterojunction structure, CdS served as the n-type window layer. A solution-growth, or chemical dip method, was selected to deposit the CdS onto the glass/Mo/CIS film after selenization. This technique utilizes a metastable solution containing a Cd source such as cadmium-acetate (Cd-Ac), a sulfur source such as thiourea, and a complexing agent which serves as the rate controlling agent. A solution of all of these ingredients are mixed with NH_4OH to maintain a pH of about 10. Deposition takes place at solution temperatures above 50°C.

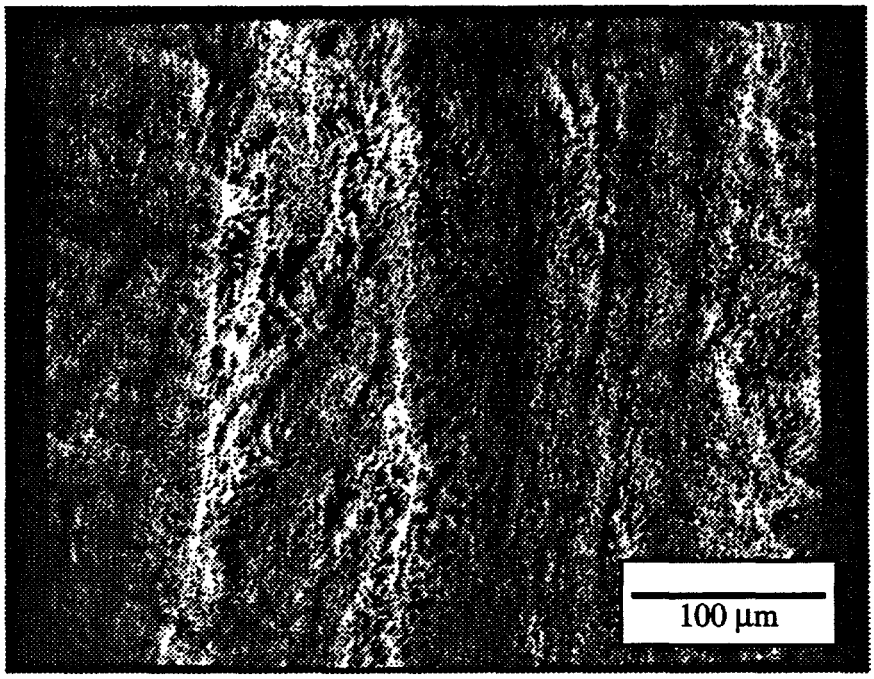

Figure 4.1.5.3-1 SEM Micrograph of In Target Surface Showing Dark and LIght Bands.

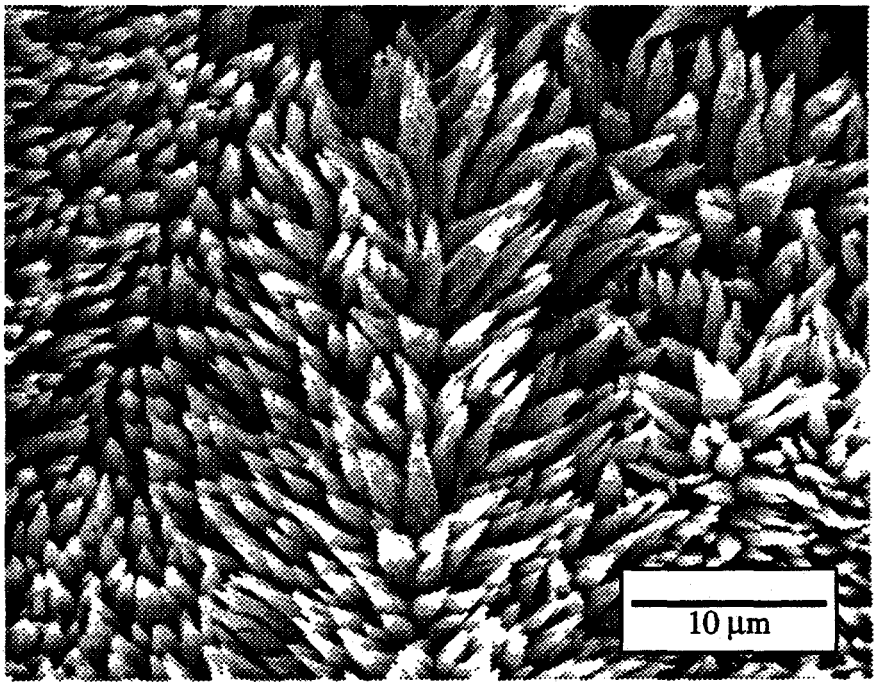

Figure 4.1.5.3-2 SEM Micrograph of In Target Surface Showing Preferential Erosion.

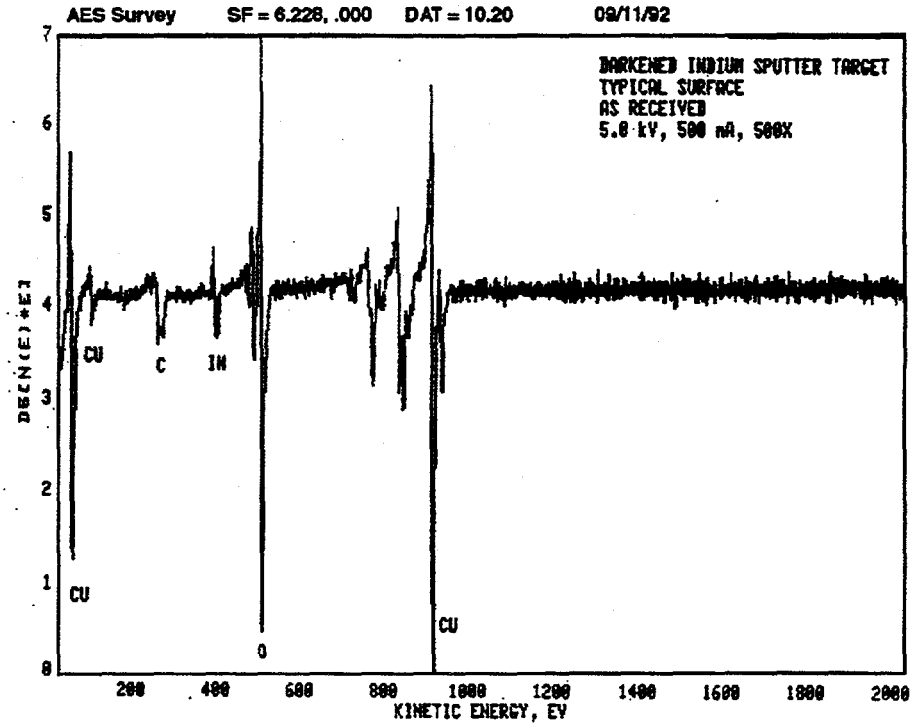

Figure 4.1.5.3-3 AES of One of the Tips Shown in Figure 4.1.5.3-2 Confirming the Presence of Copper.

4.1.7 Transparent Conductive Oxide

The transparent conductive oxide for the CIS devices was ZnO which was formed by MOCVD techniques to a nominal thickness of 1 μm to 1.8 μm by ISET [7]. Resistivity of the films typically were in the 2 x 10^{-3} Ω-cm range. Substrate temperatures were maintained at 170°C for a deposition rate of approximately 1500Å/min.

4.2 DEVICE FABRICATION

Films from both H_2Se and Se-vapor selenization with sufficient adhesion and low electrical conductivity (Cu-lean) were used in device fabrication. Results from the H_2Se selenized films provided the best response with an efficiency of 8.4% (total area) as measured at NREL (Fig. 4.2-1). These devices displayed a respectable 66.57% fill factor and a 29.18 mA/cm^2 current density. V_{oc} of this device was low at 0.4317V. Other devices on the same substrate were also tested, with the lowest efficiency of the batch at 7.7%, indicating a good uniformity across the substrate.

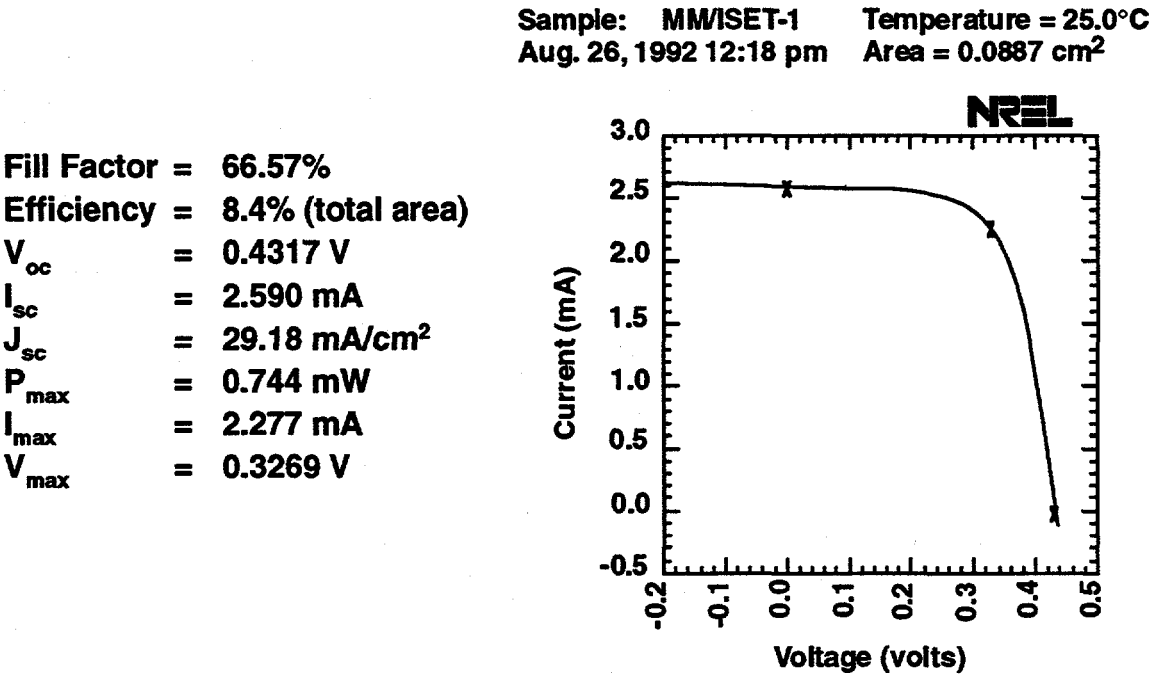

Figure 4.2-1 Results from CIS Devices Manufactured by H_2Se Two-Stage Selenized C-Mag Films.

In addition, other CIS devices were manufactured from Se-vapor selenized films. As shown in Figure 4.2-2, Se-vapor devices posted a respectable 7.45% efficiency with a fill factor of 64.9%. In both the H_2Se and Se-vapor selenization, processing parameters were not optimized for the CIS films. Consequently, the processing parameters are being optimized during the second phase of the contract.

4.3 DEVICE CHARACTERIZATION

Although the devices have just been fabricated, some EBIC and SEI analysis was performed at NREL on the 8.4% efficient devices. Figure 4.3-1 shows an cross-section of the heterojunction by SEI/EBIC. SEI image with EBIC signal superimposed on it, indicating that the junction is displaced approximately 1 μm from the heteroface.

In addition, some pinholes in the CdS film were identified by SEI/EBIC. Figure 4.3-2a and 4.3-2b show the same image by SEI and EBIC respectively, indicating little response from the pinhole region. An enlargement of this region shows near-zero response within the hole at 30 kV.

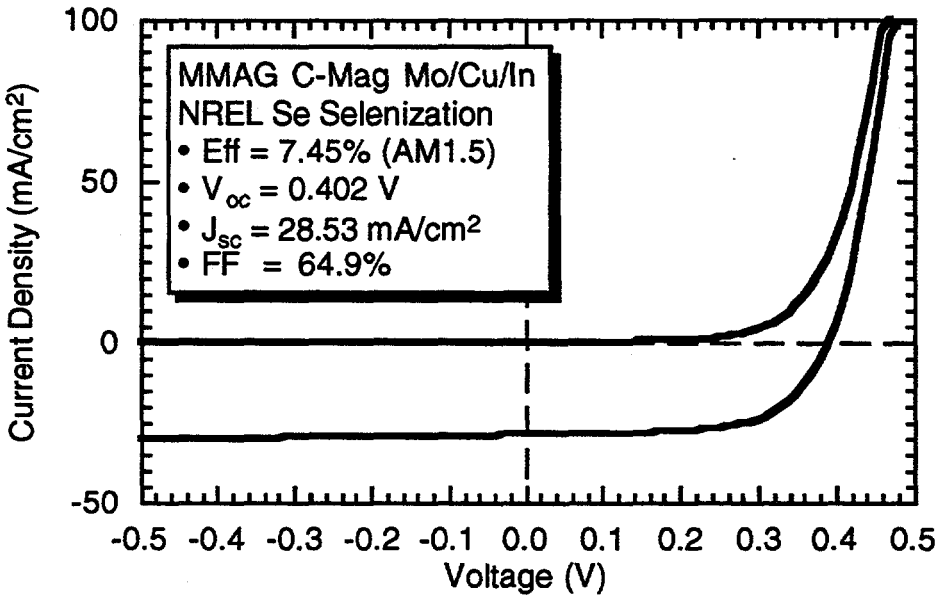

Figure 4.2-2 ***I-V Characteristics of a CIS Device from Se-Vapor Selenized CIS Film.***

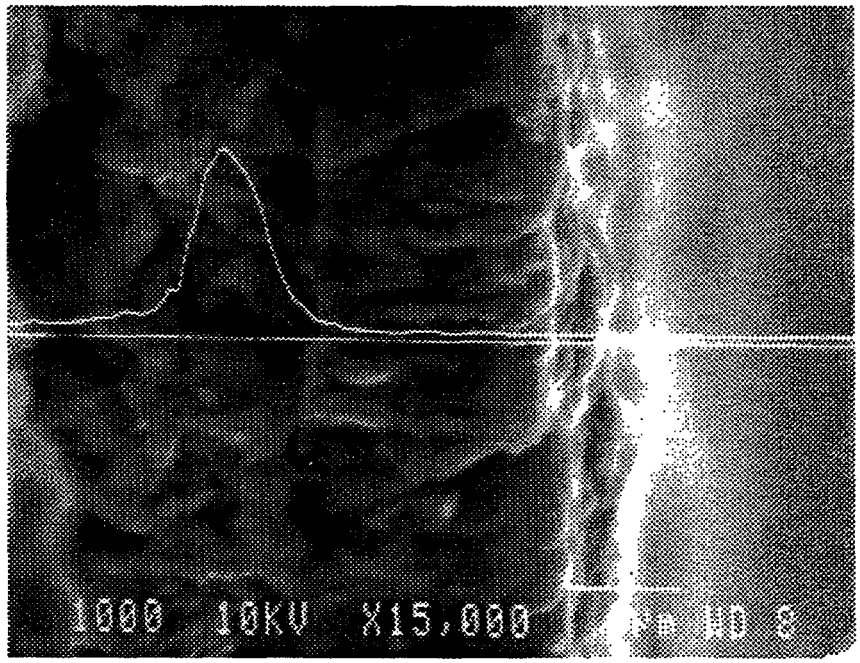

Figure 4.3-1 ***EBIC/SEI Image of Heterojunction of CIS Device Indicating the Displacement of the Junction Approximately 1 μm.***

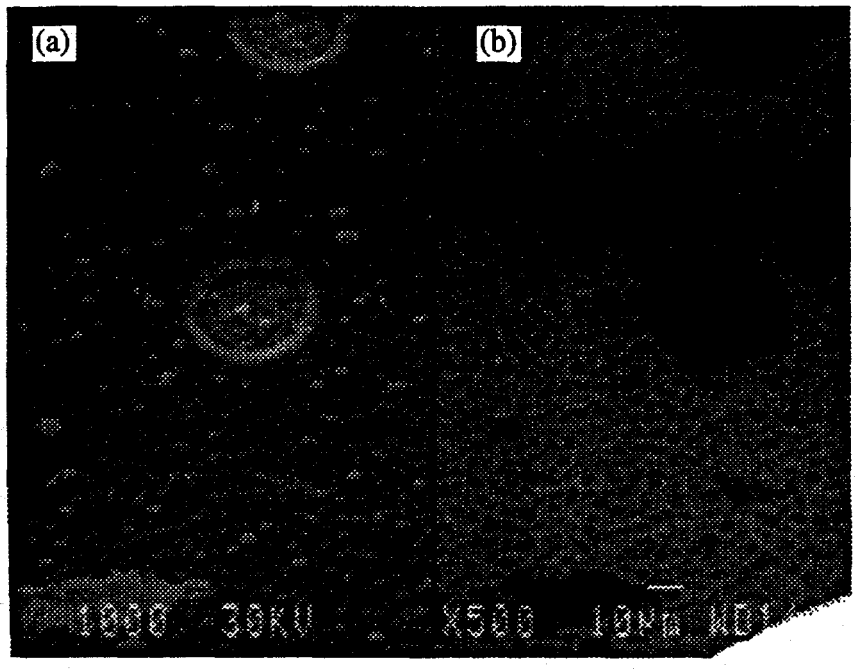

Figure 4.3-2 ***An (a) SEI and (b) EBIC Image of a CdS Pinhole Indicating Little Response from the Area.***

An EBIC closeup of the pinhole noted earlier indicated little or no response within the hole (Fig. 4.3-3). Repeated e-beam scans of the same area results in increased EBIC response, indicating that the beam is acting to move the junction in this area forward (Fig. 4.3-4). These results are being investigated to determine the correlation between the CdS pinhole performance and metallurgical properties of the underlying CIS.

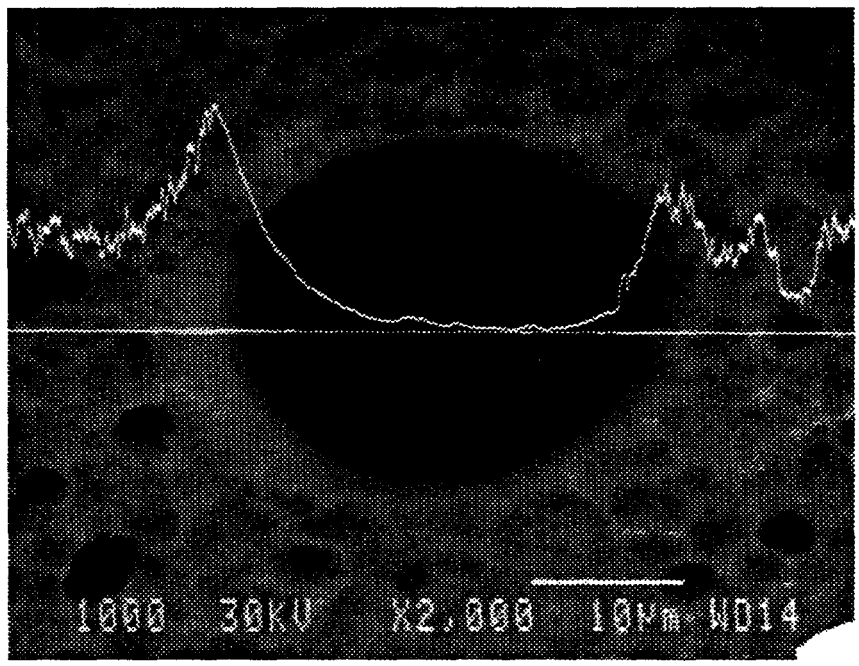

Figure 4.3-3 ***EBIC Closeup of Pinhole Region Indicating No Response Within the Hole.***

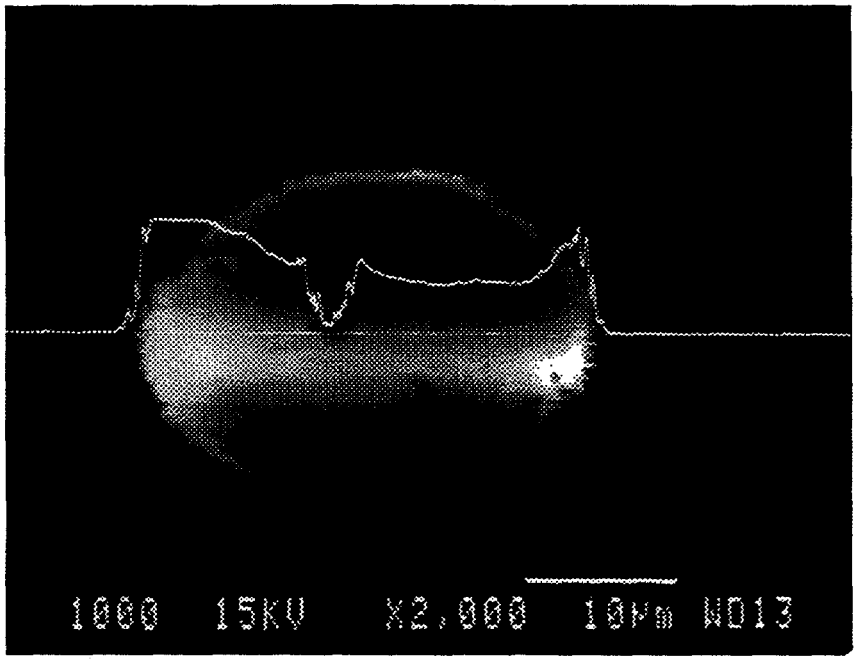

Figure 4.3-4 ***EBIC at 15 kW Indicating Response after Repeated e-Beam Scans.***

5.0 POLYCRYSTALLINE CdTe FILMS AND DEVICES

Progress in the development of CdTe heterojunction solar cells was accomplished in two sequential tasks of work. The first task focused on the optimization of chemical and mechanical properties for each of the individual films in the cell stack; i.e. transparent conductive oxide (front contact), CdS (transparent window), and CdTe (absorber layer). The goal was to produce uniform, adherent, and stoichiometric coatings of CdS and CdTe on ITO-coated glass substrates. As part of the requirements for the contract, 4 cm^2 stacks of CdS and CdTe were deposited onto ITO-coated glass and delivered to NREL on 3/92.

In the second task of work, films from the first task of work were to be incorporated into CdTe heterojunction devices and further optimized, from a device standpoint, to yield > 6 % efficient solar cells. The requirement from this task of work was to produce a 1 cm^2 (active area) CdTe solar cell with an efficiency of at least 6 %.

Since the development of each film and its interaction with the over and underlying film(s) constituted a research task in itself, the results from this development effort will be presented in terms of each of the constitutive elements or films in the cell. For the superstrate configuration, this involved the following stacked sequence:

1) rigid glass substrate 2) transparent conductive oxide, 3) CdS window layer, 4) CdTe absorber layer, and 5) back contact (i.e. back surface field). TCO-coated glass substrates were supplied and therefore results from the first task was divided into just the CdS window layer and CdTe absorber layer development tasks.

5.1 FILM DEVELOPMENT/CHARACTERIZATION

5.1.1 Solution-Grown CdS

Based on preliminary results from work completed under IR&D (D-17R), i.e. development of stability/distribution diagrams which defined CdS precipitation equilibria as a function of cadmium and complexing ion (ammonia) concentration, solution-grown CdS films were deposited onto ITO-coated glass substrates. Films, with uniform thicknesses ranging from 200 to 3800 Å, were deposited onto substrates with areas up to

930 cm^2 (1 ft^2). Coating thicknesses across a 930 cm^2 (1 ft^2) area were measured using surface profilometry and variations in the thickness were less than 5%.

By varying the specific solution chemistry and concentrations in the deposition bath, CdS films could be produced at rates between 500-4000 Å/hr, with specific crystallographic structures and orientations, and with little or no homogeneous precipitation in the bulk solution. Optical transmission, Auger Electron Spectroscopy (AES), and X-ray Diffraction (XRD) were used to evaluate the quality of the CdS films prepared in this manner and the results from these analyses, presented below, confirm that the films are stoichiometric, uniform, planar, and pinhole-free.

Optical transmission was used to evaluate not only the light transmitting characteristics of the CdS, but the quality/integrity of the film. For example, in the presence of pinholes in the coating, the optical transmission at wavelengths below the 520 nm absorption edge increases above the low, flat response of a coherent, uniform film. This behavior is shown in the transmission spectrum presented in Figure 5.1.1-1. A typical spectrum for a uniform, continuous 1600 Å-CdS coating is given by curve (a) where the transmission decreases sharply to less than 10% for wavelengths less than 520 nm (transmission is through a glass/ITO/CdS substrate). The sharp increase in the transmission at 520 nm corresponds to the absorption edge for CdS. As the pinhole density increases and the film thickness remains constant, percent transmission will increase in the 300-520 nm range of the spectrum; this is shown by curve (b) where the observable pinhole density was much greater than the film of curve (a).

In addition to the pinholes, the optical transmission curve was used to qualitatively evaluate the impurity content of the film. Above 520 nm, there is usually an observable maximum in the spectral response of the CdS. Shifts in this maximum to longer wavelengths is indicative of extraneous interface states in the bandgap (formation of lower bandgap window (ref. 1)) or impurities/defects in the coating. Shifts in the maximum were observed although the correlation between peak shifts and device performance is still in progress.

Auger Electron Spectroscopy (AES) was used to evaluate the effect of thermal processing treatments on the surface composition of CdS films. Since oxides and non-stoichiometric cadmium/sulfur concentrations on the surface of the film effect the window interface states as well as the behavior of the p-n junction in the heterojunction device, the

surface and near surface composition of heat treated films were evaluated. AES depth profiles for CdS samples, heat treated at 300°C and 450°C in a H_2/Ar purge gas, are presented in Figure 5.1.1-2. According to these analyses, oxides formed in the top 300 Å of the surface and cadmium was depleted to a depth of 500 Å for both heat treatment temperatures. The extent of cadmium depletion increased with increasing heat treatment temperature. Cadmium/sulfur ratios for the 300°C and 450°C heat treatments were 0.75 and 0.65 respectively.

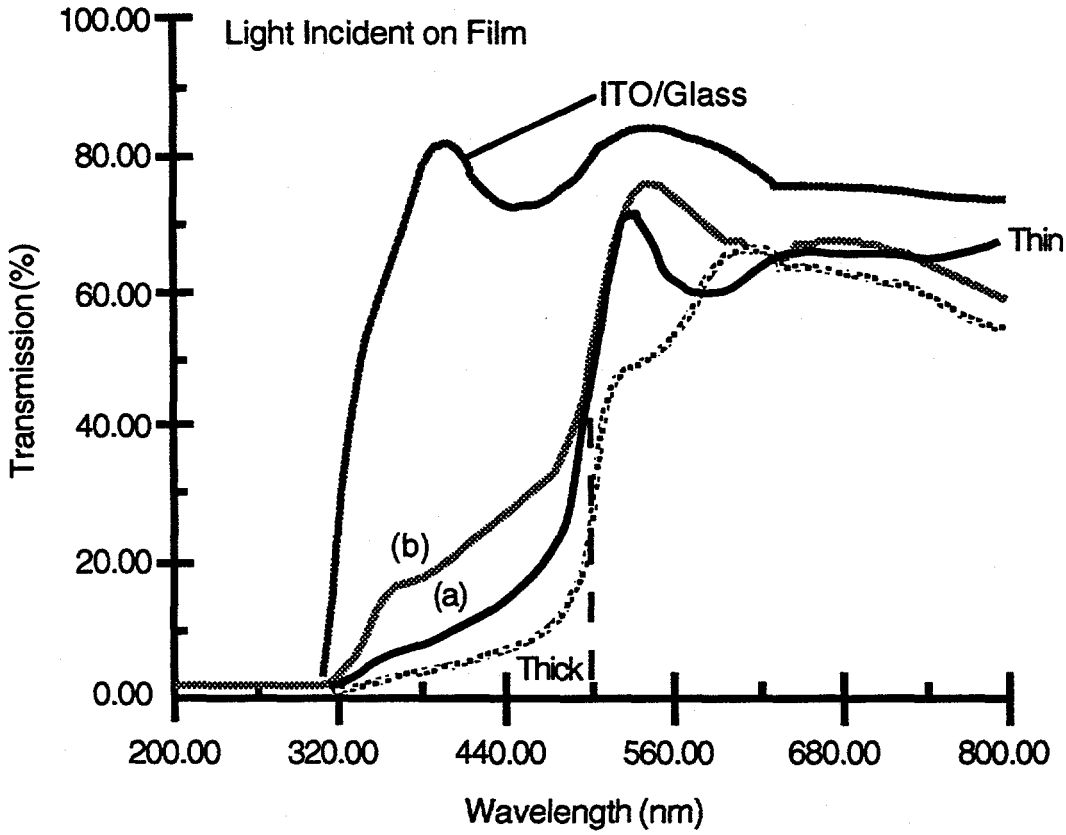

Figure 5.1.1-1 Transmission Spectrum for Solution-Grown, 1600Å Thick CdS Films on Glass/ITO Substrates (Also Shown are Spectrum for an Uncoated Glass/ITO Substrate and 3500Å "Thick" Coating).

As-deposited, solution-grown CdS films were analyzed with X-ray diffraction and the results are shown in Figure 5.1.1-3. These films are hexagonal with measured lattice parameters of a = 4.07 Å – 4.1 Å and c = 6.653 Å – 6.654 Å. In the as-deposited condition, the films are highly oriented with preferred growth directions of (002). When heat treated at 450°C for 30 minutes in H_2/Ar, the structure of the film does not change; the films remain highly oriented. When sandwiched between the TCO and an electrodeposited CdTe film, however, the CdS structure is not thermally stable. Results will be present-

ed in Section 5.2 which shows that CdS becomes more crystalline(peak sharpening) and the lattice expands with the 400°C post processing heat treatment for CdTe.

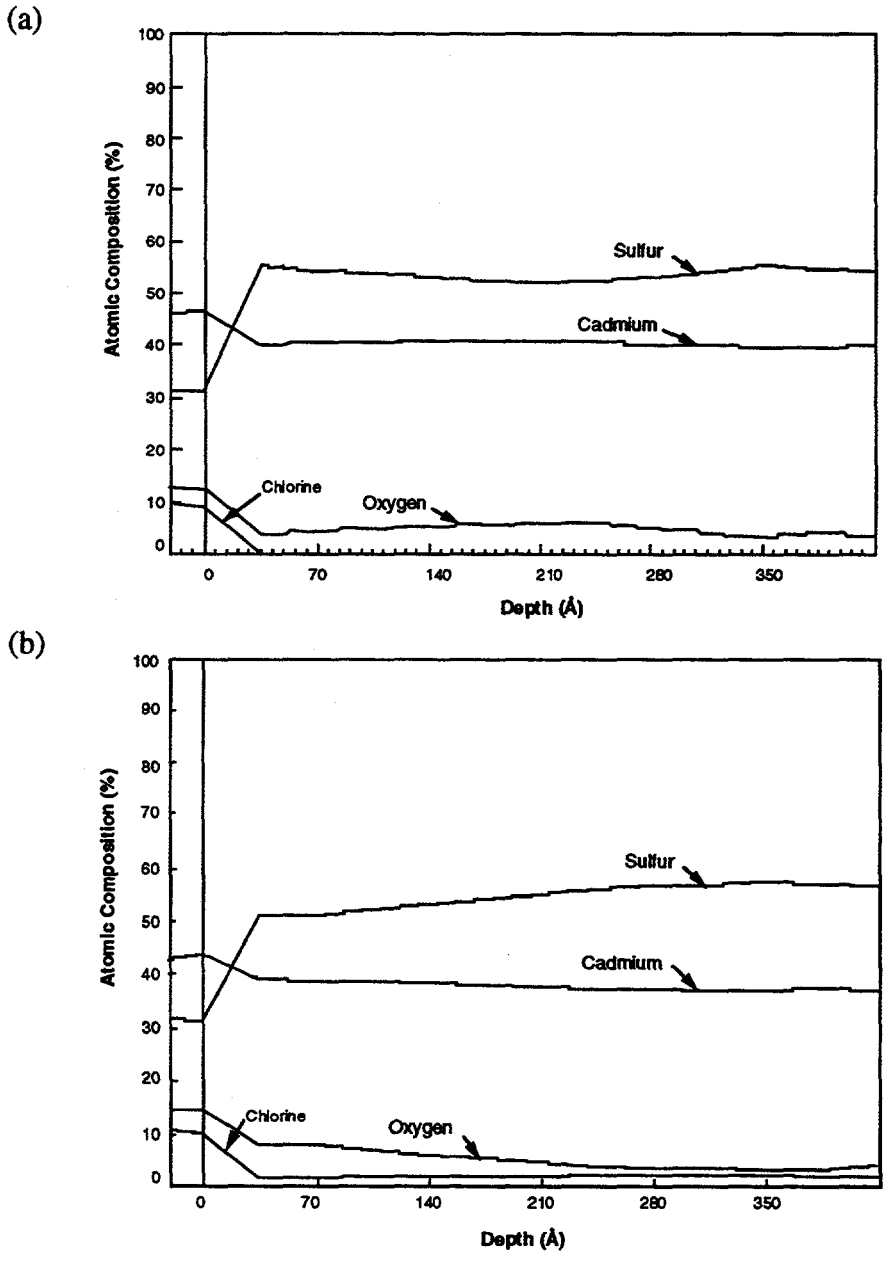

Figure 5.1.1-2 AES Depth Profiles of CdS Films Heat Treated for 15 Minutes in 4% H_2/Ar Atmosphere at 300°C (a) and 450°C (b).

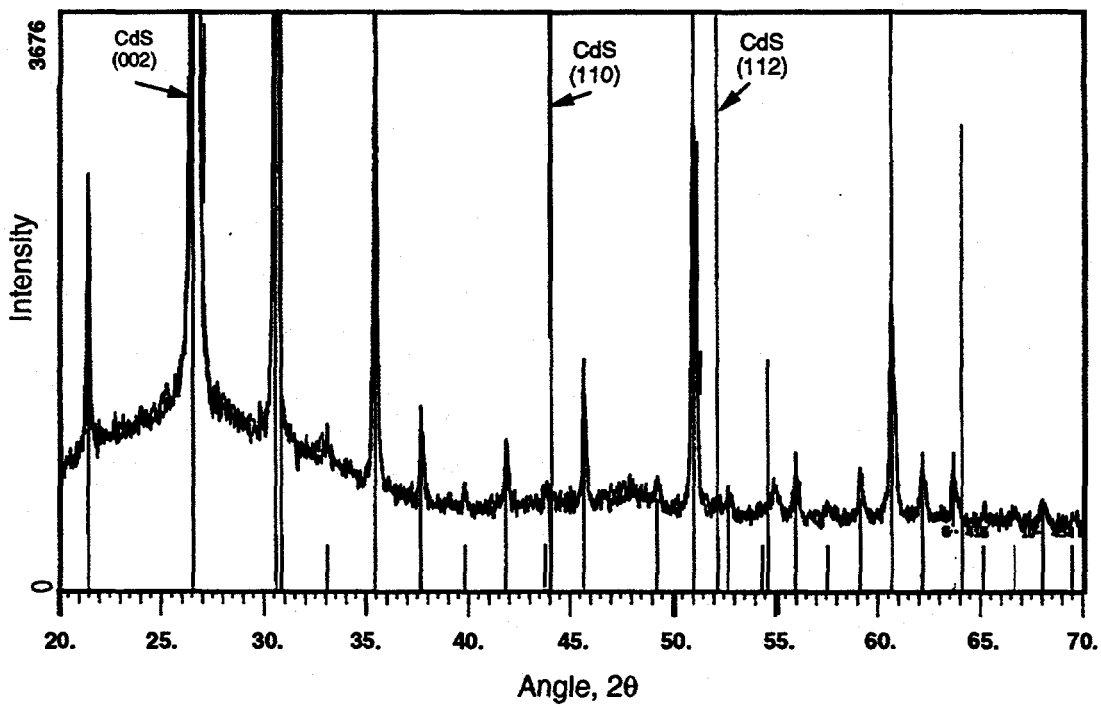

Figure 5.1.1-3 X-Ray Diffraction of As-Deposited, Solution-Grown CdS Film on Glass/ITO Substrate (Unlabeled Peaks Due to Indium-Tin-Oxide).

5.1.2 Electrodeposited CdTe

CdTe was electrodeposited onto CdS/ITO/glass substrates using both constant potential and constant current control. Films deposited under potential control were fine-grained, adherent, and uniform and were reproducibly deposited at thicknesses between 1.5 mm – 2.0 mm. TEM bright field and XRD were used to characterize the as-deposited and heat treated CdTe films. Results from these analysis indicated the films were micro-crystalline with grain sizes in the range of 500 Å – 1000 Å. With heat treatments for 20 minutes at 400°C, grain sizes increased to 0.5 mm although the grains were heavily faulted and exhibited a high density of dislocations. An example of a heat treated CdTe grain is presented in the bright field TEM micrograph of Figure 5.1.2-1.

The structure of as-deposited CdTe films is cubic (zincblende) with a measured lattice parameter of ~6.51 Å. These films are partially amorphous with a preferred growth direction of (111). When heat treated at 350-400°C for 20-30 minutes in air (in the presence of $CdCl_2$), the lattice parameter contracts from 6.51 to 6.487 Å as the grain size increases and the film becomes more crystalline (polycrystalline). This shift in lattice parameter

can be seen in the peak shifts in the XRD spectra shown in Figure 5.1.2-2. With the heat treatment, the peak height increases and width decreases as the peak maximum shifts to higher angles (smaller d-spacings). Birkmire (ref. 1) has attributed this peak shift to the formation of a solid solution phase between the diffusing sulfur and CdTe (i.e. the phase, $CdTe_{(1-x)}S_{(x)}$).

Figure 5.1.2-1 TEM Bright Field Examination of Heat-Treated CdTe Film.

In addition to constant potential/current electrodeposition of CdTe, pulsed electroplating of CdTe has also been used with limited success to produce rapidly deposited, adherent , CdTe films. Using this technique in dilute solutions, deposition rates were increased an order of magnitude over conventional constant DC plating rates. However, in order to optimize device performance, this technique was temporarily discontinued in favor of the more conventional, proven approaches.

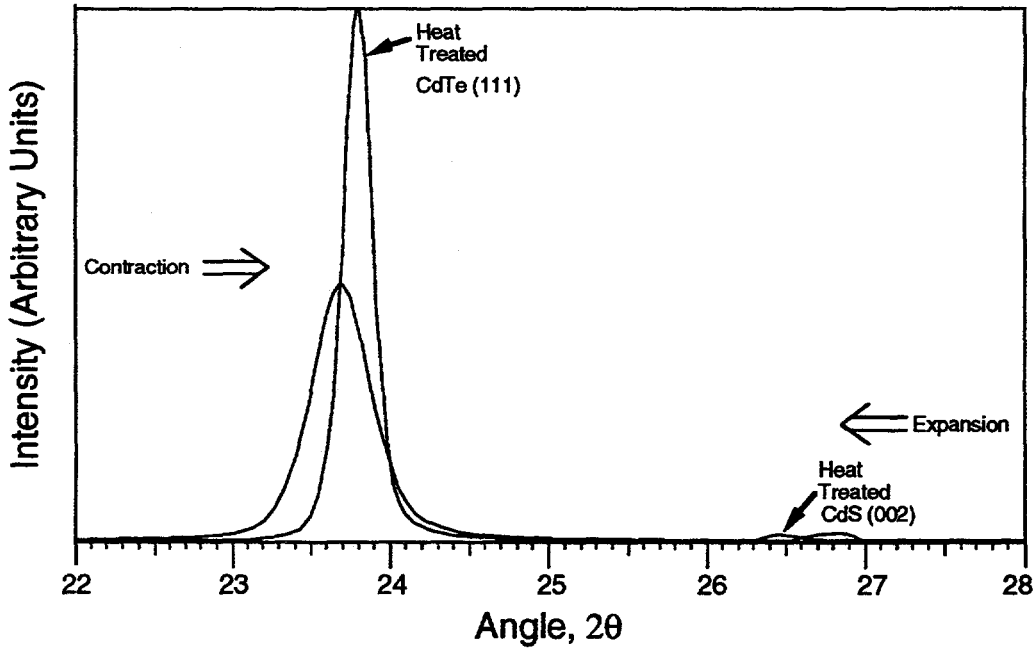

Figure 5.1.2-2 X-Ray Diffraction of Heat-Treated and As-Deposited Glass/ITO/CdS/CdTe Stacks Revealing the Formation of Solid Solutions Across Heterojunction.

5.2 DEVICE OPTIMIZATION

The objective in this task was to optimize electrodeposited polycrystalline, thin-film, heterojunction CdTe devices in the superstrate configuration using films developed in Section 5.1. From Task I, we confirmed that CdTe growth behavior was intimately related to the morphology and chemical stability of the underlying substrate. Since device performance is dependent on the grain size and orientation of the CdTe film, which is in turn dependent on the underlying substrate, variations in each film had a marked effect on the overall performance of the device. For example, in the formation of the glass/TCO/CdS/CdTe stack, the as-deposited CdTe grain size was dependent on the CdS morphology/chemistry, which in turn was dependent on the properties and quality of the transparent conductive oxide. There was a 'memory', or prior history to the underlying substrate which effected the characteristics, both chemical and electrical, of the electrodeposited CdTe and the overall solar cell performance.

In general, deposits of CdTe were fine-grained because the underlying CdS deposit was fine-grained. For coherent/adhesive coatings, the electrodeposited CdTe should be fine-grained. As a highly efficient absorber layer in a thin-film 'polycrystalline' solar cell, the CdTe film should be large-grained; preferably columnar grains oriented perpendicular to the substrate surface. In the formation of thin-film polycrystalline CdTe deposits, there is therefore a trade-off between fine-grained deposits which are adherent and course-grained deposits which are good p-type layers but loosely adherent.

For the devices prepared in this task, TCO-coated glass substrates were obtained from four different sources. These substrates represented a cross-section of surface morphologies and chemistries that ultimately effected the deposition behavior and electrical characteristics of the CdS and CdTe films. Not only were there issues and concerns with the TCO-coated glass, but there were concerns with each film as it effected the glass/TCO/CdS/CdTe stack during post processing. Progress in the CdTe cell development has been directly related to the understanding of synergistic effects of the films in the device. Results for individual film characteristics and their effect on device performance is presented below.

5.2.1 Transparent Conductive Oxide

Irrespective of the conductive oxide film, CdS was reproducibly and uniformly deposited onto glass/TCO substrates. Blemishes and irregularities on the TCO surface however, did

effect the CdS coatings by superimposing those artifact patterns in the TCO onto the outer CdS surface. For example, a linear defect in the TCO surface would subsequently appear as a linear defect in the CdS surface. Although macroscopic artifacts in the TCO can be detected, local atomistic variations in the TCO are more difficult, if not impossible, to detect and both types can effect the quality of the CdS coating.

Along with the optical quality of the TCO, there has been concerns with the resistivity instability and the chemical stability of the TCO. Up to this point, the most efficient CdTe devices have been fabricated with tin oxides, with sheet resistances of ~40 Ω/square and indium tin oxides, with sheet resistances of ~20 Ω/square. Tin oxides are thermally stable throughout all of the processing steps although the electrochemical stability of SnO_2 in aqueous solutions at pH's < 3.0 is uncertain. Indium tin oxide, on the other hand, is compatible (stable) with all processing chemistries although the sheet resistivity tends to increase with heat treatments greater than 200°C. Current efforts to improve the TCO quality include 1) utilizing quality F-doped SnO_2, 2) developing both solution grown Sb-doped SnO_2 and sputtered SnO_2 capabilities and 3) modifying existing surface cleaning practice of as-received TCO coatings.

5.2.2 CdS Window Layer

Solution-grown cadmium sulfide, although chemically pure and stoichiometric, can deposit in a loosely-adherent powdery form on top of a TCO/glass substrate. These powdery deposits tend to form islands that coincide with irregularities in the TCO. Although the CdS is ultrasonically cleaned after the growth process, these deposits may not be completely removed. Mechanical polishing is one approach for removing the loose deposits but drag marks from the particles or polishing cloth can cause irregularities in the CdS coating. Polishing has been used however, with limited success in the lab although this practice would certainly not be used in a production operation. Loosely adherent particulates and islands on the CdS surface would have to be removed since these deposits ultimately lead to the formation of pinholes in the CdTe stack during post processing.

Loosely adherent particles have a direct effect on surface morphology. Since surface morphology of the CdS directly affects properties of the CdTe film, efforts are currently in progress to improve this surface morphology. Impurities and contaminants, in a variety of forms (i.e. particulates, colloids, etc.), can become selectively absorbed or non-uniformly

deposited on the CdS surface during the CdTe electroplating process and impurity absorption is influenced by electrode surface morphology. Impurities absorb onto high spots in the CdS coating and temporarily 'poison' or polarize the surface. This shifts CdTe deposition to adjacent activated sites, such as valleys or recessed areas. These valley' areas grow and then become de-activated as new adjacent sites become re-activated. The result of this process is a deposit which is built up of fine grains, none of which have remained active long enough to grow to any appreciable size. Surface profile of the substrate is one cause of fine CdTe grains but other local irregularities, such as surface charge, chemistry, and electrical resistance, can also affect the polarization behavior between adjacent sites on the CdS surface and these effects are currently under investigation.

As-deposited CdS is a stable, highly oriented film whereas CdS, sandwiched between an underlying TCO and overlying CdTe, is modified during post processing heat treatments. When heat treated at 400°C for 30 minutes in the presence of $CdCl_2$, the CdS layer becomes more crystalline with corresponding shifts in the individual x-ray peaks. The original, highly oriented CdS layer (predominantly (002) growth) exhibited more crystallinity(more peaks in the spectrum) with increased exposure time at 400°C; FWHM of the peaks also decreased with increased exposure time. These affects can be seen when comparing the as-deposited and heat treated spectra shown in Figure 5.2.2-1.

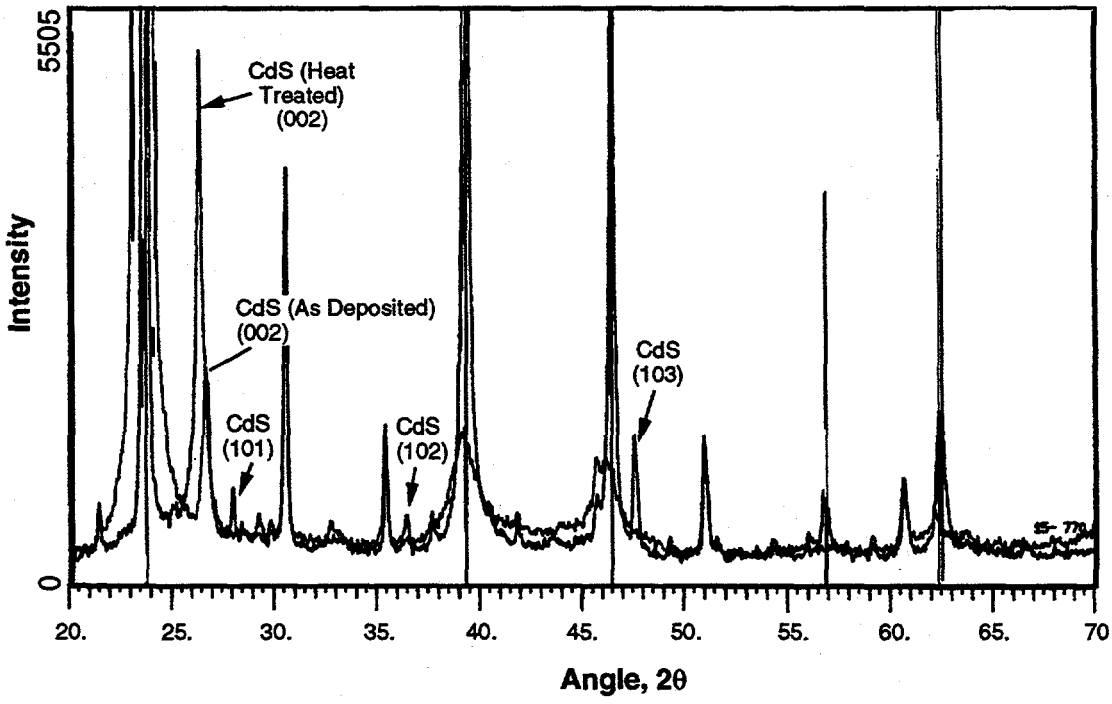

Figure 5.2.2-1 X-Ray Diffraction of Heat-Treated Glass/ITO/CdS/CdTe Stack Revealing Shift in CdS Structure.

One explanation of the shift from the as-deposited to heat treated CdS spectra shown in Figure 5.2.2-1 is the incorporation of tellurium into the CdS structure. According to Birkmire (ref. 2), CdS can form a solid solution with tellurium. Since tellurium rapidly diffuses into the CdS film during heat treatment, the shift in the x-ray peaks could be due to the formation of a $CdS_{(1-y)}Te_{(y)}$ solid solution task. Lattice parameters for the heat treated CdS film are a = 4.14 Å and c = 6.728 Å; this represents a 1.1% expansion in the c-direction over the as-deposited film. Given the relative size of tellurium, the expansion of the CdS lattice is consistent with theoretical predictions and this conclusion is supported by the experimental results.

5.2.3 CdTe Absorption Layer

Device efficiency is a direct function of as-deposited CdTe film properties, such as grain size, carrier concentration (and type), impurities, and defects. Since concentration of acceptors and donors can be nullified by the self-compensating nature of CdTe, type and form of native defects in the as-deposited film can have a significant impact on the performance of the device. For example, if the as-deposited CdTe contains excess tellurium as a separate phase instead of as an intrinsic defect, then the concentration of acceptor sites (i.e. tellurium interstitials) would be much lower than expected and the p-type carrier concentration would be very low. Hence, formation of an intrinsic p-type CdTe film directly from an electrodeposition bath may be difficult depending on the types of impurities and the way in which these impurities are incorporated into the film. Due to the reproducibility of consistent as-deposited p-type films, current efforts have been directed toward optimizing the acceptor concentration in the CdTe with an n-p type conversion process (i.e. conversion of an as-deposited n-type film into a p-type film with thermal conversion (Ref. 2)).

Another film property which is being investigated is the as-deposited grain size. In the electrodeposition process, the grain size is controlled by 1) current density, 2) temperature, and 3) concentration. High current density and elevated temperature favor course-grained, loose deposits. The current density in CdTe deposition, however, is limited by the requirement to control the deposition potential; since the applied potential controls the Cd/Te ratio in the deposit, CdTe stoichiometry (and current density) are set by the deposition potential (under current control, more CdTe can be deposited, but the deposits become more cadmium-rich as the current density is increased). Therefore, the requirement to control CdTe stoichiometry with a potentially controlled system places a limit on the maximum current density for the process.

The other process variables are bath temperature and composition. Bath temperature has been maximized for this aqueous system by setting the temperature just below the boiling point. The effect of bath composition is similar to temperature in that higher concentrations of tellurium and cadmium usually favor courser-grained deposits. Both tellurium and cadmium concentrations have been increased to essentially the upper practical limit for quality, CdTe deposits (e.g. tellurium concentration is always at saturation). For cadmium, the concentration is at a level for optimum formation of CdTe; if the concentration of cadmium is increased beyond the current level (i.e. 0.5 M), then excessive cadmium in the bulk solution can lead to higher levels of cadmium in the CdTe deposit.

In the electrodeposition of CdTe, there is a balance between the reduction of tellurium, cadmium, and hydrogen and this balance depends on the concentration of each of these species and the current density at the surface of the electrode. Although overlooked in most cases, atomic hydrogen can become incorporated into as-deposited CdTe and effect further post processing steps. To investigate the issue of atomic hydrogen in CdTe films, an as-deposited CdTe film was heated in vacuum ($>10^{-6}$ atm.) and the residual off-gas stream was analyzed with a residual gas analyzer (RGA). Hydrogen was detected in the exit gas stream as the sample was heated to 200°C. There were, however, no other elements, with atomic masses less than 100, detected in the exit stream.

Although unnoticeable in the appearance of the as-deposited film, hydrogen did become a problem in the high temperature post processing steps by creating blisters in the CdTe film. Blisters formed in this manner are unstable and could subsequently rupture to create pinholes in the CdTe device. An example of ruptured blisters in the CdTe device is shown in the micrograph of Figure 5.2.2-2. Since atomic hydrogen formation during electrodeposition is a function of the hydrogen overpotential on the CdS surface, changes were made in the deposition and thermal processing of the CdS to reduce atomic hydrogen formation (It should be noted that it's not just the formation of atomic hydrogen that is detrimental, but the inability of atomic hydrogen to recombine at the surface to form molecular hydrogen during electrodeposition; molecular hydrogen, as a gas, would not be a problem). It's difficult to completely eliminate the hydrogen reduction reaction in an aqueous system and therefore, a minimum level of atomic hydrogen will be incorporated into the CdTe film. Depending on the consistency of post processing thermal treatments, there is always the probability that atomic hydrogen can form micron sized blisters which can subsequently rupture to form pinholes. A major effort in the process development has been directed toward minimizing this problem.

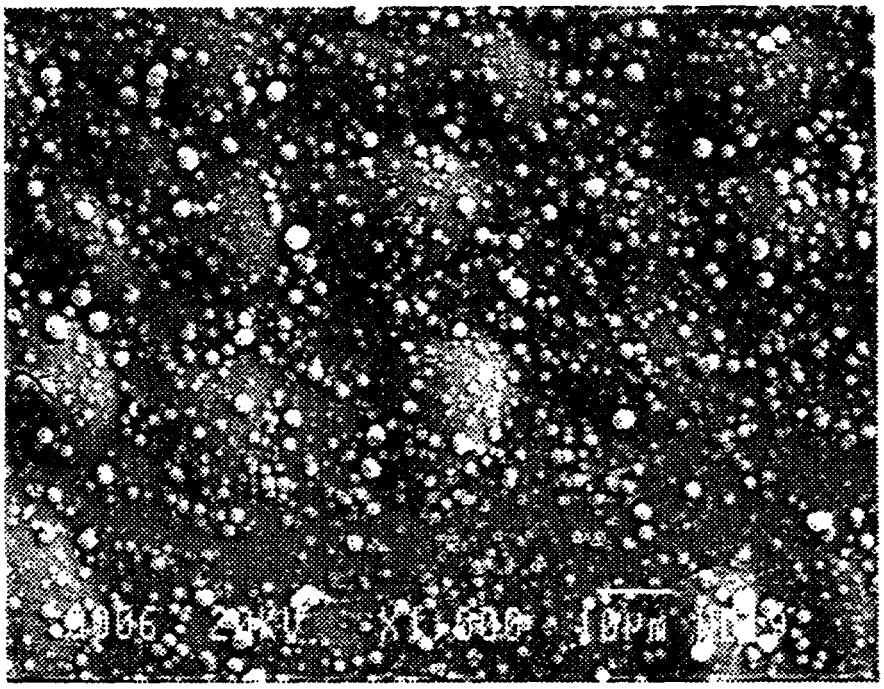

Figure 5.2.2-2 SEM Micrograph of Blistering in CdTe Film After Heat Treatment.

5.2.4 Device Characterization

Two primary new efforts were started in phase II of this activity to characterize the electrical behavior of the CdTe devices: (1) computer modeling and (2) I-V curve measurement and analysis. These efforts proved to be very useful in guiding this second phase of CdTe process development and should help define the direction for achieving device efficiencies over 10 % in the future.

5.2.4.1 Computer Modeling -- The starting point for solar cell model development was the conventional five parameter equivalent circuit consisting of a diode with saturation current I_{sat} and diode ideality factor A; a parallel current source I_L to represent generation of current with light flux; a parallel resistance Rp to represent leakage around the junction; and a series resistance R_s. The I-V curve solution for this equivalent circuit was computed using Newton's method.

This model proved to be inadequate in simulating the I-V behavior of initial CdTe devices. The difficulty was found to be associated with the presence of a Schottky barrier at the back contact to the device, which was responsible for a distinctive "kink", or inflection point, in the I-V curve at forward biases of a few tenths of a volt. To accom-

modate this phenomena, an additional, reversed diode, along with a parallel resistance and current source, was added to the model. This equivalent circuit was capable of representing the electrical behavior of all the devices measured and was convenient for evaluating the efficiency degradation due to Schottky contacts to the CdTe. A simulation of an early device with a large Schottky barrier contact is shown in Figure 5.2.4.1-1. Figure 5.2.4.1-2 shows the illuminated device with a low-resistance ohmic contact.

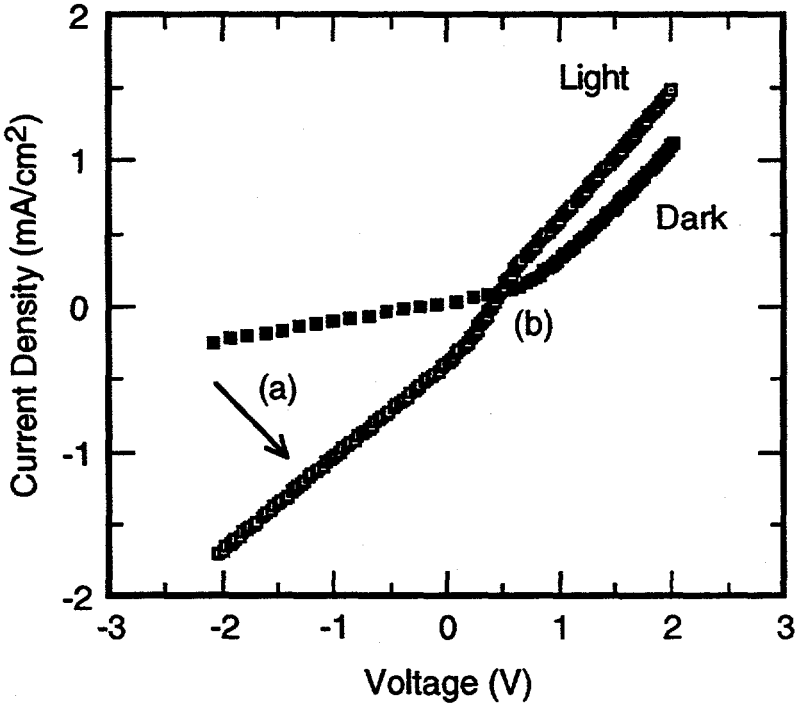

Figure 5.2.4.1-1 Model of CdTe Device Simulating the Effects of a Large Schottky Barrier Upon Its I-V Characteristics.

<u>5.2.4.2 I-V Curve Measurement and Analysis</u> -- A preliminary experimental setup was assembled to allow rapid evaluation of CdTe device characteristics. This setup consisted of a swept I-V curve measurement with oscilloscope display and an uncalibrated light source.

Measurement and analysis of initial CdTe devices showed that at least two problems needed to be addressed, namely (1) increasing the carrier concentration and quality of the p-type CdTe and (2) eliminating the back Schottky contact. Since early CdTe films were mainly grown directly as p-type films, it was decided to concentrate on using a process in which type-conversion of n-type CdTe was obtained by a 350°C to 400°C post anneal.

Earlier work by Basol indicates that superior p-type material can be grown by this approach. The current process being used is discussed below.

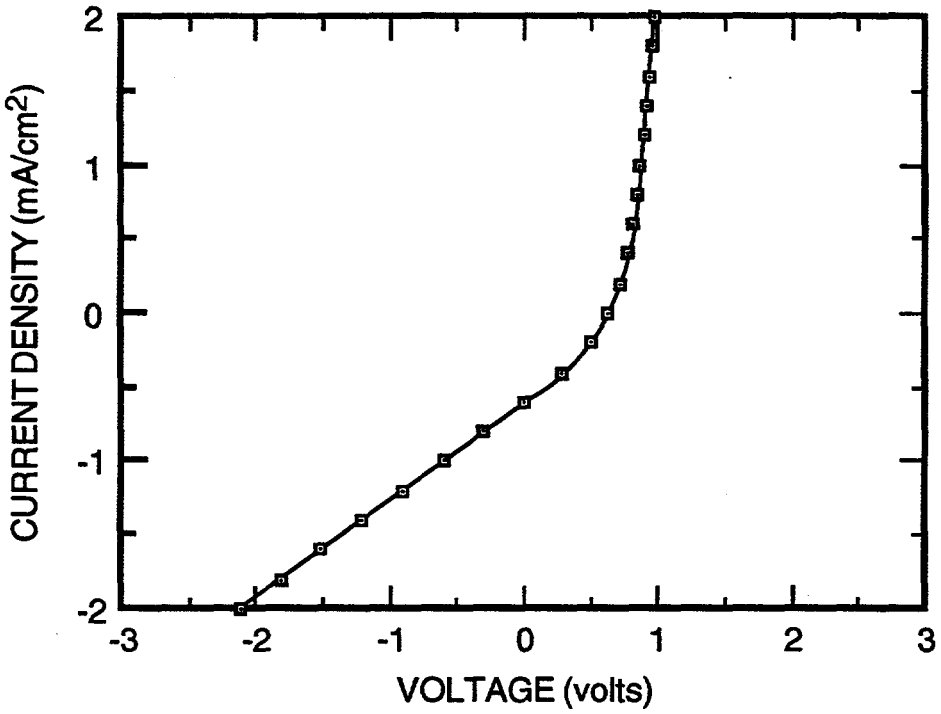

Figure 5.2.4.1-2 Model of CdTe Device Simulating the Effects of a Low-Resistance Ohmic Contact Upon Its Illuminated I-V Characteristics.

To improve the back contact, careful attention was given to the etching of the CdTe just prior to contacting, so that a Te-rich surface could be obtained. Gold contacts to both the CdTe and to the Transparent-Conductive-Oxide (TCO) were then evaporated through an aluminum mask. Electrical contact for I-V measurements was done through wire probes to the Au-CdTe and through indium-soldered contacts to the Au-TCO.

Electrical and optical characteristics of a CdTe device with 6.3 % efficiency, fabricated with this process, are shown in Figures 5.2.4.2-1 and 5.2.4.2-2. The equivalent circuit parameters for this device are

Device area = 0.0764 cm^2	I_{sat} = 2.494 x10-4 mA
R_s = 103.9 Ω	I_L = 1.22 ma
R_p = 7143 Ω	A = 3.5.

Sample: 820-A1-2 Temperature = 25.0°
Sep. 2, 1992 2:49 pm Area = 0.0764 cm^2

Fill Factor	=	53.69%
Efficiency	=	6.3% (total area)
V_{oc}	=	0.7372 V
I_{sc}	=	1.220 mA
J_{sc}	=	15.98 mA/cm^2
P_{max}	=	0.483 mW
I_{max}	=	0.958 mA
V_{max}	=	0.5042 V

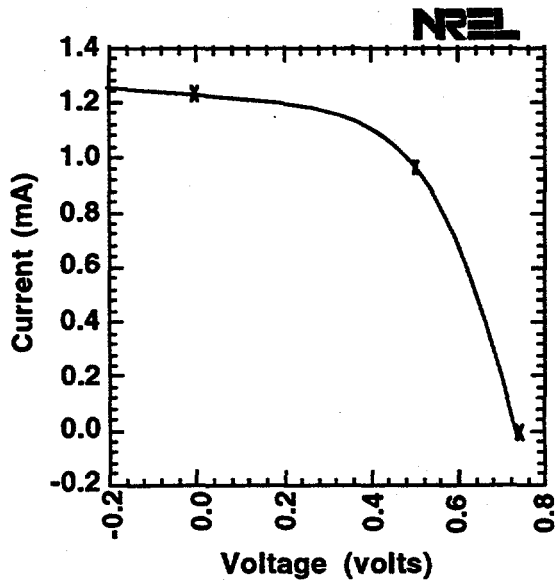

Figure 5.2.4.2-1 Electrical Properties of Electrodeposited CdTe Device.

Sample: 820-A1-2 Temperature = 25.0° C
Sep. 2, 1992 1:48 pm Area = 0.0764 cm^2

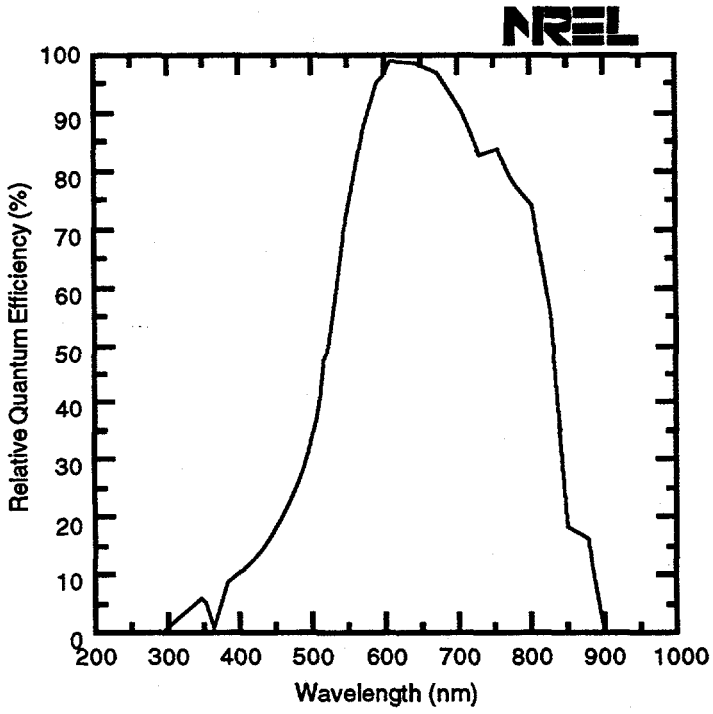

Figure 5.2.4.2-2 Optical Properties of Electrodeposited CdTe Device.

The high series resistance is primarily due to the poor TCO used, which had a resistance of about 56 Ω/square. Figure 5.2.4.2-3 shows a simulation of this device, first with the measured series resistance, and second with a simulated series resistance of10 ohms. As can be seen in the figure, the poor quality TCO causes the device efficiency to be degraded from 7.4 % to the 6.3 % measured.

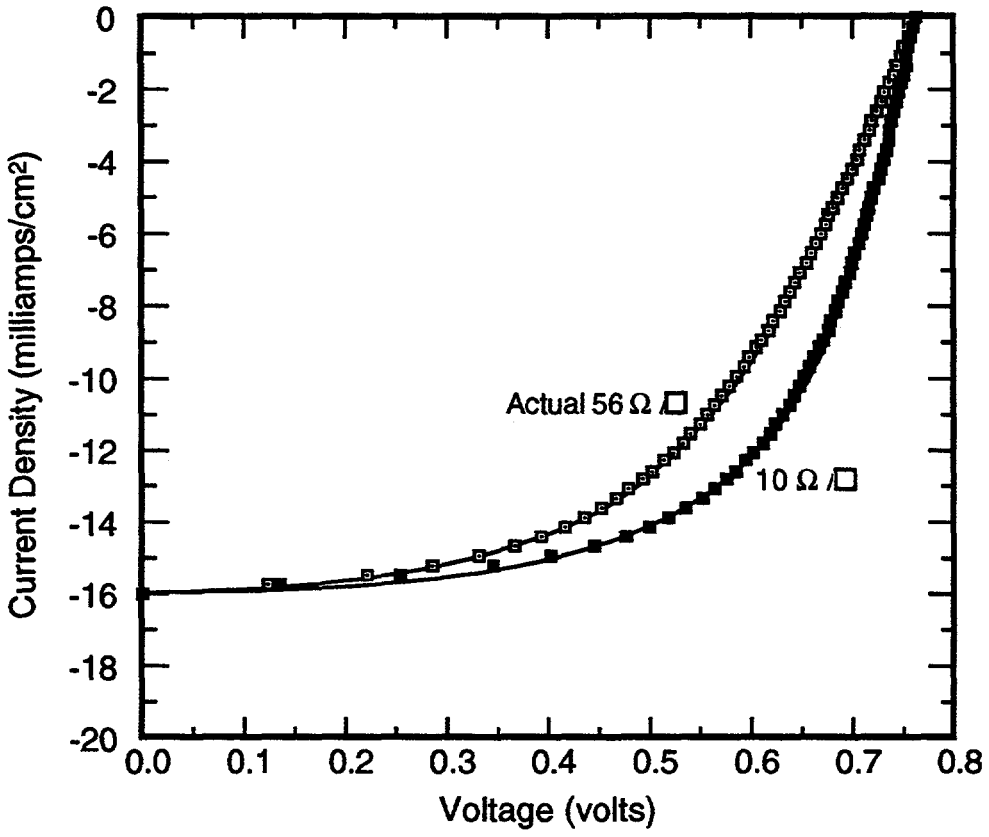

Figure 5.2.4.2-3 Modeling of a CdTe Device with Low and High-Resistance TCO.

Another technical issue raised by these measured device parameters is the high diode ideality factor A. The device likely is dominated by recombination effects, possibly at the grain boundaries. Future work will address this issue.

5.2.5 Post Processing

Current post processing of CdTe devices for NREL consists of: 1) $CdCl_2$ treatment, 2) 350°C — 400°C thermal anneal in breathing air, 3) Br_2-CH_3OH etch to produce a telluri-

um-rich surface, and 4) evaporation of gold for a back contact. Devices, using this post processing procedure, have been produced with efficiencies greater than 6%. With an improvement in the formation of the back contact (i.e. use of a dopant, such as copper, to form a p+-layer and optimization of the etching procedure), it is anticipated that efficiencies of the devices should increase to over 8%.

Another efficiency limiting factor, along with the back contact, is the issue of pinholes and defects in the films. Most flaws or imperfections in the device do not develop, or become apparent, until the post processing steps. In the first heat treatment at 350°C – 400°C for type-conversion and grain growth, pinholes and blisters can form in the device. Pinholes and defects associated with blisters have already been attributed to the formation of hydrogen in the films. When blisters form and rupture, the TCO is exposed and the device is shorted. Aside from blisters, another primary source of pinholes is due to imperfections in the glass/TCO substrate. Defects in the TCO, as reported earlier, can propagate irregularities in each of the overlying films and ultimately form pinholes during the post processing steps. Although deposition processes other than electrodeposition are less sensitive to these substrate irregularities, electrodeposited films, when properly deposited, will form mechanically compatible interfaces with underlying substrates and maintain stability with time.

6.0 AREAS FOR FURTHER INVESTIGATION

In Phase 2 of this program, we are to investigate the scaleup of size and performance of devices developed in Phase 1. This will involve the area scaleup of the C-Mag process to accommodate areas up to 930 cm^2 (1 ft^2). Mo film deposition has already been demonstrated up to this area, and preliminary investigations under Martin Marietta IR&D D-17R have demonstrated laser scribing at this size using completely in-house capabilities. Both these techniques will be implemented to realize the ultimate goal of Phase 2 of producing a 930 cm^2 (1 ft^2) monolithically-integrated CIS submodule on glass. Small minimodule demonstration articles are in progress.

In addition, it was evident that some C-Mag issues regarding uniformity must be addressed. Our IR&D program is studying the performance of this aspect of the sputtering system. Preliminary results indicate that corrective measures implemented to eliminate target poisoning have worked, and these technologies will be transferred to the Phase 2 effort. Also, glass/Mo/CuIn stacks with improved compositional controls have been completed for device fabrication by both H_2Se and Se vapor selenization.

While our Mo films appear to adhere quite well in most cases, it is imperative that characterization of this phenomenon be addressed. As before, IR&D D-17R is studying the stresses in thin films using innovative x-ray techniques developed at the University of Denver under a Seed Grant instituted by the Colorado Advanced Materials Institute in 1992. These early investigations indicate that our Mo films area in compression, which would explain our good adhesive properties. However, results from further studies regarding the tailoring of residual stresses by process parameter modification will be implemented into Phase 2 as they become available.

7.0 SUMMARY

The first phase of this investigation has shown that both the C-Mag and electrodeposition have great potential for low-cost photovoltaics. In particular, the C-Mag demonstrated a deposition rate limit much higher than that available with planar sputtering cathodes. Furthermore, the C-Mag system at Martin Marietta has demonstrated excellent film thickness uniformity. Devices with 8.4% total area efficiency were fabricated with reasonable fill factor. Once noted variations in composition between runs on the C-Mag have been corrected, it is felt that devices with excellent performance can be produced.

In addition, the electrodeposition process, originally developed under Martin Marietta IR&D D-17R, has produced devices with 6.3% total area efficiency. Two main limitations with these devices have been CdS thickness and low-conductivity SnO_2 transparent conductive oxide. Improved TCO conductivity should account for an efficiency increase to 8% or better, and thinner CdS films would improve the device performance as well. Both will be addressed in Phase 2.

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16. Abstract (Limit: 200 words)

This report describes work done during Phase 1 of the subject subcontract. The subcontract was designed to study innovative deposition techniques, such as the rotating cylindrical magnetron sputtering system and electrodeposition for large-area, low-cost copper indium diselenide (CIS) and cadmium telluride (CdTe) devices. A key issue for photovoltaics (PV) in terrestrial and future space applications is producibility, particularly for applications using a large quantity of PV. Among the concerns for fabrication of polycrystalline thin-film PV, such as CIS and CdTe, are production volume, cost, and minimization of waste. Both rotating cylindrical magnetron (C-Mag™) sputtering and electrodeposition have tremendous potential for the fabrication of polycrystalline thin-film PV due to scaleability, efficient utilization of source materials, and inherently higher deposition rates. In the case of sputtering, the unique geometry of the C-Mag™ facilitates innovative cosputtering and reactive sputtering that could lead to greater throughput, reduced health and safety risks, and, ultimately, lower fabrication cost. Electrodeposited films appear to be adherent and comparable with low-cost fabrication techniques. Phase 1 involved the initial film and device fabrication using the two techniques mentioned herein. Devices were tested by both internal facilities, as well as NREL and ISET.

17. Document Analysis

a. Descriptors

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