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Thin Silicon Solar Cells

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The authors gratefully acknowledge the valuable contributions of C.L. Kendall, J.C. Checchi, D.L. Brooks, and C.J. Colgan in the fabrication and processing of Silicon-Film™ solar cells. Additionally, the authors thank Dr. Paul Basore of Sandia National Laboratories for providing comprehensive device measurements and analyses on laboratory-scale solar cells.

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Acknowledgment

The authors would like to acknowledge the valuable contributions of Dr. Paul A. Basore of Sandia National Laboratories for providing comprehensive device measurements and analyses on laboratory-scale solar cells, including detailed modeling of light trapping properties. The assistance of Dr. Kent Schubert, also of Sandia National Laboratories, in the chemical analysis work is appreciated.

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1 Introduction

This report covers contract work for the period from July 1990 to October 1991.

The Silicon-Film process involves the deposition of a silicon layer on a conducting ceramic substrate. The ceramic has been coated with a reflective metallurgical barrier layer. The device structure has been designed to incorporate light trapping, and maximize the collection efficiency of photogenerated carriers. Obtaining back surface passivation at the Silicon-Film/metallurgical barrier is a key element in achieving high collection efficiency.

Device results for Product II structures on ceramic are presented that show the metallurgical barrier is up to 70% reflective, and significant levels of light trapping are present. The long wavelength spectral response and reflectance measurements are analyzed to estimate the level of light trapping achieved. Device efficiency has been limited to 6.6% by low minority carrier diffusion lengths. Significant levels of impurities have been detected in the silicon films and are believed to be causing the low diffusion lengths.

1.1 Silicon-Film Product Families

The development of the Silicon-Film process has generated a family of three products. They are pictured in **Figure 1.** Product I, being developed for production now, utilizes a 100-μm-thick active layer of silicon on a supporting substrate. There is no barrier layer between the active layer and the substrate, and no light trapping features are designed in the structure. A recent review of the production development of Product I reported an efficiency of 9.45% [1].

Light trapping is incorporated into the Product II design shown in **Figure 1.** Product II differs from Product I by the presence of a metallurgical barrier layer, and by the reduction in thickness of the active silicon layer (30 μm). There are performance and cost advantages to using a thin silicon structure as opposed to a thick conventional device. These advantages are 1) improved V_{oc}, 2) reduced dependence on diffusion length (and therefore less stringent material

purity and quality requirements), and 3) reduced cost through the use of less silicon. Light trapping must be incorporated into a thin device structure to assist in the absorption of the long wavelength light. Long wavelength light (wavelength range 0.9 μm to 1.1 μm) is weakly absorbed in crystalline silicon. The design, modeling, and fabrication of the Product II device are reviewed in this work.

Product III utilizes the Silicon-Film process developed for Product II, therefore enjoying the performance and cost benefits of the thin silicon light trapping design. The active silicon layer is configured into a monolithically integrated, high-voltage structure. This structure allows all electrical contacting to be made on the back of the device, therefore simplifying module assembly. The high-voltage, low-current configurations possible with such a device minimize contact resistance problems and avoid front surface shadowing by current carrying metallic bus bars. The Product III design allows the use of the large ceramic substrates (10 cm x 60 cm)[1] generated by the Silicon-Film process.

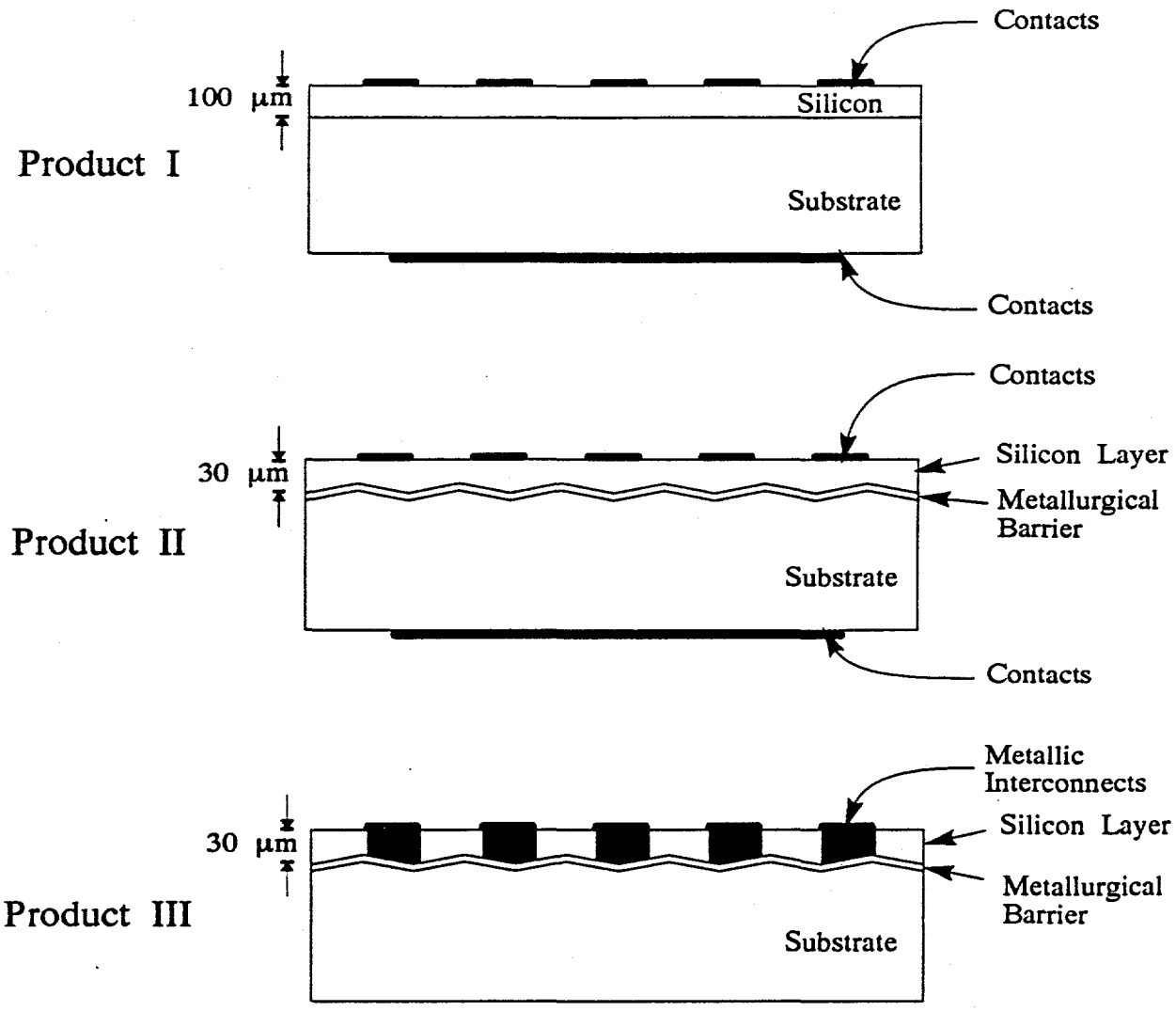
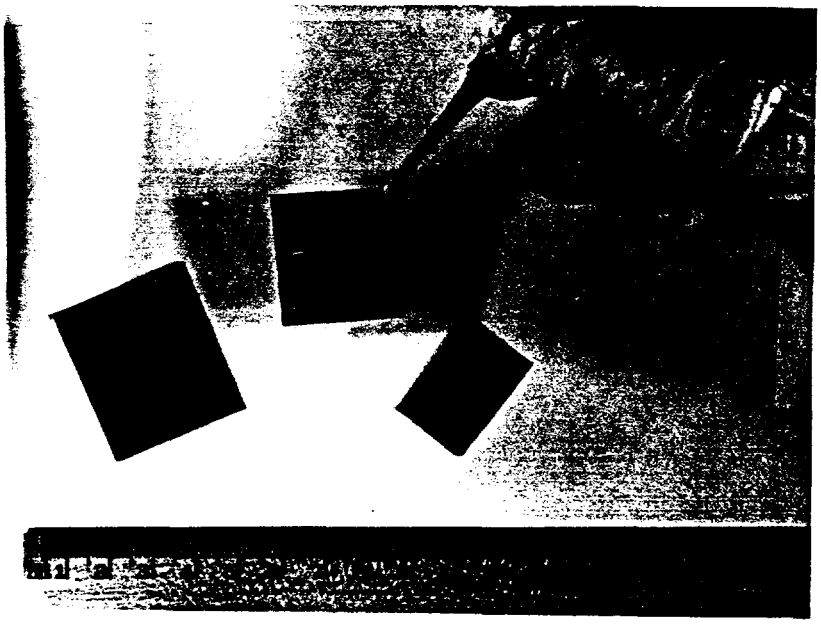


Figure 1. *The Silicon-Film product families.*

1.2 Product II Device Structure

Three Silicon-Film Product-II wafers are shown in **Figure 2(a)**. The grain structure is long grains, millimeters in width and centimeters in length. A cross section is shown **Figure 2 (b)**, where the grown crystalline silicon layer can be seen over a coarse ceramic substrate. The silicon layer pictured is approximately 70-μm thick on a 600-μm-thick ceramic. The relatively large grain structure results in an aspect ratio exceeding 10 (ratio of the lateral grain dimension to the film thickness).

(a)



(b)

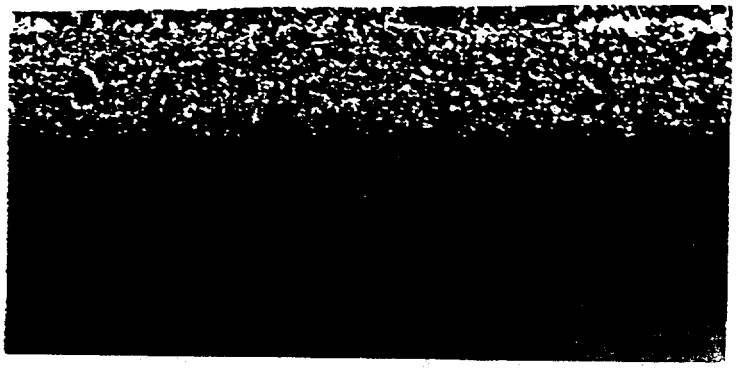


Figure 2. *Silicon-Film Product II. Samples of Silicon-Film on ceramic are shown in (a). A cross section is shown in (b), revealing a 70-μm-thick silicon layer on a 600-μm-thick coarse ceramic substrate.*

The ceramic is fabricated from low cost powdered materials, and is formed into its 10 cm x 10 cm x 0.5 mm pieces, then heat treated to remove binders. Properties of the ceramic have been carefully chosen to maintain strength at the high silicon deposition temperatures, be expansion matched to silicon, and be electrically conductive.

The metallurgical barrier is deposited by production-based, low-cost processes. Interaction of the barrier and silicon active layer needs to result in a low-recombination surface to maximize efficiency [2]. High reflectivity and low recombination have been key design elements of the metallurgical barrier development.

The silicon active layer is deposited by the proprietary Silicon-Film technique. Films 50 to 500 μm thick are grown. Aspect ratios (grain width to thickness ratio) exceed 10, with grain dimensions on the order of centimeters. Samples have been fabricated with and without metallurgical barrier layers using the same Silicon-Film process.

1.3 Contract Objectives

The primary objective has been to demonstrate that the high efficiency potential of crystalline silicon can be preserved while using an inexpensive growth process. Technology criteria were established by Sandia to guide the development effort, and are listed below.

1) The active silicon layer should have a thickness of at least 10 μm, with a 100 cm^2 spatial thickness uniformity of +/- 25% or better. This lower thickness limit is dictated by considerations of product uniformity, defect tolerance, and absorption of the incident light.

2) The active silicon layer thickness should be less than the minority carrier diffusion length. This is necessary for collection of most of the photogenerated charge carriers. For the low-cost silicon, this limits the active carrier layer thickness to less than about 100 μm. For multicrystalline silicon, it also requires columnar grain structure with grain diameters at least four times the layer thickness.

3) The effective back-surface recombination velocity should be less than the layer's transit velocity, which is the ratio of the minority carrier diffusivity to the layer thickness.

This is necessary for collection of most of the photogenerated charge carriers. For thin layers of silicon, this requires an effective rear-surface recombination velocity of less than about 10,000 cm/s.

4) The front surface, back surface, or both surfaces of the active silicon layer must be textured (non-planar) so that most of the light that enters the cell can be trapped within the silicon layer by total internal reflection, thus maximizing the photogeneration of carriers.

5) The optical reflectance of the internal rear surface of the active silicon layer must be sufficient to avoid parasitic absorption of light. The reflectance must be greater than about 80% for photon energies between 1.0 eV and 1.5 eV to avoid excessive optical losses.

6) Ohmic contacts to the back surface are required at spatial intervals comparable to those on the front surface, so that series resistance associated with conduction through the barrier layer is less than 0.5 Ωcm^2.

7) The substrate, barrier and thin active silicon layer must be mechanically and chemically capable of being subjected to the high-temperature processing necessary to form the emitter junction.

8) The substrate, barrier, and thin active silicon layer satisfying the above specifications should be capable of being formed at a usable-area production rate of at least 5 m^2/week per $100,000 of production equipment.

The total effort was delineated into 4 tasks addressing the development of the

1. Substrate,
2. Barrier-Layer,
3. Active Silicon Layer, and
4. Solar Cell Fabrication.

A set of solar cell devices and test structures were established as deliverables to assess product and process development. Solar cell deliverable goals were established to be a 1.0 cm^2 device fabricated on a textured substrate, with a metallurgical barrier layer, silicon active layer,

front and back metal contacts and an anti-reflection layer. The efficiency goal of the 1.0 cm^2 device was 10% AM1.5. A 100 cm^2 device deliverable was established without an efficiency target.

1.4 Summary of the Results

The capabilities of the Silicon-Film process was demonstrated with the fabrication of 100 cm^2 structures, 1.0 cm^2 solar cells, and various resistance and reflection test structures. A high conductivity ceramic fabrication process was developed. Many required elements of the process were developed, including: demonstration of light trapping properties, a Silicon-Film/ metallurgical barrier reflection of 70%, fabrication of 100 cm^2 conductive ceramic substrates, and demonstration of large grain silicon films 100 μm thick over areas of 40 cm^2.

A conductive ceramic was fabricated using low cost production based processes. 100 cm^2 ceramics were tested at Sandia and found to have a resistivity of 10 Ωcm, which would be sufficiently conductive for a one-sun device. Ohmic contact to the ceramic was demonstrated using standard screen printing techniques. A low contact resistance value was measured.

Silicon-on-ceramic structures were fabricated with and without intervening barrier layers. Thin silicon active layers with large columnar grains and thicknesses of 50 to 100 μm were fabricated. This represents a grown layer thickness less than 1/2 that demonstrated in earlier work. The achievement of grown layers less than 100 μm thick required careful control of the metallurgical barrier properties. A set of thin grown layer structures with and without barriers were evaluated for internal silicon layer/barrier reflectance. The use of thick barrier layers resulted in barrier layer reflectivity approaching 80%. Thin barrier layers, utilized to grown thin silicon film layers, resulted in reduced reflection (<50%).

Light trapping properties have been measured and quantified in solar cell devices. With the help of models developed at Sandia, effective optical path lengths have been measured that indicate that light trapping properties of the randomly textured ceramic and reflectivity of thick barrier layers result in optical path lengths nine times the physical device thickness.

Solar cell devices were formed on silicon-on-ceramic structures formed with and without barrier layers. Overall efficiency remains limited by low short-circuit current. Low currents

have been the result of low minority-carrier diffusion lengths. Metallic impurities have been found in both silicon feedstock and in grown films at levels that could significantly affect minority carrier properties. Overall AM1.5 conversion efficiency has been limited to 6.6% in a thin silicon-on-ceramic structure with a barrier present.

2 Device Modeling

The effects of light trapping and back surface passivation are critical to realizing the high efficiency potential of the thin silicon films. The effects of these variables on overall device energy efficiency are shown in **Figure 3.** Values of back surface recombination of 10^6 cm/sec (unpassivated) and 10^3 cm/sec (passivated) are used. A single diode model (diode ideality factor = 1) has been used to compute open circuit voltages. This assumption eliminates any dependence of fill factor on changes in doping and diffusion length. A value of 0.82 for the fill factor has been used for all the efficiency calculations in **Figure 3.** A non-ideal relationship between doping and minority carrier lifetime has been used to determine the diffusion length dependence on doping. Lifetime values predicted for single crystal silicon (values taken from PC-1D [3]) have been reduced by a factor of 5 to reflect the non-ideal nature of the Silicon-Film material. This estimate was determined from measurements made on Silicon-Film material over a narrow doping range. This modeling method highlights the limited dependence of the Silicon-Film devices on material quality and minority carrier diffusion length.

Figure 3 shows that the efficiency of a 35-μm-thick device with both light trapping and back surface passivation is superior to that of a conventional device at all doping levels of interest. Peak efficiencies for the thin device are predicted for doping levels in the range of N_a=2x10^{17} cm^{-3} to 5x10^{17} cm^{-3}. These doping levels correspond to diffusion lengths in the range of 40 μm to 80 μm. The efficiencies of the thin devices are predicted to decrease as base doping is decreased (and diffusion length is increased). This is a result of the decreasing V_{oc} that occurs at lower doping levels. The same effect occurs in the conventional device, however current increases offset the lower V_{oc} values, and efficiency remains constant.

The limited dependence on diffusion length allows the thin device to use higher base doping levels and therefore achieve high V_{oc}. This option is not available to thick conventional devices as long diffusion lengths are required to collect minority carriers generated deep in the base layer. The long diffusion length requirement in conventional devices allows high efficiency to be obtained only with high quality, relatively expensive silicon wafers.

Model Parameters

		S_{BACK}	Optical Path Length
A -	400μm Thick Conventional Device	10^6 cm/s	Z = 1
B -	35μm Thick Conventional Device	10^6 cm/s	Z = 1
C -	35μm Thick Device with Back Surface Passivation	10^3 cm/s	Z = 1
D -	35μm Thick Device with Light-Trapping	10^6 cm/s	Z = 20
E -	35μm Thick Device with Light-Trapping and Back Surface Passivation	10^3 cm/s	Z = 20

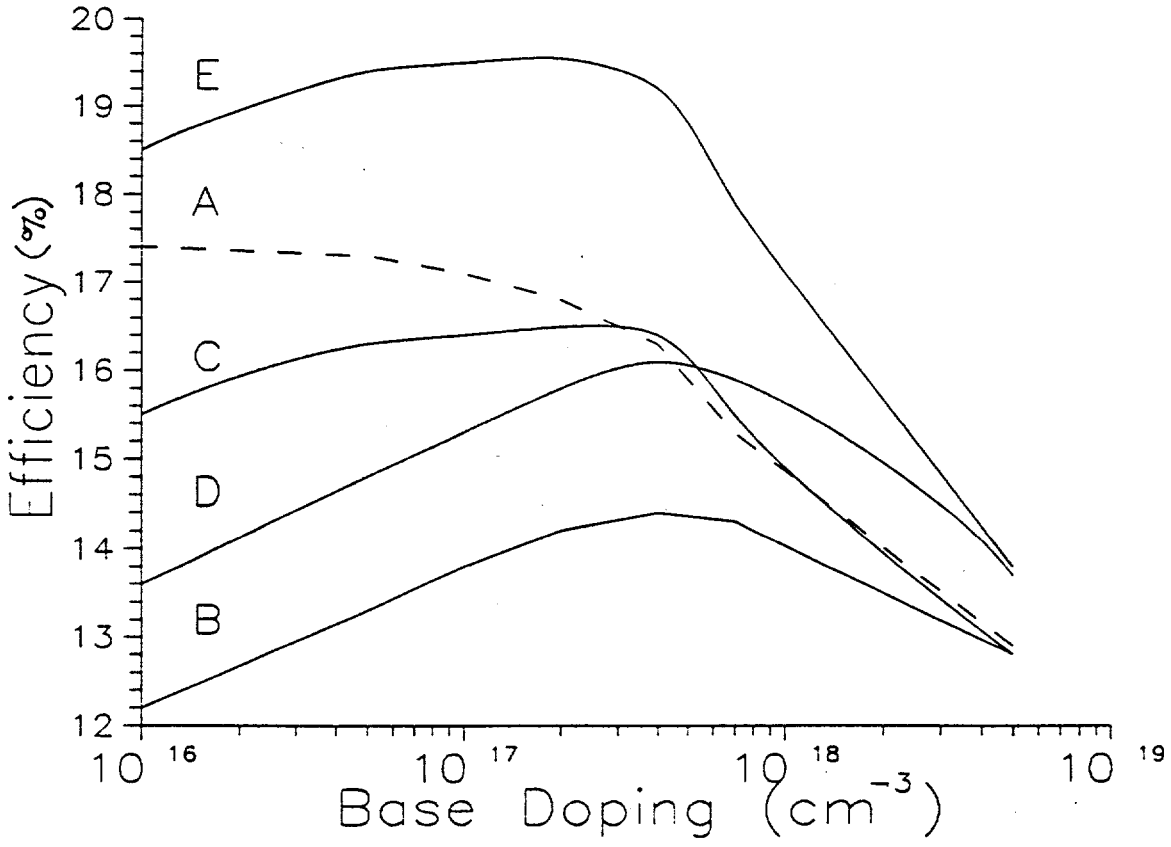


Figure 3. *Predicted conversion efficiency (AM1.5G) as a function of base doping. Diffusion lengths are adjusted to be consistent with doping levels.*

3 Device Fabrication and Characterization

3.1 Conductive Ceramic Substrate

Control of ceramic conductivity has been achieved through the control of the relative portions of the ceramic composition and the resulting mass density. Early efforts to produce conductive ceramic materials resulted in a resistivity of approximately 50 Ωcm. Contact resistance was monitored through the fabrication of test structures with metal paste contacts on the front and back of isolated 1.0 cm^2 ceramic samples. The overall resistance of the low density ceramics with a grown silicon layer was approximately 3 Ωcm^2.

Altering the ceramic composition resulted in a more dense, more conductive material. Volume resistivity was lowered to the range of 10 Ωcm (as measured at Sandia) and contact resistance was lowered to 0.74 Ωcm^2. Overall ceramic thickness is 635 μm, resulting in a substrate that would not significantly affect overall device series resistance.

Ohmic contact was made to the ceramic samples by production screen printing techniques. A silver/aluminum paste was used to form parallel lines on ceramic samples. Printed ceramics were fired in open-air belt furnaces. Resistance measurements could then be made between parallel lines. The resulting data is shown in **Figure 4.** The ceramic under test was 520 μm thick, with printed line widths of 180 μm on 0.33 cm spacings. The contacts were ohmic, with a measured R_c = 0.74 and 0.89 Ωcm^2 for the two devices (average of 0.81 Ωcm^2). This value is slightly greater than that required to minimize impact to device fabrication. Solar cells fabricated on full silicon-on-ceramic structures measured a total series resistance lower than that measured with the test structure. The series resistance of a 1.0 cm^2 solar cell was measured to be 0.4 Ωcm^2 by Sandia. This difference is due in part to localized thinning of the ceramic in the solar cell structure to assist in contacting. From the data in **Figure 4**, the resistivity is measured to be 11.7 and 12.1 Ωcm for the two tests (average 11.9 Ωcm). This agrees with the Sandia measurement of 10 Ωcm.

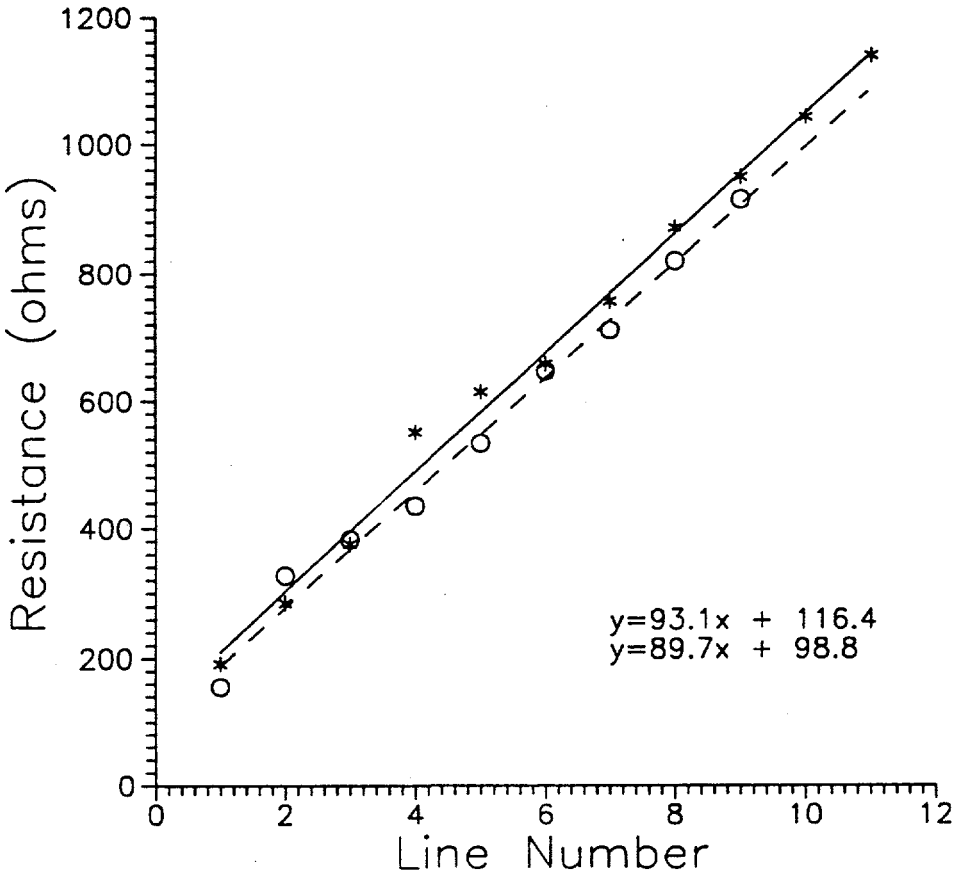


Figure 4. *Resistance measurements made on conductivity test structures fabricated on conductive ceramic substrates. The resistance between consecutively numbered parallel lines for two samples is shown. The resulting analysis revealed a contact resistance of 0.81 Ω cm² and a resistivity of 11.9 Ω cm.*

3.2 Metallurgical Barrier Layer

The metallurgical barrier (MB) layer plays a critical role in the thin device design. As **Figure 3** showed, recombination at the back surface is critical to the overall device efficiency. This recombination will be influenced by the Silicon-Film/MB interface. An effective light trapping design also requires that the interface be reflective to confined light. Additionally, the metallurgical barrier must have the mechanical strength to withstand the silicon deposition process, and it must not be a source of impurities that may have a deleterious effect on device performance.

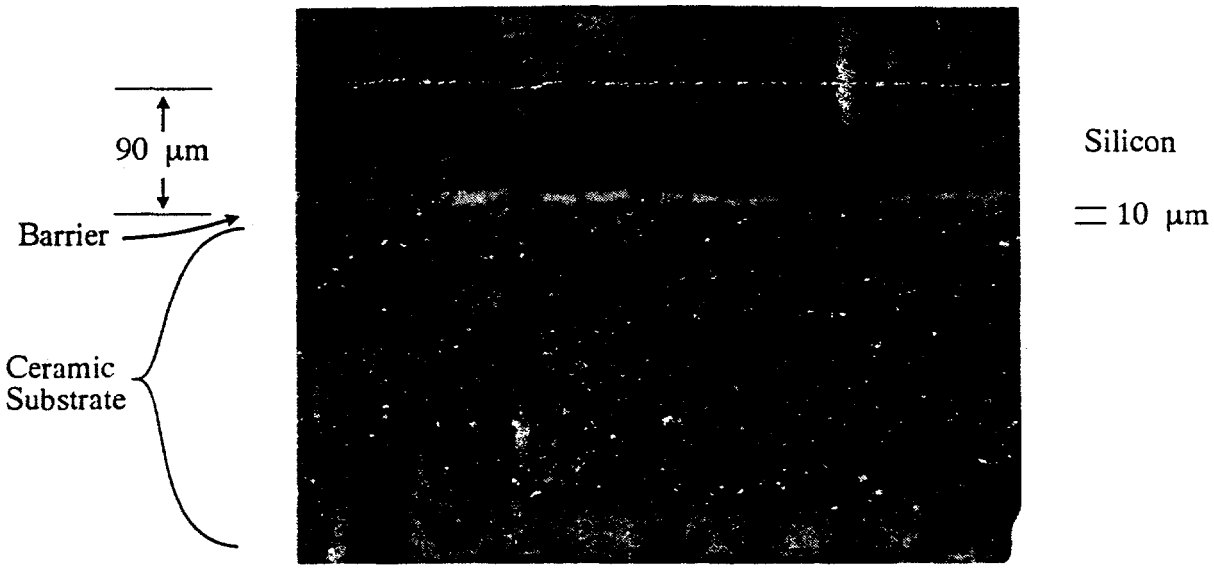


Figure 5. *Cross section of a Silicon-Film/metallurgical barrier/textured ceramic substrate structure. Scratches due to polishing.*

To satisfy these requirements, barrier layers are formed with combinations of materials including dielectric compounds. The barrier layers are deposited using production-type low-cost processes. Present barrier layers have proven effective at mechanically protecting the Silicon-Film layer from large-scale interaction with the ceramic. A cross section of a Silicon-Film/metallurgical barrier/ceramic structure is shown in **Figure 5**. The Silicon-Film layer is approximately 75 μm thick. The metallurgical barrier layer is approximately 10 μm thick. The coarse ceramic can be seen below the barrier layer, and no obvious interaction with the silicon layer is present. Random openings are present in the barrier layer to allow for electrical contact with the ceramic. Much of the scratching of the silicon surface is an artifact from imperfect cross section preparation.

An objective of this work has been to fabricate Silicon-Film layers less than 100 μm thick to maximize collection efficiency. A relationship between the thickness of the barrier and the minimal silicon layer thickness that could be grown was determined. Thinner silicon layers could only be achieved by reducing barrier thickness. The thicker barriers used in the formation of silicon layers 200 μm thick (similar to that seen in **Figure 5**) resulted in an irregular silicon surface when thin silicon layers were grown. A thin barrier deposition process was developed that allowed for the growth of 100-μm-thick silicon layers with smooth surfaces and excellent aspect ratios.

The reflectivity of the barrier-coated ceramics has been tested. During barrier development, reflectance has been measured from an air/barrier interface. (In the final device configuration, reflection from a silicon/barrier interface is required.) Weakly absorbed light is coupled into the grown silicon layer, reflects off the metallurgical barrier, and is emitted out the front surface. The reflected long wavelength light can be analyzed to determine barrier reflection properties (reflection characteristics are covered in detail in the light trapping section). The final device requires a high reflectivity from a Silicon-Film/metallurgical barrier interface.

Subbandgap reflectance test structures have been fabricated. The resulting measurements have shown the silicon/barrier reflectance to be in the range of 11% to 52% (dependent on the assumed internal front surface reflection). This can be compared with similar samples fabricated without a barrier, where the barrier reflection was measured to be 2% to 27% percent. The thinner barriers are not as reflective as the thick barriers (which have obtained reflectivities approaching 70% [4]). Highly reflective thick barriers can be reintroduced to the device structure when the material quality issues are resolved. A more detailed discussion of reflection properties is contained in Section 3.3.1: Reflection Characteristics.

3.3 Light-Trapping Properties

Light trapping must be incorporated in thin crystalline silicon films to enhance the absorption of long wavelength light. Light in the wavelength range 0.9 μm to 1.1 μm is only weakly absorbed in a 50-μm-thick silicon film. Of the photons in the AM1.5G spectrum with energy greater than the bandgap of silicon, 24% are in the wavelength range 0.9-1.1 μm. Without light trapping, a significant portion of these photons are transmitted through the silicon film and lost.

The back surface of the active Silicon-Film layer must be reflective to internally confined light to effectively trap the light. In conventional thick devices, this high reflectivity can be obtained by the application of metallic layers on the back surface. The high temperatures involved in the processing of the Silicon-Film solar cells do not readily accommodate the use of metallic reflectors. A further requirement on the back surface is that it minimizes recombination. Such performance requirements can be met by a silicon/dielectric interface.

The light-trapping properties of a solar cell structure can be deduced from the measurements of reflectivity and quantum efficiency. Reflectivity measurements can be analyzed to compute a range of values for the back surface reflectivity (Silicon-Film/ metallurgical barrier interface) [3]. Experimental quantum efficiency measurements indicate higher levels of response for long-wavelength light than predicted by a simple non-light-trapping model. Analysis of these results reveals light-trapping properties.

3.3.1 Reflection Characteristics

The reflectance of a Silicon-Film on ceramic structure is shown in **Figure 6** with and without a barrier. The increased long-wavelength reflectance of the sample with the barrier is due to light being initially transmitted into the silicon, internally reflected, and then transmitted back out the front. The re-emitted subbandgap light is referred to as the escape reflectance (R_{ESCAPE}). R_{ESCAPE} is defined as the difference between the total subbandgap reflectance (R_{TOTAL}) and the external front surface reflectance (R_{FE}).

$$R_{ESCAPE} = R_{TOTAL} - R_{FE} \quad (1)$$

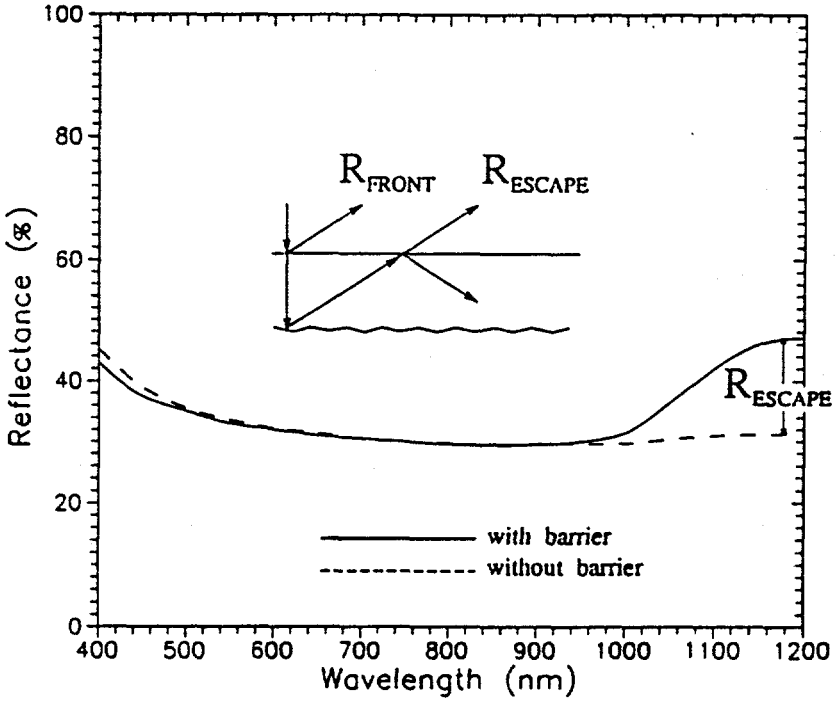


Figure 6. Normalized reflectivity of a Silicon-Film Product II structure. Data is shown for samples fabricated with and without a barrier.

The silicon-barrier reflectance (R_{BACK}) can be calculated (for non-absorbed light) based on the following relationship [3]

$$R_{TOTAL} = \frac{R_{FE}(1 - R_{BACK}) + (1 - R_{FI})}{1 - R_{BACK}R_{FI}} \tag{2}$$

where R_{FI} is the internal front surface reflectance. Solving (2) for R_{BACK} gives

$$R_{BACK} = \frac{R_{ESCAPE}}{1 - \left(R_{FI}(1 - R_{ESCAPE}) + R_{FE}(1 - R_{FI})\right)} \tag{3}$$

The internal front surface reflectance (R_{FI}) is an unknown quantity, although minimum and maximum values can be calculated. The minimum value is that of an uncoated silicon/air surface. The maximum is defined by the best-case texturing scheme that would allow for re-direction of the trapped light, and total internal reflection at the silicon/air surface. For this analysis the Lambertian limit of 92% is used as the best case [5]. This best case assumes the light reflected from the back surface is distributed as the cosine of the angle from the horizontal. The resulting range of barrier reflectance values can be calculated. **Table I** shows that the presence of the barrier layer increases the net back surface reflectivity to the range of 32% to 80%.

Table I. *Analysis of long-wavelength reflectivity.*

	R_{ESCAPE}	R_{FE}	R_{FI} Estimated	R_{BACK}
With Barrier	17.5	29.5	29.5 (min)	31.9
			92.0 (max)	80.5
No Barrier	1.5	29.6	29.6 (min)	3.0
			92.0 (max)	21.4

3.3.2 Quantum Efficiency Characteristics

Quantum efficiency measurements were made on structures with and without barriers. The data for a silicon-on-ceramic sample with a barrier is shown in **Figure 7**. The silicon layer in the samples under test is 190 μm thick. The red response is poor, indicative of material with low minority carrier diffusion length (L_N).

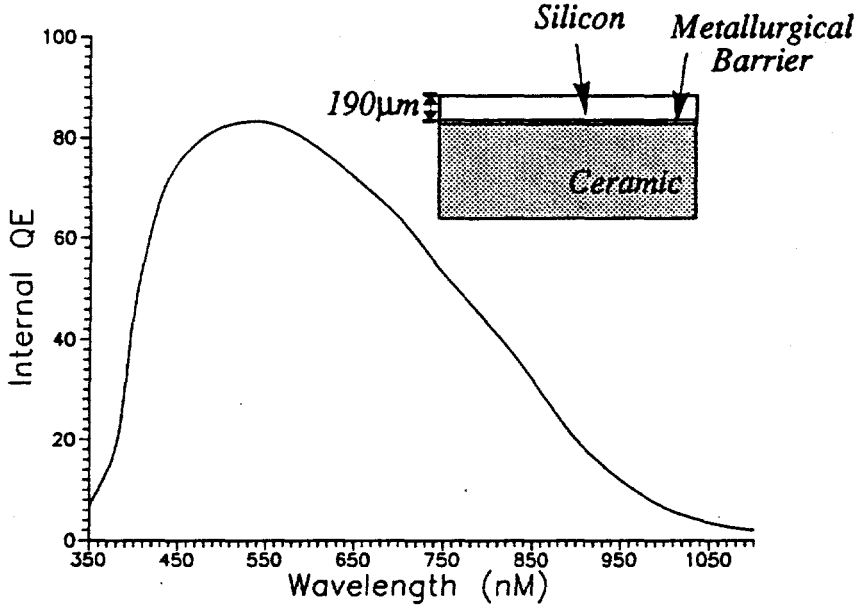


Figure 7. Quantum efficiency of a silicon-on-ceramic structure with a metallurgical barrier layer.

Based on non-light-trapping theory, a measurement of L_N can be made using internal quantum efficiency data. For a device that has a diffusion length less than the device thickness, and photocurrent from the emitter is negligible, the following relationship exists for weakly absorbed light

$$\frac{1}{QE_{INTERNAL}} = 1 + \frac{1}{\alpha L_N} \tag{4}$$

This relationship predicts a linear region in the plot of 1/QE verses $1/\alpha$. These data are shown in **Figure 8** for the QE data from **Figure 7**. Two linear regions are shown. The first linear region appears when $1/\alpha < 100$ μm. The inverse slope of this line predicts a $L_N = 8$ μm, which can be interpreted as the effective minority carrier diffusion length of the silicon film. The data deviates from simple theory as $1/\alpha$ exceeds 100 μm. Higher levels of collection efficiency are recorded than predicted by the simple theory of equation (4). The slope and intercept of this line can reveal detailed properties of the light trapping characteristics [3]. For the device data in **Figure 5**, a Z of approximately nine is indicated (where Z is the optical path length given in multiples of the device thickness). The optical path length of long wavelength light was therefore 1.7 mm for this 190-μm-thick film. The low levels of QE measured at the long wavelengths make the exact evaluation of Z uncertain. The high level of light trapping seen in the QE data implies a high degree of scattering by the back surface reflector. In this case the internal reflection of the front surface is estimated to approach the Lambertian limit of 92%, and the silicon/barrier interface has a reflectivity of approximately 70%. The details of the light-trapping model used to generated these parameters are reviewed in the following section.

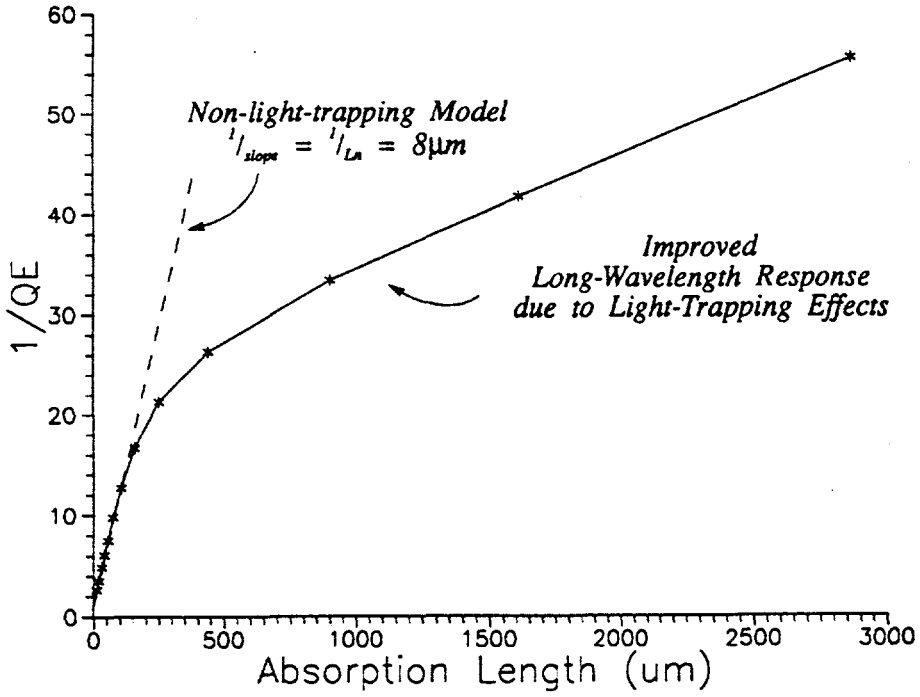


Figure 8. Absorption length versus the inverse of the internal quantum efficiency for the silicon-on-ceramic structure.

3.3.3 Light-Trapping Analysis

A method to identify and quantify light trapping in solar cells has been developed at Sandia and AstroPower [6]. Light-trapping effectiveness depends on the internal reflectivity and texturing of device surfaces. The incorporation of light-trapping features can experimentally be seen in spectral response and reflectance measurements, as well as in the overall light-generated current. Due to the large number of variables that affect light-generated current, an analysis is proposed that evaluates only the optical properties of the structure. The effective optical path length of confined light is proposed as a figure of merit of the optical design. This effective optical path length is shown to be a function of wavelength. Analysis of the nearbandgap light is presented as a monochromatic case with appropriate simplifications. Analyses of thin Silicon-Film solar cells formed on ceramic substrates with and without barriers are presented. Finally, the overall impact of the optical design on the current-generating properties is discussed and an expression for full-spectrum light-trapping effectiveness is defined.

Experimentally, measurements of spectral response and reflectivity are used to evaluate optical properties. Due to the light-trapping nature of the solar cells under evaluation, care must be taken to interpret both measurements correctly. Weakly absorbed light is initially coupled into a device, and after an indeterminate number of internal reflections, is transmitted back out the front surface. This re-emitted light must be distinguished from the light reflected from the front surface initially (R_{FE} vs. R_{ESCAPE} as discussed in Section 3.3.1: Reflection Characteristics). As the reflectance is used to calculate the internal quantum efficiency (IQE), this differentiation must be accounted for in the IQE results. These points are further illustrated in the following section on optical path length.

The following sections describe the nomenclature and theory used to evaluate the extended optical path length found in light-trapping solar cells. Sections 3.3.3c and 3.3.3d review the impact of the derived figures of merit on device current- generating capabilities. Specific theoretical examples are given. Section 3.3.3d also presents a full-spectrum figure of merit, closely related to current-generating properties.

3.3.3a Model for Effective Optical Path Length

The optical properties of a light-trapping structure can be characterized by introducing an effective optical path length factor, $Z(\lambda)$, and an effective optical path length factor for

uniformly absorbed nearbandgap light, Z_o. The following model also utilizes a collection efficiency term $\eta_c(\lambda)$. These terms are defined as:

$Z(\lambda)$: The wavelength-dependent optical path length of light required to generate absorption equal to that found in the device under test. Z is expressed as a multiple of the device thickness.

Z_0: Similar to $Z(\lambda)$, only limited to nearbandgap light that is weakly absorbed. Z_o is also expressed as a multiple of the device thickness. A weakly absorbed photon is one in which the absorption length is much greater than the device thickness ($\alpha W << 1$). Such weakly absorbed photons are uniformly absorbed throughout the device thickness.

$\eta_C(\lambda)$: The collection efficiency of photogenerated carriers. For a well-designed silicon device η_C approaches unity for light in the wavelength range 600-800 nm. For nearbandgap, uniformly absorbed light, η_C approaches a constant value dependent on the recombination properties of the device.

An expression can be derived for $Z(\lambda)$, based on an extension of the model for a non-light-trapping solar cell [3]. For monochromatic light of wavelength λ, the photogenerated current (J_L) from the base of a non-light-trapping solar cell of thickness W is

$$J_L(\lambda) = \eta_c(\lambda) q F(\lambda)\left(1 - R_{TOTAL}(\lambda)\right)\left(1 - e^{-\alpha(\lambda)W}\right) \tag{5}$$

where the incident photon flux density is represented by F, q is the elementary charge, and α is the absorption coefficient. $R_{Total}(\lambda)$ represents the experimentally measured light leaving the front surface (as defined in Section 3.3.1: Reflection Characteristics). The internal quantum efficiency is conventionally defined as

$$IQE(\lambda) = \frac{J_L(\lambda)}{qF(\lambda)\left(1 - R_{TOTAL}(\lambda)\right)} = \eta_c(\lambda)\left(1 - e^{-\alpha(\lambda)W}\right) \tag{6}$$

For a light-trapping structure, the simple front-surface reflection term becomes slightly more complex. An example of the reflection from a light-trapping solar cell [4] was shown in **Figure 6.**

An internal quantum efficiency measurement based on either $R_{Total}(\lambda)$ (defined as IQE) or $R_{Front}(\lambda)$ (defined as IQE_{LT}) can be defined. Equation (6) can be restated for a light-trapping structure using R_{Front} in place of R_{Total}.

$$IQE_{LT}(\lambda) = \frac{J_L(\lambda)}{qF(\lambda)\left(1 - R_{FRONT}(\lambda)\right)} \tag{7}$$

The internal quantum efficiency for a light-trapping solar cell (IQE_{LT}) only considers R_{Front} as light not available for collection. Note that this quantity, $IQE_{LT}(\lambda)$, is **not** the quantity computed from experimental measurements of spectral response and reflectance, because the experimentally measured reflectance is R_{Total}, not R_{Front}. The IQE_{LT} is not directly measurable, as R_{Front} is not measurable in a light-trapping solar cell. R_{Front}, however, can be approximated from the total reflectance data by extrapolating from shorter wavelengths through the escape-reflectance regime (**Figure 6**), making the approximation of IQE_{LT} possible. The relationship between the conventional $IQE(\lambda)$ and $IQE_{LT}(\lambda)$ is

$$IQE(\lambda)_{LT} = IQE(\lambda)\left[\frac{1 - R_{TOTAL}(\lambda)}{1 - R_{FRONT}(\lambda)}\right] \tag{8}$$

To account for the extended path length found in light-trapping structures and the resulting additional absorption of nearbandgap light, the device thickness (W) in equation (6) is replaced by the effective optical path length, $Z(\lambda)W$.

$$IQE_{LT}(\lambda) = \eta_c(\lambda)\left(1 - e^{-\alpha(\lambda)Z(\lambda)W}\right) \tag{9}$$

Solving for $Z(\lambda)$;

$$Z(\lambda) = \frac{-1}{\alpha(\lambda)W}\ln\left[1 - \frac{IQE_{LT}(\lambda)}{\eta_c(\lambda)}\right] \tag{10}$$

Examining equations (10), it can be seen that Z is not directly measurable, because in general $\eta_c(\lambda)$ is not known. The IQE_{LT} is also not directly measurable; however, it can be approximated

as discussed above.

The determination of $\eta_c(\lambda)$ requires knowledge of the ray path angles, internal reflectance, minority carrier diffusion length, and back surface recombination velocity. Simplifications are possible in two regimes: for uniform photogeneration (nearbandgap wavelengths) and when η_c approaches unity.

Experimentally determined values of $Z(\lambda)$ for a light-trapping structure are shown in **Figure 9**. The quantum efficiency for this silicon-on-ceramic device is shown in **Figures 7** and **8**. Values of η_c have been estimated from the analysis of nearbandgap light presented below. The effective optical path length of the AstroPower device begins to saturate at a value approaching Z=7.5. The longest wavelength measurements are subject to experimental error as the IQE reading approaches zero.

For the case of uniformly-absorbed nearbandgap light, simplifying assumptions allow Z_o to be extracted directly from measurable quantities. The optical model, based on experimental assumptions, is presented below.

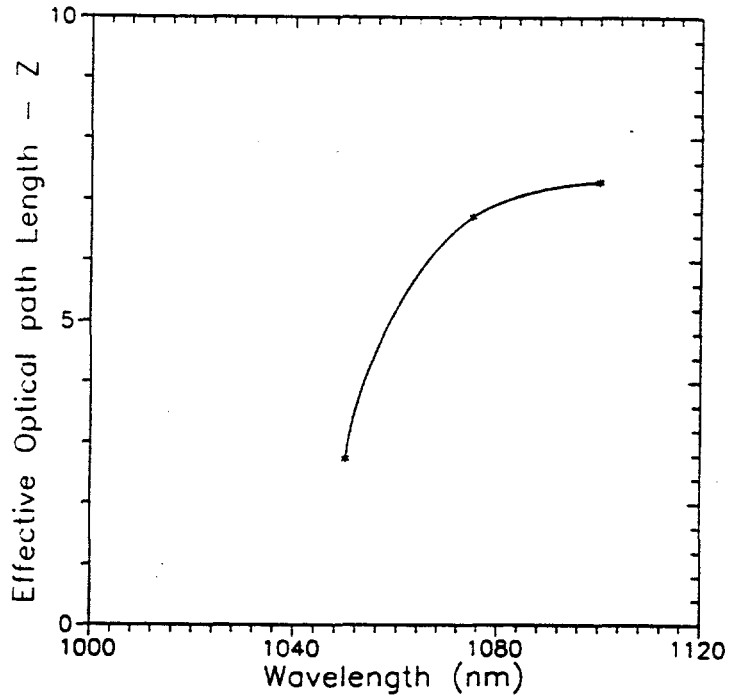


Figure 9. *Z(λ) for an AstroPower silicon-on-ceramic device as derived from equation (10).*

3.3.3b *Modeling for the Nearbandgap Case*

Limiting the analysis of the spectral response and reflectivity to the nearbandgap light, a model-based analysis has been developed at Sandia that determines the effective optical path length (Z_o) based on experimental data. Considering non-absorbed light, an expression for the Z_o can be derived [3,6,7];

$$Z_o = \frac{W_{IQE}}{\eta_c W}\frac{(1-R_{TOTAL})}{(1-R_{FRONT})} \tag{11}$$

where W_{IQE} represents the inverse slope of a IQE^{-1} vs. α^{-1} plot when $\alpha^{-1} >> W/\cos\theta_n$, and η_c is the collection efficiency of photogenerated minority carriers. η_c is related to the y-intercept, $1/\eta'_c$, of the IQE^{-1} vs. α^{-1} curve [8].

$$\eta_c = \eta'_c\left[\frac{1}{2}+\frac{2\rho_B}{(1+\rho_B)^2}\right] \tag{12}$$

where ρ_B is the back-surface reflectance. Making certain assumptions regarding the distribution of confined light within the device [3], a value of ρ_B can be determined, and Z_o can be computed from the other experimentally measured values. For $\rho_B > 0.5$, η_c can be replaced directly with η_c' in equation (11) and accuracy will remain within 5%.

This analysis has been carried out for a Silicon-Film device formed with a metallurgical barrier (**Figure 10**) and a Silicon-Film device formed without a metallurgical barrier (**Figure 11**). For the silicon-on-ceramic device with a barrier, $R_{Total}(\lambda=1200\text{ nm}) = 0.29$, $\rho_B = 0.72$, and $R_{Front} = 0.14$, for the 190-μm-thick silicon layer. The resulting Z_o estimate of 9.1 compares favorably to the $Z(\lambda)$ data shown in **Figure 9** for the same device. Differences in the two methods may be due to inconsistencies in the optical path length in the device as compared to the model.

Data for the silicon-on-ceramic device without a barrier are shown in **Figure 11**. Optical characteristics of the device are $R_{Total}(\lambda=1200\text{ nm}) = 0.21$, $\rho_B = 0.33$, and $R_{Front} = 0.11$, for the 109-μm-thick silicon layer. Due to the low ρ_B in this case, $\eta_c = 0.87\,\eta_c'$. Even with the low back surface reflectivity, a $Z_o = 3.3$ is achieved in the device with no barrier.

This modeling-based approach has the advantage of determining Z_o at much shorter wavelengths than the $Z(\lambda)$ approach presented earlier. Experimental error will therefore be less significant.

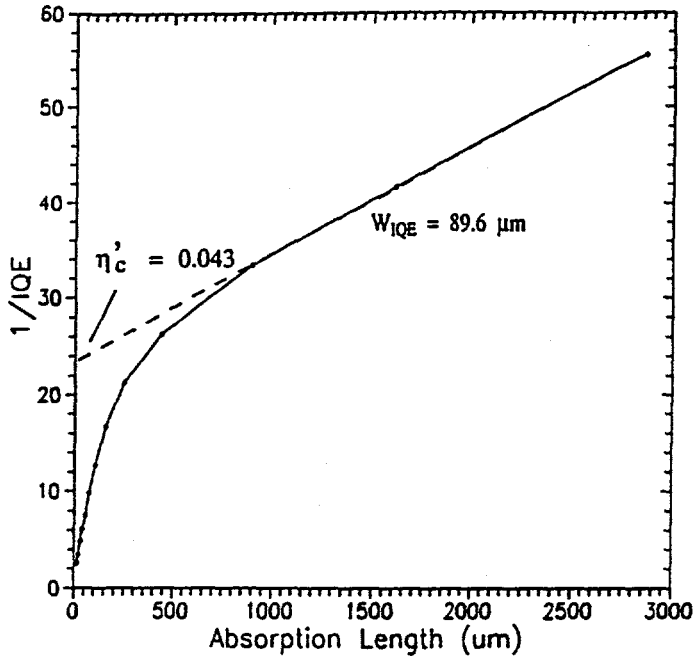


Figure 10. *Analysis of the nearbandgap spectral response of a silicon-on-ceramic device formed with a metallurgical barrier revealing* $\eta_c' = 0.043$ *and* W_{IQE}*=89.6* μ *m, resulting in a* Z_o*=9.1.*

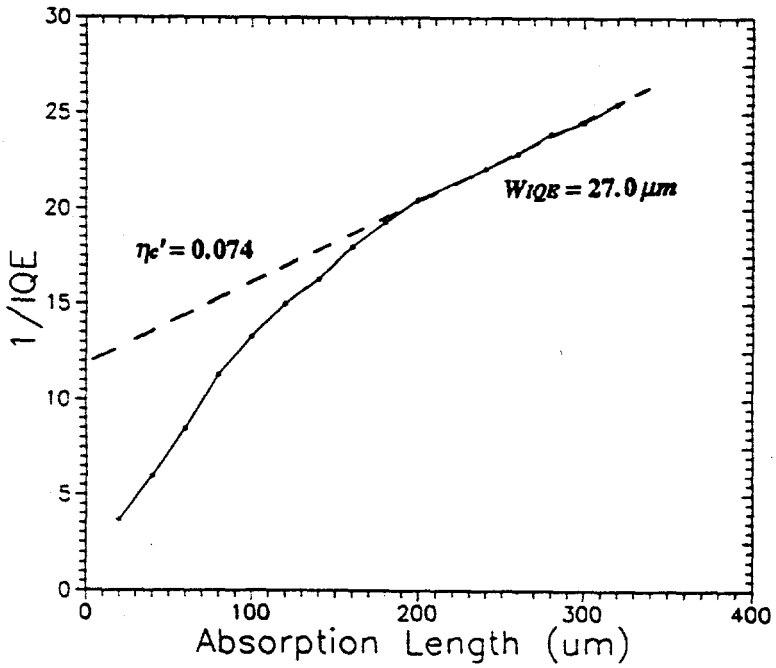


Figure 11. *Analysis of the nearbandgap spectral response of a silicon-on-ceramic device formed without a metallurgical barrier revealing* $\eta_c' = 0.074$ *and* W_{IQE}*= 27.0* μm*, resulting in a* Z_o*= 3.3.*

3.3.3c *Optical Effects on Light-Generated Current*

The purpose of light trapping is to enhance the light-generated current of a photovoltaic device. Although significant light-trapping information can be extracted from the nearbandgap quantum efficiency and reflectivity, the most critical response is in the wavelength range of 800 to 1100 nm (dependent on the thickness of the device). This range is important due to the relatively high solar energy available and the relatively high absorption coefficient. To fully evaluate a light-trapping structure the shape of the $Z(\lambda)$ curve must be analyzed.

To highlight the impact of the shape of the $Z(\lambda)$ curve on J_{sc}, two theoretical examples are given below (**Figure 12**). These devices were chosen to have the same nearbandgap effective optical absorption length. The first example, case (a), is for a device that utilizes a regularly textured back surface. All the light follows the same path, which generates an optical path length 5 times the device thickness (Z=5 for 100% of the light). The second example is a device with a randomly textured back surface that has a poor back surface reflectivity (case (b)). The portion of light that is reflected from the back surface in case (b) travels obliquely through the device, and is modeled as having an optical path length of 20 (Z = 20 for 20% of the light, Z = 1 for 80% of the light, net Z = 5). Such a situation would occur if the back surface reflector was randomly textured, and total internal reflection was the dominant mechanism for optical confinement. Any internally reflected light would therefore have to strike the back surface at an angle of incidence greater than some critical angle (dependent on the indices of the interface materials). This internally reflected light would then be traveling obliquely through the device, making reflection from the front surface probable, for a long effective optical path length.

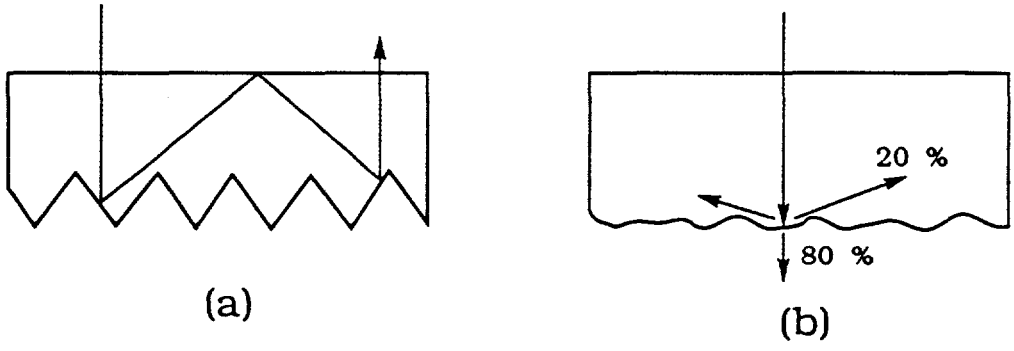


Figure 12. *Two theoretical cases of light-trapping structures that generate similar nearbandgap absorption but differ greatly in current-generating properties. Case (a) confines all the light for an optical path length 5 times the device thickness. Case (b) transmits 80% of the light initially, but retains 20% for an optical path length 20 times the device thickness.*

The light-generated current from these two extreme cases can be calculated using a model that computes the current generated by each subsequent pass of the light [2]. The model assumes no losses to external front-surface reflectivity, and carrier collection is unity ($\eta_c = 1.0$).

The effective optical path-length factors, $Z(\lambda)$, for both structures shown in **Figure 12** have been computed according to equation (10). The results are shown in **Figure 13.** Case (a), where 100% of the light is confined for an optical path length 5 times the thickness, reaches is nearbandgap value of $Z = 5$ at a wavelength of less than 1000 nm. By comparison, case (b) does not reveal significant light-trapping properties until much longer wavelengths. This effect can also be seen in the theoretical J_{SC} values for the two devices under an AM1.5G spectrum. For a device thickness of 100 μm, case (a) generates J_{sc}=40.3 mA/cm^2 (8.3% higher than an equivalent thickness without any light trapping) while case (b) generates 38.3 mA/cm^2 (2.9% higher than non-light-trapping device).

The effect on J_{sc} becomes more pronounced as the device thickness is reduced. For a 35-μm-thick device, the current generated by case (a) is 13.1% higher than the non-light-trapping case, while case (b) is 4.1% higher.

The calculation of $Z(\lambda)$ over the entire wavelength range of interest is possible in this theoretical case because a collection efficiency of unity ($\eta_c = 1.0$) was assumed. A similar calculation can be made for an experimental device if $\eta_c(\lambda)$ is explicitly known or can be accurately estimated over the wavelength range of interest.

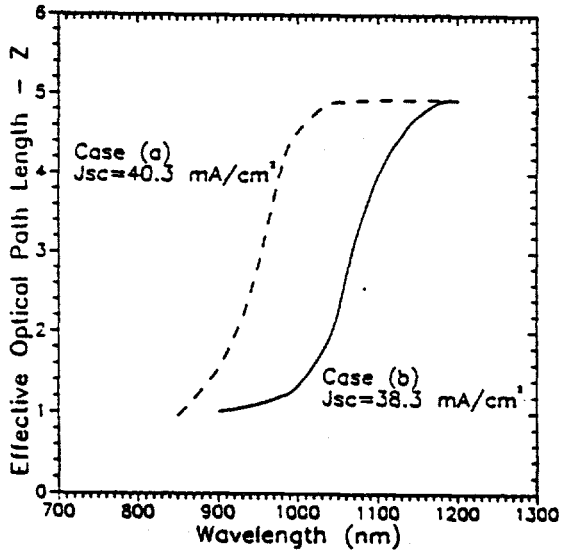


Figure 13. *The theoretical effective optical path length of the two devices portrayed in Figure 12.*

3.3.3d *Full-Spectrum Light-Trapping Effectiveness*

A full-spectrum light-trapping effectiveness term has been developed at Sandia and AstroPower that evaluates Z(λ) and the photon flux density across a given spectrum. A figure of merit is generated that is related to the current-generating capabilities of a device for a given solar spectrum.

The total photon absorption (Γ) for the AM1.5G spectrum can be established from the measured value of J_L and an estimate of η_C to be

$$\Gamma = \int_{AM1.5G} \frac{J_L(\lambda)}{q\eta_c(\lambda)} d\lambda \tag{13}$$

An equivalent determination of the total photon absorption can be modeled utilizing an effective device thickness, W' = Z(AM1.5G)W.

$$\Gamma = \int_{AM1.5G} F(\lambda)\left(1 - R_{FRONT}(\lambda)\right)\left(1 - e^{-\alpha(\lambda)W'}\right) d\lambda \tag{14}$$

Equations (13) and (14) can be equated and rearranged as

$$\int_{AM1.5G} \frac{qF(\lambda)IQE_{LT}(\lambda)}{\eta_c(\lambda)} d\lambda = \int_{AM1.5G} qF(\lambda)\left(1 - e^{-\alpha(\lambda)W'}\right) d\lambda \tag{15}$$

For a given spectrum, the right-hand side of equation (15) represents the total photogenerated current for an absorption thickness W'. **Figure 14** shows photogenerated current (AM1.5G) as a function of absorption thickness, W'. The left hand side of equation (15) can be calculated utilizing spectral response, reflectance data, and an estimate of η_c. Finding the absorption thickness (W') on **Figure 14** that corresponds to this current and dividing by the device thickness will give Z(AM1.5G).

The light-generated currents of the theoretical structures shown in **Figures 12** and **13** can be used directly in this analysis since they were modeled assuming η_c=1.0 and no external front-surface reflection. The Z(AM1.5G) can therefore be calculated to be 5.0 for case (a) and

approximately 1.5 for case (b). This analysis shows that two device structures with the same Z_o can have significantly different current generating properties and full-spectrum light-trapping effectiveness.

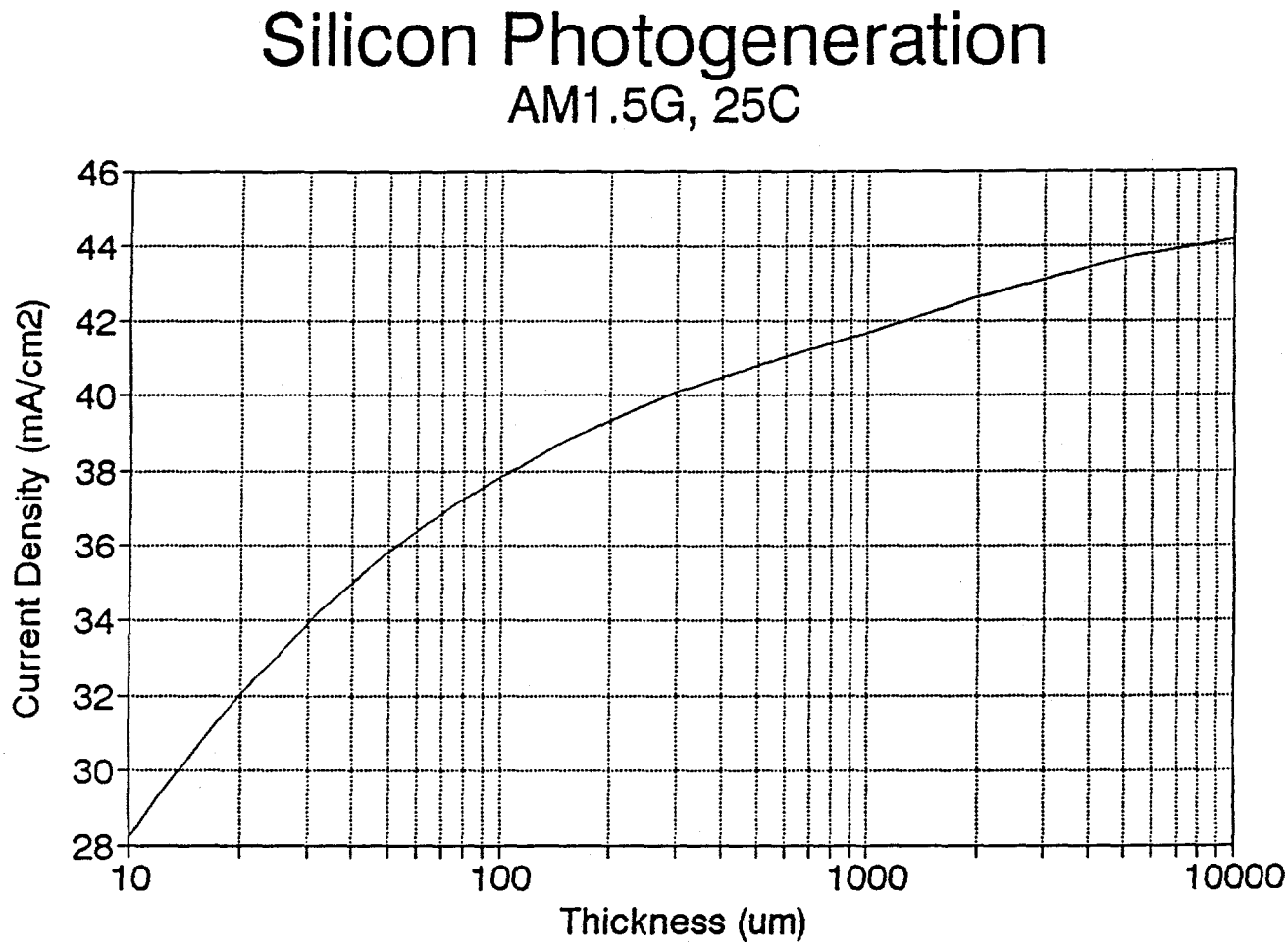


Figure 14. *The photogeneration in silicon for the AM1.5G spectrum at 25°C, as a function of absorption thickness [8].*

4 Solar Cell Device Results

Silicon-Film on ceramic structures have been fabricated into 1.0 cm^2 devices utilizing standard solar-cell processing techniques. The full process sequence is shown in **Table II.**

Table II. *Device Processing Sequence.*

Surface Etch	•	30 second chemical polish etch
Pre-Diffusion Clean	•	Modified RCA clean
Diffusion	•	PH_3 source
	•	840 °C
	•	5 min. pre-deposition
	•	15 min. drive-in
	•	HF strip
P-Type Contact	•	Screen Printed Al paste
	•	880 °C Fire in open-air belt furnace
N-Type Contact	•	Define metallization areas with photoresist
	•	Evaporate Ti/Pd/Ag
	•	Lift-off unwanted metal
	•	Electroplate Ag
Isolation	•	Mask active area with photoresist
	•	Plasma etch 5-8 min.
	•	Photoresist strip
Test	•	AM1.5G

A brief surface etch was used to generate uniform surfaces for all devices fabricated. This etch was not required in all cases. The silicon deposition process generates silicon-on-ceramic structures with very clean, low-defect surfaces, capable of going directly into emitter formation with little change noted in device performance.

In results verified by Sandia, an AM1.5G efficiency of 6.6% was measured. Specific results are shown in **Table III.**

Table III. *Measured I-V Characteristics on 1.0 cm² Silicon-Film Product II.*

	V_{oc} (mV)	J_{sc} (mA/cm²)	FF	η (%)
Sandia Verified Device (9/90)	513	19.3	65.8	6.6

Improvements in device processing, and changes in doping levels, have increased V_{oc} and FF in more recent samples. A V_{oc} of 546 mV and a FF of 70.2 have been measured. Overall J_{sc} values remain low, limited by poor minority-carrier diffusion length (L_N). Values for L_N have been in the range of 5 to 10 μm.

Investigations of the cause of the low minority carrier diffusion length include analysis of stress-induced defects, grain-boundary losses, and impurities. Through the use of test structures and defect etching, stress has been found to play a small role. Defect densities (measured after Secco etching) have been found to be as low as 3×10^5 cm^{-2}. Residual stresses have been low, as no warping or cracking has occurred over the 50 cm² areas presently under development. Grain-boundary recombination effects are also insignificant as columnar grains are formed with aspect ratios exceeding 10. Chemical analysis has shown significant levels of metallic impurities.

Chemical analysis of Silicon-Film samples and silicon feedstock were initially conducted by Sandia National Laboratories. The results indicated that high levels of metallic impurities were present in both the silicon feedstock and grown Silicon-Film layers. Levels of iron and chromium were found in the 10 ppm level. This compares poorly to the concentration level that causes 10% degradation in single-crystal cells (0.01 ppm for Fe). The measured concentration levels could easily explain the poor recombination properties of the material. Measurements were made by inductively coupled plasma mass spectrometry (ICP-MS).

The discovery of metallic impurities initiated a materials and processing investigation to understand contamination sources. A second silicon vendor was found. All process steps were closely scrutinized. Chemical analysis by neutron activation was utilized to help in determining impurity sources and highlighting problem process steps. The new feedstock and improved handling was successful in lowering metallic impurity levels to the detection limit of the neutron activation analysis (approximately 1 ppm). Although improved, Fe could still be present in levels high enough to significantly impact device results.

The incorporation of high levels of oxygen was investigated as a cause of the poor minority-carrier recombination properties. To investigate the effects of oxygen, test structures were fabricated with oxygen-rich CZ single-crystal wafers and oxygen-deficient float-zone (FZ) single-crystal wafers. The test structures were put through the same thermal sequence as Silicon-Film samples receive during growth and device processing. The results indicated that both FZ and CZ reacted similarly, indicating that the thermal sequence used does not activate oxygen impurities. This data agrees with earlier experiments performed with silicon-on-ceramic samples. Silicon-Film samples were heat treated in a fashion to minimize the formation of oxygen precipitates, while similar samples were heat treated to maximize precipitate formation. Devices formed on the heat treated samples remained similar to controls that saw neither heat treatment. It was therefore concluded that oxygen was not presently limiting device performance.

Samples of Silicon-Film on ceramic have been evaluated by Secco etching. Levels of defects are compared to Silicon-Film Product I structures that were run through the Product II processing equipment. Before defect etching, mesa devices were formed, and minority carrier diffusion length measured. The results are shown in **Table IV.**

Table IV. *Defect density measured on Silicon-Film Products.*

	L_N	Defect Density
Product I Sample	31-56 μm	2-10 x 10^5 cm^{-2}
Product II Sample	< 5 μm	8 x 10^5 cm^{-2}

For the Product II structure the majority of defects were clustered near the grain boundaries. Intra-grain regions of the Product II device look as good, or better, than the corresponding Product I sample. Product II aspect ratios continue to be large, with grain sizes in excess of 500 μm. Recombination at the grain boundaries alone can not be driving the poor Product II diffusion length. The large disparity in L_N between the two samples is a continuing area of investigation, highlighting sources of impurities. Differences between the Product I and II processes include silicon deposition techniques and the presence of the metallurgical barrier.

5 Conclusion

The Silicon-Film on ceramic structure has been designed to generate high efficiency utilizing imperfect materials. This design involves thin silicon layers in light-trapping structures. Excellent optical characteristics have been measured, with silicon/barrier back surface reflectivities of 70%, and optical path lengths nine times the device thickness. Device efficiency has been limited to 6.6% in 1.0 cm^2 devices by low minority-carrier diffusion lengths. Impurities have been identified as the leading cause of the poor recombination characteristics. Actions are being taken to identify and control the contamination sources.

Conductive ceramic substrates have been developed at AstroPower with resistivities of approximately 10 Ωcm. This ceramic was found to be easily contacted with screen printed metal pastes. Contact resistance is slightly higher than required for optimal device operation and further development of firing conditions is needed.

A method to identify and quantify light trapping in solar cells has been presented. The results indicate that a wavelength-dependent figure of merit, describing light absorption, can be generated. This figure of merit is the effective optical path length of weakly absorbed light. A limiting case of the optical path length can be found through a modeling-based analysis of the nearbandgap light. The wavelength-dependent optical path length can also be analyzed to generate a full-spectrum light-trapping effectiveness term for a given solar spectrum. This full-spectrum effectiveness is closely related to the device's current-generating capabilities.

The test results of two experimental light-trapping devices were analyzed. The analysis of the experimental devices, and specific theoretical test cases, reveal that accurate analysis of the current-generating properties of specific devices requires careful examination of light trapping properties as a function of wavelength. Results indicate that the back surface reflectivity plays a critical role in the current-generating properties of light-trapping solar cells.

6 References

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