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A High Performance Multi-Channel Preamplifier ASIC

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Abstract

A new preamplifier ASIC has been designed and built to improve performance of the VTPC (Vertex Time Projection Chamber) at Fermilab's Colliding Detector Facility. Design of the semicustom IC was completed using a Tektronix QuickChip 2S bipolar linear array. The ASIC has 6 channels on a chip and provides lower noise, higher gain, lower power, and lower mass packaging than the device which it replaces. Actual performance of the preamplifier was found to match very closely the simulated performance. To reduce the mass of the complete circuit board, bare IC dice were mounted directly on a G-10 substrate using COB (chip on board) techniques. The preamplifier and packaging should be applicable to numerous other systems.

I. INTRODUCTION

The Colliding Detector Facility at Fermilab originally contained an 8 module Vertex Time Projection Chamber with 2 planes of wires per module. The original front end electronics, which included preamplifier cards and amplifier-shaper-discriminator boards was described at the 1985 Nuclear Science Symposium [1]. After several years of operation, an upgraded version of the VTPC now called the VTX wire chamber is being installed. The VTX chamber has 28 modules with again 2 planes of wires per module.

The electronics originally designed for the VTPC required several improvements. Although some changes were made to the amplifier-shaper-discriminator board, most of the required changes related to the preamplifier. The major preamplifier requirements which were addressed were 1) higher gain so that the wire chamber could be run at a lower voltage and have greater lifetime, 2) significantly lower power to reduce the heat load and improve dimensional stability of the detector, 3) lower noise at a given input capacitance to improve the signal-to-noise ratio, and 4) lower mass to reduce the effect of secondary interactions with the preamplifier board which is mounted deep within the detector. To meet the requirements a new preamplifier ASIC was designed to replace the commercially available Fujitsu MB43458.

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The new preamplifier, which is called the VTX preamplifier, had to be designed, fabricated, assembled onto circuit boards, and be available for installation within a one year time span. After studying all the requirements, a decision was made to implement the design using a Tektronix QuickChip linear array. The linear array design tools and experience using the tools were already in place at Fermilab. It was felt that this approach would meet all the requirements and have a high chance of success in the allotted time span. After further review, the QuickChip 2S linear array was chosen for the design.

II. CIRCUIT DESCRIPTION

The QuickChip 2S linear array is characterized by NPN transistors with an fT of about 6 GHz. Initially the preamplifier ASIC was designed with 4 channels. After careful review of the final design, it was found that 6 channels could be placed on the die instead of the planned 4 channels. The increased silicon utilization resulted in a reduction in cost per channel.

A. Operation

The VTX preamplifier is comprised of 3 stages. The well known common emitter transimpedance feedback amplifier is the topology chosen for the input amplifier, since this allows low supply voltage and has been proven to give good results in previous QuickChip designs. However, a one stage amplifier in this technology will not provide the desired gain and impulse response. Therefore a multistage design was pursued. Since high frequency PNP transistors are not available in QuickChips, the natural output pulse polarity is positive. This allows large dynamic range for relatively small output standing current in an NPN output driver. In order to provide positive output pulse polarity with a negative input current pulse, three inverting feedback stages are required. A three stage configuration naturally suggests that the second stage be a shaping stage which also provides the required additional gain, with the third stage functioning as an output driver. Using a feedback stage for the output driver has the advantage that its output impedance is quite low, even for relatively low driver standing current. This assures good linearity.

One important issue in a multistage design is the coupling method. For DC coupling, which is desirable, offsets and drifts can be a problem. For this reason, all three amplifier stages were designed using a very similar common emitter configuration. The DC quiescent operating points of all stages are then approximately equal, and tend to track with process variations and over temperature. This assures a relatively stable operating point.

A single channel schematic is shown in Figure 1, indicating the various stages. An "E15" is the smallest

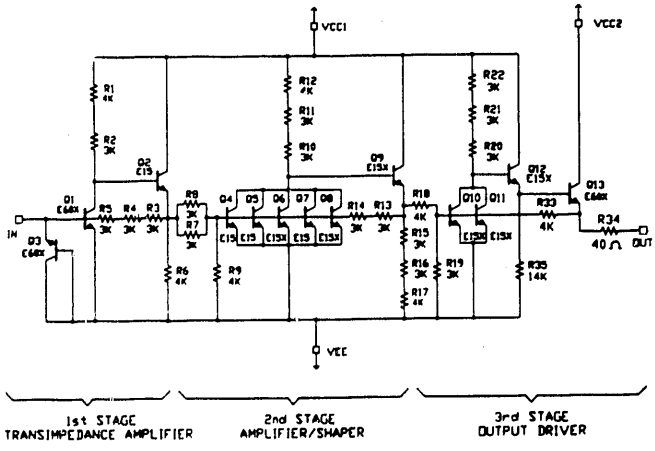


Figure 1 - Single channel schematic of the VTX preamplifier

transistor available, and has an emitter length of 15 microns, and width of 2 microns. An "E60" has four times the emitter area. The input transistor of the first stage, Q1, is an E60 in order to minimize noise due to the base resistance. Since power dissipation is an important constraint, the collector resistance, R1-2, is set to give a collector current of approximately 0.35 ma. A dominant open loop pole is formed at the input (at about 0.9 MHz) due to the sum of the detector capacitance, the Q1 Miller capacitance, and the effective open loop input resistance. For detector capacitances of 5 pf to 15 pf, the Miller capacitance dominates. This configuration has the desirable feature that the amplifier response is not very sensitive to variations in detector capacitance. A second pole is formed at the collector node, from the Cμ of Q1 and the effective collector resistance. A dominant closed loop pole exists for the first stage which depends on the gain bandwidth and the value of the feedback resistor, R3-5. The resistor value is chosen to put the dominant pole at approximately 25 MHz. This sets the impulse response fall time to a reasonable value, and allows sufficient phase margin, since the second pole is at about 60 MHz. In reality, there is some interaction between the poles so that the closed loop poles are not real, but they can be fairly well approximated by two real poles, one at 25 MHz, and one at 60 MHz. The simulated impulse response of the first stage is shown in Figure 2 (-40 fc input, Cin =15 pf).

The second stage is of similar configuration. The addition of resistance R7-8 to the input node converts the transimpedance feedback amplifier to a voltage amplifier. The

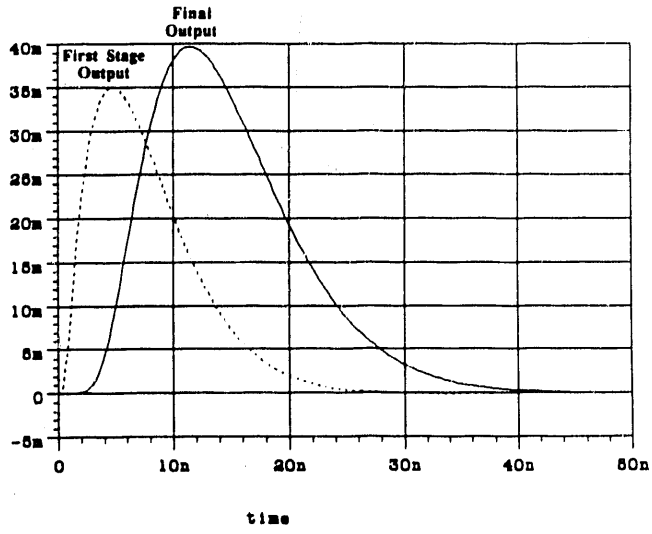


Figure 2 - Simulated first stage and output stage VTX response

collector resistance, R10-12, is higher than in the first stage in order to minimize power dissipation. The dominant pole of this stage, used for shaping, is controlled by the Miller capacitance of Q4-8, and the effective input resistance at the base. The transistor size is adjusted by paralleling identical devices in order to place the closed loop dominant pole at approximately the same value as the first stage dominant pole (30 MHz). The closed loop gain is set to boost the impulse gain at the second stage output to approximately 2 mv/fc. Since the pulse polarity is negative at this point, the dynamic range is limited by the second stage output DC operating point. As the pulse gets larger, the emitter foilower, Q9, begins to run out of current. A simple but effective way to increase the output range in the negative direction is to supply a DC offset current at the input, provided by R9. This biases the second stage output at about 1.5V instead of 0.8V.

The third stage, an inverting driver, is again of similar configuration. A large geometry output driver, Q13, can draw large currents and necessitates the use of a pre-buffer, Q12. Also, a separate pad is dedicated for the output buffer supply, VCC2, to avoid power supply coupling to previous stages. An input offset resistor, R19, is used to cancel out the intentionally introduced offset from the second stage output, so that the final output has plenty of range in the positive direction. The output standing current of Q13 is set by the user with an external pulldown resistor, and is nominally 1 ma for VTX, to allow some dynamic range in the negative direction.

A series back termination is used to drive the output cable. This termination is made from a custom nichrome resistor. Addition of nichrome resistors to the chip entails some extra cost, but flexibility and accuracy are gained. Nichrome resistors can be laser trimmed for exceptional accuracy, but this is costly, especially for small runs. Even without trimming, the resistance tolerance of nichrome is better than the other available QuickChip resistors, and in addition, any

reasonable nominal resistance value can be designed with ease. Therefore, a fixed nichrome resistor was designed to place the nominal output resistance at 43 ohms, to match the cable used. The addition of a series termination reduces the impulse gain by a factor of two, to about 1 mv/fc. The output impulse response (simulated) with a capacitively coupled 43 ohm termination is shown in Figure 2. Since large value resistors are in limited supply, R35, the pulldown resistor for Q12, is also made from nichrome. This allows a large value to keep power dissipation low.

B. Performance

One of the reasons for designing the amplifier with QuickChip is the excellent simulation accuracy, proven by past experience. An actual measured amplifier response for an input impulse of -40 fc (Cin = 15 pf) is shown in Figure 3.

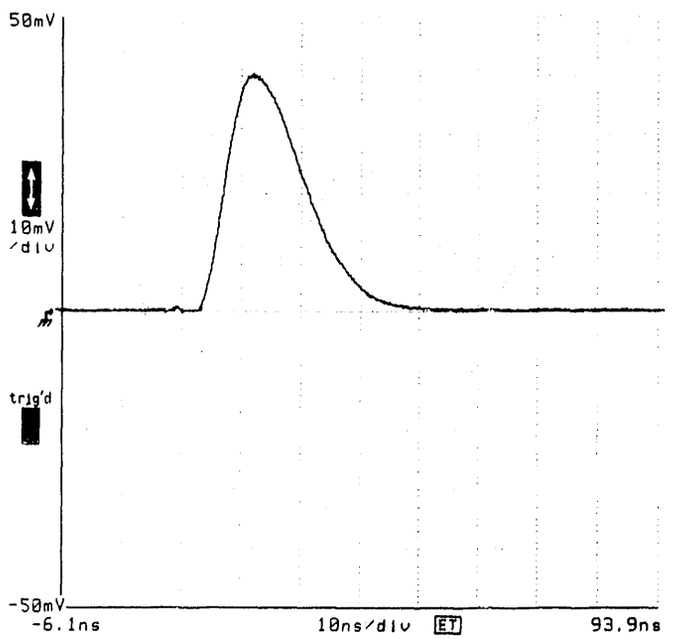


Figure 3 - Measured VTX preamplifier response to a 40 fc input signal.

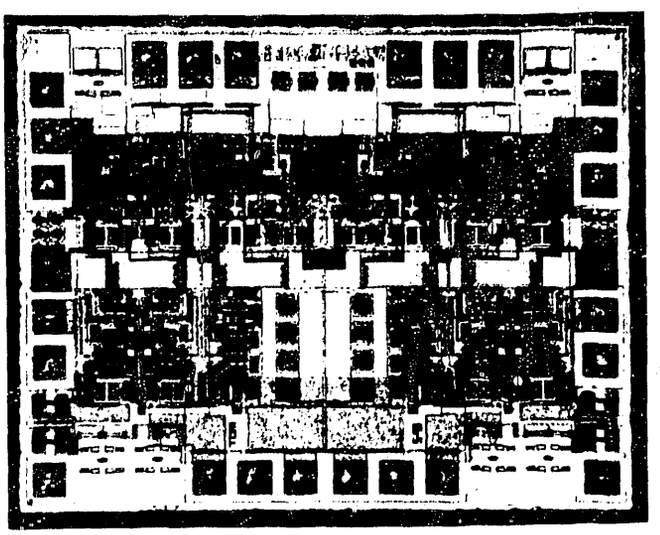
It is virtually indistinguishable from the design simulation result in Figure 2, again proving the accuracy of the models and the tight process control. Specifications and measured performance are as follows:

Preamplifier type: Single ended common emitter, three stage inverting
Channels/chip: 6 (independently powered sections of 4 and 2 channels)
Power supply: 4V
Inputs: One signal and one ground per channel
Quiescent input voltage: 0.7V
Input impedance: 130 ohms
Outputs: One per channel, single ended. External pulldown to negative voltage required.
Quiescent output voltage: 1.0V
Output impedance: 43 ohms
Impulse gain: 1.0 mv/fc (with a capacitively coupled 43 ohm load)
Impulse risetime (10-90%): 5 ns
Impulse falltime (90-10%): 16 ns
Dynamic range: -400 fc to +20 fc inputs, linear to within 3% at the maximum output (1 ma output pulldown current)
Power dissipation: 10 mw/channel (1 ma output pulldown current)
Input noise: 860 electrons + 47 e/pf (100 MHz bandwidth)
Crosstalk: <0.5% between any two channels

All measurements were very close to simulation results.

C. Layout and Packaging

The layout of the VTX chip was done with system issues in mind. The previously used MB43458 preamplifier had one channel in each "corner" of the chip. A much better configuration is to place all inputs along the "bottom" edge of the chip, all outputs along the "top", and power supply connections on the sides (which get bussed across the chip).



Pin	Function	Pin	Function
1	Ch 2 Input	13	VCC1 (Ch2-5)
2	Ch2 Gnd	14	Ch 6 Out
3	Ch 3 Input	15	Ch 5 Out
4	Ch 3 Gnd	16	Ch 4 Out
5	Ch 4 Gnd	17	Ch 3 Out
6	Ch 4 Input	18	Ch 2 Out
7	Ch 5 Gnd	19	Ch 1 Out
8	Ch 5 Input	20	VCC1 (Ch 2-5)
9	Ch 6 Input	21	VCC1 (Ch 1&6)
10	Ch 6 Gnd	22	VCC@ (Output collectors)
11	VCC2 (Output collectors)	23	Ch1 Gnd
12	VCC1 (Ch 1&6)	24	Ch1 In

Figure 4 - VTX die photo (0.08" x 0.10)". Pin 1 is in the lower left hand corner with pins numbered counter clockwise.

This facilitates efficient PC board layout and minimizes output to input coupling. The QuickChip 2S by good fortune has its pads and components arranged in a way that is very conducive to this type of multichannel preamplifier layout. A picture of the die is shown in Figure 4, with pad assignments. A separate ground pad is used for each channel to minimize common impedance coupling. Power connections exist on both sides, and can be connected on one side only if desired. VCC2, the output driver supply, is common to all six channels. VCC1 is split in order to separately power a group of four and a group of two channels. If VCC1 is not connected for a group of channels, those channels dissipate no power. Therefore, this chip can be configured as a two, four, or six channel amplifier. The power connections can all be bonded to the same power source on the PC board, as close as possible to a bypass capacitor. For maximum performance, lead parasitics should be as small as possible. Direct chip on board mounting is one way to minimize parasitics. Since the total mass is also kept small with this method, it represents a natural solution. Channel pitch is then essentially limited only by the width of the discrete surface mount components on the board. The signals flow linearly from one side of the board to the other. Power is routed under the chips in an inner layer.

Chips are assembled onto 16- and 24-channel boards. A 24-channel circuit board is shown in Figure 5. The additional passive components shown are for capacitive input coupling, input protection, and power supply bypassing. Also, separate MMAD1103 diode packages are placed directly on the wire chamber for additional preamp input protection.

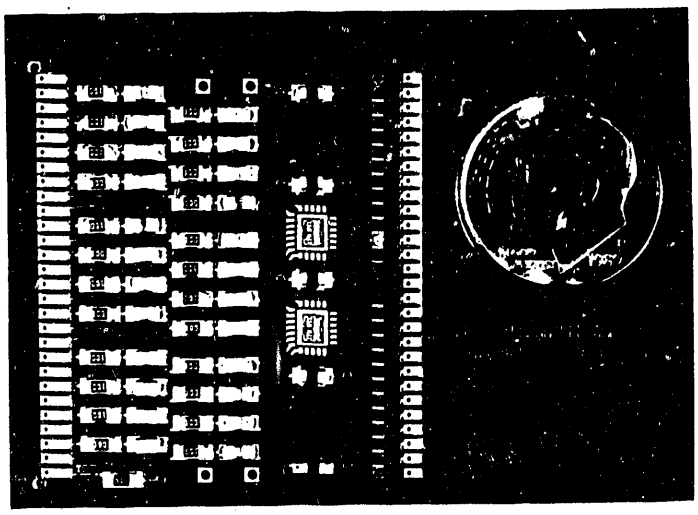


Figure 5 - Twenty-four channel VTX preamplifier card with 2 dice uncoated to show wire bond area.

III. CIRCUIT PRODUCTION

A. Prototypes

Prior to the design of the VTX preamplifier ASIC, several other ASIC's had been designed with excellent results using Tektronix QuickChip linear arrays. There are two reasons for the prior successes. First, there was good correlation between simulations and actual performance for these chips due in large part to the excellent models provided by Tektronix. Second, with each design, there was an independent review of the design at Tektronix by Tektronix personnel.

Based on previous experience and the short time schedule, a contract was let to Tektronix to fabricate all of the required chips without the benefit of a separate prototype run. Success on the first try would save money in the long run. When the ASIC's were received, they were found to perform as expected and all of the devices were immediately shipped to a vendor for board assembly.

B. Costs

The VTX preamplifiers were fabricated on 4 inch wafers with 1200 dice per wafer with an estimated yield of 75% for 900 parts or 5400 channels per wafer. Since the VTX wire chamber required about 10000 channels including spares, 3 wafers were ordered.

Design of the VTX preamplifier utilized a nichrome layer for fabrication of precision resistors which added some cost to the production. Setup and production of the first wafer was $36K including $4K for the nichrome layer. Each additional wafer was about $9K (including nichrome). If additional wafers had been fabricated, the cost per wafer would have decreased dramatically. Testing of all the channels cost an additional $11K. There were no packaging costs since the chips were received as bare dice for chip on board attachment. The foundry run at Tektronix yielded 2714 good chips. Thus, the cost for the bare dice is about $4 per channel.

An outside vendor wire bonded the bare chips and attached the other surface mount components on a thin G-10 multilayer substrate. Over 700 completely functional circuit boards were fabricated. Substrate, miscellaneous parts, assembly, encapsulation, and testing added about another $1.90 to the cost per channel.

C. Circuit Tester

Since the circuit board substrate is so thin and small, a circuit tester was developed which greatly simplified checking the circuits and more importantly enhanced the production yield of the circuits during fabrication. The circuit board substrate was designed with testing in mind just as the chip pin out was designed with the circuit board layout in mind. The chip design, board design, and tester design were all considered at the same time.

The circuit tester was designed to accommodate both the 16 and 24 channel versions of the preamplifier board. The circuit board is placed on a fixture as shown in Figure 6 and clamped in place. When installed on the detector, connections to the circuit are normally made to both the top and bottom of the board. However, the circuit board is designed so that for testing purposes all connections can also be made only to the bottom of the board. Thus all input, output, and power

connections are made to the bottom of the circuit board via conductive elastomeric material. Actual testing of the circuits is done by sequentially injecting charge into each channel from a pulser via a coax cable and examining the output impulse response. At Fermilab, this testing is automated using a Macintosh computer and Labview software package. At the assembly house, the testing is done by manually routing pulses to the test fixture and examining the output pulses on an oscilloscope.

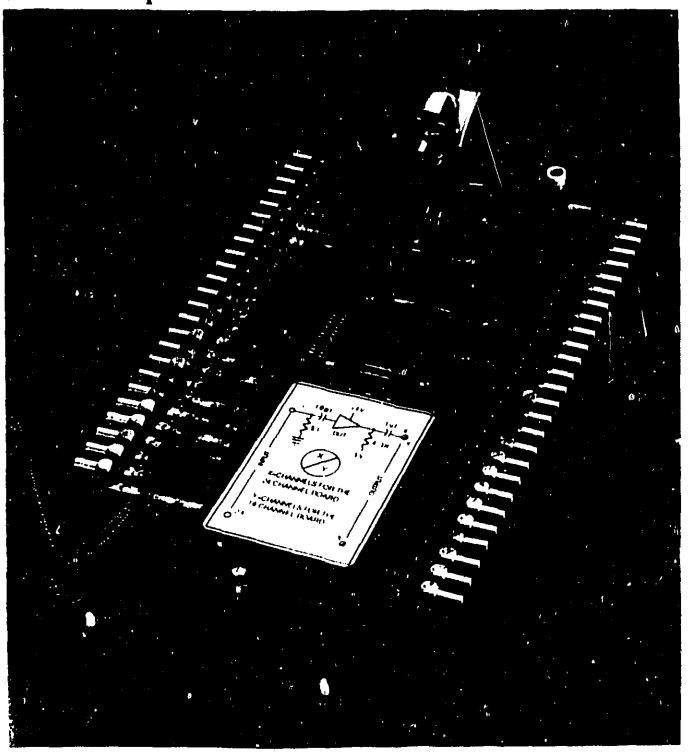


Figure 6 - VTX preamplifier circuit board tester with latch open to show circuit card.

Testing at the assembly house is important. After the bare dice and other surface mount components are attached to the substrate, the board is tested. If any bad dice are found, they are replaced and the board is retested before coating the dice. Once the dice have been coated, replacement is no longer possible. The boards are tested again after coating at the vendor before shipping. The boards are retested at Fermilab and a hard copy of the test results is filed for future reference. Upon testing at Fermilab, 99% of the boards were found completely good. The few other boards typically had one bad or marginal channel.

IV. PREAMPLIFIER INSTALLATION

The VTX wire chamber is cylindrical in shape with a length of about 95 inches and an active diameter of about 17 inches. The chamber is comprised of 28 modules, each with 2 planes of wires, thus providing 56 proportional wire chambers. The wires in each plane are strung in an octagonal pattern.

To minimize preamplifier input capacitance and thus system noise, the preamplifier cards are mounted directly on the outside of the chamber, as close to the wires as possible. The completed assembly uses 288 sixteen channel cards and 160 twenty-four channel cards. Figure 7 shows a section of the detector with the preamplifier cards mounted on the surface of the detector.

Large sections of the detector and associated preamplifier cards have been operated without a problem. No problems such as system oscillation are expected in the completed installation.

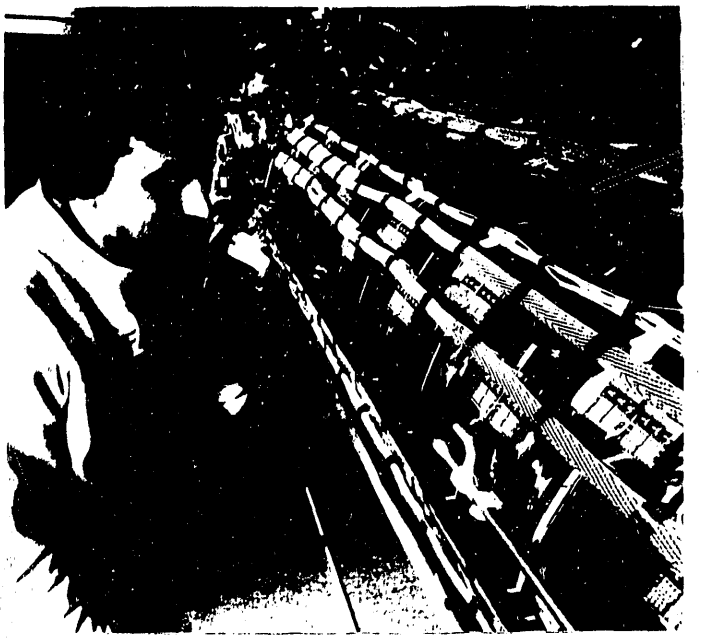


Figure 7 - VTX preamplifier boards mounted on the outside of the VTX wire chamber.

V. SUMMARY

A new 6 channel preamplifier ASIC has been designed for use on a new VTPC at Fermilab's Colliding Detector Facility. The new device, called the VTX preamp, has substantially lower power, lower noise, and higher gain than the commercially available device which it replaces. In addition, COB assembly techniques were used to significantly reduce the mass of the overall assembly. The VTX preamplifier chip and the assembly technique used should be useful in numerous other applications.

VI. REFERENCES

[1] R. J. Yarema, et. al., "A Surface Mount Amplifier-Shaper-Discriminator and Preamplifier for the CDF Tracking Chambers,"IEEE Transactions on Nuclear Science, Vol. 33, pp. 933-936, February 1986.

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