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Logistics for the Implementation of Lead-Free Solders on Electronic Assemblies[1]

Paul T. Vianco

Center for Solder Science and Technology
Sandia National Laboratories
Albuquerque, NM 87185

Iris Artaki

AT&T Bell Laboratories
Engineering Research Center
Princeton, NJ 08540

ABSTRACT

The prospects of legislative and regulatory action aimed at taxing, restricting or banning lead-bearing materials from manufactured products has prompted the electronics community to examine the implementation of lead-free solders to replace currently used lead-containing alloys in the manufacture of electronic devices and assemblies. The logistics for changing the well established "tin-lead solder technology" require not only the selection of new compositions but also the qualification of different surface finishes and manufacturing processes. The meniscometer/wetting balance technique was used to evaluate the wettability of several candidate lead-free solders as well as to establish windows on processing parameters so as to facilitate prototype manufacturing. Electroplated and electroless 100Sn coatings, as well as organic preservatives, were also examined as potential alternative finishes for device leads and terminations as well as circuit board conductor surfaces to replace traditional tin-lead layers. AT&T and Sandia National Laboratories has implemented a program to qualify the manufacturing feasibility of surface mount prototype circuit boards using several commercial lead-free solders by infrared reflow technology.

put SNL first, you're the 1st author

have

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I. Introduction

Soldering continues to be a critical technology in the assembly of both military and consumer electronic products. The high volume manufacturing processes used to fabricate increasingly smaller electronic hardware (including the computer chips themselves) have been developed for use with tin-lead solders. However, lead, which is a principal component of electronic-grade solders, poses a hazard to human health as well as to wildlife and the environment. Efforts to restrict the use of lead in manufactured products, through either legislation or taxation, will force the electronics community to investigate alternative solders to replace tin-lead alloys. The prospect of having to significantly alter or replace well established manufacturing technology such as soldering with lead-containing materials, must be confronted with sound engineering alternatives if the multibillion dollar a year electronics industry is to come through this dilemma without major economic or technological setbacks.

The logistics for implementing alternative, lead-free solders into electronic products, given the vast array of reliability requirements and cost constraints, require (1) optimization of the solder material properties to meet reliability specifications and (2) the development of manufacturing processes which can accommodate the new materials. Although the implementation of advanced soldering processes and equipment should be encouraged, it is also critical that alternative solders be adaptable to present-day assembly technologies in order to avoid the capital expenditures for alternative equipment which may economically cripple many smaller companies.

Through support from the Department of Energy's Environmentally Conscious Manufacturing Program, an effort has been underway at the Center for Solder Science and Technology, Sandia National Laboratories (Albuquerque, NM) to study the implementation of currently available, lead-free solders on printed wiring board assemblies. This effort includes fundamental wetting and intermetallic compound growth studies as well as assembly process development (automated as well as hand soldering). A principal part of the assembly process investigation involves a collaborative effort between AT&T/Engineering Research Center (Princeton, NJ) and Sandia to prototype surface mount circuit boards with presently existing, lead-free solders (both off-the-shelf and new commercial materials). Infrared

reflow was targeted as the automated assembly technology for prototype development. Issues such as device lead and termination finishes as well as circuit board conductor coatings and solder paste properties have been addressed as part of this investigation.

II. Experimental Analyses and Discussion

A. Engineering Research to Support Prototype Processing - Wettability Studies.

The manufacturing of prototype products using new solder alloys requires the determination of numerous process parameters and material specifications. Material specifications include candidate solders, fluxes, and substrate finishes. Process parameters include solder and flux application techniques, reflow temperatures and atmospheres, as well as cleaning methodologies. Narrowing the selection of even a few of these factors through laboratory tests can greatly reduce the cost and time requirements for prototyping.

The *wettability* between a molten solder and a substrate material is a critical property towards determining the manufacturability of an electronic product. Wettability of a particular solder-substrate-flux system is assessed quantitatively through the contact angle, θ_c, of the solder meniscus formed on a vertically oriented, base material surface (Fig. 1). The value of θ_c is based upon an equilibrium between the three surface tensions as expressed through Young's equation:

$$\gamma_{SF} - \gamma_{SL} = \gamma_{LF}\cos\theta_c$$

where:

γ_{SF} is the *substrate-flux* interfacial tension which depends upon the cleanliness of the substrate surface,

γ_{SL} is the *substrate-liquid (solder)* interfacial tension which is a parameter intrinsic to the metallurgical reaction at the solder/substrate interface,

γ_{LF} is the *liquid (solder)-flux* interfacial tension and is a function of the chemistries of the flux and solder.

Wettability is optimized by minimizing the value of θ_c. Under manufacturing process control, this goal is achieved by providing a substrate surface free of oxides and organic contamination (which promote a large value of γ_{SF}) and through the selection of a flux which will lower the value of γ_{LF}. The substrate-liquid (solder) interfacial tension is an inherent property of the solder and substrate materials and is largely unaffected by cleaning or process techniques.

The value of the contact angle is measured by the meniscometer-wetting balance technique[1]. In this procedure, the meniscus height, **H**, and the meniscus weight, **W**, are measured experimentally. The value of θ_c is calculated through the following equation:

$$\theta_c = \sin^{-1}\left\{[4W^2-(\rho g P H^2)^2] / [4W^2-(\rho g P H^2)^2]\right\}$$

where:

ρ is the solder density,

g is the acceleration due to gravity (980 cm/sec^2),

P is the sample perimeter.

These experiments will also determine the value of γ_{LF} through the following expression:

$$\gamma_{LF} = (\rho g/4)\left\{[4W^2/(\rho g P H)^2] + H^2\right\}$$

where all of the symbols are previously defined. From Young's equation, the difference $\gamma_{SF} - \gamma_{SL}$ can then be calculated.

Use of the contact angle to assess wettability is demonstrated by the data in Table 1 in which the values of θ_c, γ_{LF} , and $\gamma_{SF} - \gamma_{SL}$ were calculated with the use of a rosin-based flux (R), a mildly-activated, rosin-based flux

(RMA), and in several cases, a water soluble, organic acid flux (OA). Contact angle data for 60Sn-40Pb are also included as the control condition. It is apparent that, although 60Sn-40Pb was the best performing alloy with contact angles considered "very good to excellent", the lead-free solders demonstrated "good to very good" contact angles, causing them to be considered as viable alternatives to the lead-containing alloys. The higher contact angles of the lead-free solders are due largely to higher values of γ_{LF} caused the absence of lead in the compositions.

The wettability tests also provide preliminary indications of the effects of process parameters on the performance of new solders. For example, shown in Table 2 are the contact angle values for the 50Sn-50In alloy as a function of solder temperature. Working temperatures are typically set at 40°C above the respective liquidus temperature. It is apparent that the wettability of the 50Sn-50In solder improved by increasing the temperature higher than the 40°C guideline. This trend suggested that the higher temperatures more effectively activated the flux. Therefore, the advantage of less heat damage to components anticipated by the use of solders with lower melting temperatures (and hence, lower working temperatures) may not be fully realized due to poor solderability. Moreover, these data indicate that at the prototype stage of process development, currently available flux technology will require the use of solder temperatures greater than the traditional 40°C margin.

A similar analysis was made of the tin-silver and tin-antimony alloys. It was hypothesized that the higher contact angles of the tin-rich, lead-free solder may have been caused by re-oxidation of the substrate surface due to the high working temperatures of these alloys. Therefore, wettability tests were conducted to examine the dependence of θ_c on the solder temperature. Data for 95Sn-5Sb shown in Table 2 demonstrate that wettability was not significantly changed, or deteriorated slightly, at the lower soldering temperatures. Therefore, lower operating temperatures did not improve the wetting performance of this alloy (nor the 96.5Sn-3.5Ag alloy). However, these date did illustrate that a processing margin exists whereby slightly lower temperatures can be used to decrease heat damage to the circuit board laminate, yet maintain the same level of wettability.

← this sounds a little awkward

In summary, it has been illustrated that the meniscometer/wetting balance technique is a valuable technique to assess the wettability of lead-

free solders as potential replacements to the traditional tin-lead alloys. Also, this evaluation provides a preliminary examination of the effects of process parameters on the wetting performance of solder alloys.

B. Prototype Test Vehicles - Lead Finishes.

The manufacturability of the electronic assembly depends upon not only the wettability properties of the solder (note the previous section) but also upon finishes on the devices and circuit boards. Surface finishes on device terminations or leads as well as circuit board lands and traces are used to protect the solderability of the conductor feature prior to the solder attachment of devices. The traditional coatings have been eutectic or near-eutectic tin-lead solders. These finishes are applied by electroplating or by immersing the part in molten solder. However, tin-lead coatings will have to be phased out, not only from the regulatory aspects of using lead-containing materials, but also from the metallurgical effects that lead contamination have on the lead-free alloys.

The consequences of lead contamination include the appearance of lower melting lead-bearing phases in the solder as well as depression of the melting temperature of the solder[2]. These points are illustrated in Fig. 2 which show the differential scanning calorimetry (DSC) plots of 96.5Sn-3.5Ag and same solder contaminated with 6.4 wt% lead. In the latter case, the appearance of the "low temperature" 63Sn-37Pb peak (onset, 183°C) is accompanied by a large decrease in the melting temperature of the matrix component from 221°C to 206°C. Advantages such as higher service temperatures and joint reliability can be jeopardized by lead contamination.

Candidate finishes for devices leads and terminations include electroplated 100Sn and hot 100Sn dipped coatings. The deposition of electroplated tin must be part of the lead frame fabrication process. Hot dipping is performed after the package has been fully assembled, thereby limiting disruption of established package manufacturing processes. Layer thicknesses are specified by MIL-STD-1276D. These coatings are well suited for alternative lead-free solders based upon the element, tin.

Coatings for circuit board conductor lands and traces can be an integral part of the fabrication process. Options include 100Sn as well as organic protective coatings based on azole or resin chemistries. Electroplated

tin is introduced onto the circuit board conductors during fabrication. Electroless or "immersion" metal coatings (tin, nickel, etc.) as well as organic preservatives (e.g., imidazole) are deposited on the bare conductor traces as the last step of the fabrication process. The protection offered by azole-based organic preservatives against oxidation is severely degraded after multiple reflow cycles in non-inert environments[3]. Immersion tin appears to provide improved protection against oxidation of the conductor[4]; however, solderability loss due to intermetallic compound growth between copper and the very thin tin coatings (1-2 microns thick) must be fully documented for long-term storage product storage.

C. Prototype Assembly Trials

Once the candidate solder alloys have been selected, their performance in the assembly of printed circuit boards as well as product reliability must be assessed. The design of prototype manufacturing trials must be based upon clearly defined objectives. Generally, two goals are sought through these trials: (1) determining the manufacturing feasibility of the solder alloy in assembly processes and (2) assessing the service reliability of the solder joints after fabrication. A manufacturing feasibility study may represent a stand alone objective. However, a reliability assessment must necessarily be preceded by the feasibility study to ensure satisfactory and reproducible solder joints from which to obtain the reliability data. Failure to consistently produce proper solder joint geometries (whether due to poor wettability or inadequate process control) will cause excessive data scatter that may obscure otherwise significant trends in the reliability analysis.

A feasibility study is being conducted by AT&T and Sandia to assess the manufacturability of several commercially available, lead-free solders on surface mount test vehicles. A photograph of the test vehicle is shown in Fig. 3. The printed circuit board is FR-4 with solder mask. Devices include 50 mil pitch 68 I/O plastic leaded chip carriers (PLCC) package with J-leads ; 24 I/O small outline integrated circuit (SOIC) package with gull-wing leads; and 1206 discrete chip capacitors. The circuit board was not fully populated in order to leave vacant lands for solder spreading evaluations.. These devices comprise a representative range of solder joint configurations .

Assembly is by means of an infrared furnace, using either ambient atmosphere or nitrogen cover gas. Preliminary trials, based circuit board land wettability evaluations, were conducted first in order to narrow the processing parameters for the assembly of the test vehicles.

The solders currently being investigated include both high and low melting temperature alloys: 95Sn-5Sb (T_s=232°C, T_l=240°C), 96.5Sn-3.5Ag (T_s=T_l=221°C), 63Sn-37Pb (T_s=T_l=183°C) as the control, 50Sn-50In (T_s=118°C, T_l=125°C), and 42Sn-58Bi (T_s=T_l=183°C). These solders are contained in paste form, accompanied by a conventional rosin-based, mildly activated flux.

The feasibility assessment is based upon a defect analysis of the prototype circuit boards. Criteria include: (1) non-wetting of lands, device leads, and terminations; (2) de-wetting of lands, device leads, and terminations; (3) crack and void formation in the solder joints; (4) solder ball formation which includes the IPC test *and* an evaluation of the prototype board solder joints; and (5) damage to devices and the circuit board laminate. The performance of a particular solder paste is quantitatively ranked by the number of such defects observed on the test vehicles.

Manufacturing feasibility is also being assessed for several corollary criteria. For example, the printability of the solder paste must be examined prior to device placement. Excessive slump or viscosity causes solder bridges or skips, respectively. An inconsistent volume of paste deposits results in "starved" joints. Also, the alignment of leadless chip devices (resistors as well as capacitors) over the lands, which is affected by the melting and surface tension properties of each solder, is being documented. "Tombstoning" of discrete chip devices is a defect directly related to device alignment.

Finally, it is important to note that the acceptance criteria noted above should not be used solely to describe the performance of a particular solder alloy. Rather, the data must be analyzed from a "system" point-of-view, the "system" being comprised of: (1) the solder alloy, (2) the paste binder, (3) surface finishes, (4) the package configuration(s), and (5) the assembly process parameters. For example, the solder paste binders used with lead-free solders have been optimized for the traditional tin-lead eutectic and near eutectic alloys. Therefore, defects such as poor solderability are also caused by properties of the paste and not simply wettability of device or circuit board finishes.

A second example is the solder ball evaluation. It has been observed by the authors that the standard (IPC) solder ball test, which is paste reflowed on a glass slide, does not always represent the propensity for solder ball formation on the actual test vehicle, given the same process conditions. In fact, solder ball formation may vary between devices on the same circuit board. This behavior is caused by dissimilar heating dynamics of different package configurations (point 4 above) as compared to one-another, or with respect to the glass slide used in the standard test.

These examples illustrate the need to consider all processes and materials in the assembly effort when analyzing the defect data so that root causes can be unambiguously identified for subsequent optimization procedures.

III. Summary

The implementation of lead-free solders into electronic assemblies is comprised of several tasks. The selection of candidate solder(s) can be facilitated by laboratory experiments which provide preliminary data on the performance of the material. The meniscometer/wetting balance technique examines the wetting characteristics of the solder-flux-substrate system. Such a study not only provides a relative ranking of material performance from which to narrow the candidate field for follow-on studies, but the wetting properties can also be used to establish operating windows on the processing parameters for prototype development. An example of the latter approach is the wettability as a function of solder temperature.

The fabrication of prototype printed circuit boards must address several issues aside from the selection of a suitable solder. The use of lead-free surface finishes on device leads and terminations as well as on the conductive surfaces of circuit boards, must be addressed. The leading finish is 100Sn, owing to tin being the predominant component in most of the candidate lead-free solders. Electroplating processes for tin finishes on either device leads or circuit board surfaces require alterations to the fabrication processes. On the other hand, organic preservatives for circuit board surfaces or electroless tin coatings for either circuit boards or device I/O's are simpler to implement since the finish is deposited *after* the hardware has been manufactured.

The assembly of prototype circuit boards must have one of two clearly defined objectives: (1) the demonstration of manufacturing feasibility and (2) the testing of service reliability which *must* be preceded by the establishment of manufacturing feasibility. A collaborative effort between AT&T/Engineering Research Center and Sandia National Laboratories has examined the manufacturing feasibility of several lead-free solders on 50 mil pitch, surface mount test vehicles. Defect analysis was used to identify those factors in the assembly process, such as heating schedule, paste properties, and device packages, which were responsible for the artifacts.

References

[1] P. Vianco, "An Overview of the Meniscometer/Wetting Balance Technique for Wettability Measurements", The Metal Science of Joining, eds. M. Cieslak, et al., (TMS, Warrendale, PA; 1992), p. 265.

[2] P. Vianco and J. DalPorto, "Use of High Temperature Solders for Edge Clip Attachment on Polyimide-Quartz Circuit Boards", Proc. Third Elec. Mat. and Proc. Cong., (TMS, Warrendale, PA; 1990) p. 25.

[3] I. Artaki, U. Ray, H. Gordon, and R Opila, "Corrosion Protection of Copper Using Organic Solderability Preservatives", Proc. Surf. Mount Intern., San Jose, CA, Sept. 1992, p. 503.

[4] I. Artaki and P. Vianco, unpublished data.

Figures

Fig. 1 Solder meniscus geometry used to evaluate solderability.

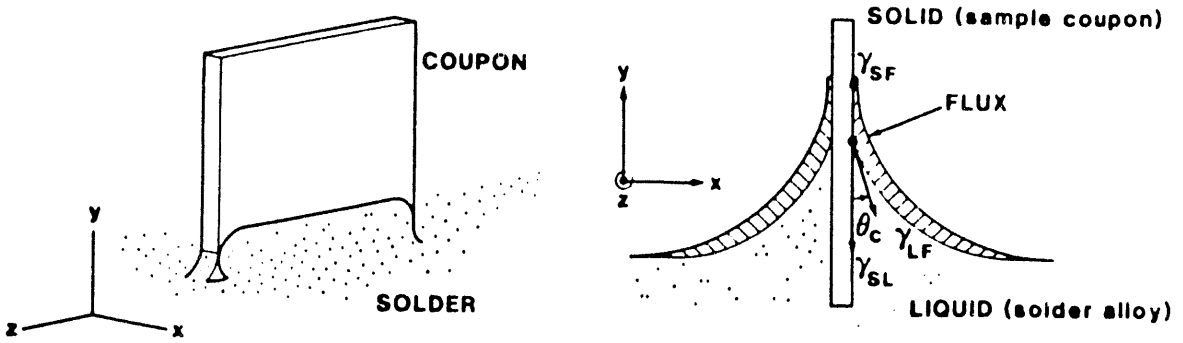
Fig. 2 Differential scanning calorimetry curves of (a)96.5Sn-3.5Ag and (b) 90.9Sn-2.7Ag-6.4Pb solders. The onset temperatures of 96.5Sn-3.5Ag and 63Sn-37Pb are 221°C and 183°C, respectively. The onset of the "96.5Sn-3.5Ag" peak in (b) has dropped to 206°C. Scanning rate: 10°C/min.

Fig. 3 Lead-free solders feasibility study test vehicle.

Tables

Table 1 Wettability parameters for several lead-free solders. The solder pot temperature appears adjacent to the alloy designation. The fluxes were rosin-based (R), rosin-based, mildly activated (RMA), and water-soluble, organic acid (OA).

Table 2 Wettability parameters as a function of solder temperature for 50Sn-50In and 95Sn-5Sb alloys.

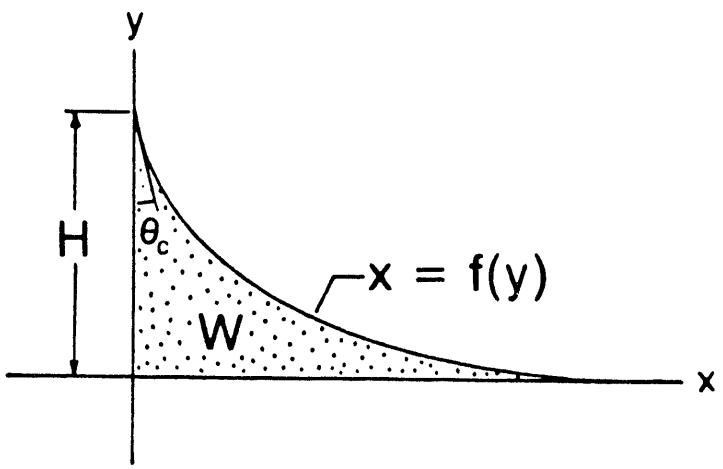


Young's Equation

$$\gamma_{SF} - \gamma_{SL} = \gamma_{LF} \cos \theta_C$$

Physical interpretation:

- γ_{SF} substrate surface condition
- γ_{SL} solder–substrate interactions
- γ_{LF} solder "surface tension"



$$\theta_c = \sin^{-1}\left[\frac{4W^2 - (\rho g P H^2)^2}{4W^2 + (\rho g P H^2)^2}\right]$$

Fig. 1

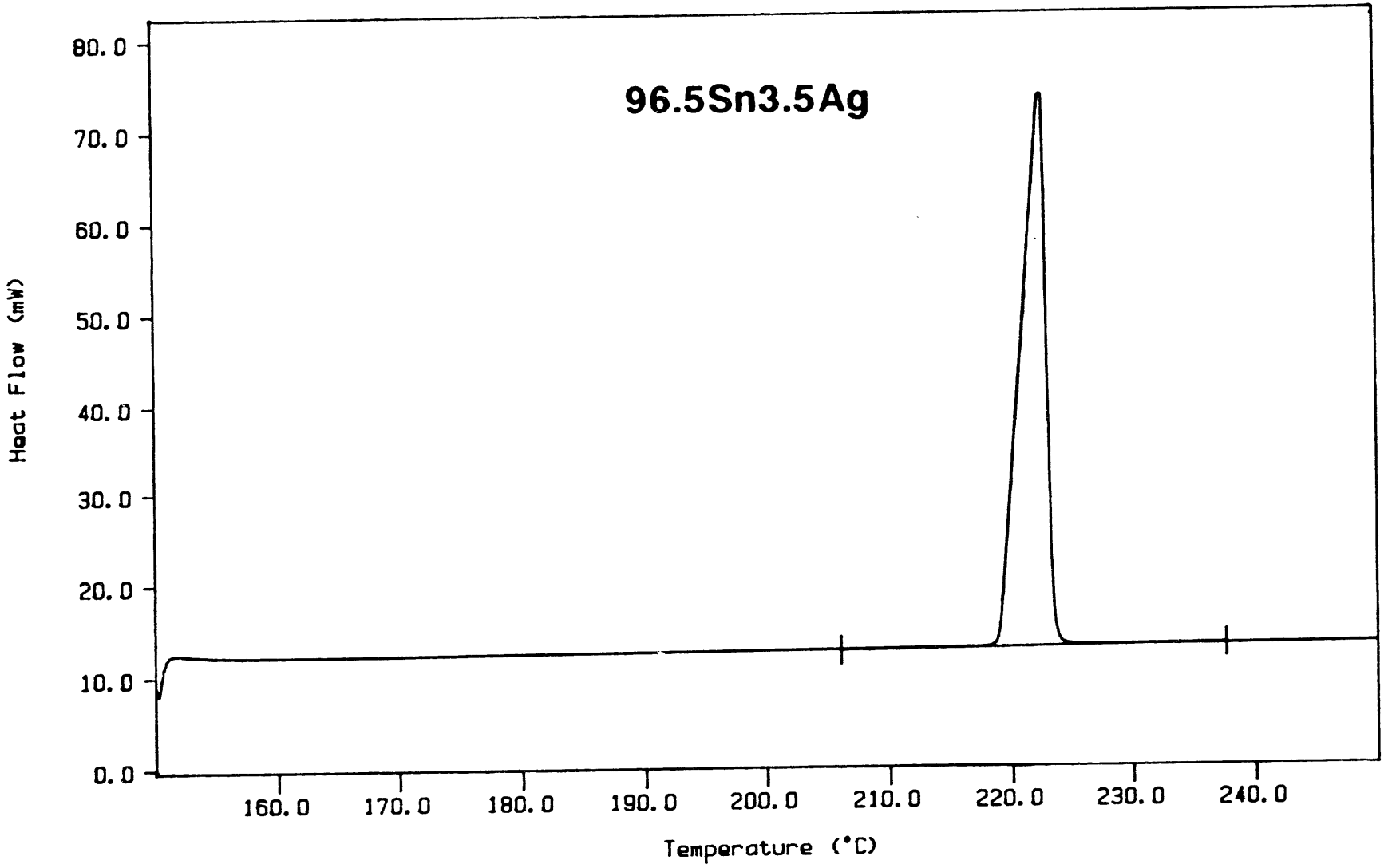

96.5Sn3.5Ag
Heat Flow (mW)
80.0
70.0
60.0
50.0
40.0
30.0
20.0
10.0
0.0
160.0
170.0
180.0
190.0
200.0
210.0
220.0
230.0
240.0
Temperature (°C)

FIG. 2a

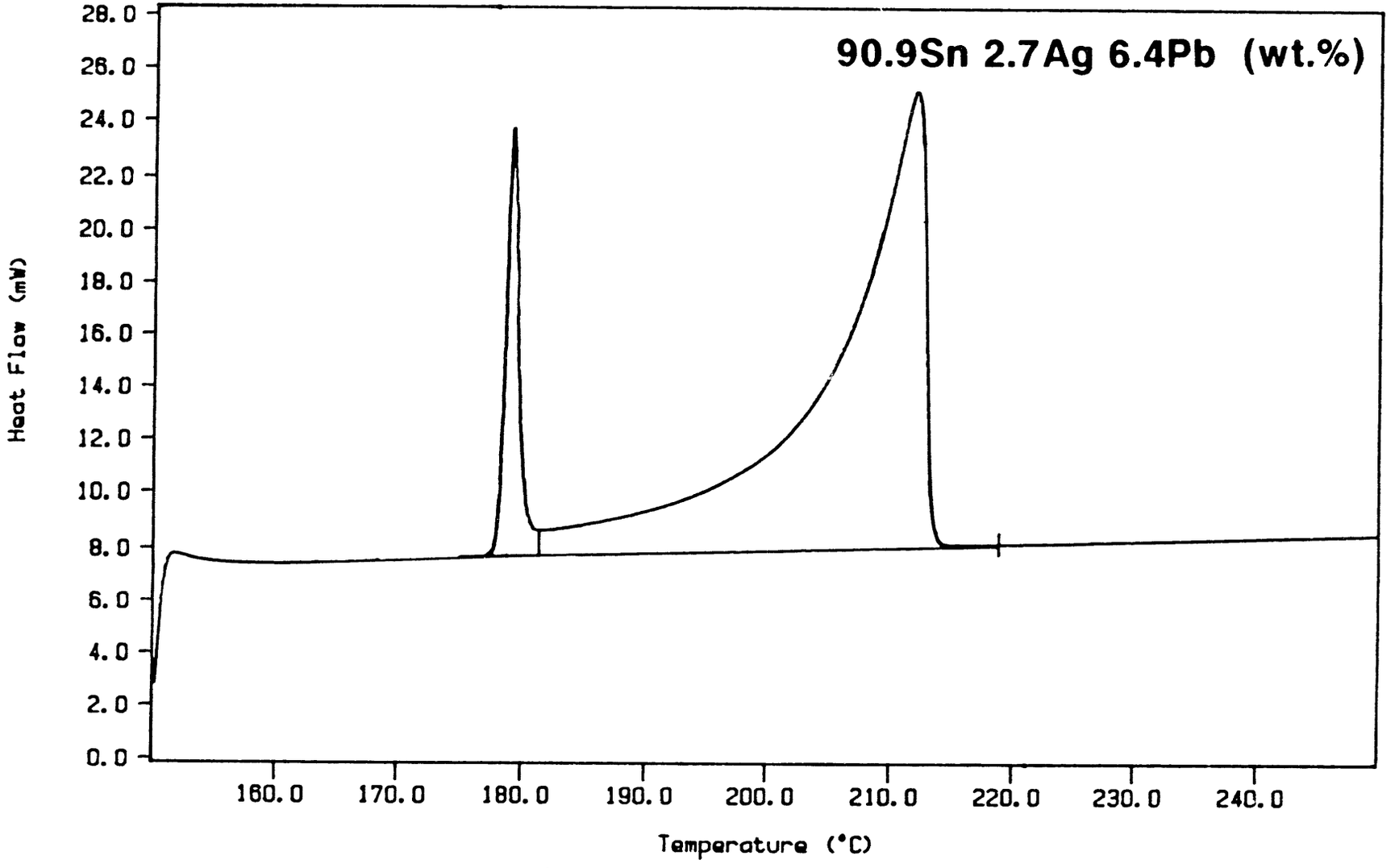

90.9Sn 2.7Ag 6.4Pb (wt.%)
Heat Flow (mW)
28.0
26.0
24.0
22.0
20.0
18.0
16.0
14.0
12.0
10.0
8.0
6.0
4.0
2.0
0.0
160.0
170.0
180.0
190.0
200.0
210.0
220.0
230.0
240.0
Temperature (°C)

FIG. 26

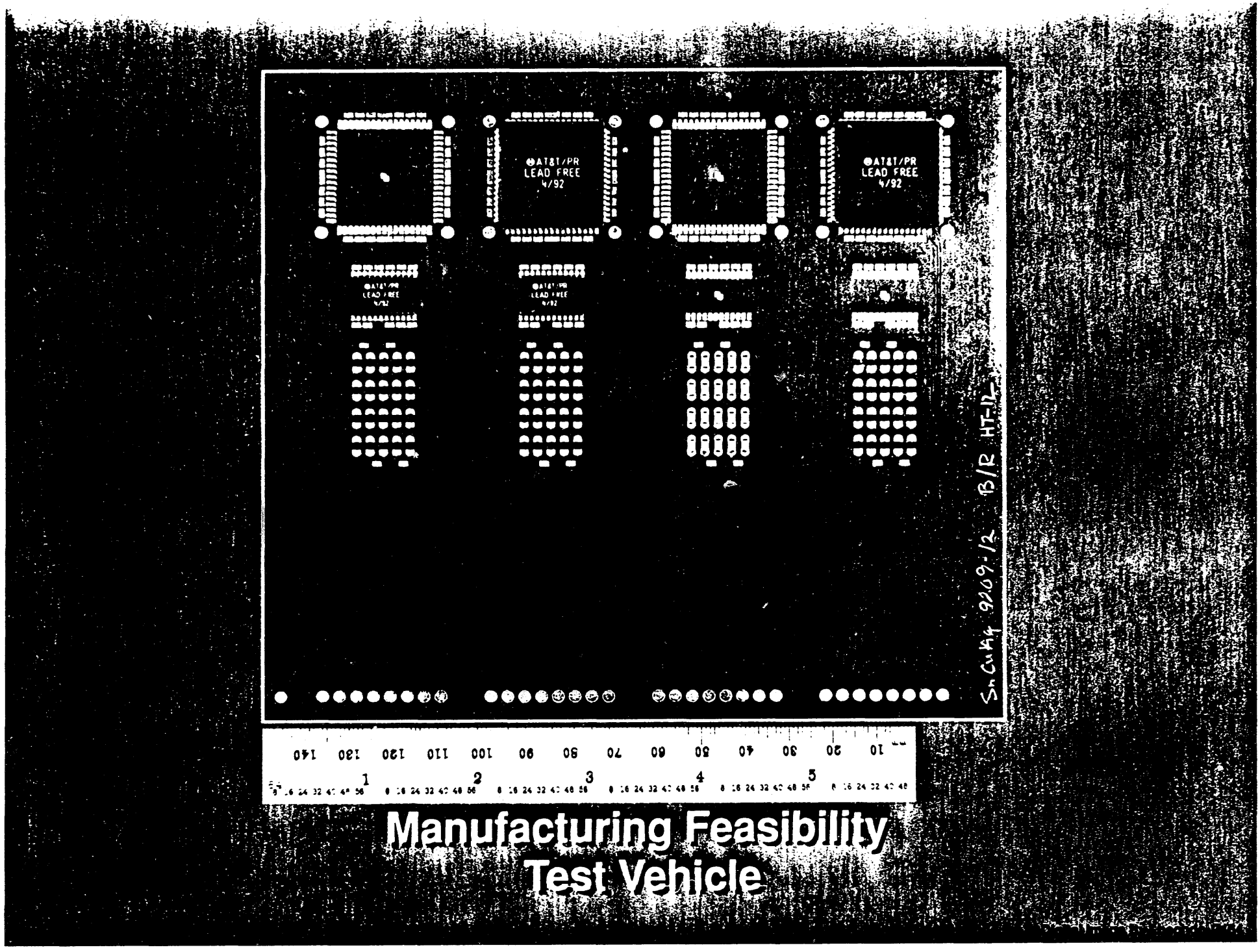

@AT&T/PR
LEAD FREE
4/92
@AT&T/PR
LEAD FREE
4/92
Sn Cu Ag 92.09/2 B/R HT-12
Manufacturing Feasibility
Test Vehicle

FIG. 3

BASE METAL	FLUX*	SOLDER/ TEMP. (C)	CONTACT ANGLE	γ_{LF} (dyne/cm)	$\gamma_{SF} - \gamma_{SL}$ (dyne/cm)	$\dot{W}$ (dyne/sec)	t (sec)
Cu	R	Sn–In/230	55+5	460±80	260±70	40±30	47±4
Cu	RMA	Sn–In/230	41±9	380±90	290±90	260±140	12.6±1.3
Cu	R	Sn–Ag/260	40±3	440±30	340±40	2190±310	4.0±0.2
Cu	RMA	Sn–Ag/260	36±3	460±30	380±40	3500±360	2.0±0.2
Cu	OA	Sn–Ag/260	47±1	530±20	360±20	3410±540	2.1±0.2
Cu	R	Sn–Sb/280	55±3	450±40	260±40	1360±230	3.9±0.8
Cu	RMA	Sn–Sb/280	43±4	470±70	340±70	2180±10	3.3±0.1
Cu	OA	Sn–Sb/280	43±8	370±80	270±80	2550±660	3.0±0.5

(1) Sn–In: 50Sn–50In
(2) Sn–Ag: 96.5Sn–3.5Ag
(3) Sn–Sb: 95Sn–5Sb

* R – rosin flux

RMA – rosin, mildly activated flux

OA – organic acid flux

TABLE 1

BASE METAL	FLUX	SOLDER/ TEMP. (C)	CONTACT ANGLE
Cu	RMA	Sn–Sb/280	43±4
Cu	RMA	Sn–Sb/268	42±7
Cu	RMA	Sn–Sb/255	51±9

BASE METAL	FLUX	SOLDER/ TEMP. (C)	CONTACT ANGLE
Cu	RMA	Sn–In/215	63±6
Cu	RMA	Sn–In/230	41±9
Cu	RMA	Sn–In/245	33±5

TABLE 2

END

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