LOW-TEMPERATURE EMITTER-PASSIVATION FOR SILICON SOLAR CELLS

Douglas S. Ruby
Sandia National Laboratories
Department 6213
Albuquerque, New Mexico 87185
USA
Phone: 505-844-0317
FAX: 505-844-6541

Jules D. Levine
Texas Instruments, Inc.
P.O. Box 655012, MS 35
Dallas, Texas 75265
USA
Phone: 214-995-5616
FAX: 214-995-2337

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ABSTRACT: We have developed a process that provides much of the performance improvement possible from a high-quality emitter passivation while maintaining cell temperatures at or below 400°C. Using atmospheric-pressure chemical-vapor deposition (CVD) of SiO_2 at 400°C followed by a 400°C forming gas anneal, we have been able to produce a 3.1-fold increase in the blue response of cells compared to that of unpassivated cells. This has resulted in up to an 11% increase in AM1.5G short-circuit current due to the passivating qualities of the CVD oxide.

This technique represents a low-cost approach to boost the performance of cells that do not presently employ passivating oxides. It would be of particular value to any silicon cell process in which material or other constraints preclude the use of a high-temperature thermal oxidation for the purpose of emitter passivation. This also applies to cells using material whose bulk lifetime is reduced by multiple high-temperature thermal excursions.

1. INTRODUCTION

Texas Instruments, Inc. (TI) is pursuing a unique solar cell design described recently as the Spheral Solar technology, which consists of silicon spheres embedded in an aluminum foil matrix [1]. Because the spheres are held in the low-melting-point foil early in the fabrication process, TI has been unable to take advantage of the high-efficiency passivated-emitter approach applied so successfully by the University of New South Wales, which employs a high-temperature furnace oxidation [2].

Passivation of the emitter surface with a thin high-quality thermally grown oxide layer has been shown to dramatically increase the blue response of cells with a relatively light emitter diffusion. A more lightly diffused emitter region generally has longer diffusion lengths, which, together with a well-passivated surface, results in increased collection of carriers generated in the emitter by short-wavelength photons.

Sandia National Laboratories is working with TI to develop a process that provides much of the performance improvement possible from a high-quality, high-temperature emitter passivation while remaining within the temperature and chemical constraints imposed by having the aluminum foil present during the processing. These constraints restricted our investigation to processes that require temperatures of 400°C or less and which avoid chemical treatments that would damage the aluminum foil.

Many low-temperature oxidation techniques have been reported in the literature, such as plasma-enhanced chemical vapor deposition, UV-light enhanced oxidation, or the use of oxygen plasmas [3-5]. Our investigation focussed on the low-cost approach of atmospheric-pressure chemical-vapor deposition (APCVD) of SiO_2.

2. EXPERIMENTAL PROCEDURE

The process we developed applies to n^+/p cells that have the phosphorus glass etched off the emitter surface after the phosphorus diffusion. Any additional etching of the Si emitter surfaces that the cell design calls for would need to be done at this point. Next, the bare Si surface was cleaned in a mixture of 10:1 deionized water to 37 Wt% HCl at room temperature for up to 10 minutes. This HCl cleaning did not react destructively either with aluminum evaporated on Si wafers or with the Al foil used in actual Spheral cells.

This was followed by a one-minute atmospheric-pressure chemical-vapor deposition (CVD) of SiO_2 at 400°C using SiH_4 and O_2. The resulting CVD-oxide thickness was measured using ellipsometry and ranged from 12 to 20 nm. These thin CVD oxide layers increase the weighted reflectance of an overlying antireflection coating by less than 2 percentage points. The deposition was followed by an anneal in forming gas (12.5% H_2, 87.5% Ar) at 400°C for 30 minutes.

This process was first attempted on high-resistivity (370 Ω-cm) float-zoned (FZ) Si wafers that underwent a phosphorus diffusion designed to produce an emitter sheet resistance similar to that of TI's Spheral cells. Photoconductance decay measurements were then made on the wafers to determine the emitter saturation current density (J_{oe}), which is related to the emitter recombination rate, using a technique developed at Sandia [6]. Using

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these measured values, we were able to calculate the improvement in performance expected of solar cells with the reduced levels of emitter recombination.

This technique was then used on textured, n^+/p solar cells fabricated on single-crystal Si wafers to verify the predictions and prove that the technique is compatible with the rest of our cell fabrication process.

3. RESULTS

Three different surface conditions were compared in this study. The first was that of a bare-Si surface after an HF etch and water rinse, similar to that of TI's Spheral cells before antireflection coating. The second was a surface that received the CVD-oxide layer. The third was a surface that underwent a high-temperature dry thermal oxidation at 950°C. The J_{oe} measurements at 25°C for these three cases are shown in Figure 1.

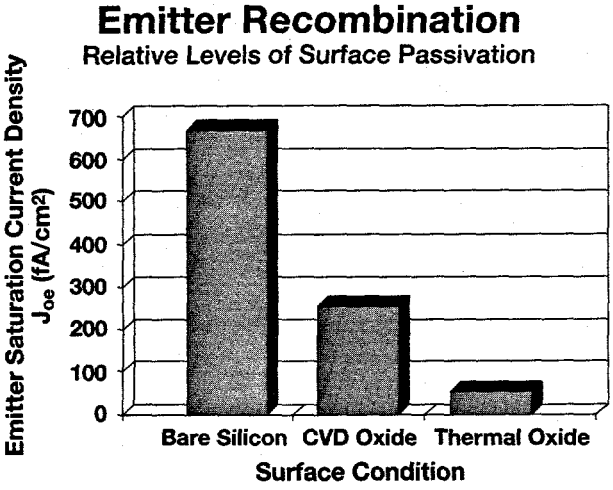

Figure 1: Emitter saturation current densities measured on high-resistivity FZ Si wafers with 100-ohm/square phosphorus-diffused emitters.

Comparison of the two left bars in Fig. 1 shows that a 2.6-fold reduction in the emitter recombination rate was obtained after the CVD oxide was applied to the bare Si surface. The right bar shows that this represents only part of the benefit attainable by the use of a high-quality thermal oxidation.

A computer program, PC-1D, was used to predict the short-circuit currents that should be obtained under AM1.5 global illumination due to the various levels of surface passivation [7]. First, the surface doping density and junction depth were adjusted to match the measured emitter sheet resistance and bare-surface J_{oe} values while using a front-surface recombination velocity (S_f) of $1x10^7$ cm/s. S_f was then reduced until the calculated J_{oe} values matched those measured on the oxide-passivated wafers. These values of S_f were then used in a solar cell simulation to calculate the cell's short-circuit current. The results of these calculations are shown in Table 1 and Figure 2.

Table 1: Surface recombination velocity and calculated short-circuit current density for the surface conditions and measured J_{oe} values shown in Fig. 1.

Surface Condition	S_f [cm/s]	Calculated J_{sc} [mA/cm^2]
Bare silicon	$1x10^7$	27.0
CVD oxide	$1.2x10^5$	28.4
Thermal oxide	$5.6x10^3$	30.0

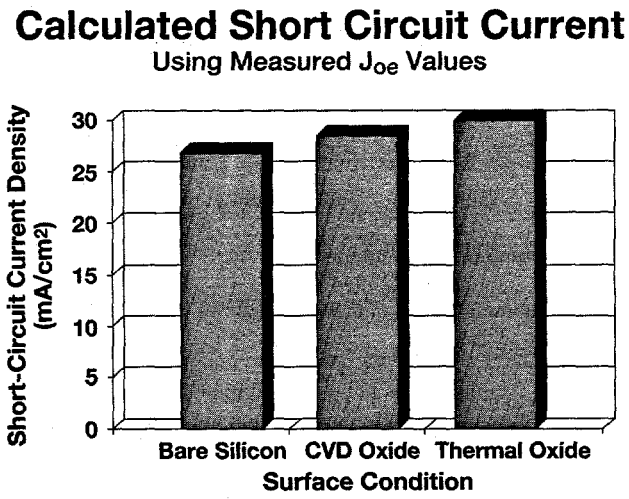

Figure 2: Calculated short-circuit current densities for the surface conditions and measured J_{oe} values shown in Fig. 1.

The 1.4 mA/cm^2 increase (5%) in J_{sc} for the CVD-oxide coated surface is entirely due to its surface passivating qualities. It can be seen to provide about half of the 3.0 mA/cm^2 increase obtainable using a high-temperature thermal oxide.

Cleaning the bare-Si surface with HCl prior to the CVD oxide deposition was found to result in improved surface passivation. Figure 3 shows the measured J_{oe} values of another set of high-resistivity wafers with a 200-ohm/square diffusion. Comparing the second and third bars shows that applying the CVD oxide after etching the phosphorus glass in an HF solution, but without cleaning in HCl, provides only part of the benefit attainable from the CVD-oxide passivation. Tests with aluminum-evaporated Si wafers and actual TI Spheral cells confirmed that the HCl did not etch the aluminum or degrade cell performance.

Simple n^+/p solar cells were fabricated on textured single-crystal Si wafers to compare the effect of the different surface conditions on cell performance. Table 2 and Figure 4 show the measured AM1.5, Global, short-circuit current densities (J_{sc}) for the three surface conditions.

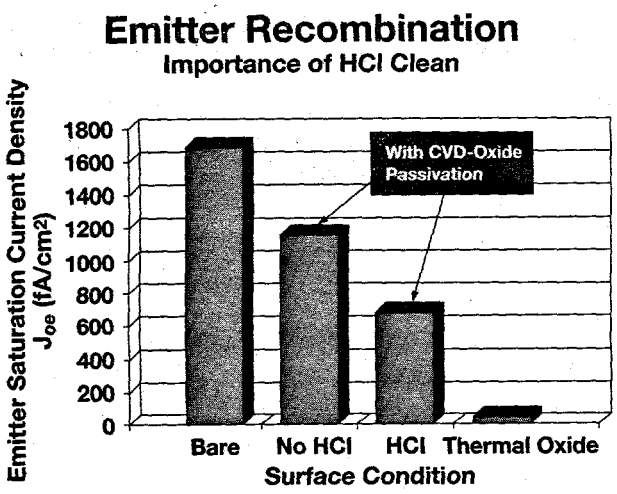

Figure 3: Emitter saturation current densities measured on high-resistivity FZ Si wafers with 200-ohm/square phosphorus-diffused emitters.

Table 2: Measured performance of solar cells fabricated with three different emitter surface conditions.

Surface Condition	# Cells Tested	Average J_{sc} [mA/cm^2]	Increase [%]
Bare silicon	13	27.0±0.6	--
CVD oxide	11	30.0±1.0	11
Thermal oxide	9	34.2±1.3	27

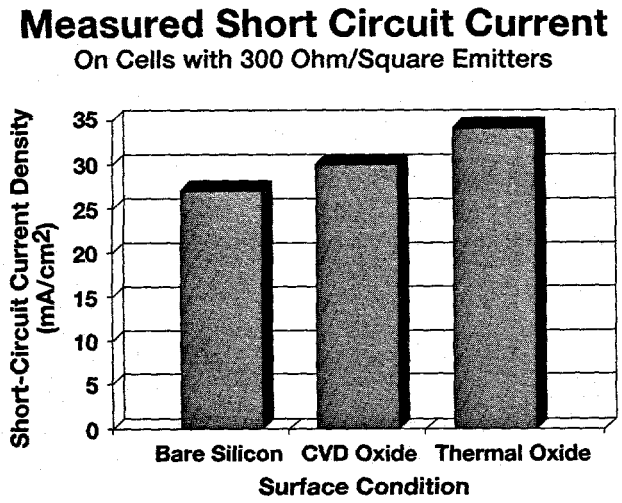

Figure 4: Average measured J_{sc} of cells fabricated with three different emitter surface conditions.

The 15 nm CVD-oxide layer was too thin to have any significant effect on cell reflectance. Therefore, the 11% increase in short-circuit current over that of the bare cell is entirely due to surface passivation by the CVD oxide. This is larger than the amount predicted because the 300-ohm/square sheet resistance of the fabricated cells was higher than the 100-ohm/square value obtained for the J_{oe} measurements and used in the calculations. Thus, the blue response increased more than predicted because lower surface recombination velocities are obtainable for passivated surfaces when the surface doping concentration of phosphorus is reduced [8].

Part of the 27% current increase for the thermally passivated wafer is due to reduced reflectance, because the 100-nm thermal oxide grown on these cells also acted as an antireflection coating. The open-circuit voltages of the passivated cells also increased slightly, mostly due to the increased short-circuit currents, but also from reduced emitter and surface recombination.

To compare the effect of the different surfaces on intrinsic cell performance, internal quantum efficiencies (IQE) of each of the three types of cells were measured and are shown in Fig. 5.

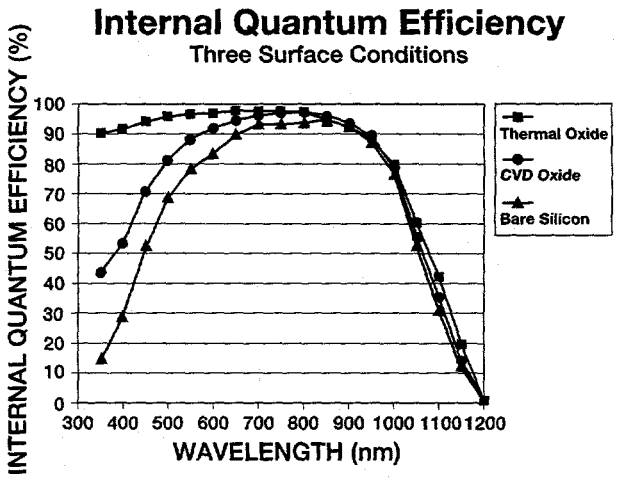

Figure 5: Measured internal quantum efficiencies of three cells fabricated using different emitter surface conditions showing varying levels of front surface passivation.

Figure 5 shows that the CVD oxide results primarily in increased blue response, as expected from improved surface passivation. There is a 3.1-fold increase in the 350-nm IQE for cells with CVD-oxide passivation compared to that of the bare cells. This level of passivation can be seen to be intermediate between the bare and thermally oxidized cases.

4. DISCUSSION

This low-temperature emitter-passivation technique represents an approach to boost the performance of cells that do not presently employ passivating oxides. Many manufacturers of terrestrial one-sun solar cells may be using simple diffusion schedules to minimize processing costs that do not produce passivated emitters. Many of these cells use material such as Czochralski or multicrystalline silicon, whose bulk lifetime is reduced by multiple high-

temperature thermal excursions, so that an additional high-temperature step for the purpose of growing a passivating thermal oxide must be avoided. In addition, many cell manufacturers already employ CVD equipment in their production lines for high-throughput dielectric film deposition for antireflection (AR) coatings. It could be cost-effective to modify this equipment to deposit a passivating SiO_2 layer just prior to the AR coating.

We have also shown that the benefit of surface passivation becomes even more pronounced when the emitter doping concentration is reduced. Cell designs that were forced to rely on heavily doped emitters to shield carriers from an unpassivated surface can now be modified to benefit from reduced diffused-region recombination as well. Many of these cells use screen-printed gridlines that require a high surface doping density under the metal to achieve low contact resistance. Further work remains to be done to investigate how patterned contact-region doping can be accomodated at low cost.

5. CONCLUSIONS

The low-temperature emitter-passivation technique described could be of value to any silicon cell fabrication process in which material or other constraints preclude the use of a high-temperature thermal oxidation for the purpose of emitter passivation. This applies not only to TI's Spheral™ cells, but also to many types of cells that use Si material whose bulk lifetime is reduced by multiple high-temperature thermal excursions.

6. ACKNOWLEDGEMENTS

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