CONF-941203--12
SAND94-3077C

RAPID THERMAL PROCESSING OF HIGH-EFFICIENCY SILICON SOLAR CELLS WITH CONTROLLED *IN-SITU* ANNEALING

P. Doshi[1], A. Rohatgi[1], M. Ropp[1], Z. Chen[1], D. Ruby[2], D. L. Meier[3]

[1]University Center of Excellence for Photovoltaics Research and Education, Georgia Institute of Technology, Atlanta, GA 30332
[2]Sandia National Laboratories, M.S. 0752, Albuquerque, NM 87185
[3]EBARA Solar, Inc., 811 Rt. 51 South, Large, PA 15025

ABSTRACT

Silicon solar cell efficiencies of 17.1%, 16.4%, 14.8%, and 14.9% have been achieved on FZ, Cz, multicrystalline (mc-Si), and dendritic web (DW) silicon, respectively, using simplified, cost-effective rapid thermal processing (RTP). These represent the highest reported efficiencies for solar cells processed with simultaneous front and back diffusion with no conventional high-temperature furnace steps. Appropriate diffusion temperature coupled with the added *in-situ* anneal resulted in suitable minority-carrier lifetime and diffusion profiles for high-efficiency cells. The cooling rate associated with the *in-situ* anneal can improve the lifetime and lower the reverse saturation current density (J_o), however, this effect is material and base resistivity specific. PECVD antireflection (AR) coatings provided low reflectance and efficient front surface and bulk defect passivation. Conventional cells fabricated on FZ silicon by furnace diffusions and oxidations gave an efficiency of 18.8% due to greater short wavelength response and lower J_o.

INTRODUCTION

Low-cost and high efficiency are the keys to large-scale acceptability of photovoltaic (PV) systems. PV modules today cost about $4/Watt, which can produce electricity at a rate of about 25¢/kWhr. A factor of two in cost reduction is needed to make PV attractive for peak load applications and about a factor of 3 or 4 reduction would make it extremely competitive with conventional energy sources for base load utility applications. No PV material or technology has yet been able to achieve the cost and efficiency goals simultaneously because the efficient cells are too expensive and the cheaper cells are not efficient enough. Rapid thermal processing directly addresses the issue of fabrication cost by significantly reducing the cell process time, thermal budget, and wafer cleaning steps, without a significant loss in cell efficiency. RTP cell fabrication in this study involves a rapid, simultaneous front and back diffusion for the formation of an emitter and back-surface-field, followed by a rapid low-temperature PECVD of SiN/SiO_2 coating for efficient front surface passivation and AR coating [1]. Conventional furnace processing (CFP) generally involves separate furnace diffusions and oxidations at high temperatures, which require extensive wafer cleaning, prolonged cell processing, and use more chemicals and gases.

Various investigators [2-8] have attempted RTP techniques in the past for silicon solar cell fabrication with only moderate success. Until recently, RTP techniques involving simultaneous front and back diffusions, using tungsten-halogen lamps, have resulted in cell efficiencies in the range of 12-15.4% [2-8] on single and multicrystalline silicon (Fig. 1).

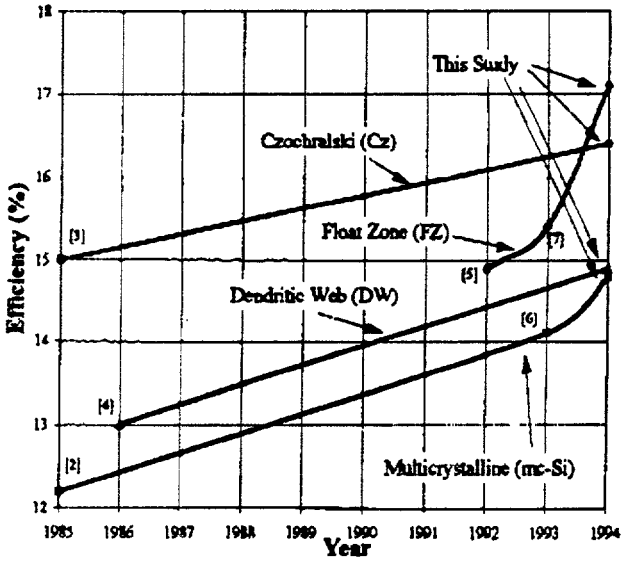


Fig. 1. Progress of RTP-diffused silicon solar cells without any furnace treatment. (The number in brackets represents the reference.)

Lower RTP cell efficiency is predominantly due to inappropriate diffusion profiles and lifetime degradation by rapid cooling rates and high quench temperatures, as will be discussed later.

Campbell and Meier [4] attempted to revive the lifetime of rapidly-cooled cells by performing post-RTP furnace anneals at high temperatures. They succeeded in raising the efficiency of n-type, 2 Ω-cm, DW cells from 13% to 15.2% with the anneal. This anneal, however, mitigates the attractiveness of RTP since it requires a long furnace step.

This work was supported by the United States Department of Energy under Contract DE-AC04-94AL85000.

DISCLAIMER

Schindler et al. [7], fabricated a 15.4% efficient cell on 1 Ω-cm FZ without a post-RTP furnace anneal. RTP diffusion at 1000°C with a cooling rate of 50°C/sec can lead to plastic deformation via excessive thermal stress [9] and lifetime degradation due to quenching. In addition, the high diffusion temperature resulted in a low emitter sheet resistance of 28 Ω/□ which is accompanied by a thick dead layer and reduction in short wavelength response due to Auger recombination and bandgap narrowing. High emitter-surface concentration also contributes to poor front-surface passivation.

Recently, we reported 16.9% efficient RTP cells on FZ silicon [10]. In this study, the diffusion temperature and cooling rates were controlled to achieve the best RTP cell efficiencies to date on FZ, Cz, mc-Si, and DW silicon, without any pre or post-RTP furnace anneal.

FABRICATION OF RTP/PECVD SOLAR CELLS

The fabrication of RTP/PECVD cells was recently published in ref. [10]. These cells are fabricated without any furnace anneals. Instead, a short *in-situ* lamp anneal is incorporated for lifetime recovery, appropriate junction depth, and suitable sheet resistance. Simple n^+-p-p^+ cells are fabricated by a short and simultaneous RTP diffusion of spin-on phosphorus dopants on the front and evaporated aluminum on the back, followed by a 9 min deposition of SiN/SiO_2 AR coatings by PECVD.

A number of experiments were performed to select the RTP thermal cycle (Fig. 2). Each segment of the thermal

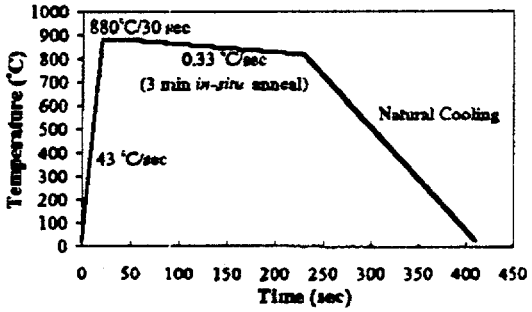


Fig. 2. Programmed thermal cycle for RTP simultaneous diffusion.

cycle is important. For example, the 880°C/30 sec peak-temperature step determines the surface concentration, J_o, and sheet resistance; similarly, the slow cooling rate of 0.33°C/sec for 3 min allows the formation of an Al back-surface-field, performs Al gettering [11], prevents lifetime degradation due to rapid quenching from high temperatures, and creates appropriate junction depths and diffusion profiles for high-efficiency cells. The 880°C processing temperature falls within the optimum range of 850°C-900°C [12] for RTP phosphorus gettering and is sufficiently low to prevent slip dislocations, which may emerge at temperatures > 1000°C [9]. The 30 sec time at peak-temperature also allows sufficient time for the partial lifetime "recovery" phenomenon [13] to occur. PECVD SiN/SiO_2 coatings provide good surface passivation, very efficient, double-layer AR properties, and passivation of grown-in or process-induced bulk defects in silicon. Thus, the combination of appropriate RTP sequence and PECVD coatings allows control of key material and device parameters necessary to fabricate high efficiency cells. Additionally, it reduces the thermal budget, relaxes the wafer cleaning requirements, reduces the use of chemicals and gases, and increases the yield. In addition, there is the potential for high throughput because RTP systems are well suited for continuous wafer heating by conveyor belts [7].

RESULTS AND DISCUSSION

Comparison Between RTP and CFP Cells

Table 1 summarizes the cell parameters along with the highest RTP cell efficiencies achieved on FZ, Cz, mc-Si, and DW silicon. Fig. 3 illustrates the front and back diffusion

Table 1. High-efficiency RTP/PECVD Si solar cells. All cells have been measured at Sandia National Labs (SNL).

Material	V_{oc} (mV)	J_{sc} (mA)	FF	Eff. (%)
FZ (0.2 Ω-cm)	637	32.8	0.819	17.1
Cz (0.8 Ω-cm)	609	35.2	0.763	16.4
mc-Si (0.8 Ω-cm)	594	33.0	0.756	14.8
DW (11 Ω-cm)	559	34.5	0.771	14.9

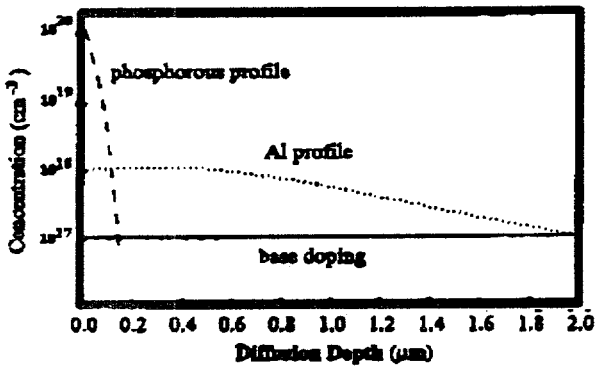
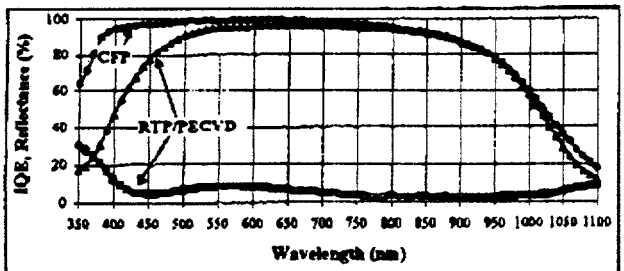


Fig. 3. Front and back diffusion profiles simultaneously diffused during the RTP treatment in fig. 2. (Measured on 0.2 Ω-cm FZ sample.)

profiles obtained by the 7 min. time/temperature cycle in fig. 2. Phosphorus emitter profiles, measured by spreading resistance, had a surface concentration about $2x10^{20}$ cm^{-3} and a junction depth of 0.15 μm. This resulted in a sheet resistance of 80 Ω/□. The aluminum back-surface-field profile, determined by C-V measurements using an electrochemical etching profiler, had a surface concentration of 10^{18} cm^{-3} and a junction depth of 2 μm. These simultaneously diffused profiles are quite consistent with the requirements for high-efficiency silicon cells and can be optimized further for even better results. Fig. 4 shows the internal quantum efficiency (IQE) of a typical 16.9%-efficient RTP/PECVD cell. The IQE analysis gave a bulk diffusion length (L_d) of 212 μm corresponding to a bulk lifetime (τ_b) of about 22 μs in the 0.2 Ω-cm base.

Fig. 4 also shows a comparison of the IQE between



Process	Voc (mV)	Jsc (mA/cm²)	FF	Eff. (%)	L_d (μm)
RTP	664	33.6	0.808	16.9	212
CFP	623	35.3	0.803	18.8	255

Fig. 4. Comparison between RTP and CFP cells on 0.2 Ω-cm FZ silicon.

typical CFP and RTP diffused cells on 0.2 Ω-cm FZ Si. CFP cell fabrication involved 930°C/25 min phosphorus diffusion on the front, followed by an etch back to obtain a comparable emitter sheet resistance of 80 Ω/□, and 850°C/45 min Al diffusion on the back which includes a 10 min thermal oxide passivation on the front. The conventional cell gave an efficiency of 18.8% with a slightly better long wavelength response but considerably better short wavelength response indicating somewhat higher bulk diffusion length (255 μm) and much lower front surface recombination velocity (FSRV). Emitter doping profile measurements for the conventional cell showed a much lower surface concentration of $2x10^{19}$ cm^{-3} and a junction depth of 0.6 μm. The order of magnitude higher surface concentration of the RTP emitter can increase FSRV, Auger recombination, and bandgap narrowing to account for the poor short wavelength response. Research is underway to increase the short and long wavelength response of the RTP/PECVD cells by optimizing the J_{oe} via emitter etch-back [14] and by improving τ_b values to bridge the gap between the conventional and RTP cells. The RTP cell efficiencies in excess of 17% achieved in this study demonstrate the potential for low-cost, high-efficiency RTP cells. To improve the efficiencies further, a better understanding of the effects of the RTP cooling rates associated with the *in-situ* anneal is needed.

Effects of RTP Cooling Rate on τ_b, J_o, and Efficiency

Several researchers have attributed many of the problems associated with RTP to quenching-induced recombination centers particularly introduced by activation of residual metallic impurities [15,16]. Rohatgi et al. [17], have shown that, during CFP, rapid cooling rates and high quench temperatures can freeze grown-in or process-induced impurities into electrically active sites or decorate defects to make them more detrimental. Several researchers [13,15] have shown significant diffusion length degradation with the increase of RTP quench temperature. In this paper, the problems associated with rapid cooling rates during RTP are investigated in detail by using four different cooling rates (Fig. 5) between the temperatures of 880°C and 820°C:

0.1°C/sec which involves a 10 min *in-situ* anneal,
0.33°C/sec which involves a 3 min *in-situ* anneal,
1°C/sec which involves a 1 min *in-situ* anneal, and
50°C/sec which involves no annealing (Quenched).

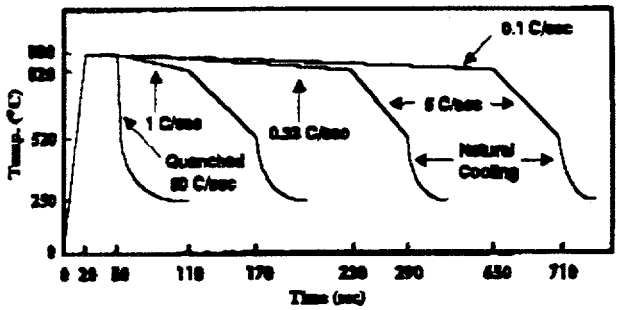


Fig. 5. Temperature cycles for RTP cooling rate experiments.

Preliminary experiments on FZ silicon involving 880°C peak temperatures exhibited no major quenching problems below 820°C.

First, high-resistivity, high-lifetime FZ silicon wafers were used to investigate the effects of RTP cooling rate on τ_b. Fig. 6 establishes, for the first time, a trend in the cooling rate induced lifetime degradation for an RTP system. In this experiment, sample preparation mimicked cell fabrication including the emitter formation steps in order to manifest any RTP induced P-gettering. Prior to the measurements, the emitters were etched away and τ_b was measured by the photoconductive decay technique with the samples immersed in HF. Quenching from 880°C resulted in a poor τ_b of only 180 μs; however, slow cooling at a rate of 0.1°C/sec gives very high lifetimes above 1.8 ms on high-resistivity FZ Si. Such high τ_b values demonstrate that RTP techniques are capable of achieving lifetimes compatible with very high-efficiency solar cells.

The effect of some of these cooling rates on PV devices fabricated from the same DW crystal is shown in fig. 7.

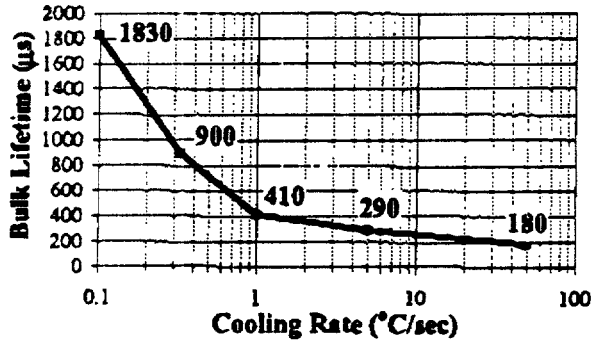
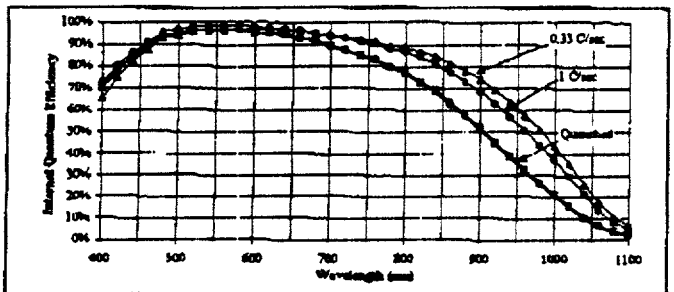


Fig. 6. Effect of RTP cooling rate on the bulk lifetime of high resistivity (500-1000 Ω-cm) FZ silicon. (Peak temperature = 880°C.)

The DW cells exhibit a strong dependence on RTP cooling rates. Quenching resulted in only a 10.2% efficient DW cell; however, it improved to 14.9% when slow-cooled at a rate of



Cool. Rate	Voc (mV)	Jsc (mA/cm²)	FF	Eff. (%)	L_d (μm)	J_o (pA/cm²)
50	514	28.1	0.703	10.2	45	45
1	535	33.4	0.745	13.3	112	22
0.33	559	34.5	0.771	14.9	194	8.7

Fig. 7 Effect of RTP cooling rate on 11 Ω-cm dendritic web Si solar cell performance. Lighted I-V measured at SNL.

0.33°C/sec. Substantial improvement in the long wavelength IQE response (fig. 7) is attributed to bulk diffusion length enhancement with slower cooling rates. Controlling the cooling rate to 0.33°C/sec achieved a factor of 4 improvement in diffusion length and a factor of 5 decrease in J_o. The fact that the bulk diffusion length enhancement is accompanied by an improvement in J_o, suggests that J_{ob} is the dominating component of the total $J_o = J_{oe}+J_{ob}$ and that recombination in the base is the efficiency-limiting mechanism for DW cells.

The effect of RTP cooling rates on different materials reveals a more complex phenomenon. The effect is highly material and base resistivity specific. For example, in contrast to DW, cells fabricated on FZ showed little or no improvement in τ_b. Unlike FZ, DW contains point defects and dislocations; consequently, vacancies, silicon self-interstitials, and possibly impurity atoms such as oxygen may be quenched into electrically active sites upon rapid cool down. Also, the high base doping of $\sim 10^{17}$ cm^{-3} in the 0.2 Ω-cm FZ base masks the impact of quenching due to two reasons. First, quenching may not influence the lifetime of heavily doped materials as much because of the low starting lifetime associated with dopant-related complexes. Secondly, these low-resistivity cells generally are more emitter (J_{oe}) controlled so that small changes in τ_b, which affect J_{ob}, do not alter the total J_o. In fact, the longer annealing times associated with the slower cooling rates hurt the short wavelength response of FZ cells due to excessive heavy doping effects in the emitter. Preliminary results of slow-cooling on 0.8 Ω-cm Cz and mc-Si exhibit the similar competition between τ_b enhancement and the undesirable increase in J_{oe}. Proper optimization of RTP cooling rates thus requires tuning both the τ_b and J_o for maximum efficiency.

CONCLUSIONS

By developing an RTP temperature/time cycle consisting of an *in-situ* anneal for simultaneous front and back diffusion with suitable τ_b and J_o, silicon solar cell efficiencies of ~17% and diffusion lengths > 200 μm have been achieved on FZ without any furnace treatment. Use of low temperature PECVD SiN/SiO_2 coating further speeds up the process in addition to providing bulk defect and surface passivation in conjunction with excellent antireflection properties. High cell efficiencies on Cz, dendritic web, and multicrystalline demonstrate the competitiveness of RTP as an alternative to furnace processing.

The understanding of the effect of RTP cooling rates has been improved. For emitter influenced cells, slower cooling rates may offer better lifetimes; but, a penalty in terms of J_o may ensue. Therefore, to design cells compatible with high efficiency, a proper optimization of the cooling rate is necessary in order to simultaneously enhance the lifetime AND suppress the increase of J_o. Emitter etch-back is one technique that can reduce J_o without sacrificing bulk lifetime [16]. Research is underway to incorporate cost-effective techniques for surface texturing and screen printing to make the RTP/PECVD technique more attractive for low-cost high-efficiency cells.

REFERENCES

[1] Z. Chen, P. Sana, J. Salami, A. Rohatgi, *IEEE Trans. on Electron Devices* 40, 1993, p. 1161.

[2] A. Usami, M. Tsunekane, T. Wada, Y. Inoue, S. Shimada, N. Nakazawa, Y. Meada, in *18th E.C. PV Solar EnergyConf.*, 1985, pp. 1078-1083.

[3] A. Usami, M. Ando, M. Tsunekane, K. Yamamoto, T. Wada, Y. Inoue, in *18th E.C. PV Solar Energy Conf.*, 1985, pp. 797-803.

[4] R. Campbell, D Meier, *J. Electrochem. Soc.* 133, 1986, 2210.

[5] B. Hartiti, A. Slaoui, J. C. Muller, P. Siffert, in *11th E.C. PV Solar Energy Conf.*, 1992, p. 420.

[6] B. Hartiti, A. Slaoui, J. C. Muller, P. Siffert, in *Proc. 23rd IEEE PVSC* (IEEE, Louisville, 1993), p.224.

[7] R. Schindler, I. Reis, B. Wagner, A. Eyer, H. Lautenschlager, C. Schetter, W. Warta, in *Proc. 23rd IEEE PVSC* (IEEE, Louisville, 1993), pp.162-166.

[8] S. Sivoththaman, B. Hartiti, J. Nijs, A. Barhdadi, M. Rodot, J. Muller, W. Laureys, D. Sarti, in *12th E.C. PV Solar Energy Conf.*, 1994.

[9] G. Bentini, L. Correra, and C. Donolato, "Defects introduced in silicon wafers during rapid isothermal annealing: Thermoelastic and thermoplastic effects," *J. Appl. Phys.*, 56, 1984, pp. 2922-2929.

[10] A. Rohatgi, Z. Chen, P. Doshi, T. Pham, and D. Ruby, "High-efficiency silicon solar cells by rapid thermal processing," *Appl. Phys. Lett.*, 65, 1994, pp. 2087-2089.

[11] B. Hartiti, A. Slaoui, J. Muller, and P. Siffert, "Large diffusion length enhancement in silicon by rapid thermal codiffusion of phosphorus and aluminum," *Appl. Phys. Lett.*, 63, 1993, p. 1249.

[12] B. Hartiti, A. Slaoui, J. Muller, R. Stuck, and P. Siffert, "Phosphorus, diffusion into silicon from a spin-on source using rapid thermal processing," *J. Appl. Phys.*, 71, 1992, pp. 5474-5478.

[13] A. Poggi, E. Susi, M. Bumari, and M. Carrota, "Rapid thermal annealing of p-type silicon," *J. Electrochem Soc.*, 141, 1994, pp. 754-758.

[14] DOE Annual Report, Sandia National Laboratories Subcontract No. AA-1638, 1993-1994.

[15] W. Eichammer, V. Quat, and P. Siffert, "On the origin of rapid thermal process induced recombination centers in silicon," *J. Appl. Phys.*, 66, 1989, pp. 3857-3865.

[16] B. Hartiti, J. Muller, and P. Siffert, *IEEE Trans. Electron Devices*, 39, 1992, p. 96.

[17] A. Rohatgi, P. Rai-Choudhury, in *Silicon Processing*, ASTM STP 804, D. C. Gupta, Ed., American Society for Testing and Materials, 1983, p. 389.