Advanced Qualification Techniques*

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Abstract

This paper demonstrates use of the Qualified Manufacturers List (QML) methodology to qualify commercial and military microelectronics for use in space applications. QML "builds in" the hardness of product through statistical process control (SPC) of technology parameters relevant to the radiation response, test structure to integrated circuit (IC) correlations, and techniques for extrapolating laboratory test results to low-dose-rate space scenarios. Each of these elements is demonstrated and shown to be a cost-effective alternative to expensive end-of-line IC testing. Several examples of test structure-to-IC correlations are provided and recent work on complications arising from transistor scaling and geometry is discussed. The use of a 10-keV x-ray wafer-level test system to support SPC and establish "process capability" is illustrated and a comparison of10-keV x-ray and Co^{60} gamma irradiations is provided for a wide range of CMOS technologies. The x-ray tester is shown to be cost-effective and its use in lot acceptance/qualification is recommended. Finally, a comparison is provided between MIL-STD-883D, Test Method 1019.4, which governs the testing of packaged semiconductor microcircuits in the DoD, and ESA/SSC Basic Specification No. 22900, Europe's Total Dose Steady-State Irradiation Test Method. Test Method 1019.4 focuses on conservative estimates of MOS hardness for space and tactical applications, while Basic Specification 22900 focuses on improved simulation of low-dose-rate space environments.

I. INTRODUCTION

Over the past 10 years, there have been a number of advances in methods to assess and assure the radiation hardness of CMOS devices used in space and/or high-energy particle accelerator applications. Some of the most significant are: (1) the incorporation of "rebound testing" into standard total-dose test methods [1-5], (2) the development of laboratory irradiation sources (e.g., 10-keV x-ray wafer-level irradiator, Cf^{252}, and lasers) for process control and lot acceptance/qualification testing [6-11], and (3) the introduction of QML methodology for radiation hardness assurance [12,13]. QML is a very positive program for US industry and is essential to ensure an ongoing supply of the highest quality and most reliable microcircuits for government, DoD, and space applications. QML provides higher quality product through continuous improvement, a streamlined customer interface with improved conversion of customer requirements, and a framework for the rapid implementation of new and enabling technologies. To stress the latter point, QML migration to next generation technology is simply a "delta" qualification approach of identifying and controlling *additional* technology parameters that affect radiation hardness. This is made possible by a "baselined" technology in which critical nodes are under SPC and process capability is high. In the US, QML has matured to the point that space customers are often willing to wave Group E (radiation) tests from a QML vendor. Efforts are presently underway to revise MIL-I-38535 Appendix B requirements to reflect the real (and new) business environment that demands reduced qualification costs.

In this paper, key elements required to implement QML will be addressed. To start with, the basic QML methodology will be introduced. The role of SPC in establishing process capability will be discussed and several examples will be provided of test structure-to-IC correlations. This will be followed by discussion of an x-ray wafer-level test system and its application in process control and improvement. Dose enhancement, recombination, and dosimetry effects will be quantified to permit a meaningful correlation between radiation-induced damage resulting from x-ray and Co^{60}-gamma irradiations. In the final section of the paper, a comparison of MIL-STD-883D, Test Method 1019.4 and ESA/SSC Basic Specification No. 22900 (Draft Issue 5) will be provided. These test methods, which define total-dose testing for qualification, will be compared with regard to test philosophy, similarities, differences, advantages and disadvantages, and simulation fidelity. The physics underlying these test methods will be discussed and important areas for future work and research will be identified.

II. QML METHODOLOGY

Under the sponsorship of the Defense Electronics Supply Center (DESC), the US government has instituted the QML methodology for qualifying microcircuits. The details of QML methodology are defined in military specification MIL-I-38535B [12]. In this approach, the quality of an IC is "built-in" by the proper control of the manufacturing sequence from design through assembly. (Quality in these discussions refers to high reliability and radiation hardness.) The primary goals of QML are to: (1) reduce the cost of microcircuits to system users, (2) improve the availability of highly reliable microcircuits, and (3) provide a mechanism for continual quality improvement. QML replaces the Qualified Parts List (QPL) methodology which relied on extensive testing of product microcircuits to determine their radiation hardness levels. In fact, a QPL to QML transition plan now exists to upgrade QPL product to the QML. QPL suppliers are listed in a QPL section of the QML and may elect to transition to full QML certifica-

*This work was supported by the Defense Nuclear Agency through its hardness assurance program, and by the U.S. Department of Energy through Contract No. DE-AC04-94AL85000

tion by conforming to the requirements of MIL-I-38535. To emphasize DESC's desire to support QML, *there will be no new QPL product listings!*

Several technical challenges associated with implementing QML are illustrated in Fig. 1 The vertical axis on the figure is the "savings" derived by implementing QML. The box in the lower left corner labelled "IC TESTS IN THREAT ENVIRONMENT" is similar to the conventional QPL approach. This approach is costly and involves extensive IC testing. The boxes in the upper right corner represent QML approaches that rely on evaluation of test structures and in-line SPC of technology parameters relevant to the radiation response. Here end-of-line testing is reduced and the savings are high. The horizontal axis represents the knowledge required to implement these different approaches toward qualification. The knowledge required to implement QML is considerably higher than those requiring IC testing alone, and is incomplete at the present time. That knowledge will of necessity include physical models, statistical models, 3D codes and circuit simulators, improved design tools, etc.

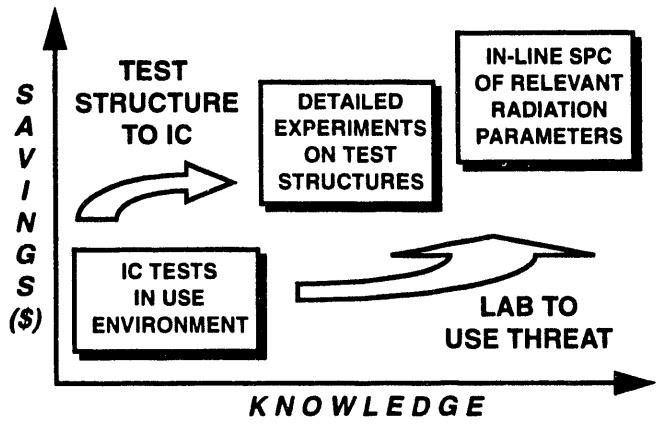

Fig. 1. Implementation of QML methodology involves (1) in-line SPC of relevant technology parameters and test structures, (2) test structure-to-IC correlations, and (3) extrapolating laboratory test results to the radiation environment of interest. (After Ref. [13].)

A. Test Structure-to-IC Correlations

An important aspect to QML is the ability to establish test structure-to-IC correlations. Once these correlations are demonstrated, information on test structures can be substituted for IC testing. An example of a test structure-to-IC correlation is given in Fig. 2, where the change in "read" time, Δt_{RD}, of radiation-hardened 2k SRAMs is plotted versus the threshold-voltage shift due to interface traps, ΔV_{it}, of n-channel transistors, both fabricated in Sandia's 4/3-μm technology [13]. The memories and transistors were irradiated in a Cs^{137} cell at a dose rate of 0.2 rads(Si)/s. The data show a strong correlation between ΔV_{it} shifts and increases in circuit timing and suggest that ΔV_{it} is an excellent monitor of timing degradation for these devices. In addition to the simple correlation shown in Fig. 2, test structure-to-IC correlations often involve the use of circuit simulators like SPICE. In SPICE applications, current-voltage (I-V) curves, taken before and after irradiation, serve as test-structure input to evaluate the radiation hardness of a given technology. Test structures can be as simple as transistors or slightly more complex like inverters or delay chains, but they must exhibit the failure mode of interest. Once a correlation between test structures and ICs has been established, the real key to manufacturing and qualifying consistent, reproducible product is to control variations in the test- structure parameter space. (In addition to controlling these variations, the manufacturer of radiation-hardened ICs will, no doubt, attempt to reduce the magnitude of parameter shifts following irradiation.) For example, to control changes in Δt_{RD}, one must control changes in ΔV_{it}. ΔV_{it} is subject to lot-to-lot, wafer-to-wafer, and intra-wafer variations. One of the most powerful tools for improving and controlling technology parameters is SPC. In the next sub-section, data will be provided on SPC of ΔV_{it} for this technology.

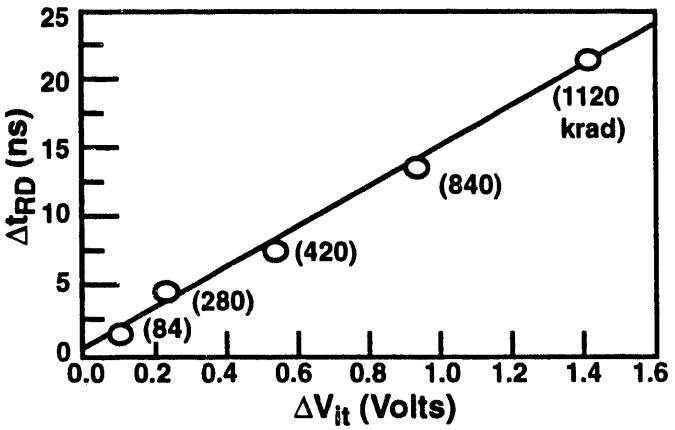

Fig. 2. Correlation between ΔV_{it} measured on n-channel transistors and Δt_{RD} on 2k SRAMs irradiated with 10-V bias at 0.2 rads(Si)/s. Total-dose levels corresponding to each data point are given in parentheses. (After Ref. [13].

It has been suggested that sources of variation in test structures may not be problematic if a "deterministic" test structure-to-IC correlation is performed. In a "deterministic" approach, attempts are made to correlate a test structure and IC *on the same die.* If this approach is successful, variations in test structure response across wafers and lots should be unimportant [14]. This approach has many drawbacks and is contrary to the quality principles and approaches espoused in this paper. Its intent can be abused to allow the user to "cherry-pick" good parts from bad wafers. If the manufacturing sequence is under control, all yielding parts from the wafer should meet radiation hardness requirements. In addition, this approach may not be successful for several other reasons. Recent data have shown that the radiation response of MOS transistors can strongly depend on device scaling and geometry. Scarpulla *et al.* [15] and Shaneyfelt *et al.* [16] have examined the radiation response of n- and p-channel transistors with gate lengths varying from 1 to 100 microns. The data of Shaneyfelt *et al.* are reproduced in Fig. 3 and clearly show the dependence of the threshold-voltage shift, ΔV_{th}, on device scaling. In this work, the authors show the dependence arises from variations in oxide-trap charge, ΔV_{ot}, and not interface traps. In the work of Scarpulla *et al.* [15], a similar dependence of threshold voltage on device scaling is observed and attributed to variations in interface traps. Due to

this geometry dependence, it will be difficult to use measurements on a transistor with a unique gate length to predict the response of its neighboring IC which contains transistors with many different gate lengths. These geometry effects must be accounted for when performing test structure-to-IC correlations. Instead of a "deterministic" approach, a "statistical" one is recommended, in which all sources of variation are included and used to map test structure into IC response. If ΔV_{ot} or ΔV_{it} varies with gate length, that variation must be included in the correlation.

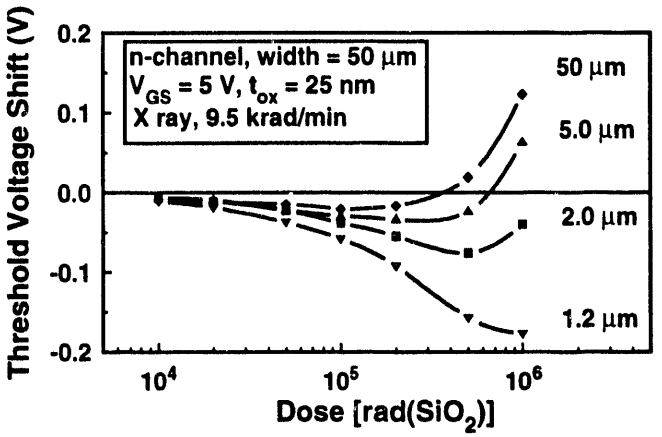

Fig. 3. Threshold-voltage shifts (ΔV_{th}) for n-channel transistors with gate lengths from 1.2 to 50 μm irradiated to 1 Mrad(SiO_2) at 5 V. (After Ref. [16].)

Up to this point, primary sources of variation have been identified as intrawafer, wafer-to-wafer, and lot-to-lot. Figure 4 shows that even intra-die variations can be significant - that is, variations among the 16,384 memory cells or bits on the die! Figure 4A shows address access time variations across a 16k SRAM die following 5-Mrads(SiO_2) irradiation, and Fig. 4B is a histogram of the data. The histogram clearly shows a bimodal distribution for the memory cells. There are several sources for the intra-die variation in Fig. 4 including geometry, process, and design layout. In terms of design, a cell in the middle of the memory may take longer to respond than a cell near the periphery. Process variations may arise from variations in critical dimensions (CDs) due to a non-uniform etch over varying topography on the die; these variations may become even more pronounced as die size increases to several square centimeters. Perhaps even more disturbing is that die from different wafers had a simple gaussian or even trimodal distribution of address access times, while the die pictured in Fig. 4 exhibited a bimodal distribution of address access times,. The bottom line is all sources of variation must be controlled and taken into account when establishing process capability (discussed in next sub-section)

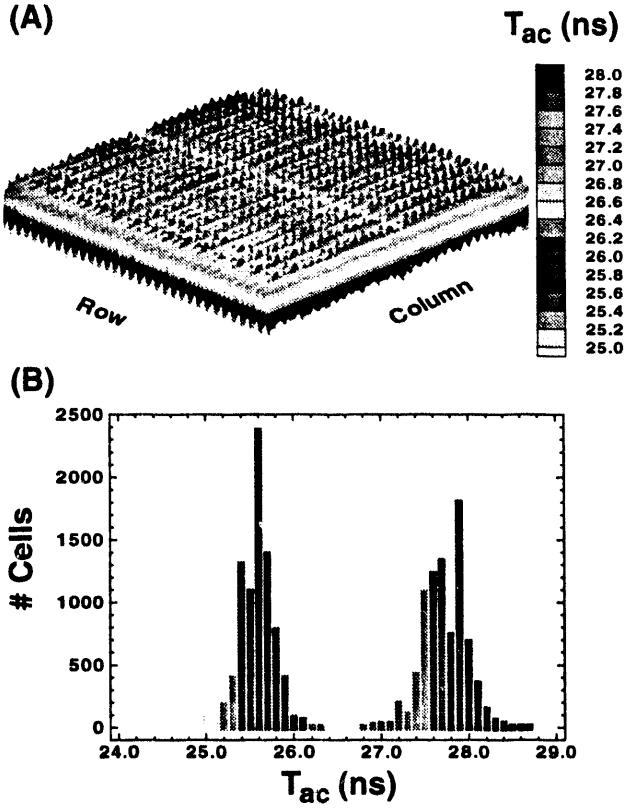

Fig. 4. Variations in address access time across 16k SRAM die. (A) 3D physical bit map (row and column) of address access time; scale on right provides values in ns. (B) Histogram of address access time showing a bimodal distribution of values.

B. SPC for Process Capability

Whether it is a commercial or a radiation-hardened technology, the key to achieving consistent hardness and manufacturability is establishing SPC of technology parameters relevant to the radiation response. These parameters are referred to as "critical nodes" and are used by process and design engineers to baseline a technology in its development stages. For total-dose hardness, critical nodes are gate-oxide thickness, polysilicon critical dimensions (CDs), anneal schedules, ΔV_{th}, ΔV_{ot}, ΔV_{it}, etc. Consider the example of a commercial technology in which the dominant effect of ionizing radiation is usually charge buildup in isolation or "field-oxide" regions. A typical isolation technique is called LOCOS in which a thick SiO_2 layer, typically 400 to 1000 nm, is grown while the channel region is masked by a nitride layer that prevents its oxidation. During irradiation, there is positive charge buildup in the thick SiO_2 layer which inverts the underlying p type Si and forms radiation-induced leakage paths between the source and drain. For commercial technology to be used in space applications, a critical node will be required to insure the integrity of the isolation oxide under irradiation, i.e., to prevent inversion and shut off the leakage path. That node may be a doping level for a p^+-guardband structure or a design rule that guarantees the guardband extends under both channel and field regions. In a similar fashion, the thickness of the gate oxide and the width of polysilicon lines will need to be controlled to insure total-dose radiation hardness.

To get a measure of process capability, "capability indices" must be calculated, namely, C_p and C_{pk}. These indices relate process control to "target" values and specification limits. C_p is a measure of the spread of the distribution relative to the specification limits, and C_{pk} is a measure of how centered the distri-

bution is with respect to a "target" value. The capability index C_p is defined as

$$C_p = \frac{Distribution Width}{Specification Width} = \frac{|USL - LSL|}{6\sigma}, \quad \text{(EQ 1)}$$

where the upper and lower engineering specification limits are described by USL and LSL, and the 6σ distribution width contains 99.73% (±3σ) of the population. A second capability index C_{pk} is defined by

$$C_{pk} = C_p(1-k), \quad \text{(EQ 2)}$$

where

$$k = \frac{|T-\mu|}{(USL-LSL)/2}. \quad \text{(EQ 3)}$$

T is the "target" value and μ is the mean of the distribution. In general, $C_p \approx C_{pk} \geq 2$ for a process to be under control. Technology parameters under SPC are often charted and violations noted. These violations certainly include values outside the control limits, but they also flag non-random trends in the parameter of interest, e.g., eight consecutive points above (below) the center line, 4 of 5 points above (below) ±1σ, etc.

For most radiation-hardened CMOS technologies in space applications (i.e., dose rates ≤ 1 mrad(Si)/s), shifts in threshold-voltage are dominated by ΔV_{it} and accompanied by a degradation in transistor mobility and transconductance. This occurs at low dose rates because many of the trapped holes can be annealed leaving mainly the interface traps. The dominant failure mechanism in space environments for many radiation-hardened CMOS technologies is a "timing" change caused by the buildup of radiation induced interface traps [3-5,17-19]. To meet system requirements for total-dose in space, the vendor must control ΔV_{it} shifts within acceptable limits. An example of SPC for 256 lots fabricated in Sandia's 4/3-μm technology is given in Fig. 5. ΔV_{it} shifts are shown following 500-krads(SiO_2) x-ray irradiations performed on the wafer level.

Clearly, SPC of technology parameters can most effectively be performed at the wafer level, and not readily on packaged parts using a Co^{60} irradiator. This permits real-time feedback and the statistics necessary to characterize intrawafer, wafer-to-wafer, and lot-to-lot variations. In the next section, issues dealing with wafer level testing will be discussed.

III. X-RAY/WAFER-LEVEL TESTING

Wafer-level radiation test systems are capable of baselining, controlling, and monitoring technology processes and parameters relevant to the radiation hardness. These systems are becoming increasingly popular and provide important feedback for process control and improvement. They permit detailed studies of intrawafer, wafer-to-wafer, and lot-to-lot uniformity required to accurately measure, establish, and improve process capability. At the heart of these systems is a low-energy (≈ 10-

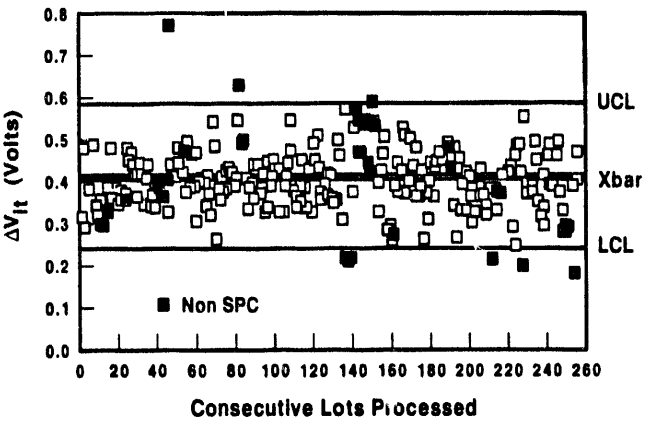

Fig. 5. Control chart showing lot-to-lot variation of ΔV_{it} over a 40-month period for 256 lots fabricated in Sandia's 4/3-μm technology. Average values (Xbar) and upper and lower control limits (UCL and LCL) are shown for ΔV_{it} following 500-krads(SiO_2) irradiation. SPC violations are indicated by solid squares. (After Ref. [13].)

keV) x-ray source that has been proposed as an alternative to Co^{60} for ionizing radiation effects testing of microelectronic devices [6]. Due to the limited penetration of 10-keV photons, x-ray irradiations are performed on unlidded devices or wafers. The x-ray spectrum commonly uses L-shell emissions from a tungsten target, but details of the spectrum are not important. The x-ray beam is collimated by a tantalum filter to allow for separate irradiations of individual die or test patterns on a die.

In addition to providing wafer-level radiation data required for SPC, there are many benefits to x-ray testing. These benefits include reduced test time and cost since the x-ray tester operates at higher dose rates, i.e., 200 to 3000 rads(SiO_2)/s, and fewer environmental and safety concerns. The x-ray tester has always been recognized as an excellent tool for process improvement and control. Interest now turns to extending its use to qualification and lot acceptance. Before that can be done, the effects of ionizing radiation caused by low-energy x rays must be calibrated against those caused by Co^{60} gammas. In the US, an ASTM standard [20] has been developed by Dennis Brown of the Naval Research Laboratory. In an Appendix of this standard, differences between the physical effects caused by x rays and Co^{60} gammas are discussed. Important factors include dosimetry, absorbed dose enhancement, electron-hole recombination, and time-dependent effects describing defect growth and annealing. Each of these effects will be discussed briefly.

In the final analysis, the relative effects of x-ray and Co^{60}-gamma irradiation depend on the number of holes produced in critical device insulators. Shifts in many measurable parameters, such as threshold voltage, can be related to the number of holes which are generated in the oxide and escape subsequent recombination. This is true because (1) there is an obvious connection between the number of unrecombined holes and the number of holes trapped in the oxide, i.e., oxide-trapped charge, and (2) almost all models describing radiation-induced interface traps suggest their buildup is proportional to the number of radiation-generated holes escaping the initial recombination process [17]. In general, when correlating the x-ray tester to the

Co^{60} cell, we can write

$$RelativeEffect = \frac{\#Holes(Co^{60})}{\#Holes(X\text{-}Ray)}. \qquad \text{(EQ 4)}$$

It is important to note that the number of holes that escape the initial recombination process is sensitive to both absorbed dose enhancement and electron-hole recombination effects.

The dose from x-ray testers has most commonly been measured using a calibrated PIN detector [6]. This method results in a measured dose rate in rads(Si)/s. This dosimeter absorbed dose must be converted to the equilibrium absorbed dose of the material of interest in the critical region within the device under test, for example, the SiO_2 gate oxide of an MOS device. Conversion from dose in the PIN detector to equilibrium dose in the SiO_2 region of a device can be performed using the following equation:

$$D_{SiO_2} = D_{Si}\frac{(\mu_{en}/\rho)_{SiO_2}}{(\mu_{en}/\rho)_{Si}} \cong \frac{D_{Si}}{1.8} \qquad \text{(EQ 5)}$$

where D_{SiO_2} is the equilibrium dose in the SiO_2 region, D_{Si} is the absorbed dose in the PIN diode, $(\mu_{en}/\rho)_{SiO_2}$ is the mass absorption coefficient for SiO_2, and $(\mu_{en}/\rho)_{Si}$ is the mass absorption coefficient for the PIN detector.

Dose-enhancement effects are expected when there are regions of different atomic number within hundreds of nanometers of the region of interest in the device under test. In absorbed dose enhancement, electrons which are produced by the deposition processes in one layer can ultimately deposit energy in another layer, after electron transport and diffusion occur. In order for these effects to be significant, the layers must be close together in comparison with the ranges of the relevant Compton electrons (for Co^{60} gammas) and photoelectrons (for 10-keV x rays). An example of a case where significant dose enhancement effects should be expected is a device with a tantalum silicide metallization within 200 nm of the SiO_2 gate oxide. Dose enhancement effects are greatest for low-energy x-ray irradiations because the photoelectric cross section (which dominates at 10 keV) varies as the fourth power of the atomic number, leading to significant differences in equilibrium or "bulk" dose for materials of differing atomic number. For Co^{60} irradiation, the Compton cross section is roughly proportional to atomic number and differences in equilibrium doses for materials with differing atomic number are far less significant.

When MOS structures are exposed to ionizing radiation, electron-hole pairs are created along the track of the incident particle. In general, some fraction of these electron-hole pairs will recombine, and that fraction is a complicated function of the oxide material, the kind of radiation, and the applied electric field. Experimentally, the "yield" or fraction of holes that escape recombination in SiO_2 is consistent with an electron-hole pair creation energy of ≅ 17 eV [21,22]. This yield is determined mainly by two factors: the magnitude of the oxide electric field E_{ox}, which is acting to separate the charge pairs, and the initial line density of electron/hole pairs created by the incident radiation particle. In general, recombination is greater for low-energy x rays than high-energy gammas because the line density is greater for x rays. Under low-field conditions (< 10^5 V/cm), approximately twice as many electron-hole pairs recombine for 10-keV x-ray radiation as compared to Co^{60} gamma radiation [23]. At moderate fields (1 to 2 MV/cm), electron-hole

Table 1: Ratio of Relative Effects of Co-60* and X-Ray Irradiations†

Case Description	(Co^{60}/X-Ray)		# Holes(Co^{60}) / # Holes(X-Ray)
	Electron-Hole Recombination Factor	Absorbed-Dose Enhancement Factor	
Gate Oxide (ON) *Thickness = 25 -50 nm* *Field = 1 MV/cm*	1.4	1/1.6 = 0.6	≈ 0.9
Gate Oxide (OFF) *Thickness = 25 -50 nm* *Field = 0.2-0.4 MV/cm*	1.8	1/1.6 = 0.6	≈ 1.1
Field Oxide (ON) *Thickness = 400 - 600 nm* *Field ≈ 0.1 MV/cm*	≈ 2	0.7 to 0.8	1.4 to 1.6
Gate With TaSi *Thickness = 25 -50 nm* *Field = 1 MV/cm*	1.4	1/2.5 = 0.4 (max)	0.6
SOI Back Gate *Buried Oxide Thickness = 0.4 - 2.0 μm* *Field = 10^4 V/cm*	1.5 for 0.4-μm SIMOX 3 for 2-μm ZMR	≈ 1 ≈ 1	≈ 1.5 ≈ 3

*Assuming a Pb/Al walled test box during Co-60 irradiations

†Assuming no saturation effects

recombination is 10 to 30% greater for x rays. At very high fields (> 5 MV/cm), yields approach 1 and there is no difference between low-energy x rays and high-energy gammas.

To summarize the discussions in this section, estimates of the combined effects of absorbed-dose enhancement (ADE) and electron-hole recombination (EHR) are listed in Table 1 for several important cases for standard MOS technology. EHR and ADE "factors" are defined as the ratio of these effects in Co^{60} to x-ray. In the last column of the table, a ratio per Eq. 5 is provided as an approximate measure of the relative effects of Co^{60} and low-energy x-ray irradiations. The results in Table 1 have been calculated assuming that the Co^{60} data are taken in a Pb/Al walled test box and that saturation effects are not present. Also, an additional 10 to 20% of dose enhancement may occur during Co^{60} exposures even inside a Pb/Al box if high atomic number elements are present, such as Au deposited on the inside of Kovar device lids [5]. Not factored into Table 1 is that practical x-ray irradiations are typically performed at much higher dose rates than Co^{60} irradiations and, consequently, radiation-induced defects have annealed less.

Five cases of practical interest are considered. The first case is a standard gate oxide biased "on" during irradiation. The EHR factor (the fraction of unrecombined holes for a Co^{60} gamma source to the fraction of unrecombined holes obtained using an x-ray tube) is 1.4. The ADE factor is 1/1.6 since it is 1 for Co^{60} and 1.6 for 10-keV x rays [23,24]. Overall, the two factors (which are multiplied) nearly cancel and the number of holes from Co^{60} is roughly 90% of those produced for the comparable x-ray irradiation. The second case deals with a gate oxide biased "off" during irradiation. Due to the semiconductor work function difference between the gate and substrate, i.e., $\phi_{ms} \equiv 1.1$ V, there is still a field of 0.2 to 0.4 MV/cm at zero applied gate bias for gate oxides from 25 to 50 nm. The EHR factor is 1.9 indicating twice the yield of holes for Co^{60} irradiation at these low fields. The ADE factor remains the same as for the first case, and the ratio of Co^{60} to x-ray effects is ≈ 1.1. For the third case we consider thick field oxide structures which have low electric fields even under "on" bias conditions, typically in the range of 0.1 to 0.2 MV/cm. The EHR factor is approximately 2 in the low-field region, and the ADE factor is closer to 1 at these oxide thicknesses [25,26]. ADE decreases as the oxide thickness increases since the range of secondary photoelectrons ($\approx$ 100 nm) becomes small compared to the oxide thickness. At 2000 nm, ADE factors in SiO_2 are essentially 1. A fourth case looks at corrections for devices with heavy metals. Devices are now being manufactured with metallization layers of tungsten and tantalum silicide. The presence of such layers is expected to result in significant dose-enhancement in adjacent SiO_2 gate oxides for x-ray irradiation [25,26]. ADE factors as high as 2.5 have been reported for some cases [26]. EHR factors or devices with heavy-metal silicides are expected to be similar to more conventional polysilicon-gate devices. The net ratio of effects from Co^{60} to x-ray can be as low as 0.6. In other words, considerably more dose is deposited in the SiO_2 gate insulator under x-ray irradiation. In a final case, a comparison is provided for the irradiation of back gates in an SOI technology. Buried oxide thickness of 0.4 to 2 μm are considered to be irradiated with zero back-gate bias and associated fields $\approx 10^4$ V/cm. For these thick oxides, dose enhancement factors are 1 for both Co^{60} and x-ray irradiations. The EHR factor and overall ratios at these very low fields range from 1.5 to 3 for the 0.4-μm (SIMOX) and 2-μm (ZMR) buried oxides, respectively [27].

Clearly, a strong and accurate correlation can be provided between Co^{60} and x-ray irradiations of microelectronic devices. The low-energy x-ray source will be able to support the qualification of devices. At the present time, one QML vendor in the US relies on the x-ray tester for qualification and lot acceptance.

IV. COMPARISON OF TEST METHOD 1019.4 AND BASIC SPECIFICATION NO. 22900

Qualification testing of ICs for radiation hardness assurance is carefully defined by test methods which are an integral part of QML methodology or an equivalent parts procurement system. MIL-STD-883D, Test Method (TM) 1019.4 [1] is the test method that governs total-dose testing of microelectronics in the US DoD, while ESA/SCC Basic Specification (BS) No. 22900 [2] is its European counterpart. In this section, with the aid of Table 2, these two test methods will be compared. The general philosophy of each method will be discussed and differences in their detailed protocol will be examined in light of the underlying physics. It is hoped that an understanding of similarities/differences between these test methods will promote coordination between the US and Europe toward a goal of improved hardness assurance. This discussion will focus on the use of these test methods for qualifying parts in low-dose-rate (1) space or (2) high-energy particle accelerator applications.

As presently configured, both TM 1019.4 and BS 22900 are intended to provide a conservative estimate of MOS hardness in low-dose-rate applications. To accomplish that goal, TM 1019.4 is a two-part test. The first part of its main test sequence is an irradiation to a specified dose at a dose rate of 50 to 300 rads(Si)/s followed by electrical test. This part of the method is a conservative test for parametric or functional failure caused primarily by *n*-channel gate-oxide or parasitic field-oxide transistor shifts due to radiation-induced oxide-trapped charge. This part of the test plays an important role in screening commercial CMOS technologies for use in space, where leakage from "isolation" oxides can be the primary degradation mode. The second part of the method is an accelerated aging or "rebound" test [3-5] for estimating ionizing radiation effects on devices in low-dose-rate environments. At the present time, this test is only applied to MOS-like technologies that are known to exhibit time-dependent effects (TDE), e.g., trapped-hole annealing and interface-trap buildup, over long time periods. Specifically, the main sequence of the second part of the test consists of an additional irradiation equal to 50% of the specified dose, followed by a 168 hour anneal at 100°C under bias and a second electrical test. This part of the method is a conservative test for parametric or functional failures due to timing degradation resulting from the long term buildup of interface traps and will play an

important role in screening both commercial and hardened CMOS technologies. A part intended for space application must pass *both* tests.

Basic Specification 22900 has a similar test flow. Irradiations are performed in a range of dose-rate *windows*, i.e., either between 1 to 10 rads(Si)/s or 0.01 to 0.1 rads(Si)/s. In either case, room and elevated temperature anneals are performed under bias for periods of 1 and 7 days, respectively. Similar to TM 1019.4, these anneals are used in an effort to account for time-dependent effects in the space environment. Electrical testing is performed following (1) initial radiation and (2) room/elevated temperature anneals. BS 22900 also provides a flow chart for evaluation testing. This test flow is intended for either the vendor or user and provides important information on technology characterization including process variability, magnitude and degree of TDE and post-irradiation effects (PIE), and inputs for the qualification test sequence described above. For example, worst-case bias is identified and anneal schedules specifying time and temperature are developed during evaluation testing.

A. Test Philosophy

The primary goal of a test method is to provide consistent and reproducible results. Toward that end, both TM 1019.4 and BS 22900 provide specific guidance on how testing is to be performed. For example, they specify bias and temperature conditions, allowable dose rates, time between irradiation and test, anneal procedures, etc. In general, BS 22900 allows greater latitude of test conditions. Not only does BS 22900 permit a wider range of dose rates, but test conditions can be tailored on a technology by technology basis during the evaluation phase. The second goal of a test method is to provide test results that provide useful information on the radiation response of devices in realistic radiation environments. Toward that end, both TM 1019.4 and BS 22900 have added tests that provide significant insight into device behavior in low-dose-rate space environments. However, it is the user's responsibility to evaluate test results and to determine their applicability to part performance in the environment of interest. In other words, a test method is a tool for system engineers, but it provides no explicit guarantees or assurances for every device type, technology, or use environment. A radiation-effects expert will always be required to evaluate and interpret data.

TM 1019.4 is simply a test procedure for measuring the piece-part hardness of ICs by exposing them in a Co^{60} source. It is a "stand-alone" test method. The guidance it provides is independent of whether testing is being performed for technology evaluation, part qualification, or lot acceptance. TM 1019.4 seeks to control test conditions within fairly tight limits so that (1) results are consistent at different laboratories and (2) a "level" playing field is provided in evaluating the radiation hardness of vendor technology. TM 1019.4 does not concern itself with setting system specifications, but seeks to provide valuable and meaningful test results to system engineers responsible for radiation hardness assurance. BS 22900, on the other hand, has separate paths or "phases" due to the differing requirements and logistics of technology evaluation versus qualification/lot procurement. Different procedures are actually provided for "Evaluation Testing" versus "Qualification and Procurement Testing," and the test method is tightly coupled to detail specifications and procurement documents.

B. Similarities

In Table 2, it is seen that dosimetry and temperature requirements are the same in both test methods. Also, the requirement to irradiate and anneal parts using worst-case bias is similar, as well as to maintain bias at all times, except during electrical parameter measurement. Both test methods prescribe that ICs be placed in conductive foam during transfer from the irradiation source to a remote tester and back again for further irradiation. This procedure is intended to minimize annealing or other time-dependent effects between irradiations and assures a worst-case conservative response. It is further recommended because (1) it provides for more consistent, reproducible results and (2) it is practical and protects against electrostatic discharge (ESD). It is also useful to note that at the lower dose rates and longer irradiation times (typically > 30 hrs) specified in BS 22900, the bias applied between irradiation and test is relatively unimportant. This is because differences in annealing between applied and zero bias over 1 to 2 hours following an irradiation that lasts tens of hours are not significant [18]. Both test methods require that samples be placed in a Pb/Al container to minimize dose enhancement effects caused by low-energy, scattered radiation. This Pb/Al container produces an approximate charged particle equilibrium for Si and for commonly used thermoluminescent dosimeters such as CaF_2. Finally, details of the testing sequence are the same for both test methods, namely (1) the time from the end of an irradiation to the start of electrical measurements shall be a maximum of 1 hour, and (2) the time to perform electrical measurements and return the device for a subsequent irradiation, if any, shall be within two hours of the end of the irradiation.

C. Differences

There are three primary areas in which TM 1019.4 and BS 22900 differ. They are (1) dose rate, (2) dose, and (3) anneal schedules. Each of these will now be discussed.

When performing total-dose radiation-effects testing, it is important to specify the dose rate of the incident radiation because it has been demonstrated that failure dose for an IC can be a complicated function of dose rate [3-5,18]. Clearly, the time-dependent nature of the buildup and anneal of oxide-trapped charge and interface traps is the reason for these dose rate dependencies. The strong dependence on dose rate is observed for both commercial and radiation-hardened CMOS and some modern bipolar devices.

As seen in Table 2, TM 1019.4 suggests testing in a range of dose rates from 50 to 300 rads(Si)/s; however, please note

Table 2: Comparison of ESA/SCC Basic Specification No. 22900 and US MIL-STD-883D, Method 1019.4

Parameter	ESA/SSC Basic Spec. No. 22900	MIL-STD-883D, Method 1019.4
Scope	Test method for steady-state irradiation testing of ICs and discretes during technology evaluation & qualification/procurement *for space applications*	Test method for steady-state irradiation testing of packaged semiconductor ICs
Radiation Source	Co-60 gammas (ionizing); electron accelerator (ionizing & displacement); alternate sources permitted	Co-60 gammas (ionizing)
Dosimetry	Intensity ±5%; field uniformity ±10%	Intensity ±5%; field uniformity ±10%
Pb/Al Container	Minimum 1.5 mm Pb/0.7 mm Al unless no demonstrated dose enhancement.	Minimum 1.5 mm Pb/0.7 mm Al unless no demonstrated dose enhancement.
Dose	±10% of specification	±10% of specification; an additional 0.5x overtest for *"rebound"*
Dose Rate	Exposure time ≤ 96 h; Window 1, Standard Rate is 1 to 10 rads(Si)/s; Window 2, Low Rate is 0.01 to 0.1 rads(Si)/s; ***or*** lower rate if agreed to by parties to test	50 to 300 rads(Si)/s ***or*** at ≥ dose rate of intended application if agreed to by parties to test
Anneals: *Room temperature* *Elevated temperature*	 For 24 h At 100°C for 168 h	 None "Rebound:" At 100°C ±5°C for 168±12 h
Temperature *Irradiation* *Test*	 20°C±10°C 25°C±3°C	 24°C±6°C 25°C±5°C
Bias *During Irradiation & Anneals* *Between Irradiation & Test*	 ±10%; Worst-case damage Device leads shorted (e.g., in conductive foam)	 ±10%; Worst-case damage Device leads shorted (e.g., in conductive foam)
Test Sequence *Time Between Irradiation & Test* *Time Between Multiple Irradiations*	 Begin within 1 h, end within 2 h 2 h maximum	 Begin within 1 h, end within 2 h 2 h maximum

that TM 1019.4 permits testing to be performed at the dose rate of the intended application if this is agreed to by the parties to the test [1]. BS 22900 suggests testing in a range of dose-rate *windows*, i.e., either between 1 to 10 rads(Si)/s or 0.01 to 0.1 rads(Si)/s and, once again, at the dose rate of the intended application if this is agreed to by the parties to the test [2]. Clearly, laboratory dose rates defined in both test methods differ by several orders of magnitude from dose rates typically encountered in space environments. The challenge in testing parts for use in space scenarios is then to predict their response based on measurements performed in the laboratory at moderate dose rates. Laboratory measurements have the advantage of being more controllable, practical, and cost effective. For example, performing a measurement at a space-like dose rate (i.e., ~ 1 mrad(Si)/s) might take months to years, is not practical for qualifying parts, and is fraught with pitfalls [5]. Both TM 1019.4 and BS 22900 attempt to extend results from laboratory measurements to space-like dose rates, but their approaches are somewhat different. The discussions below examine how these test methods assess TDE/PIE effects and simulate the effects of oxide-trapped charge growth/annealing responsible for IC leakage-related failures and interface-trap buildup responsible for timing-related failures.

Figure 6 illustrates how the failure dose of three commercial CMOS devices depends on the dose rate of the irradiation [18,28,29]. The "parametric" failure dose was defined as static power current in excess of 100 mA for OKI 81C55 2k and Harris HM6504 4k static RAMs, and 1 mA for SGS 4007 inverters, though the trends illustrated in the figure are independent of this exact definition. For these commercial devices, the failure dose either remains constant or improves as the dose rate is lowered [5,18,19]. A similar trend is observed for transistors built in a special radiation-soft process at Sandia (G1916A/W33) [18]. At the present time, testing at TM 1019.4 dose rates leads to a very conservative measure of the failure dose. Less-conservative variations of TM 1019.4 have been proposed for estimating the failure dose of commercial technologies [29,30]. These varia-

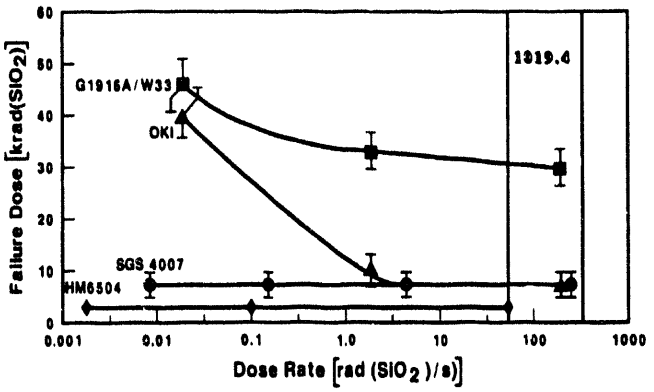

Fig. 6. Failure dose versus dose rate for three types of commercial MOS devices and a specially softened Sandia device (G1916A/W33). (After Refs. [18,29].)

tions typically allow for room-temperature biased anneals following irradiation in order to take advantage of oxide-trapped charge annealing and provide a more accurate and, therefore, less conservative estimate of failure dose in space. BS 22900 has the advantage of testing at lower dose rates. These lower dose rates provide a more accurate measure of failure dose for the space environment.

A major difference in the test methods is in the procedure used for the accelerated aging test that provides an estimate of timing-related failures for MOS microcircuits in low-dose-rate environments. This test is sometimes referred to as a "rebound" test. Both test methods employ an accelerated aging test, but details of the test differ. Specifically, TM 1019.4 calls for an additional irradiation to 0.5-times the specification prior to elevated temperature annealing and electrical test. The additional irradiation to 0.5-times the specified dose is required because of uncertainty in defining worst-case bias during irradiations and anneals [5,28,29]. Typically, irradiations and anneals are performed under static bias conditions, and do not account for the possibility of significantly enhanced rebound voltages often observed during switched-bias or ac irradiations [31-34]. To compensate for this uncertainty, margin is provided in the form of additional dose. In addition, one must consider the response of p-channel transistors, which following the elevated temperature anneal have (1) a lower value of V_{th} than observed in low-dose-rate irradiations (because of increased trapped-hole annealing at elevated temperatures), (2) greater drive than would be expected in the low-dose-rate environment, and therefore, (3) a slightly non-conservative estimate of timing degradation. BS 22900 does not require an additional irradiation to 0.5-times the specified dose, but instead seeks to accurately identify worst-case bias conditions during the evaluation phase to be applied during qualification testing. Both test methods do an excellent job of simulating interface-trap buildup and associated timing related failures in low-dose-rate environments, but TM 1019.4 is more conservative due to the overtest.

In recent years, it has been reported [35,36] that some modern bipolar technologies experience increased gain degradation as the dose rate of an irradiation is lowered. Bipolar technologies manufactured with polysilicon emitters, in which a sacrificial gate oxide is implanted through and remains in place over the base-emitter junction, have been observed to show this effect. This gain degradation results from increased surface recombination and base current due to the buildup of radiation-induced interface traps. For CMOS technologies, the accelerated aging test was designed to account for increased interface traps at lower dose rates. The thought was to try this test on bipolar technologies exhibiting similar dose-rate effects. The data in Fig. 7 [36] plots the increase in base current for standard emitter NPN transistors following a Co^{60} irradiation to 500 krads(Si) at 240 rads(Si)/s. In addition, these parts were annealed both at room and elevated temperatures ranging from 60 to 250°C. The figure clearly shows that neither room nor elevated temperature anneals exhibit *increased* gain degradation. Instead they show decreased gain degradation! The accelerated aging test specified in TM 1019.4 and BS 22900 will not work for this technology. The only approach to take is to measure at a lower dose rate. BS 22900's standard (1 to 10 rads(Si)/s) and low (0.01 to 0.1 rads(Si)/s) dose-rate windows will provide a more accurate measure of failure dose for this bipolar device. Once again, the reader is reminded that bipolar technology is specifically excluded from TM 1019.4's accelerated aging test. Users of TM 1019.4 would be well advised to irradiate parts from these technology at lower dose rates [36].

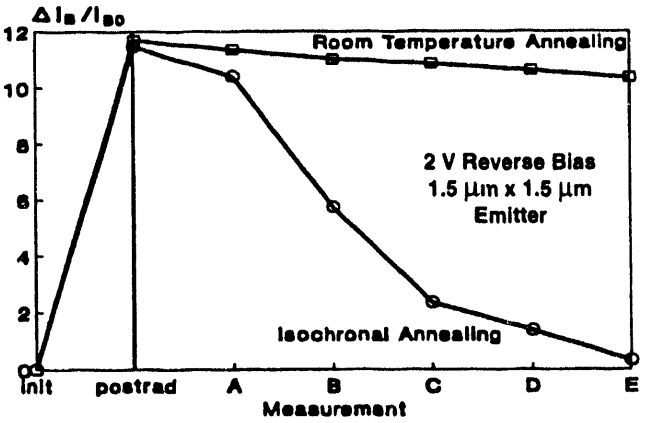

Fig. 7. Increase in base current, $\Delta I_B/I_{B0}$ of reverse-biased, standard emitter NPN transistors following (1) Co^{60} irradiation to 500 krads(Si) and (2) a series of room temperature and isochronal anneals at (A) 60°C, (B) 100°C, (C) 150°C, (D) 200°C, and (E) 250°C. (After Ref. [36].)

In addition to the differing dose requirement for rebound testing, TM 1019.4 and BS 22900 also differ slightly in their anneal schedules. Both TM 1019.4 and BS 22900 require a one-week biased anneal at 100°C. But 22900 also calls for an additional 24 h room temperature biased anneal prior to the elevated temperature anneal and subsequent electrical test. TM 1019.4 does not specify this anneal because previous work has shown that parts will experience the same buildup of interface traps (and timing degradation) under positive bias, even if interrupted by temporary storage in conductive foam [37]. To put this in perspective, it is useful to examine the effectiveness of the different anneals in extending laboratory measurements to the space environment. For reference, a 10-year space mission is equivalent to 3.2×10^8 seconds. If a part is irradiated to 100 krads(Si) at a dose rate of 1 rad(Si)/s, that takes 10^5 seconds. A

24-hour room temperature anneal is only an additional 0.86 x 10^5 seconds, and does little toward extending the time frame of measurement toward the space application. However, elevated temperature anneals are far more effective in extending the time scale. Both trapped-hole annealing and interface-trap buildup processes are temperature activated with activation energies, E_A, of ≈ 0.4 eV [4,38,39] and ≈ 0.8 eV [4,17,40,41], respectively. Therefore, elevated temperature anneals provide acceleration factors of ≈ 27 for trapped-hole annealing and ≈ 720 for interface-trap buildup. For the trapped holes, a one-week anneal at 100°C corresponds to $1.6x10^7$ seconds. For interface traps, which are more strongly activated, a one-week anneal at 100°C corresponds to $4.4x10^8$ seconds and provides excellent simulation for space application.

D. Advantages & Disadvantages

Ideally, both TM 1019.4 and BS 22900 allow the user to screen out "bad" parts and, at the same time, not be overly conservative by failing "good" parts unnecessarily. TM 1019.4 provides conservative measures of failure dose for space and tactical applications. It is easy and inexpensive to apply to ICs, permits effective inter-laboratory comparisons, is readily extendable to x-ray testers which can operate at higher dose rates, and provides significant flexibility to "parties to the test." This flexibility permits irradiations at the dose rate of the intended application. Since TM 1019.4 uses higher dose rates, it more readily supports QML, SPC, and other quality initiatives that depend on gathering large and statistically significant amounts of data. For space qualification, BS 22900 is less conservative than TM 1019.4 because it allows testing at lower dose rates closer to those encountered in space. For some technologies, lower dose rates provide more accurate measures of failure doses in space. These technologies include commercial CMOS dominated by oxide trapped charge buildup (most notably in isolation oxides) and some modern bipolar technologies, e.g., those with polysilicon emitters. BS 22900 also has a built-in flexibility that enables "parties to the test" to choose dose rates closer to that of the application. The latest versions of TM 1019.4 and BS 22900 are both improvements over previous issues.

In terms of disadvantages, BS 22900 is more time consuming and expensive than TM 1019.4 since it requires longer irradiation times. In addition, the evaluation flow at the vendor or user requires radiation effects expertise and potentially a great deal of latitude in test conditions. Some of this latitude may be unwanted and make comparisons between different laboratories more difficult. The biggest disadvantages of TM 1019.4 is that it provides a very conservative estimate of hardness for technologies that exhibit strong annealing of oxide-trapped charge and does not explicitly account for dose-rate effects in some modern bipolar technologies.

V. CONCLUSIONS

The QML approach to radiation hardness assurance "builds in" the quality of parts, as opposed to relying on expensive end-of-line testing. QML is cost effective and permits easy migration to next generation technology. A key to applying QML is identifying the technology parameters that control the radiation hardness and bringing them under SPC. This is vital since there are many sources of variation including lot-to-lot, wafer-to-wafer, and intrawafer. As die size increases in the realm of several square centimeters, even intradie variations may be significant. Caution should be exercised in procuring parts from a commercial vendor who may not fully understand or control the technology parameters relevant to the radiation response. SPC can best be accomplished by wafer-level testing. An x-ray/wafer-level test system is cost-effective, supports SPC and improvement of technology parameters relevant to the radiation response, and should be extendible to qualification/lot acceptance. Several researchers in the past have demonstrated an excellent correlation between x-ray and Co^{60} test results. Both TM 1019.4 and BS 22900 provide reasonable estimates of IC response for low-dose-rate space applications. In many ways, the test methods are quite similar. Major differences occur in the allowable dose rates used and some details of the "rebound" test. TM 1019.4 places a premium on consistent, repeatable, and reproducible results while BS 22900 seeks to simulate the space environment more closely.

VI. ACKNOWLDEGMENTS

The authors wish to thank Lew Cohn of the Defense Nuclear Agency and Harvey Eisen of the Army Research Laboratory who championed the latest revision of Test Method 1019.4. Special thanks to Len Adams and Bengt Johlander of the European Space Agency and Professor Andy Holmes-Siedle of Brunel University for many stimulating discussions. Finally, we would like Dr. Jean-Luc Leray and the RADECS conference organizers for this opportunity to share our thoughts on advanced qualification techniques.

VII. REFERENCES

[1] Military Standard, Test Methods and Procedures for Microelectronics, MIL-STD-883D, Method 1019.4, Steady State Total Dose Irradiation, released January 1992.

[2] Total Dose Steady-State Irradiation Test Method, ESA/SCC Basic Specification No. 22900, Draft Issue 5, July 1993.

[3] A. H. Johnston, "Super Recovery of Total Dose Damage in MOS Devices," IEEE Trans. Nucl. Sci. NS-31, 1427 (1984).

[4] J. R. Schwank, P. S. Winokur, P. J. McWhorter, F. W. Sexton, P. V. Dressendorfer, and D. C. Turpin, "Physical Mechanisms Contributing to Device Rebound," IEEE Trans. Nucl. Sci. NS-31, 1434 (1984).

[5] D. M. Fleetwood, P. S. Winokur, and J. R. Schwank, "Using Laboratory X-ray and Cobalt-60 Irradiations to Predict CMOS Device Response in Strategic and Space Environments," IEEE Trans. Nucl. Sci. NS-35, 1497 (1988).

[6] L. J. Palkuti and J. J. LePage, "X-Ray Wafer Probe for Total Dose Testing," IEEE Trans. Nucl. Sci. NS-29, 1832 (1982).

[7] D. M. Fleetwood, R. W. Beegle, F. W. Sexton, P. S. Winokur, S. L. Miller, R. K. Treece, J. R. Schwank, R. V. Jones, and P. J. McWhorter, "Using a 10-keV X-ray Source for Hardness Assurance," IEEE Trans. Nucl. Sci. NS-33, 1330 (1986).

[8] J. H. Stephen, T. K. Sanderson, D. Mapper, and J. Farren, "Cosmic Ray

Simulation Experiments for the Study of Single Event Upsets and Latchup in CMOS Memories," IEEE Trans Nucl. Sci. NS-30, 4464 (1983).

[9] A. Costantine, J. W. Howard, M. Becker, R. C. Block, L. S. Smith, G. A. Soli, and M. C. Stauber, "A New Method for Using Cf^{252} in SEU Testing," IEEE Trans Nucl. Sci. NS-37, 1916 (1990).

[10] S. P. Buchner, D. Wilson, K. Kang, D. Gill, and J. A. Maser, "Laser Simulation of Single Event Upset," IEEE Trans Nucl. Sci., NS-34, 1228 (1987).

[11] K. Richter and I. Arimura, "Simulation of Heavy Charged Particle Tracks Using Focussed Laser Beams," IEEE Trans Nucl. Sci. NS-34, 1234 (1987).

[12] MIL-I-38535B, "General Specification for Integrated Circuits (Microcircuits) Manufacturing," dated 1 June 1993.

[13] P. S. Winokur, F. W. Sexton, D. M. Fleetwood, M. D. Terry, M. R. Shaneyfelt, P. V. Dressendorfer, and J. R. Schwank, "Implementing QML for Radiation Hardness Assurance," IEEE Trans. Nucl. Sci. NS-37, 1794 (1990).

[14] M. R. Shaneyfelt, K. L. Hughes, J. R. Schwank, F. W. Sexton, D. M. Fleetwood, and P. S. Winokur, "Wafer-Level Radiation Testing for Hardness Assurance," IEEE Trans. Nucl. Sci. NS-38, 1598 (1991).

[15] J. Scarpulla, A. L. Amram, V. W. Gin, T. C. Morse, and K. T. Nakamura, "Gate Size Dependence of the Radiation-Produced Changes in Threshold Voltage, Mobility, and Interface State Density in Bulk CMOS," IEEE Trans. Nucl. Sci. NS-39, 1990 (1992).

[16] M. R. Shaneyfelt, D. M. Fleetwood, P. S. Winokur, J. R. Schwank, and T. L. Meisenheimer, "Effects of Device Scaling and Geometry on MOS Radiation Hardness Assurance," IEEE Trans. Nucl. Sci. NS-40, (1993); accepted for publication.

[17] P. S. Winokur, "Radiation-Induced Interface Traps," in Ionizing Radiation Effects in MOS Devices and Circuits (New York, Wiley, 1989), Eds. Ma and Dressendorfer, Chapter 4; also, T. R. Oldham, F. B. McLean, H. E. Boesch, Jr., and J. M. McGarrity, "An Overview of Radiation-Induced Interface Traps in MOS Structures," Semicond. Sci. Technol. 4, 986 (1989).

[18] P. S. Winokur, F. W. Sexton, J. R. Schwank, D. M. Fleetwood, P. V. Dressendorfer, T. F. Wrobel, and D. C. Turpin, "Total-Dose Radiation and Annealing Studies: Implications for Hardness Assurance Testing," IEEE Trans. Nucl. Sci. NS-33, 1343 (1986).

[19] P. S. Winokur, F. W. Sexton, G. L. Hash, and D. C. Turpin, "Total-Dose Failure Mechanisms of Integrated Circuits in Laboratory and Space Environments," IEEE Trans. Nucl. Sci. NS-34, 1448 (1987).

[20] ASTM-F1467, "Standard Guide for the Use of an X-Ray Tester (≈ 10-keV Photons) in Ionizing Radiation Effects Testing of Microelectronic Devices," Eighth Draft dated 26 June 1992.

[21] G. A. Ausman, Jr. and F. B. McLean, "Electron-Hole Pair Creation Energy in SiO_2," Appl. Phys. Lett. 26, 173 (1975).

[22] J. M. Benedetto and H. E. Boesch, Jr., "The Relationship Between Co^{60} and 10 keV X-Ray Damage in MOS Devices," IEEE Trans. Nucl. Sci. NS-33, 1318 (1986).

[23] M. R. Shaneyfelt, D. M. Fleetwood, J. R. Schwank, and K. L. Hughes, "Charge Yield for 10-keV X-Ray and Cobalt-60 Irradiation of MOS Devices," IEEE Trans. Nucl. Sci. NS-38, 1187 (1991).

[24] D. B. Brown, "Photoelectron Effects on the Dose Deposited in MOS Devices By Low-Energy X-Ray Sources," IEEE Trans. Nucl. Sci. NS-33, 1240 (1986).

[25] C. M. Dozier and D. B. Brown, "The Use of Low Energy X Rays for Device Testing - A Comparison With Co-60 Radiation," IEEE Trans. Nucl. Sci. NS-30, 4382 (1983).

[26] D. M. Fleetwood, D. E. Beutler, L. J. Lorence, Jr., D. B. Brown, B. L. Draper, L. C. Riewe, H. B. Rosenstock, and D. P. Knott, "Comparison of Enhanced Device Response and Predicted X-Ray Dose Enhancement Effects on MOS Oxides," IEEE Trans. Nucl. Sci. NS-35, 1265 (1988).

[27] D. M. Fleetwood, S. S. Tsao, and P. S. Winokur, "Total-Dose Hardness Assurance of SOI MOSFETs," IEEE Trans. Nucl. Sci. NS-35, 1361 (1988).

[28] D. M. Fleetwood, P. S. Winokur, L. C. Riewe, and R. L. Pease, "An Improved Standard Total Dose Test for CMOS Space Electronics," IEEE Trans. Nucl. Sci. NS-36, 1963 (1989).

[29] D. M. Fleetwood, P. S. Winokur, and T. L. Meisenheimer, "Hardness Assurance for Low-Dose Space Applications," IEEE Trans. Nucl. Sci. NS-38, 1552 (1991).

[30] F. W. Sexton, D. M. Fleetwood, C. C. Aldridge, G. Garrett, J. C. Pelletier, and J.I. Gaona, Jr., "Qualifying Commercial ICs for Space Total-Dose Environments," IEEE Trans. Nucl. Sci. NS-39, 1869 (1992).

[31] P. V. Dressendorfer, J. M. Soden, J. J. Harrington, and T. V. Nordstrom, "The Effects of Test Conditions on MOS Radiation-Hardness Results," IEEE Trans. Nucl. Sci. NS-28, 4281 (1981).

[32] T. Stanley, D. Neamen, P. Dressendorfer, J. Schwank, P. Winokur, M. Ackermann, K. Jungling, C. Hawkins, and W. Grannemann, "The Effect of Operating Frequency in the Radiation Induced Buildup of Trapped Holes and Interface States in MOS Devices," IEEE Trans. Nucl. Sci. NS-32, 3982 (1985).

[33] D. M. Fleetwood, P. V. Dressendorfer, and D. C. Turpin, "A Reevaluation of Worst-Case Postirradiation Response for Hardened MOS Transistors," IEEE Trans. Nucl. Sci. NS-34, 1178 (1987).

[34] D. M. Fleetwood, P. S. Winokur, and L. C. Riewe, "Predicting Switched-Bias Response From Steady-State Irradiations," IEEE Trans. Nucl. Sci. NS-37, 1806 (1990).

[35] E. W. Enlow, R. L. Pease, W. Combs, R. D. Schrimpf, and R. N. Nowlin, "Response of Advanced Bipolar Processes to Ionizing Radiation," IEEE Trans. Nucl. Sci. NS-38, 1342 (1991).

[36] R. N. Nowlin, D. M. Fleetwood, R. D. Schrimpf, R. L. Pease, and W. E. Combs, "Hardness-Assurance and Testing Issues for Bipolar/BiCMOS Devices," IEEE Trans. Nucl. Sci. NS-40, (1993); accepted for publication.

[37] D. M. Fleetwood and P. V. Dressendorfer, "A Simple Method to Identify Radiation and Annealing Biases That Lead to Worst Case CMOS Static RAM Postirradiation Response," IEEE Trans. Nucl. Sci. NS-34, 1408 (1987).

[38] G. F. Derbenwick and H. H. Sander, "CMOS Hardness Predictions for Low- Dose-Rate Environments," IEEE Trans. Nucl. Sci. NS-24, 2244 (1977).

[39] J. R. Schwank, D. M. Fleetwood, M. R. Shaneyfelt, P. S. Winokur, C. L. Axness, and L. C. Riewe, "Latent Interface-Trap Buildup and Its Implications For Hardness Assurance," IEEE Trans. Nucl. Sci. NS-39, 1953 (1992).

[40] P. S. Winokur, H. E. Boesch, Jr., J. M. McGarrity, and F. B. McLean, "Field- and Time-Dependent Radiation Effects at the SiO_2/Si Interface of Hardened MOS Capacitors," IEEE Trans. Nucl. Sci. NS-24, 2113 (1977).

[41] N. S. Saks, C. M. Dozier, and D. B. Brown, "Time Dependence of Interface Trap Formation in MOSFETs Following Pulsed Irradiation," IEEE Trans. Nucl. Sci. NS-35, 1168 (1988).

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