Investigation of Plasma Etch Induced Damage in Compound Semiconductor Devices

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We have investigated the electrical performance of mesa-isolated GaAs pn-junction diodes to determine the plasma-induced damage effects from reactive ion and reactive ion beam etching. A variety of plasma chemistries ($SiCl_4$, BCl_3, BCl_3/Cl_2, and Cl_2) and ion energies ranging from 100 to 400 eV were studied. We have observed that many of the RIE BCl_3/Cl_2 plasmas and RIBE Cl_2 plasmas yield diodes with low reverse-bias currents that are comparable to the electrical characteristics of wet-chemical-etched devices. The reverse-bias leakage currents are independent of surface morphology and sidewall profiles.

I. INTRODUCTION

Plasma etching is a critical element in the fabrication of compound semiconductor devices due to the requirements of anisotropic profiles and sub-micron features for high-density integrated circuits and optoelectronic devices. The anisotropic profile achieved with many plasma etch techniques is due to the acceleration of energetic ions from the plasma discharge to the sample. As these energetic ions strike the sample, surface damage as deep as 100 nm can occur,[1] causing degradation of electrical and optical properties of the device. Plasma-induced surface damage includes defects or dislocations in the lattice, formation of dangling bonds on the surface, implanted etch ions, or deposition of material on the sample.

Reactive ion etching (RIE) is a commonly used plasma etch technique for patterning III-V devices. RIE typically operates at discharge pressures less than 100 mTorr and ion energies

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greater than 100 eV. Since the sample is located on the powered electrode, it is directly exposed to the plasma and the energetic ions. This leads to highly anisotropic etching but can also create surface damage. Attempts to minimize the damage by reducing the ion energy below the damage threshold for compound semiconductors (< 40 eV)[2] or by increasing the chemical component of the etch results in a more isotropic etch and significantly limits minimum dimensions. Reactive ion beam etching (RIBE) uses a remote ECR-generated plasma with ion extraction grids placed between the plasma and the sample. The ion extraction grids allow for independent control of beam current (plasma power), and beam energy (extraction potential). The highly collimated beam provides extremely anisotropic etching at beam energies between 100 and 1000 eV. Although the energetic beam has potential for kinetic damage to the sample, sidewall damage may be quite low due to the directional nature of the beam. However, relatively little is known about the electrical degradation induced by etching with RIBE.

Plasma-induced surface and sidewall damage has been studied in III-V material for a variety of etching techniques.[1-15] Surface and luminescence techniques provide significant chemical and structural information about process-induced damage; however, the effects on electrical characteristics are most important for device fabrication and circuit design. Electrical studies have investigated RIE-induced surface damage on planar Schottky gate structures such as metal-semiconductor field effect transistors (MESFETs) and high electron mobility transistors (HEMTs).[3,4]

It is important to investigate the effects of plasma-induced sidewall damage on III-V pn-junction devices. Generally these devices are mesa isolated with the metallurgical junction exposed at the perimeter. Consequently, devices with large perimeter to area ratios are extremely sensitive to sidewall damage, which can affect both forward- and reverse-bias currents. Contributions by perimeter components to pn-junction forward-bias I-V characteristics have been studied[16] but little has been reported on reverse-bias I-V characteristics which are important for base-collector junctions of heterojunction bipolar transistors (HBTs) and p-i-n diodes. Fabrication of these devices is becoming more dependent on plasma etch techniques such as RIE and RIBE.

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In this paper we report plasma-induced sidewall damage effects on reverse-bias electrical characteristics of pn-junction diodes using RIE and RIBE. These data are compared to a baseline wet-chemical etch process. Both chemically and physically induced damage from plasma etching are reported. Reverse-bias leakage currents are found to have very different characteristics depending on the etch chemistry and technique. Plasma chemistries including $SiCl_4$, BCl_3, BCl_3/Cl_2 and Cl_2 at ion energies ranging from 100 to 400 eV are studied. In addition to electrical characteristics, etch rates, mesa sidewall profile, and surface morphology are reported.

II. EXPERIMENTAL

The GaAs devices used in this study are one-sided homojunction GaAs diodes grown in a Varian GEN-II MBE system. Beryllium and silicon are the p- and n-type dopants, respectively. The device structure consists of 0.5 μm n^+-doped (2×10^{18} cm^{-3}) on a n^+ substrate, a 0.5 μm n-doped epi-layer (1×10^{17} cm^{-3}), a 0.5 μm p layer (2×10^{18} cm^{-3}), and a 0.5 μm highly doped p^+ (2×10^{19} cm^{-3}) cap layer.

Diode fabrication up to the mesa etch step involves backside metallization with e-beam evaporated Ge/Au/Ni/Au metal followed by a frontside thermally evaporated Be/Au metal using a liftoff mask. All contacts are annealed at 370°C for 30 sec. The photoresist etch mask is 1.4 μm thick and slightly larger than the top-side metal contact to prevent surface damage of the mesa structure. Prior to mesa etch, the patterned wafer is exposed to an O_2 plasma for 4 min to prevent delayed etch initiation due to photoresist residue. All samples used are 100 mm^2 pieces. The wet-chemical etches are done in 1:4:45 $H_3PO_4/H_2O_2/H_2O$ for approximately 4 min to a target depth of 1.8 μm $\pm$ 0.2 μm. Reverse leakage currents at various locations on the wafer are measured to verify uniform growth across the wafer.

RIE etches are done in a 13.56 MHz rf-powered parallel plate Semi-Group RIE system. Gases are distributed through a showerhead arrangement located in the upper electrode. The lower electrode is 30.5 cm in diameter with an interelectrode spacing of approximately 3.8 cm and is completely covered with a 3.2-mm thick quartz plate. Samples are attached to the quartz plate with

a low-vapor-pressure thermal paste to ensure good thermal conduction. Immediately before loading the samples, the native oxide is removed with a 30 sec $NH_4OH:DI$ H_2O (1:20) rinse. DC biases of 100, 200, and 325 V (corresponding to power densities ranging from 0.055 to 0.20 Wcm^{-2}) at a total gas flow of 14 sccm and a pressure of 5 mT have been studied.

The RIBE system used in this study is a custom-built, load-locked reactor equipped with an Astex ECR plasma source modified by the addition of a pair of 12 cm-diameter, pyrolytic-graphite ion-extraction grids. The sample is located 35 cm from the grids and is mounted with a low-vapor-pressure thermal paste to a water-cooled stage. RIBE etches are performed at room temperature using Cl_2 gas flows of 3 and 7.8 sccm, 0.1 and 0.25 mTorr pressure, and 300 and 400 eV beam energy at 60 mA beam current.

Etch rates are calculated from the depth of the etched feature measured with a Dektak stylus profilometer. Surface morphology, anisotropy, and sidewall undercutting are evaluated with a scanning electron microscope (SEM). Samples are cleaved through an 8- to 10- μm wide feature and coated with a thin film of Au (10 nm) to prevent charging. Plasma-etch-induced damage effects on the electrical performance of pn-junction diodes are evaluated by measuring the room-temperature, dark reverse current of 60 x 60 μm^2 diodes. Reverse-bias currents from 0 to -8 V bias are compared for the different etch conditions. An HP 4145B parameter analyzer with guarded triax cables up to the probe tip is used for measurements. The pn-junction diodes were screened in both forward- and reverse-bias to verify good rectifying performance. Typical forward turn-on voltage is 1 V at 1 mA and reverse-bias breakdown voltage is -18 V. The reverse-bias dark current data reported are averages of 5 to 10 devices and represents typical diode characteristics across the sample.

III. RESULTS AND DISCUSSION

A. Etch Rates

GaAs etch rates are shown in Fig. 1 as a function of dc bias for BCl_3, $SiCl_4$, and Cl_2 flow percentages of 10, 25, 50, and 75% in BCl_3 (total flow is 14 sccm). Reported etch rates combine

results from both GaAs monitors and pn-junction devices. Monitors are used to determine the time required to etch the devices to a target depth of 1.8 μm. Device etch rates range from 75 nm/min to 1.1μm/min, with corresponding etch times of 1.5 to 24 min. The GaAs etch rate in BCl_3 is quite low and virtually independent of dc bias. The $SiCl_4$ RIE GaAs etch rate is approximately a factor of 2 greater than that of BCl_3 at 100 V and increases by almost an additional factor of 2 at 325 V. At 100 V dc bias, the GaAs etch rate increases with the addition of Cl_2 to the BCl_3 plasma. In contrast, at 200 and 325 V the 50 and 75% Cl_2 show a decrease in etch rate, which is discussed below.

Since BCl_3 is a scavenger of O_2 and H_2O, the etch data at low BCl_3 concentrations may be affected by moisture in the chamber. In fact, the RIE is not load-locked so we expect an etch initiation period for GaAs etching with BCl_3/Cl_2 chemistries. This explanation is supported by our observation that virtually no GaAs etching occurs in a pure Cl_2 RIE plasma. Furthermore, when the low BCl_3 concentration etches are run for longer times, so that the etch initiation period becomes a smaller fraction of the total etch time, we calculate higher GaAs etch rates with increasing etch times. The etch initiation period has not been quantified in this study and is expected to vary significantly as a function of the BCl_3 concentration and the moisture in the chamber. This may account for the decrease in the etch rate of GaAs as the Cl_2 concentration increases as well as the large variation in the etch rates in Fig. 1.

B. Surface Morphology

Surface morphology and etch profiles have been studied to evaluate trends relative to the electrical characteristics of pn-junction diodes. Scanning electron micrographs of the wet-chemical etch control samples are shown in Fig. 2. The etch is isotropic with crystallographic dependence and slightly rough sidewalls and surfaces. GaAs mesas etched in the RIE show sidewall profiles and roughness which vary significantly over the parameter space studied. Features etched in a BCl_3 plasma are very anisotropic with smooth sidewalls and surfaces (Fig. 3). With the addition of Cl_2 to the BCl_3 plasma the etch becomes more isotropic with very rough sidewalls and

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surfaces. These characteristics are more pronounced as the Cl_2 percentage increases to 75% (see Fig. 4). The $SiCl_4$ etches are anisotropic with widely varying roughness of the sidewall and surface. Pre-treating the GaAs surfaces with a H_2 plasma prior to $SiCl_4$ etches tends to smooth out the surface and sidewall morphologies. The Cl_2 RIBE etch is very anisotropic with smooth sidewalls and surfaces.

C. Electrical Characteristics

The data reported for reverse-bias current characteristics of pn-junction diodes show general trends resulting from plasma-induced damage and are displayed as current density versus applied voltage, J-V curves. Reverse-bias current characteristics are collectively contrasted and compared to wet-chemical-etched diode characteristics, which are considered the baseline.

All etches done in the RIE at 100 V dc bias have similar reverse-bias currents as compared to the baseline wet-chemical etch (Fig. 5), however, a sharp increase is seen for 100% BCl_3 below -6 V. The ion energies at 100 V dc etch bias are relatively low and, as the Cl_2 concentration is increased, the chemical component of the plasma is expected to dominate the etch. Although the addition of Cl_2 to the BCl_3 plasma results in an isotropic etch profile with significant sidewall and field roughness (see figures 3 and 4), there is virtually no difference in the reverse-bias current density, suggesting that the low energy, chemically dominated etch produces low sidewall damage and electronic traps.

A similar trend is observed for 200 V dc etch bias conditions where the data are comparable to the wet-chemical etch (Fig. 6). However, the 100% BCl_3 and 10% Cl_2 data shows reverse-bias currents which are slightly worse than the wet-chemical etch at applied voltages less negative than -6 V, but approximately an order of magnitude leakier at more negative voltages. As the dc etch bias becomes more negative, the ion energies and physical nature of the etch also increases, however the reverse-bias currents at 200 V are similar to 100 V indicating low sidewall damage at these plasma parameters.

High bias conditions of 325 V yield the poorest reverse-bias current characteristics. For the entire range investigated (0 to -8 V), the reverse-bias current density increases with increasing Cl_2 up to 25%, which exhibits the poorest characteristics of all the etch conditions investigated (Fig. 7). At 50 and 75% Cl_2, the reverse-bias current densities are comparable to the data obtained at 100% BCl_3 which is approximately one order of magnitude higher than the wet-chemical etch. The higher dc etch bias yields greater physical etching, which causes more plasma-induced sidewall damage and hence leakier diodes.

Definite trends are observed in the reverse-bias current densities as a function of RIE dc etch bias (100, 200, and 325 V). In general, increasing dc etch bias produces leakier diodes due to greater plasma-induced sidewall damage. With the addition of Cl_2 the reverse-bias current densities show minimal dependence on the dc etch bias between 100 and 200V. At 200 and 325 V etch bias, the reverse-bias current density increases as small concentrations of Cl_2 are added to BCl_3 (10% Cl_2 at 200 V and 10 and 25% Cl_2 at 325 V). Further addition of Cl_2 (25, 50, and 75% at 200 V and 50 and 75% Cl_2 at 325 V) however, shows an increase in reverse-bias leakage current density. This implies that an optimum ratio of Cl_2:BCl_3 exists for each of the dc etch biases where the plasma-induced sidewall damage is minimized. This ratio may be related to the competition between the chemical and physical desorption of sidewall and surface material; however, quantitative surface analysis may be required to identify the responsible reaction mechanisms.

Reverse-bias current density versus applied voltage for diodes etched in $SiCl_4$ is shown in Figure 8. Although only two $SiCl_4$ etch conditions are shown, several conditions comparing the effect of pre-treating the surface with a H_2 plasma have been investigated. Diodes etched without H_2 pre-treatment show large variations in reverse-bias current density over the die. However, diodes etched with H_2 pre-treatment show small variations over the die and considerably smoother surfaces. Regardless of the pre-treatment, all $SiCl_4$ etches yield leaky reverse-bias current density characteristics, as much as 4 orders of magnitude greater than the wet-chemical-etched devices.

The reverse-bias leakage characteristics of pn-junction diodes for RIBE are shown in Fig. 9. The results show low leakage currents that are comparable to the wet-chemical-etched devices. In addition, the reverse-bias currents are nearly independent over the beam energies and pressures studied. These results imply low sidewall damage which we attribute to the directional nature of the beam and the low process pressure. Etching at such low pressures minimizes scattering of both ions and neutrals in the chamber, reducing the potential for energetic impact with the mesa sidewalls.

IV. CONCLUSIONS

We have examined the plasma-induced sidewall damage effects from reactive ion and reactive ion beam etching using reverse-bias leakage current data of mesa-isolated GaAs pn-junction diodes. Etch rates and surface morphology are also reported. We have observed that high concentrations of Cl_2 in a BCl_3 RIE plasma yield low-reverse-leakage-current diodes comparable to those of wet-chemical-etched devices. Reverse-bias leakage current densities are independent of surface morphology and sidewall profiles. The RIE $SiCl_4$ etches yield leaky reverse-bias current density characteristics independent of the dc etch bias. In addition to RIE results, high-ion-energy RIBE Cl_2 plasmas produce minimal sidewall damage and are comparable to wet-chemical etching. These results are significant for dry etch process development for pn-junction devices such as HBTs, solar cells, and photodiodes.

ACKNOWLEDGMENTS

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Figure Captions

Fig. 1. RIE etch rate of GaAs at 5 mTorr and 14 sccm for BCl_3, $SiCl_4$, and various concentrations of Cl_2 in BCl_3 as a function of the dc etch bias.

Fig. 2. SEM micrographs showing the (a) profile and (b) surface and sidewall morphology of wet-chemical-etched GaAs.

Fig. 3. SEM micrographs showing the (a) profile and (b) surface and sidewall morphology of GaAs etched in BCl_3 at 100 V dc etch bias.

Fig. 4. SEM micrographs showing the (a) profile and (b) surface and sidewall morphology of GaAs etched in 75% Cl_2 in BCl_3 at 100 V dc etch bias.

Fig. 5. Current density versus diode bias (J-V) characteristics of pn-junction diodes etched in the RIE at various Cl_2/BCl_3 concentrations and 100 V dc etch bias.

Fig. 6. J-V characteristics of pn-junction diodes etched in the RIE at various Cl_2/BCl_3 concentrations at 200 V dc etch bias.

Fig. 7. J-V characteristics of pn-junction diodes etched in the RIE at various Cl_2/BCl_3 concentrations at 325 V dc etch bias.

Fig. 8. J-V characteristics of pn-junction diodes RIE etched in $SiCl_4$.

Fig. 9. J-V characteristics of pn-junction diodes RIBE etched.

DISCLAIMER

RIE

$Cl_2:BCl_3(X:Y)$

(25:75)

(75:25)

(50:50)

(10:90)

$SiCl_4$

BCl_3

Etch Rate (μm/min)

DC Bias Voltage (V)

Figure 1

a

b

Figure 2

b

a

Figure 3

Figure 4

Cl$_2$:BCl$_3$ RIE @ 100 V Bias

Current Density (A/cm^2)

Applied Voltage (V)
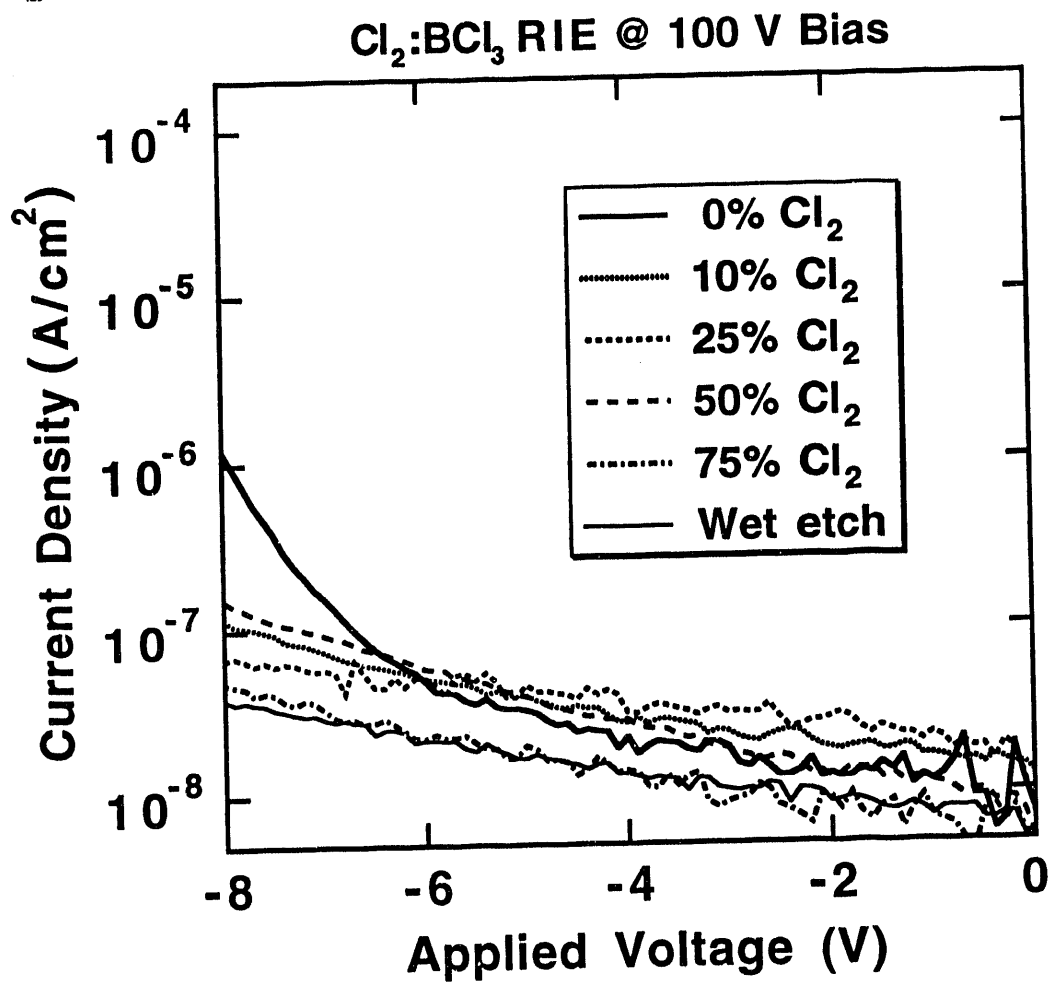
Legend:
- 0% Cl$_2$
- 10% Cl$_2$
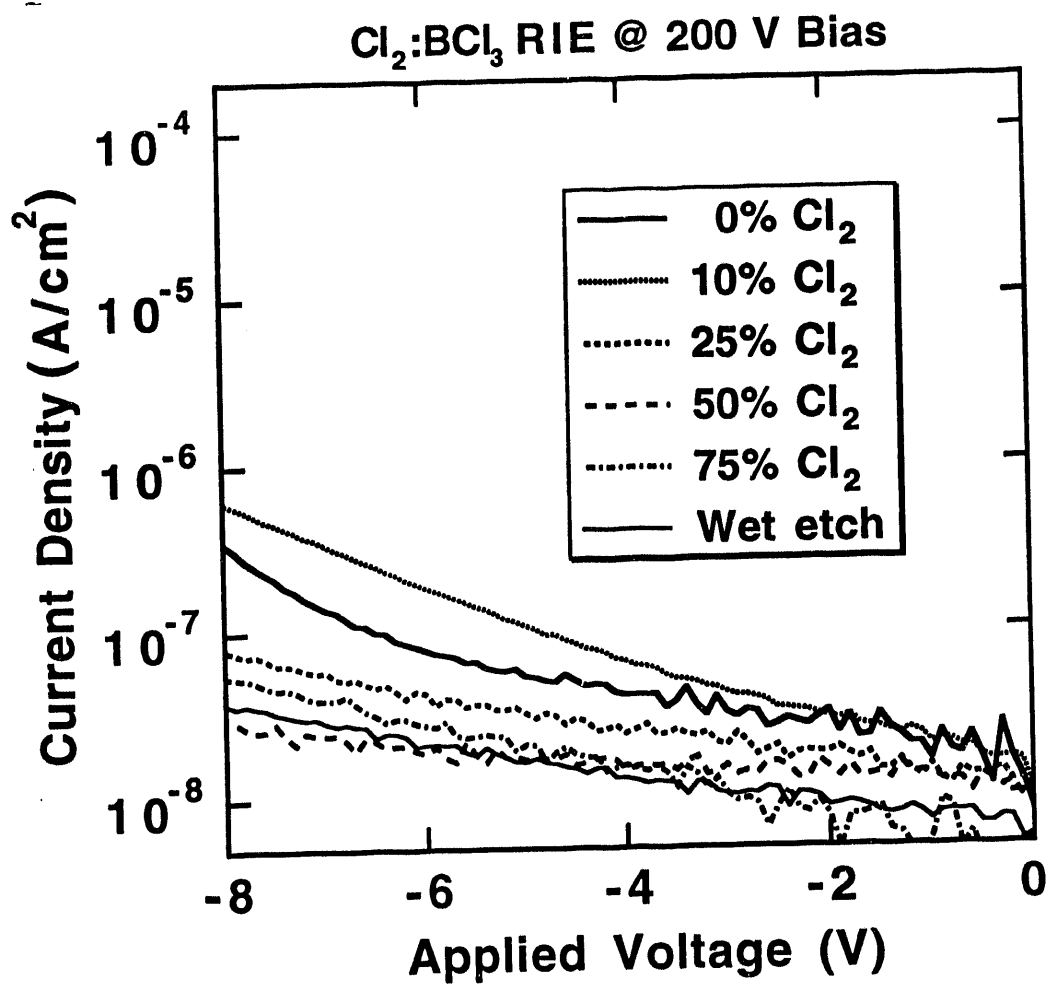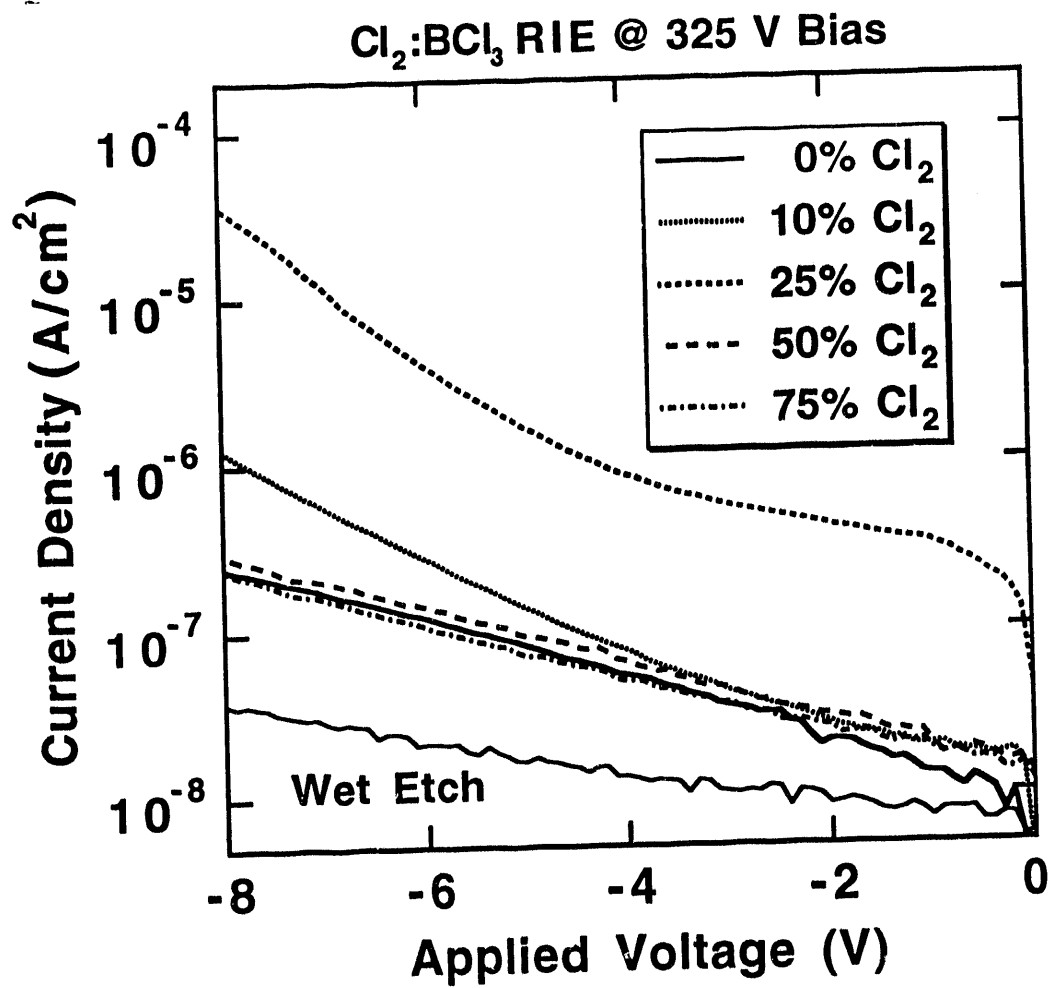- 25% Cl$_2$
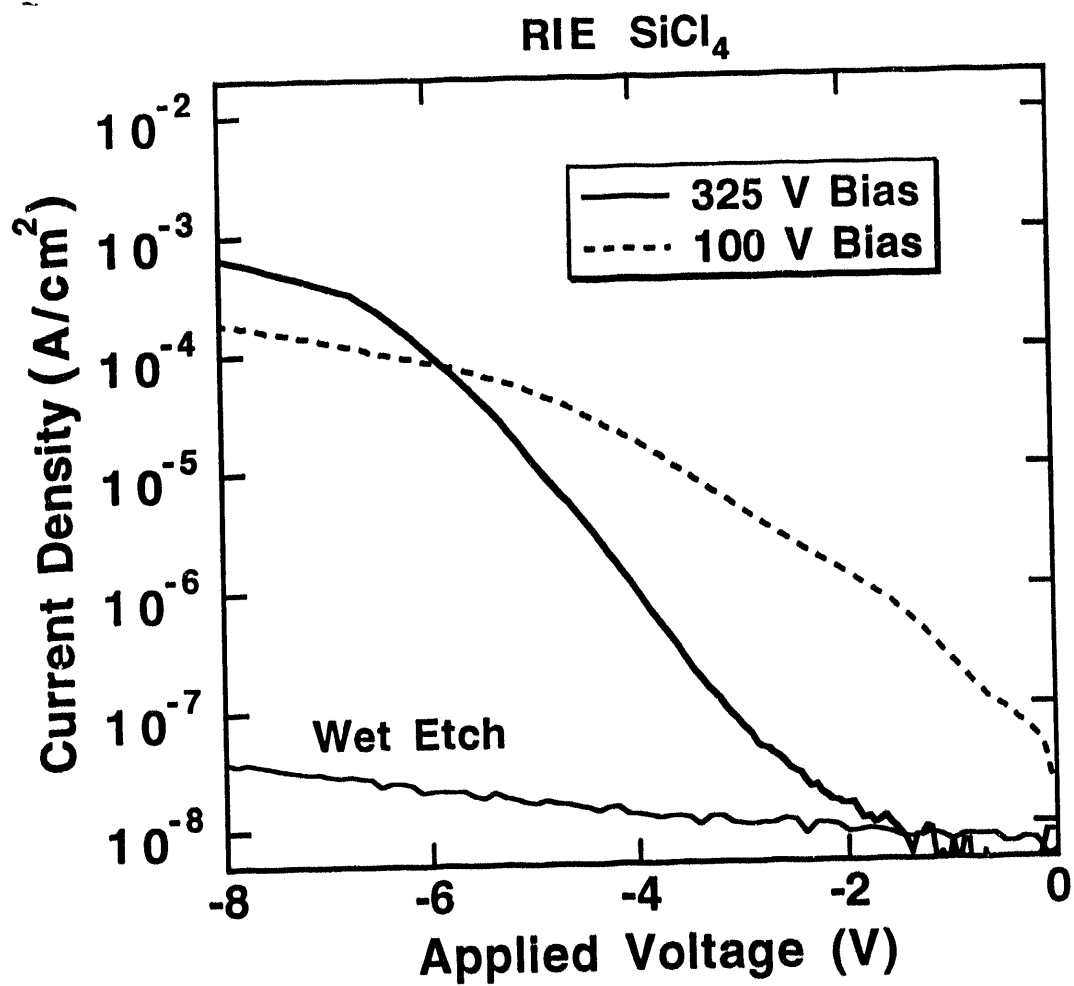- 50% Cl$_2$
- 75% Cl$_2$
- Wet etch

Figure 5

Figure 6

Figure 7

Figure 8
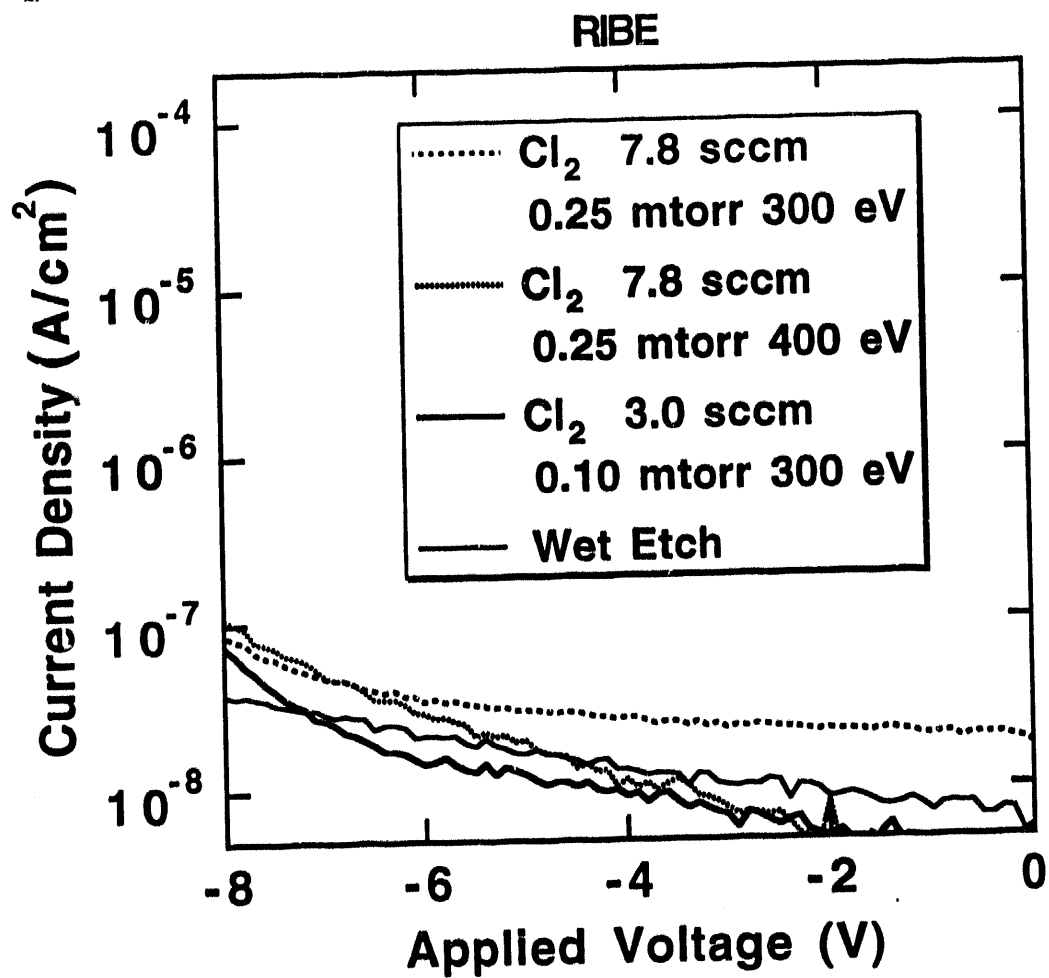
Figure 9

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