SANDIA REPORT
SAND2011-0099
Unlimited Release
Printed January 2011

Stress Testing on Silicon Carbide Electronic Devices for Prognostics and Health Management

Robert Kaplar, Matthew Marinella, Reinhard Brock, Michael King, Mark A. Smith, Stanley Atcitty

Prepared by
Sandia National Laboratories
Albuquerque, New Mexico 87185 and Livermore, California 94550

Sandia National Laboratories is a multi-program laboratory managed and operated by Sandia Corporation, a wholly owned subsidiary of Lockheed Martin Corporation, for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

Issued by Sandia National Laboratories, operated for the United States Department of Energy by Sandia Corporation.

Available to DOE and DOE contractors from
U.S. Department of Energy
Office of Scientific and Technical Information
P.O. Box 62
Oak Ridge, TN 37831

Telephone: (865) 576-8401
Facsimile: (865) 576-5728
E-Mail: reports@adonis.osti.gov
Online ordering: http://www.osti.gov/bridge

Available to the public from
U.S. Department of Commerce
National Technical Information Service
5285 Port Royal Rd.
Springfield, VA 22161

Telephone: (800) 553-6847
Facsimile: (703) 605-6900
E-Mail: orders@ntis.fedworld.gov
Online order: http://www.ntis.gov/help/ordermethods.asp?loc=7-4-0#online

SAND2011-0099
Unlimited Release
Printed January 2011

Stress Testing on Silicon Carbide Electronic Devices for Prognostics and Health Management

Robert Kaplar, Matthew Marinella, Reinhard Brock, and Michael King
Radiation Hard CMOS Technology Development
Mark A. Smith
Systems Readiness and Sustainment Technologies
Stanley Atcitty
Energy Infrastructure and Distributed Energy Resources
Sandia National Laboratories
P.O. Box 5800
Albuquerque, New Mexico 87185-MS1188

Abstract

Power conversion systems for energy storage and other distributed energy resource applications are among the drivers of the important role that power electronics plays in providing reliable electricity. Wide band gap semiconductors such as silicon carbide (SiC) and gallium nitride (GaN) will help increase the performance and efficiency of power electronic equipment while condition monitoring (CM) and prognostics and health management (PHM) will increase the operational availability of the equipment and thereby make it more cost effective. Voltage and/or temperature stress testing were performed on a number of SiC devices in order to accelerate failure modes and to identify measureable shifts in electrical characteristics which may provide early indication of those failures. Those shifts can be interpreted and modeled to provide prognostic signatures for use in CM and/or PHM. Such experiments will also lead to a deeper understanding of basic device physics and the degradation mechanisms behind failure.

ACKNOWLEDGMENTS

This work has been sponsored by the United States Department of Energy (DOE) Office of Electricity Delivery and Energy Reliability (OE) under contract to Sandia National Laboratories. The authors would like to thank Imre Gyuk of DOE for giving us the opportunity to pursue this work. We would also like to thank James Stanley of the Radiation Hard CMOS Technology Development in Sandia National Laboratories' Microsystems Science, Technology and Components Center who built and calibrated much of the equipment.

TABLE OF CONTENTS

LIST OF FIGURES

PREFACE

This is the final report of Phase II of the Power Electronics Reliability Project under the Energy Storage Systems Research Program at Sandia National Laboratories (SNL or Sandia) funded by the Power Electronics Program of the U.S. Department Of Energy (DOE) Office of Electricity Delivery and Energy Reliability (OE, http://www.oe.energy.gov/). The project continues to take advantage of a variety of Sandia capabilities to enhance power electronics reliability for power conversion applications, and in the process, it also supports Sandia's broader energy security goals.

In Phase I of this effort, Sandia used its modeling, simulation, and optimization capabilities to address DOE objectives in enhancing the reliability and availability of PE [1]. Specifically, Phase I identified reliability improvements in components, software, and operations of Silicon Power Corporation's (SPCO) Solid-State Current Limiter (SSCL). Sandia also developed and documented a general process for analyzing the reliability of any power electronics system [2].

The overall goal of Phase II of this project has been to use Sandia's semiconductor device reliability measurement and modeling capabilities to investigate and characterize stress-related failure modes of electronic devices made out of advanced, post-silicon semiconductor materials; specifically, silicon carbide (SiC). In the process, quantitative indicators of potential failure have been identified that could form the basis for condition monitoring (CM) or prognostics and health management (PHM).

Industry has shown strong enthusiasm for this work, and relationships have been formed with several leading SiC device development companies and universities. Industry is particularly interested in Sandia's potential role as a non-biased evaluator of the reliability of these types of devices.

ABBREVIATIONS

BTS	Bias-Temperature-Stress
CM	Condition Monitoring
CMOS	Complementary Metal Oxide Semiconductor
C-V	Capacitance-Voltage
DER	Distributed Energy Resources
DOE	Department of Energy
FACTS	Flexible AC Transmission Systems
GaN	Gallium Nitride
HM	Health Management
IGBT	Insulated Gate Bipolar Transistor
I-V	Current-Voltage
JFET	Junction Field-Effect Transistor
M&S	Modeling and Simulation
MOS	Metal Oxide Semiconductor
MOS-C	MOS Capacitor
MOSFET	MOS Field-Effect Transistor
NBTI	Negative Bias Temperature Instability
OE	Office of Electricity Delivery and Energy Reliability
PE	Power Electronics
PHM	Prognostics and Health Management
SiC	Silicon Carbide
SNL	Sandia National Laboratories
TDDB	Time-Dependent Dielectric Breakdown

1. INTRODUCTION

The electric grid is facing two major challenges resulting from the increasing demand for electric power: (1) increasing penetration of renewable energy sources such as solar and wind and (2) insufficient growth in transmission capacity. These challenges are being addressed by power electronics respectively through: (1) power conversion systems for distributed energy resources (DER) which include the renewable energy sources and the energy storage systems to support them and (2) flexible AC transmission systems (FACTS) for providing grid stability and power flow control. Therefore, power electronics will continue to play an increasingly important role in the delivery of electricity [1]. At the same time the power electronics equipment must satisfy stringent demands for cost effectiveness, performance, efficiency, and reliability.

Key components of power electronic equipment are the semiconductor devices including various types of diodes, transistors, and thyristors. Historically, these devices have been made out of silicon, but there is keen interest in transitioning to wide band gap devices made out of advanced materials such as silicon carbide (SiC) and gallium nitride (GaN). These materials have a number of advantages over silicon including higher breakdown field, higher operational junction temperatures, and higher thermal conductivity. These properties allow for making devices with lower on-state resistance and higher switching frequencies. This in turn leads to more efficient grid equipment with higher density and a smaller footprint. However, to deliver these benefits reliably and economically, new approaches are also needed to prevent disruptive device failures.

Traditional approaches to improving component reliability include design and manufacturing changes. A complementary approach is to better manage the impact of reliability at any given level of component maturity by using condition monitoring (CM) and prognostics and health management (PHM). Both are based on sensor input of some kind. CM consists of detecting anomalies and diagnosing problems to flag maintenance needs. PHM goes further by tracking damage growth, predicting time to failure, and managing subsequent maintenance and operations in such a way to optimize overall system utility against cost. PHM seeks to optimize the tradeoff between premature device replacement and disruptive failures.

A number of PHM approaches for electronics have been proposed and are under various stages of research and development including "monitoring precursors to failure" [3]. The current project has an ultimate view towards utility-scale power electronics and focuses on elucidating measureable changes which can be monitored in individual power electronic semiconductor devices.

The needs for PHM in the electric grid in general are reflected in DOE's Smart Grid Research & Development Multi-Year Program Plan [4]. One of the key milestones is to "demonstrate prognostic health management technologies and distributed sensors for critical distribution system assets by 2014." The report spells out a number of PHM technology development needs including embedded sensors: "Low-cost sensors embedded in components can improve prognostic health management (PHM), which can increase the reliability of the grid and the lifetime of the components themselves. The first aspect of PHM is a set of technologies that monitor components for signatures of incipient failure." It is such signatures which we aim to identify with this research.

The main goals of this particular phase of the project have been twofold:

1. Perform electrical characterization and stress testing experiments on power electronic devices.
2. Interpret and model the stress-related degradation of the devices to find opportunities for CM and PHM.

The main purpose of the experiments was to see if stress could induce measurable shifts in the electrical characteristics. With enough data, such shifts could be used rather directly for CM purposes. However, in order to develop viable models for prognostics, it is necessary to study basic physical mechanisms behind any progressive degradation. Therefore, the results of the experiments have been modeled or otherwise interpreted which in turn raises questions for further investigation.

The specific focus of this project has been on studying stress-related changes in the electrical characteristics of SiC devices, and the following devices were tested as described in subsequent sections: (1) MOS capacitors, (2) MOSFETs, and (3) Schottky diodes. Initial characterization of SiC JFETs and thyristors was also performed, but the results are not given here. The characterization and stress testing consisted of measuring dielectric breakdown voltage, capacitance vs. voltage (C-V) curves, and current vs. voltage curves (I-V). Depending on the device, these measurements were repeated over a period of time and stress cycles. For this stage of the project, the stresses consisted of (relatively) high voltage and/or high temperature including bias-temperature-stress (BTS) tests. Future tests could also include high currents.

The rest of the report is organized as follows. Section 2 focuses on the reliability of the oxide (SiO2) on SiC in the context of the simple geometry of MOS capacitors. Voltage stresses are applied to study the dielectric breakdown resulting from increasing voltage as well as increasing time. A standard reliability analysis gives a statistical prediction of the fraction of oxides that will break down over time under normal use conditions. A model for changing voltage as a result of charge trapping is presented as a potential deterministic breakdown prediction method for CM or PHM. Section 3 also addresses SiC MOS capacitors and presents the results of BTS experiments. Small-signal capacitance is measured as a function of overall voltage (swept high to low) before, during, and after temperature and voltage stress. Changes in flat-band voltage are apparent during the cycles of stress and measurement, and depending on interpretation, could be used to monitor critical charge and/or defect buildup. Section 4 presents the results of gate BTS experiments on SiC MOSFETS. Shifts in characteristic curves of drain current (I_D) vs. gate voltage (V_G) and drain voltage (V_D) are shown between and during BTS cycles. The I_D-V_GG shift appears as a change in threshold voltage indicating increasing on-state resistance and could be used as a prognostic indicator of potential failure. Section 5 shows a characteristic curve shift in a SiC Schottky diode induced by a high reverse voltage stress. Although the effect is currently unexplained, it could be used as the basis of prognostics. Finally, section 6 summarizes the accomplishments of this phase of the project, outlines the benefits of this line of research, and describes a number of avenues for subsequent work besides the basic device physics research questions listed in the main text. It also discusses progress towards being able to test other types of devices.

2. VOLTAGE-RAMP AND TIME-DEPENDENT BREAKDOWN MEASUREMENTS OF N-BODY MOS CAPACITORS

N-body 6H-SiC MOS capacitors obtained from a leading manufacturer were evaluated using both voltage-ramp testing as well as time-dependent dielectric breakdown (TDDB) testing. These samples are "research-grade" and do not necessarily represent the oxide in a commercial product. Oxide thicknesses of both 500 Å and 750 Å were examined. Voltage-ramp testing was first undertaken to determine the dielectric breakdown strength of the oxide films. This is a critical parameter for the reliability of the MOS system and any devices fabricated from it (e.g., MOS field-effect transistors). The capacitors were voltage-ramped at room temperature at a rate such that the electric field across the oxide changed at approximately 1 (MV/cm)/s, which is a standard ramp rate for this type of test [5]. The capacitors were ramped from zero volts to a positive voltage (thus the capacitors were biased into accumulation) until they failed, failure being dielectric breakdown resulting in a short-circuit through the capacitor. Two different circular capacitors were examined: a small version (approximate diameter 190 μm) and a large version (approximate diameter 390 μm). Five capacitors of each type were tested, with the results shown below.

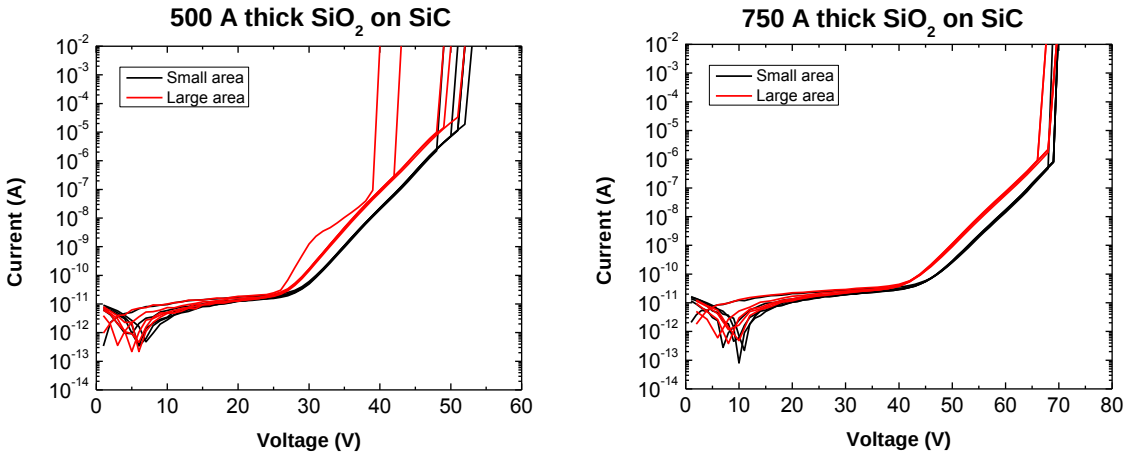

Figure 2-1. Ramp-to-breakdown of SiO_2/SiC MOS capacitors of thickness 500 Å (left) and 750 Å (right).

Several things are apparent from the plots. Consider first the plot on the left for the 500 Å thick oxide. The current (due to Fowler-Nordheim tunneling though the oxide [6]) scales with the area of the capacitors, as expected. Moreover, the larger-area capacitors show worse characteristics. This is expected because a larger-area film is more likely to contain processing defects [7]. One of the large-area capacitors shows excessive leakage current prior to breakdown, and this device and one other large-area capacitor exhibit early "extrinsic" failures (short-circuit breakdown is indicated by the near-vertical jumps in current). Even for the main, "intrinsic" parts of the distribution, the large-area capacitors show earlier failure times than do the small-area capacitors. This is again expected and is a well-known property of oxide breakdown, having been studied for many years within the context of silicon MOS technology [8]. It is observed that most of the intrinsic breakdowns occurred in the vicinity of 50 V, i.e., at an electric field of approximately 10 MV/cm, which indicates a reasonably good-quality oxide.

Moving to the data for the 750 Å oxide, we see that again the current scales with the area, and that it is lower for a given voltage compared to the 500 Å oxide, as it should be. For these thicker films, however, there appear to be no "extrinsic" failures present. The breakdown voltage tends to be clustered around 70 V, which is again near a breakdown field of 10 MV/cm.

Additionally, data such as that shown in Figure 2-1 were evaluated to examine the carrier transport mechanisms through the oxide. The Fowler-Nordheim expression is given by [6]:

$$J = AF^2 \exp\left(-\frac{B}{F}\right) \tag{2.1}$$

where J is the current density (A/cm^2) through the oxide, F is the oxide electric field, and A and B are material-dependent constants. The constant B is given by [6]:

$$B = 68.3\left(\frac{m^*}{m_0}\right)^{1/2} E_B^{3/2} \tag{2.2}$$

where m^*/m_0 is the ratio of the electron effective mass in the oxide to the free electron mass, and E_B is the height of the energy barrier at the SiO_2/SiC interface. The constant 68.3 is appropriate when the field F is specified in MV/cm and the barrier height E_B is specified in eV. A semi-log plot of J/F^2 vs. $1/F$ should therefore yield a straight line if Fowler-Nordheim tunneling is the dominant transport mechanism. Such a plot for one of our samples is shown below; note that for lower field, the curve deviates from a straight line. The high-field portion of the curve was fit to the Fowler-Nordheim expression and a barrier height of 2.4 eV was extracted; reported values for the SiO_2-SiC barrier height are typically slightly higher (and dependent upon the SiC polytype) [9]. This low barrier height (compared to SiO_2-Si) may be one factor limiting the reliability of the SiO_2/SiC MOS system, since it results in a higher gate current through oxide grown on SiC than through the same thickness of oxide grown on Si [9].

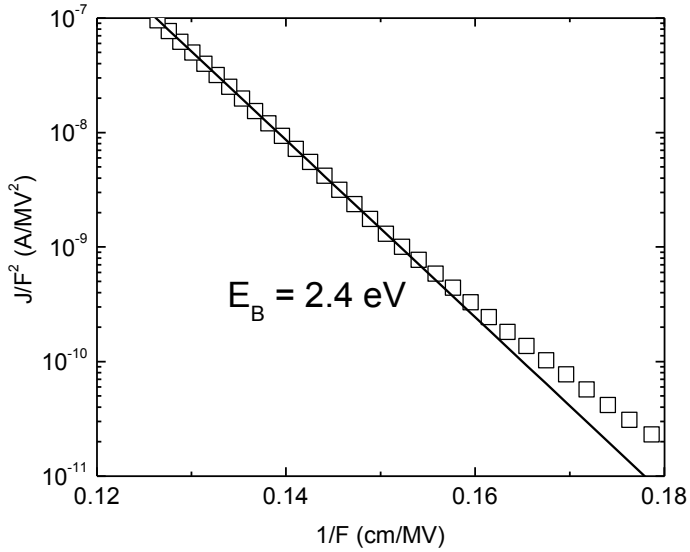

Figure 2-2. Room-temperature current-voltage data for MOS capacitor plotted on Fowler-Nordheim scale.

Oxide reliability was evaluated by time-dependent dielectric breakdown measurements (TDDB). TDDB results will only be shown for testing done on the 750 Å thick samples; results for the 500 Å thick samples were similar, scaled in a way that is analogous to the difference between the ramp results shown in the left- and right-hand panels of Figure 2-1. For TDDB testing, the sample was held at a constant voltage and the current was monitored. As was the case for the ramp testing, the voltage was positive, so the capacitors were biased in accumulation. The magnitude was chosen such that it was slightly smaller than the breakdown voltage derived from the voltage-ramp testing. During the stress, the value of the current is continuously monitored. An example of a TDDB measurement on a small-area, 750 Å capacitor stressed at +65 V at room temperature is shown below. This stress voltage is well in excess of the expected use voltage for an oxide of this thickness, and biases the sample into the Fowler-Nordheim tunneling regime. Current-vs.-time curves are shown for 20 samples; failure is again due to each capacitor short-circuiting, indicated by the near-vertical current spikes in the plots.

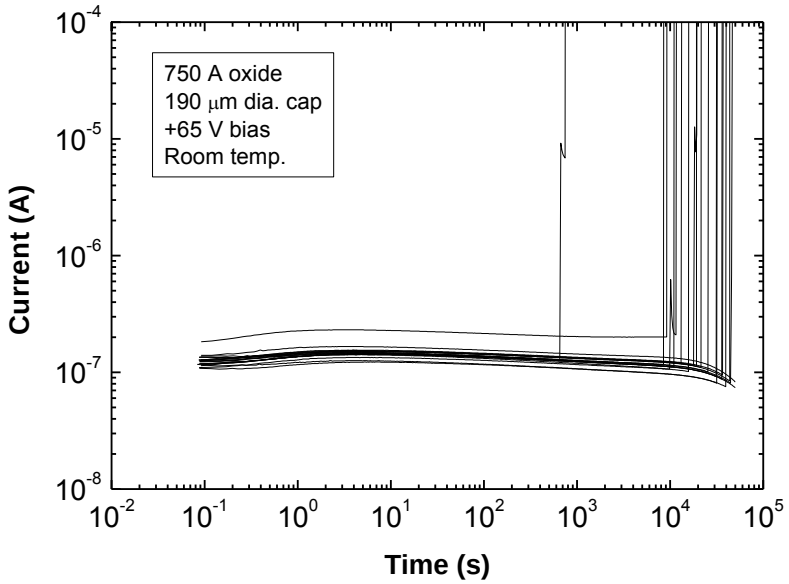

Figure 2-3. Current-vs.-time curves for 750 Å, small-area MOS capacitor biased at +65 V (accumulation) at room temperature.

The change in current as a function of stress time is due to charge trapping under the high-field stress and has been frequently observed in thick oxides grown on Si [10]. This will be discussed in more detail below, but we note now that this change can potentially be used for condition monitoring (CM) and/or prognostics and health management (PHM) of the oxide film [11]. Note that one sample suffers from an early extrinsic failure; this is analogous to the early failures observed in the voltage-ramp data. Also note that one sample exhibits slightly higher current than the remainder of the samples in the group; this could be due perhaps to local thinning of the oxide in that sample. However, that sample does not suffer from early failure. Also note that a few of the failures are "soft", i.e., the current recovers slightly prior to final failure. This can be observed, e.g., on the sample that suffers the early failure.

It is well-known that oxide breakdown follows Weibull statistics [8]. The Weibull distribution is given by:

$$F(t) = 1 - \exp\left[-\left(\frac{t}{t_{63}}\right)^{\beta}\right] \tag{2.3}$$

where $F(t)$ is the fraction of devices failed by time t. The distribution is characterized by two parameters, the "mean" time t_{63} (it is the time at which 63% of the population has failed; this is easily verified by substituting $t = t_{63}$ into the above equation) and the "slope" β. The latter quantity is a measure of the width of the distribution, and is likewise a measure of the failure rate. The Weibull distribution is often written in the form:

$$\ln[-\ln(1-F)] = \beta \ln t - \beta \ln t_{63} \tag{2.4}$$

Time-to-breakdown for nominally 750 Å thick MOS capacitors is shown below. Data for both large- and small-area capacitors is shown. Fits to the above equation are also shown. We see

that both t_{63} and β are smaller for the larger capacitor. For t_{63}, this is expected for an intrinsic failure mechanism [8]. For a single failure mechanism, however, oxides of different areas should in theory have the same β, which is expected to be dependent upon thickness only [8]; the lower β for the larger-area oxide indicates that some extrinsic, manufacturing-defect-driven failure mechanism is at work. This is not surprising, since a larger area oxide is more likely to contain manufacturing defects [7]. Similar to SiO_2-Si technology in the 1960s and 1970s, improvements in device processing should eventually eliminate such defects in the industry. Also interesting are the values obtained for β; for the large-area capacitor, $\beta < 1$ which is consistent with a manufacturing-defect driven failure mechanism ($\beta < 1$ indicates a failure rate that decreases with time, i.e., the so-called "infant mortality" portion of the bathtub curve) while for the large-area capacitor, $\beta > 1$ is consistent with a wear-out mechanism [12]. However, the value of β is somewhat smaller than what might be expected for an oxide of this thickness [8], at least extrapolating from studies done on SiO_2 films grown in Si; much more work is necessary on SiO_2 grown on SiC to establish the intrinsic relationship between β and oxide thickness, especially for thick oxides such as these.

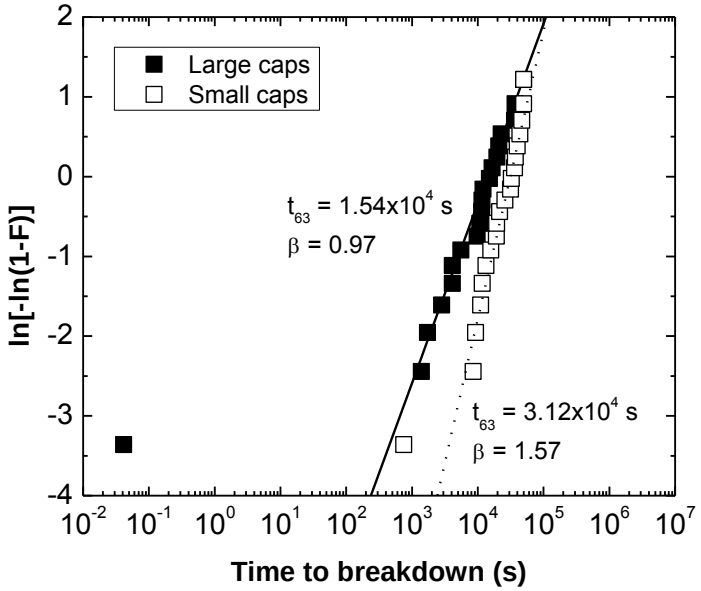

Figure 2-4. Weibull plot of time-to-breakdown data for nominally 750 Å thick SiO_2/SiC MOS capacitors measured at room temperature, +65 V.

TDDB measurements were made at several voltages and the resulting breakdown distributions were analyzed as described above. Values of t_{63} were extracted and are plotted below. It is immediately obvious that the value of t_{63} is a very sensitive function of the applied voltage. The data points were fit to the so-called "E-model" [13] given by:

$$t_{63}(V) = t_{63}^{0}\exp(-\gamma V) \tag{2.5}$$

where t_{36}^{0} is an overall multiplicative constant, γ is the voltage acceleration factor (units of 1/V), and V is the applied voltage. The "E-model" is actually formulated in terms of the electric field across the oxide (hence the name) and includes an Arrhenius factor to account for the temperature. Here, we have only performed experiments at room temperature so the latter

dependence is absorbed into the overall multiplicative factor. This model is based on the thermodynamics of field-enhanced bond breakage within the oxide, which ultimately leads to a conducting path through the oxide and thus failure. Other models, such as the "1/E model" which is based on tunneling current through the oxide [10] ("1/E" refers to the dependence of the Fowler-Nordheim expression on the inverse of the electric field), are also possibilities. The E-model is the simplest and tends to give the most conservative estimate of reliability, so we have elected to use it here. The acceleration model is used to extrapolate the accelerated test data back to use conditions. The extrapolated value of t_{63} is then used in conjunction with the measured value of β (which is assumed to be independent of voltage and temperature) and the Weibull distribution to determine what fraction of the population will have failed after a given amount of time. Taking the values shown in Figure 2-5 and a value of β = 1.6, we find $t_{63} \approx 3.5\times10^{23}$s assuming a use voltage of 30 V. Inserting these values in to the Weibull distribution, we find that even after 100 years, F is essentially unity. Thus, based on this model, the oxide in these capacitors (and by extension, the oxide in any type of device employing a MOS structure, e.g., a power MOSFET) is extremely reliable. This is of course for a device operated at room temperature (high temperature will degrade the reliability and should be studied), and is based on numerous assumptions and a very limited data set. The chief assumption is that no manufacturing-defect-related failures occur, which as we have seen tend to increase with larger oxide area and could significantly decrease the oxide lifetime. But our data indicate that the intrinsic reliability of SiO_2 grown on SiC is potentially very good. Note that if the 1/E model had been used instead of the E model, the projected lifetime would have been even longer.

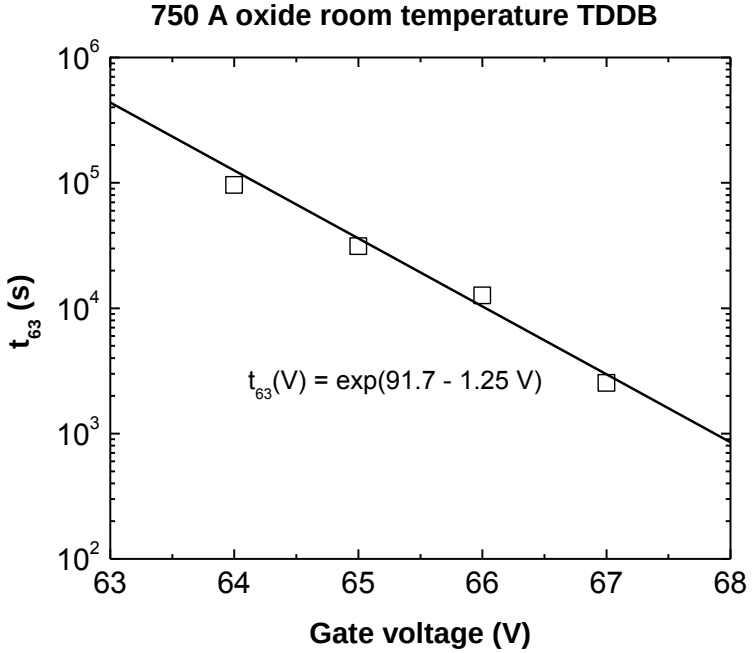

Figure 2-5. Values of t_{63} in seconds) extracted from Weibull distributions measured at four different voltages. The data points were fit to give the equation shown.

It was mentioned previously that oxide breakdown is preceded by an accumulation of charge within the oxide. This idea was used to explain the curvature of the current-vs.-time curves of

Figure 2-3. A simple model for charge (in this case electron) build-up is to assume that a density of traps N_T exists in the oxide (in reality traps will be created by the high-field stress, but that is neglected in this simple model). Assume that a density n_T traps are filled with electrons, and that the rate at which the traps are filled is proportional to (1) the density of empty traps, and (2) the number of carriers passing through the oxide per unit area, i.e., the current density J divided by the electron charge q. Under these assumptions, a rate equation can be written down:

$$\frac{dn_T}{dt} = \sigma \frac{J}{q}[N_T - n_T(t)] \tag{2.6}$$

The proportionality factor is the capture cross-section σ which has units of cm^2. For a constant-voltage TDDB experiment, the current density J depends upon the net electric field across the oxide through the Fowler-Nordheim relationship (equation (2.1)), which in turn depends upon the amount of trapped charge. Thus, in this case the equation is complicated and needs to be solved numerically. However, a constant-current experiment can also be performed. For this experiment, a constant current is sourced and the voltage across the oxide changes as a result of charge build-up. For a constant J, the solution of equation (2.6) is simple:

$$n_T(t) = N_T\left[1 - \exp\left(-\sigma \frac{J}{q} t\right)\right] \tag{2.7}$$

Assuming that all of this charge is trapped near the SiO_2/SiC interface (which is again likely not true, but simplifies the model), the shift in voltage across the oxide is given by:

$$\Delta V(t) = \frac{q}{C_{\text{ox}}} n_T'(t) \tag{2.8}$$

where n_T' is the areal density of filled traps (i.e. it is the trap density integrated over the oxide thickness) and C_{ox} is the oxide capacitance per unit area. Note that since the trapped charge is assumed to be negative, the shift in voltage across the oxide is positive (this is discussed more in one of the following sections). Also, if the trapped charge is distributed throughout the oxide rather than concentrated near the oxide-semiconductor interface, a factor needs to be introduced to account for this distribution. This is a difficult problem and does not change the overall structure of the model, so it will not be pursued here. A constant-current experiment such as described here was performed at room temperature on one of the 750 Å thick MOS capacitors. The stress current was set to 3 nA and the voltage across the capacitor was monitored. Data are shown in Figure 2-6 below. The data were fit to equations (2.7) and (2.8); the fit and the associated fit parameters are shown in the figure. Once again, this model is oversimplified, and these numbers may not be physically reasonable. Also, note that the voltage shift predicted by this model tends to saturate, since a fixed value for the total density of traps is assumed; again, it is likely that the high-field stress actually creates new traps of varying charge states. However, it illustrates an approach that may be taken regarding CM and PHM. Clearly, the voltage shift measured is an indication of the condition of the system. Going further, the model is able to predict the number of trapped charges $n_T(t)$ as a function of time. Catastrophic failure in SiO_2 films is thought to occur when a critical defect density is achieved [8] (which in terms of this simple model is the density of charged defects n_T) and thus, by monitoring the voltage across the

capacitor, it is possible in principle to determine how close the capacitor is to this critical defect density. In practice this may be difficult to employ (e.g., the voltage shift at operating conditions may be extremely small and thus difficult to measure) but again, this experiment is meant only to illustrate the principle.

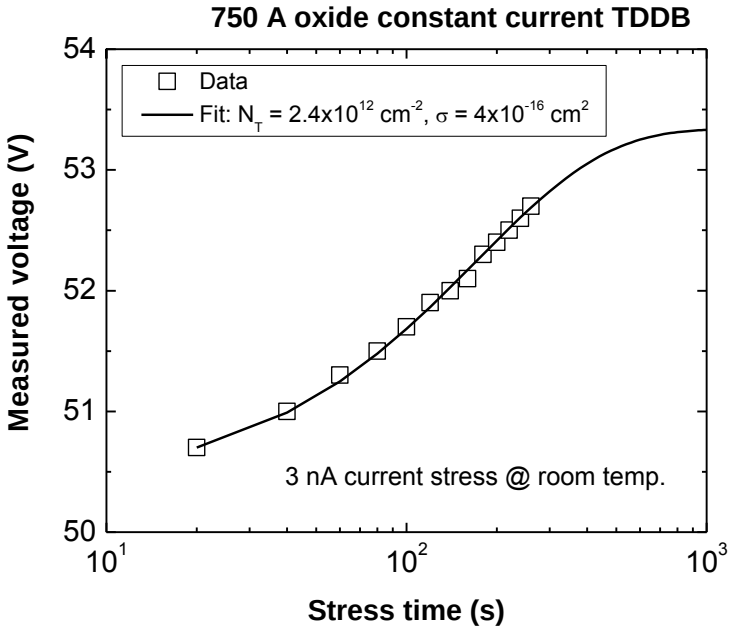

Figure 2-6. Voltage shift resulting from constant-current stress experiment with fit to equations (2.7) and (2.8).

A final set of voltage ramp measurements was done on two samples at high temperatures. Even though the extrapolation at room temperature indicated extremely good reliability for the gate oxide, there is concern that this may be substantially degraded at high temperatures. The degradation may go beyond the expected Arrhenius relationship between lifetime and temperature, since new failure mechanisms may be activated at high temperature. This is especially important for SiC-based devices, which are hoped to be used in very high-temperature environments due to the large bandgap of SiC [9]; however, the small barrier height between SiC and SiO_2 as discussed above may be detrimental to these applications, due to the enhanced Fowler-Nordheim current resulting from a small barrier height [9]. The voltage ramp measurements were done on two large-area capacitors of 500 Å thickness using the same method as described previously. In each case, however, the samples were placed on a hot chuck which was set to a temperature of either 225°C or 300°C. Results are shown below in Figure 2-7. Obviously, these curves are very different from the curves measured at room temperature (Figure 2-1). They are very noisy at low voltages (with more noise at 300°C than at 225°C). At higher voltages, they do not appear to obey the Fowler-Nordheim relationship, indicating that some other current transport mechanism is dominant. Breakdown occurs just over 45 V at 225°C, but is reduced to just over 25 V at 300°C! Also note that device failure is here characterized by a "snap-back" to a high-current, low-voltage state, although this is likely due to the power limit in the instrumentation used, which was slightly different for this experiment than that used to collect the data shown in Figure 2-1. All of these factors indicate that the reliability of the SiO_2-

SiC MOS system at high temperatures may be significantly degraded compared to room temperature. Clearly, more study is required.

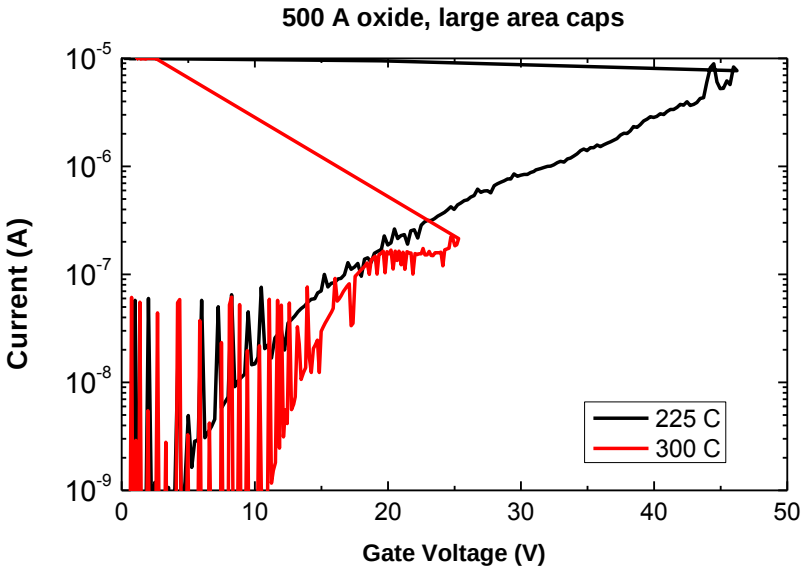

Figure 2-7. Current-voltage curves of two 500 Å thick, large area MOS capacitors at high temperature.

3. BIAS-TEMPERATURE-STRESS MEASUREMENTS ON N-BODY MOS CAPACITORS

The bias-temperature-stress measurement (BTS) is a well-known method of investigating MOS non-idealities and is very commonly used to evaluate oxide qualities and defects in the silicon community [14]. BTS measurements have also been used to uncover and study a number of non-idealities in the SiC-SiO_2 MOS capacitor such as negative bias temperature instability (NBTI) [15], charge injection [15, 16], and mobile ions [17]. The careful study and optimization of these effects is necessary to create a robust SiC-SiO_2 interface suitable for a SiC MOSFET.

The first set of measurements were performed on a device from the same 6H-SiC-SiO_2, n-body MOS-C sample used in the voltage-ramp and time-dependent breakdown measurements described in the previous section. As noted above, these devices have reasonably high breakdown voltages of about 50 V for a 500 Å oxide and 70 V for a 750 Å oxide (~10 MV/cm in both cases). The following measurement is made on a 50 Å oxide device. Our C-V measurements were performed using an Agilent 4284 impedance analyzer, using a small-signal frequency of 32 kHz (to minimize the effects of series resistance on the measurement) and a voltage amplitude of 25 mV. Voltage sweeps went from V_G = 5 V to V_G = -5 V voltage (i.e., from accumulation to deep-depletion for these n-body capacitors) in 100 mV steps. It is assumed that no inversion layer is present in the device at this temperature, due to lack of carrier generation; this is supported by experimental evidence [17].

The first step of the measurement sequence was to obtain a baseline C-V measurement at room temperature. Next, the samples were heated to 225°C and a bias of V_G =+20 V was applied. This is well below the room temperature breakdown field (F_{BD}). Finally, they were cooled back to room temperature and a post-stress C-V curve was measured. The pre-stress and post-stress measurements are plotted in Figure 3-1.

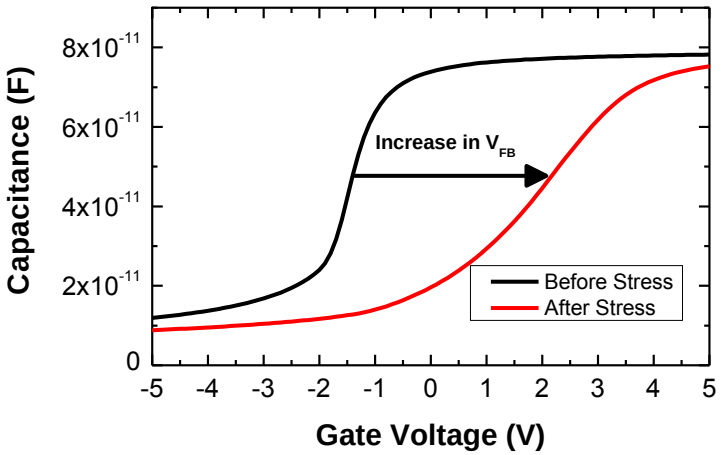

Figure 3-1. Capacitance-voltage curves for bias-temperature-stress experiment described in the text. Sample is subjected to one 10 minute, V_G = +20 V stress cycle at 225°C.

The C-V curves in Figure 3-1 demonstrate two effects of the gate voltage stress applied at high temperature. The first effect is that the flat-band voltage (V_{FB}) exhibits a large positive shift. A positive voltage shift in a MOS capacitor is generally caused by the injection of negative charge while a negative shift is caused by positively charged mobile ions moving toward the SiC/SiO_2 interface and thus increasing their effect on the charge below the oxide. In this case, the stress is a positive voltage (V_G = +20 V) which would cause the mobile ions to move to the SiC/SiO_2 interface, which would in turn result in a negative V_{FB} shift. Since the flat-band voltage shift was positive, the only plausible explanation is that negative charge was injected into the oxide or into the SiC/SiO_2 interface. This large increase in V_{FB} would cause an equally large increase in the V_T if this MOS-C were being used in the gate of a MOSFET. This is illustrated in a similar BTS measurement on a SiC MOSFET in the next section.

The second effect seen in Figure 3-1 is a large stretch-out of the transition from accumulation to deep-depletion resulting from the BTS measurement. In the pre-stress curve, the device appears to take about 2 V for the surface potential (φ_S) to change from accumulation ($\varphi_S > 0$) to deep depletion ($\varphi_S < \varphi_F$). After the stress, the same transition takes place over approximately V_G = -1 V to V_G = +5 V, giving a total of 6 V, or an increase of 4 V! This large stretch out of the C-V curve is often associated with an increased density of interface states (D_{it}) [14], such as when NBTI [15] is induced (however, since in this case V_G is positive, this is not NBTI). In this case, it appears that an increase of interface states was caused by the injection of electrons into the SiC/SiO_2 interface. The band diagram representing this charge injection is given in Figure 3-2. In a MOSFET, electron injection into the SiC/SiO_2 interface could cause instabilities in the threshold voltage and possibly decrease the channel mobility (due to the increase in D_{it}), which would lead to a higher on-resistance.

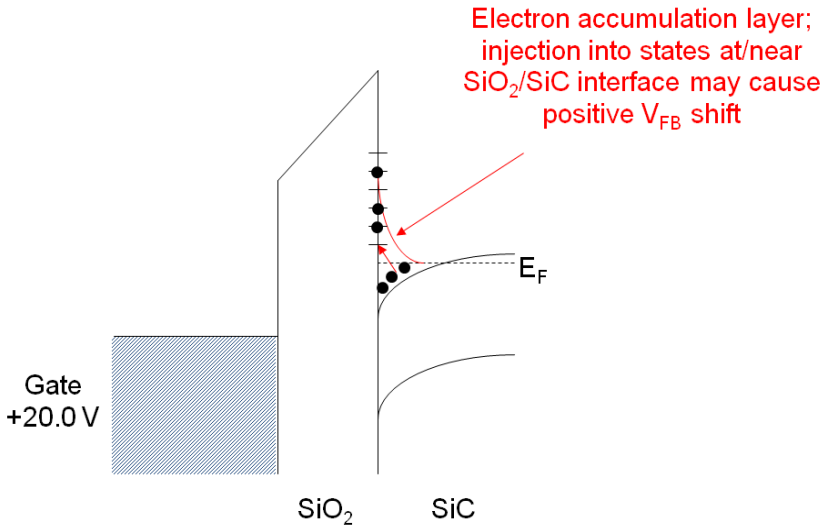

Figure 3-2. Band diagram illustrating electron injection into the SiC/SiO_2 interface corresponding to the BTS measurement shown in Figure 3-1.

For the next set of experiments, a set of n-body MOS capacitors were evaluated, also using the BTS method. Once again, these samples are "research-grade" and are not necessarily representative of anything available commercially. The BTS characterization was undertaken, in part, to determine whether or not positively ionized, mobile impurities such as Li+, Na+, and K+

were present in the oxide. Such impurities are known to result in flat-band voltage instability during device operation. Samples of nominally 500 Å thick SiO_2 thermally grown on n-type 4H-SiC substrates were tested. The C-V measurements were performed using an Agilent 4284 impedance analyzer, using a small-signal frequency and amplitude of 1 MHz and 25 mV respectively. Voltage sweeps went from positive to negative voltage (i.e., from accumulation to deep-depletion for the n-body capacitors) at a rate of approximately 40 mV/s. Results were interpreted in terms of a parallel RC circuit model.

Prior to performing the actual BTS measurement, samples were measured at room temperature, heated to 200°C and measured, then cooled back to room temperature and measured a final time. Thus, in this simpler experiment, no prolonged bias was applied to the samples at elevated temperature. The purpose of this experiment was to determine if the C-V measurement itself at high temperature was a sufficient to induce a flat-band shift. The C-V measurement does apply a DC field to the sample, the magnitude of which varies during the sweep; however, the period of time during which this field is applied is considerably shorter than what would be experienced by the oxide in a typical BTS experiment. Representative results for this experiment are shown below for a capacitor of area 520×520 μm^2.

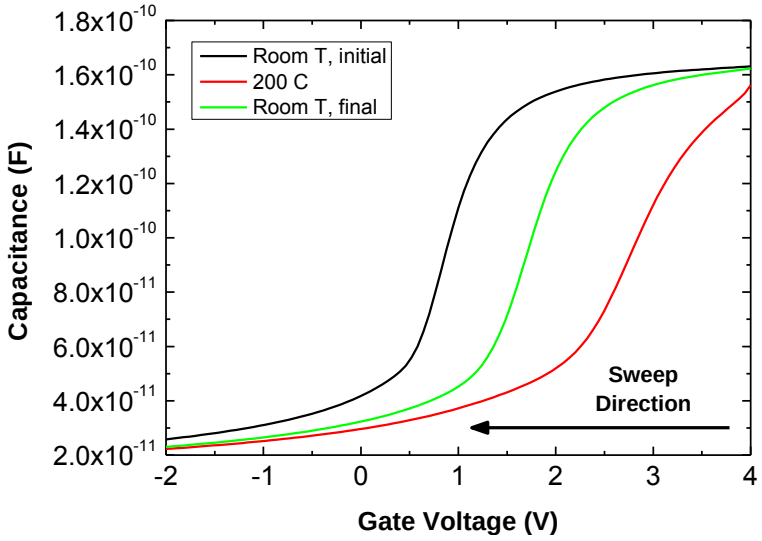

Figure 3-3. Capacitance-voltage curves for 500 Å SiO_2/SiC MOS n-well capacitor measured at room temperature, 200°C, and again at room temperature.

Several features are apparent from these curves. First, the simple act of heating the capacitor to 200°C and/or measuring it at such an elevated temperature affects the device properties significantly. A large positive shift in the flat-band voltage of roughly 2 V is readily apparent. A more subtle difference is that the shape of the curve has changed slightly; it appears to be a bit more stretched out, similar to what was observed in the capacitor from the other manufacturer. Such stretch-out is typically indicative of the presence of interface states at the semiconductor-oxide interface which have a charge state that depends upon the applied bias [14], and thus this measurement suggests that interface states are present at the SiO_2-SiC interface, also as discussed for the previous sample. After cooling back to room temperature, the flat-band voltage shift recovers somewhat, but it does not return to its original value. However, the final curve appears

to be parallel to the initial curve (i.e., it is not stretched out), suggesting that the shift relative to the original curve is due entirely to charge in the bulk of the gate oxide. The charge state of bulk traps in general does not depend upon applied bias. Taken together, these results indicate a severe temperature instability within this sample set, due to both bulk and interface traps. Obviously, devices such as MOSFETs fabricated using this particular gate process would perform very poorly in a high-temperature environment or in an environment in which the temperature is cycled frequently. It should be noted that this sample set is not necessarily representative of state-of-the-art SiO_2-SiC technology; rather, it is representative of a technology that we were able to obtain during this phase of the program. We are currently in the process of obtaining newer samples for additional, similar characterization.

More thorough BTS experiments were also performed on this sample set. In this case an initial C-V curve was first measured. The sample was then heated to 200°C and another C-V curve was taken at that temperature. Thus far this experiment is identical to the one described previously. For this second experiment, however, a bias of +3 V was applied to the sample for 10 minutes (600 seconds). A value of +3 V was chosen to avoid breaking down the oxide film. This particular value is well below the expected breakdown voltage for an oxide of this thickness, but low breakdown voltages were observed on some samples and we wanted to be sure to avoid this. Following this prolonged bias, C-V curves were again measured. The bias-measure sequence was then repeated two more times, after which the sample was cooled down to room temperature and measured a final time. Results are shown below for a large sample of area 1000×1000 μm^2.

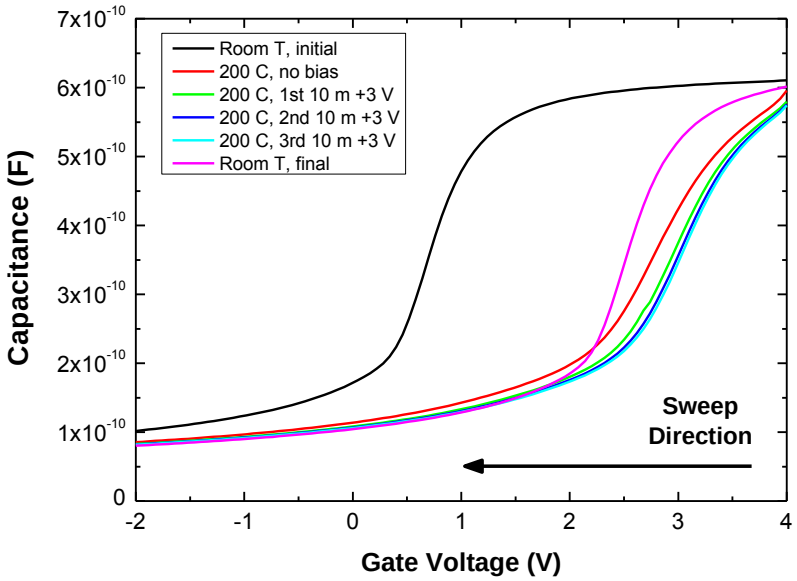

Figure 3-4. Capacitance-voltage curves for bias-temperature-stress experiment described in the text. Sample as subjected to successive 10 minute, +3.0 V stresses at 200°C.

These curves are similar in many respects to those resulting from the previous experiment in which the sample was not subjected to a voltage stress at high temperature. The curve measured at high temperature but prior to voltage stress appears similar to the one discussed previously, i.e., it has shifted towards more positive voltages and has become stretched out. Once again, the

stretch-out indicates that at least a portion of the trapped charge resides in states at the SiO_2-SiC interface. The three cycles of prolonged voltage stress at high temperature result in a slight amount of additional shift. The small magnitude of the additional shift may be explained by noting that that the initial shift brings the flat-band voltage near 2.5 V. Thus, an applied gate bias of +3.0 V actually results in quite a small electric field across the oxide (~0.1 MV/cm). Thus it is perhaps not surprising that the changes resulting from the prolonged stress are minimal. A plot of the capacitance measured at +3 V as a function of time during the three stress periods is shown below.

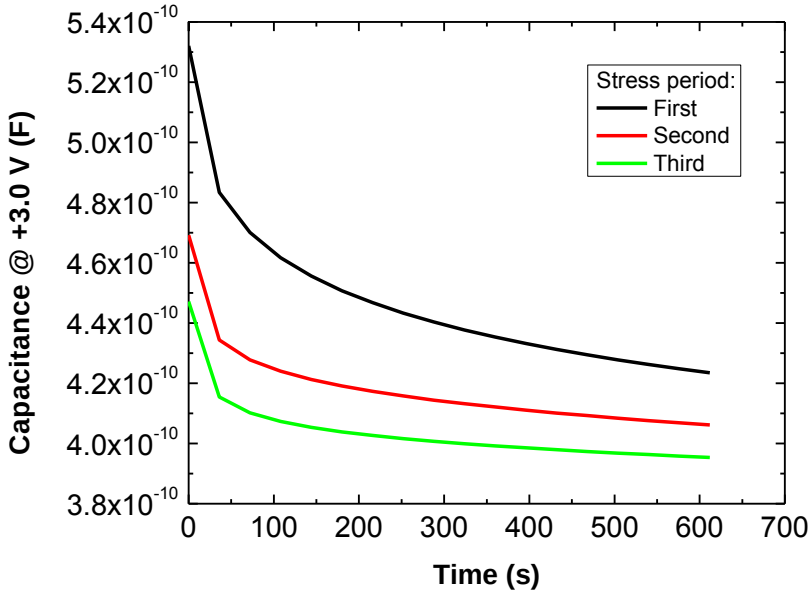

Figure 3-5. Capacitance measured at +3.0 V, 200°C as a function of time during three periods of stress.

Note that there is some recovery of the capacitance from the end of one stress period to the beginning of the next. Data measured quasi-continuously in time, such as that shown in Figure 3-5 above, could potentially be used for CM and PHM purposes, whereby the amount of shift is indicative of the degree to which the device parameters have shifted from their original values. This is similar to what was discussed above, regarding using the voltage shift resulting from charge build-up in the oxide as a precursor to breakdown. In this case, however, we assume that some point the voltage shift will be sufficiently large such that the device will not operate as intended in its application.

It is notable that the shift of the overall C-V curve (Figure 3-4) during this part of the experiment is roughly parallel to the stretched-out C-V curve observed after the initial heating of the sample, indicating that interface states remain active. Following cool-down to room temperature, the C-V curve is seen to relax somewhat, although it is nowhere near its original position, nor does it even recover to the position observed in the simpler experiment without the voltage stress at high temperature. Moreover, the slope of the curve is again parallel to the initial curve, indicating that the charge responsible for the final flat-band shift is trapped primarily in the bulk of the gate oxide. These results suggest a complex defect structure in these samples, consisting of both bulk

and interface traps with varying (likely distributed) depths within the material bandgap, and hence varying time constants and thermal responses.

In fact, these results are inconsistent with the presence of positively-charged mobile impurities within the bulk of the oxide. We consider first the small positive shift that is observed to occur as a result of the high-temperature, constant-voltage stress. For the positive bias used, the band diagram during stress is as illustrated in Figure 3-6 below (which is similar to Figure 3-2).

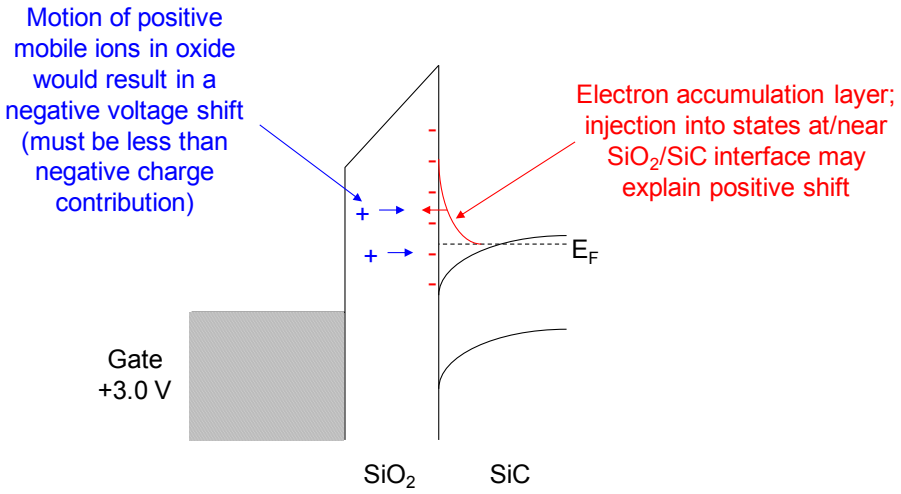

Figure 3-6. Band diagram of SiO_2/SiC system during positive (accumulation) bias.

A positive (accumulation) bias on the gate results in the bands tilted as indicated. Any positive ions in the oxide will tend to drift due to the oxide electric field towards the SiO_2-SiC interface. The flat-band voltage shift due to charge in an oxide layer is given by [14]:

$$\Delta V_{FB} = -\frac{1}{C_{\text{ox}}}\int_0^{x_{\text{ox}}} \frac{x}{x_{\text{ox}}}\rho(x)\,dx \tag{3.1}$$

where C_{ox} is the oxide (accumulation) capacitance per unit area, x_{ox} is the oxide thickness, $\rho(x)$ is the charge density within the oxide, and x is the spatial coordinate with $x = 0$ at the oxide-gate interface and $x = x_{\text{ox}}$ at the oxide-semiconductor interface. Several things are apparent from this expression. First, the shift in flat-band voltage is opposite to the sign of the oxide charge. Second, the closer the oxide charge is to the oxide-semiconductor interface, the greater is the flat-band shift. A positive applied bias would tend to move positive ions within the oxide bulk to the SiO_2/SiC interface. They would there make a maximum contribution to the shift in the flat-band voltage, but the voltage shift would be negative. Of course, we observed a positive voltage shift. This positive shift could, however, be explained by the injection of electrons (which are plentiful in the n-type substrate in accumulation) into states at the SiO_2/SiC interface, or in the SiO_2 bulk (again, the nearer these states are to the SiO_2/SiC interface, the greater their effect will be on the flat-band shift. This effect is similar to what was observed on the first set of samples, from the other manufacturer, although the magnitude of the effect appears to be more pronounced (i.e., it is observed for a much smaller applied field). The qualitative agreement between the two sets of samples from the two manufacturers suggests that this may be a

universal problem affecting the SiC- SiO_2 system, at least when the SiO_2 is grown on an n-type substrate.

What about the positive shift resulting from the simple act of measuring the sample at high temperature? In this case, the sample is swept through both positive and negative voltages (always starting at positive voltage and moving towards negative), and thus experiences both accumulation and deep-depletion bias conditions. When the sweep is at positive bias values (the initial portion of the sweep), the band diagram is as shown above. Thus, the same arguments as mentioned in the previous paragraph apply. When the sweep is at negative bias, the band diagram is as shown below. In this case, positive mobile charge would tend to move away from the SiO_2-SiC interface, resulting in a positive shift. Thus, this could potentially explain the observed data. De-trapping of previously captured electrons, resulting in their removal from the SiO_2 and replacement into the SiC, could also occur and would result in a negative flat-band shift, which is inconsistent with the data.

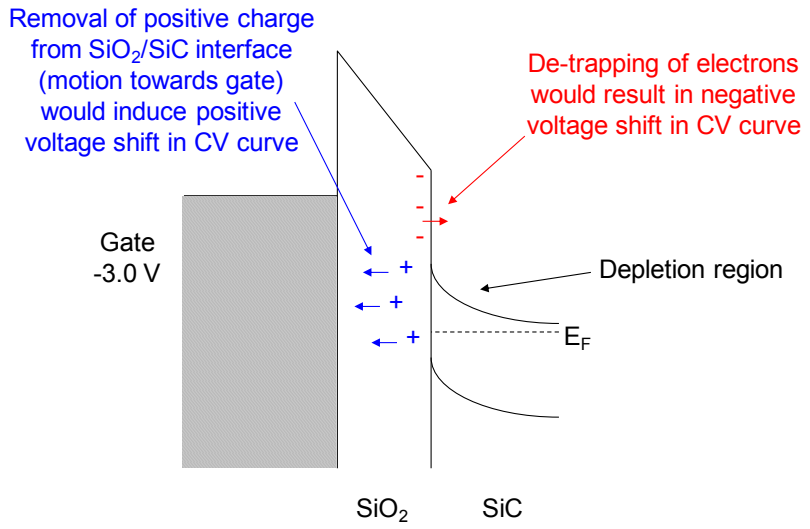

Figure 3-7. Band diagram of SiO_2/SiC system during negative (depletion-inversion bias).

During the sweep the oxide experiences both positive and negative electric fields which tend to have opposite effects on the transport and trapping of charge, making it difficult to determine the exact cause of this behavior based on the limited data set obtained to date. Further, the trapping / de-trapping kinetics will be temperature and field-dependent. It is probably safe to say that some type of electron injection from the substrate is likely, and that motion of mobile ions is perhaps a secondary effect. More detailed experiments need to be performed. In addition, better-quality MOS capacitor samples need to be obtained. As mentioned previously, the voltages / fields at which these samples were stressed are very low. If these gate oxides were to be incorporated into a device such as a MOSFET, the gate operating voltage of that device would be well in excess of the voltages examined here; thus, that device would exhibit severe instabilities even below its operating characteristics. Nevertheless, this set of experimental data gives an example of the type of experiment and analysis that may be used to examine charge transport, injection, and trapping in the SiO_2-SiC MOS system, and ultimately, provide an avenue to monitor the condition of post-silicon MOS devices during operation in energy storage applications.

A final note here is that this set of samples, from a different manufacturer, appears to be less robust than the samples from the first manufacturer. For the second set of samples, breakdown voltages tended to be < 10 V, whereas for the first set breakdown voltages were ~ 50 V for the same oxide thickness. This serves to illustrate the relatively immature nature of the SiC/SiO_2 MOS system. The Si industry faced similar issues several decades ago.

4. EFFECT OF GATE BIAS-TEMPERATURE-STRESS ON A SIC MOSFET

The preceding BTS studies on SiC MOS Capacitors are aimed at understanding the SiC/SiO_2 MOS system in order to create an optimal SiC MOSFET. In this section, we make BTS measurements on a 4H-SiC n-channel MOSFET. Measurements made on MOSFETs often correlate with the corresponding measurements made on MOS capacitors.

Characterization of the SiC n-MOSFET consisted of measuring both the drain current versus gate voltage (I_D-V_G) and the drain current versus drain voltage (I_D-V_D) behavior. The I_D-V_G curves were measured at a constant V_D = +1 V and the I_D-V_D curves were measured from V_G = +1 V to +10 V in 1 V increments. The BTS procedure started with the measurement of pre-stress curves at room temperature. Next, the device was heated to 150 °C, a gate bias of V_G = +20 V was applied for 7 minutes, and the device was subsequently cooled back to room temperature and the I_D-V_G and I_D-V_D curves were measured again. This stress and measurement procedure was repeated for temperatures of 175° - 250° C in 25 °C increments.

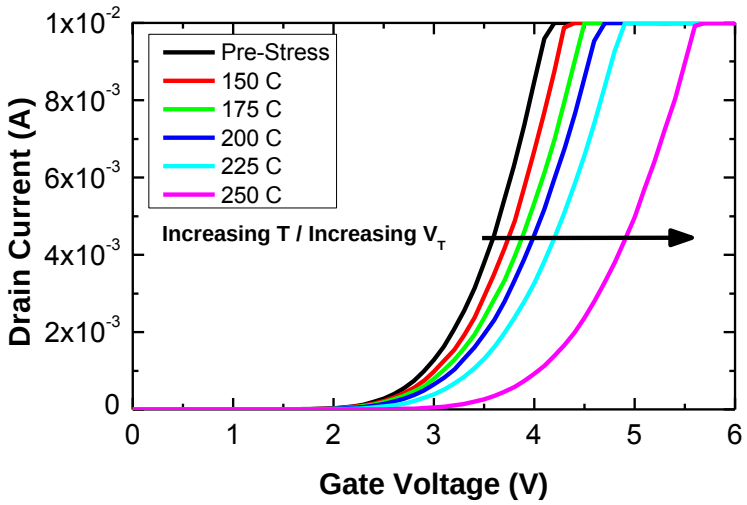

Figure 4-1. I_D-V_G plots of a SiC MOSFET with a constant drain voltage of V_D = +1 V. Each consecutive curve was measured after periods 7 minutes of biasing the gate at V_G = +20 V at the listed temperatures.

I_D-V_G and I_D-V_D curves resulting from the BTS stress are plotted in Figure 4-1 and Figure 4-2, respectively. The I_D-V_G curves illustrate the increase in V_T due to the high temperature stress. At higher temperatures, the shift in V_T appears to be greater for the same amount of time under the bias-temperature-stress. An increase in V_T due to a positive gate stress is likely to be the result of electron injection into the SiC/SiO_2 interface. This is the same effect that caused the flat-band voltage shift observed in Figure 3-1, Figure 3-3, and Figure 3-4 for a MOS capacitor except that in this case, there are no electrons available from the MOSFET's p-type body, so the n-type source and drain must provide the injected electrons. There might also be an increase in interface states as shown in Figure 3-2; this could be measured in the future by charge-pumping methods [14].

The increasing threshold voltage of this MOSFET results in a drop in drain current for a given gate voltage – drain voltage operating point. This is because for a MOSFET, whether in the linear region of operation or in saturation, the drain current is an increasing function of the quantity $V_G - V_T$. [14] Therefore, an increase in V_T results in a smaller difference between V_G and V_T, and thus a drop in I_D. Figure 4-2 shows the effect of this increase in V_T on the I_D-V_D curves of a device, at a constant V_G = +4 V. Clearly this can be a problem if the device is allowing less output current at a given operating point due to extended time at high gate biases and temperatures.

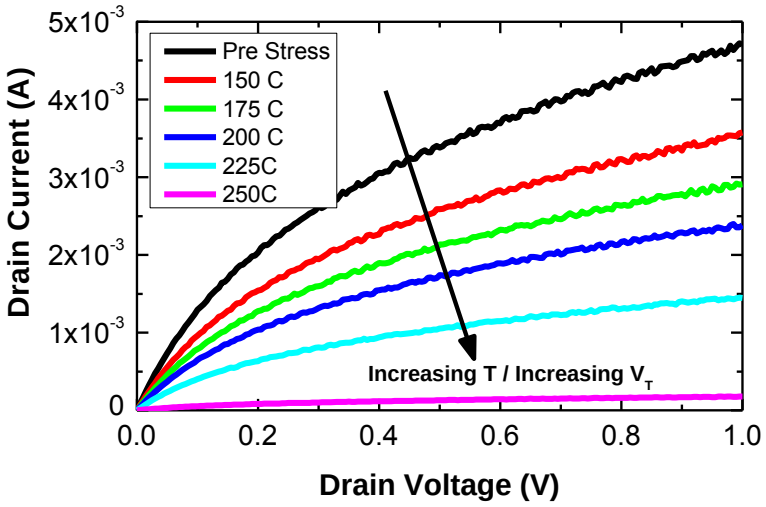

Figure 4-2. I_D-V_D plots of an n-channel SiC MOSFET with a constant gate voltage of V_G = +4 V. Each consecutive curve was measured after periods 7 minutes of biasing the gate at V_G = +20 V at the listed temperatures.

In order to further examine the shift in threshold voltage caused by stressing the gate at high temperature, a second experiment was performed which allowed us to observe this V_T shift over time at a particular stress voltage. This experiment consisted of heating the MOSFET to 225 °C and making a first I_D-V_G measurement in the same manner described above. Next, a gate bias of V_G = 20 V was applied for 2 minutes, after which another I_D-V_D curve was measured. This sequence was repeated for 4, 6, 8, 38, 68, and 98 minutes of stress. The I_D-V_D curves resulting from this measurement sequence are plotted in the right side of Figure 4-3; the left plot shows the shift in gate voltage required to achieve a particular drain current over time under stress.

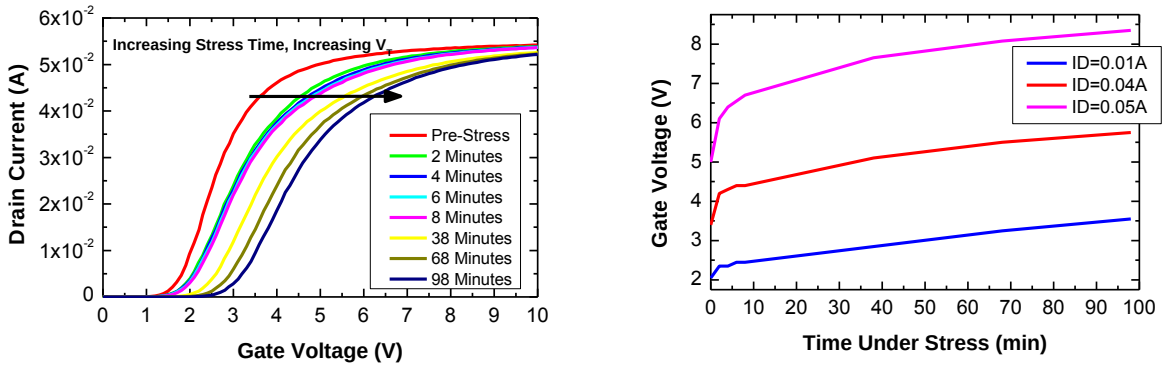

Figure 4-3. I_D-V_G plots resulting from stressing an n-channel SiC MOSFET (right) and gate voltage shift versus time (left) as described in the text.

The results in Figure 4-3 show an interesting phenomenon. It appears at first, there is a large shift in gate voltage that saturates relatively quickly. Then, there is a slow shift in gate voltage which continues for the duration of the test time. A possible explanation for this is as follows: the shift which saturates quickly is due to the filling of interface states that already exist at the SiC/SiO_2 interface. These existing states are able to fill with electrons quickly, especially at elevated temperatures. However, once these traps are filled with electrons, there is a slow gate voltage shift due to the creation of new interface states during the long term stressing of the device. We are planning further tests to confirm this, such as looking at the size of the fast shift after a long period of stressing to determine if it increases due to the generation of interface states. Also, charge pumping measurements before and after this measurement can confirm the increase in the density of interface states.

These results are significant in the context of PHM because they are allowing us to develop a model to predict the change in threshold voltage over time at a particular stress. This model will allow us to then predict the expected increase in on resistance over a period of time. At some point, the increase in on resistance will result in an unacceptable loss in power, and the replacement of this device should occur. By monitoring the output of the device, these models will allow us to plan this replacement before the system reaches this critical point.

5. HIGH-VOLTAGE STRESS ON SIC SCHOTTKY DIODES

The following experiments were performed on commercial SiC Schottky diodes in TO-220 packages. Current-voltage (I-V) curves were measured for these devices using Keithley model 2410 high-voltage source-measure units. Representative I-V curves for one packaged Schottky diode are shown below. Note that forward- and reverse-bias directions have been plotted separately due to the very different current and voltage scales required in each case.

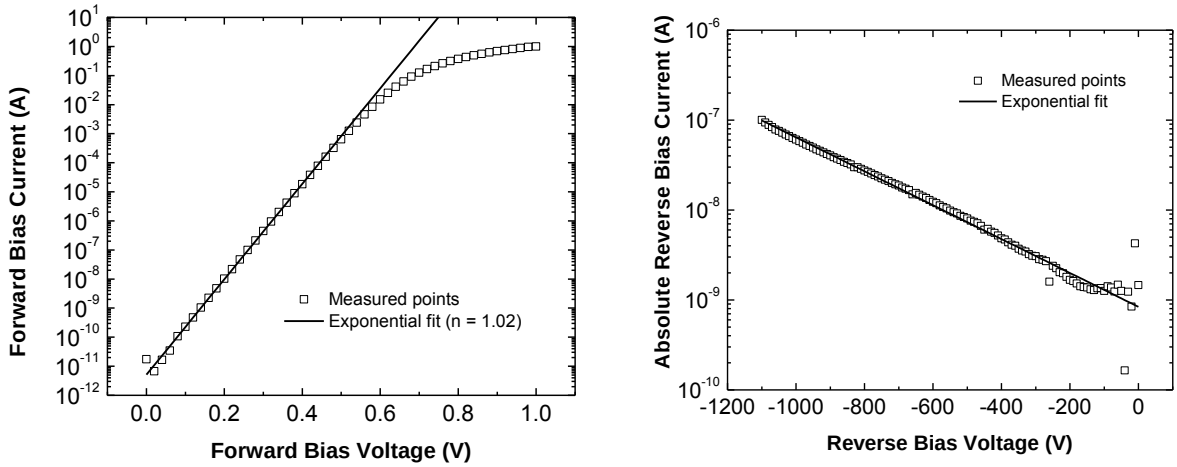

Figure 5-1. Current-voltage plots of SiC Schottky diode biased in forward (left) and reverse (right) bias configurations.

For the forward-bias case, an exponential fit has been made to the lower-voltage portion of the curve (the higher-voltage portion of the curve deviates from an exponential function due to series resistance effects). The fit is made to the following equation:

$$I = I_0 \exp\left(\frac{qV}{nkT}\right) \tag{5.1}$$

Here I_0 is a current pre-factor, q is the electron charge, V is the applied voltage, k is Boltzmann's constant, and T is the temperature. The quantity n is known as the "ideality factor" and is dependent upon the dominant carrier transport mechanism. We found n = 1.02 which is consistent with thermionic emission across a metal-semiconductor, as expected for a Schottky diode [14]. For the reverse-bias case, we also fit the data using an exponential function, although the physical interpretation is less clear in this situation. The reverse-bias current may be due to generation of carriers at the metal-semiconductor contact or within the semiconductor depletion region. We note that for this device, the current is at a very small value of 100 nA with -1100 V applied to the diode.

A different diode from the same batch was stressed at -1000 V for short period of time (5 seconds), and re-measured (reverse bias only). Results are shown below. It is seen that the reverse leakage current apparently decreases, although this appears to be a manifestation of a shift in the I-V curve towards more negative voltages; note that the point of minimum current is actually between -100 and -200 V after stress. The mechanism behind this is unclear. This may

be the result of an accumulation of charge somewhere in the device, which shifts the "flat-band" voltage of the device in a manner analogous to what was observed for the MOS capacitors. However, it is not clear what defects and/or mechanisms could be responsible for this. Further study is required.

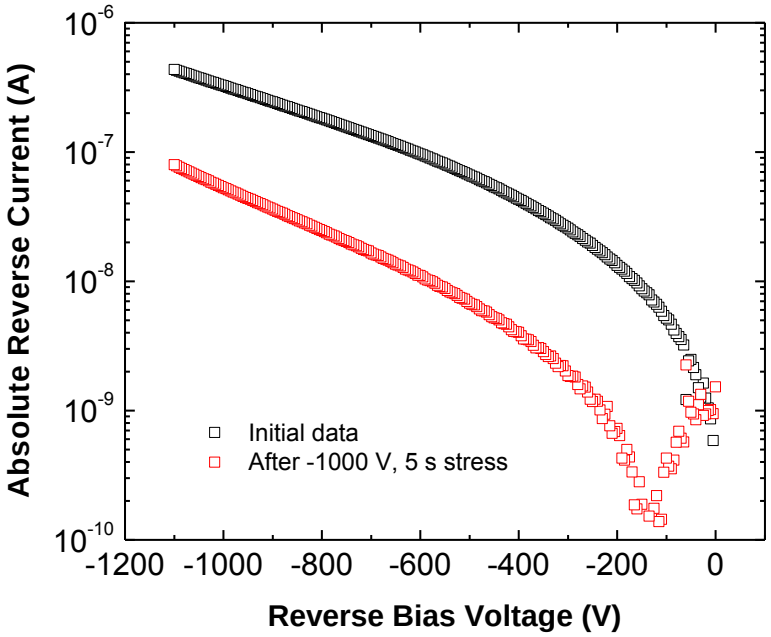

Figure 5-2. Current-voltage curves for SiC Schottky diode before and after reverse-bias high-voltage stress.

6. SUMMARY AND CONCLUSIONS

This project has been successful in advancing the state of the art in stress testing of SiC electronic devices. It is also laying the groundwork for realizing CM and PHM on advanced power electronic equipment. We have:

1. Developed relationships with several industrial and academic partners involved in post-silicon device fabrication.
2. Obtained a number of samples of SiC devices for electrical characterization and stress testing.
3. Modified experimental test set-ups to accommodate new devices and provide new stress conditions.
4. Performed electrical characterization and stress testing on several SiC devices to induce representative degradation signatures:
    a. I-V curve measurement and voltage stress to dielectric breakdown in MOS capacitors
    b. C-V curve measurement and bias-temperature-stress on MOS capacitors
    c. I-V (gate and drain) curve measurement and bias-temperature-stress on MOSFETs
    d. I-V curve measurement and reverse voltage stress in Schottky diodes
5. Demonstrated corresponding concepts for CM and PHM in the form of induced characteristic curve shifts that could be used as condition monitors or prognostic indicators of failure:
    a. Increased voltage drop for a given leakage current in MOS capacitors
    b. Flat-band voltage shift and C-V curve stretching in MOS capacitors
    c. Threshold voltage shift (increased on-state resistance) in MOSFETs
    d. Current drop for a given reverse voltage in Schottky diodes
6. Performed electrical characteristics measurements on other devices:
    a. SiC JFETs
    b. SiC thyristors.

This line of research is promising and presents a number of avenues for further work. First is the testing of additional devices and testing at higher stress levels. Testing devices under greater stresses has the potential to induce new failure modes that should be addressed in subsequent reliability improvement efforts. We have obtained a number of SiC-based devices of other types and are currently in the process of setting up testing methodologies for these devices. These include thyristors, other MOSFETs, and JFETs. In the past several months we have built a specialized test station designed to test such high-power devices in both the off-state (up to 2200 V) and the on-state (up to 400 A) which is enabling us to begin measurements on these devices. Another project would be to create simple sensors that can measure the degradation signatures that we identify. We would then be able to compare the measurements from simple sensors to those from laboratory instruments. Ideally, we will eventually be able to work with a utility partner to field a demonstration project using in situ versions of such sensors. While in situ sensors will be subject to severe environmental conditions and will never be as good as laboratory-quality instruments, it could be the case that they can provide equivalent information for prognostics purposes.

Eventually, there will be a greater need for research in theoretical and computational modeling and simulation (M&S) of physical failure mechanisms as well as development of algorithms that can use measurements along with M&S to provide predictions of time to failure. Also, once the failure mechanisms are better understood, it may be possible to work with an industrial partner to invent devices that would lend themselves more readily to CM and PHM without sacrificing performance. For example, if a device could be designed to degrade gracefully instead of suddenly and catastrophically, it would be possible to detect the changes in time to affect changes in operations or maintenance.

This research is pioneering in the field of reliability testing of post-silicon power electronics devices and will have a number of practical benefits and scientific spinoffs. If CM and/or PHM can be sufficiently developed, it will be possible to operate power electronics equipment in ways that will preclude catastrophic failures. That would in turn lead to a reduction in unscheduled downtime and a corresponding reduction in costs. Finally, the text mentioned several cases where additional research is needed to understand exactly what is happening in these devices. Resolving those questions in the course of the development will lead to original discoveries in basic device physics. More generally, research on improving the reliability of solid-state devices will play an important role in enhancing the performance and reliability of power conversion equipment as well as that of the larger electric grid.

7. REFERENCES

1. Office of Electricity Delivery and Energy Reliability, *Power Electronics Research and Development Program Planning Document*, U.S, Department of Energy Draft Document (circa 2008), http://www.ornl.gov/sci/electricdelivery/pdfs/PE_PP.pdf.
2. Mark A. Smith and Stanley Atcitty, "Power Electronics Reliability Analysis," SAND2009-8377, http://prod.sandia.gov/sand_doc/2009/098377.pdf, Sandia National Laboratories, (December 2009).
3. Nikhil M. Vichare and Michael G. Pecht, "Prognostics and Health Management of Electronics," IEEE Transactions on Components and Packaging Technologies, vol. 29, no. 1, p. 222 (March 2006).
4. Office of Electricity Delivery and Energy Reliability, *Smart Grid Research & Development Multi-Year Program Plan (MYPP)*, U.S. Department of Energy (2010), www.oe.energy.gov/DocumentsandMedia/SG_MYPP.pdf.
5. Procedure for the Wafer-Level Testing of Thin Dielectrics, JEDEC standard JESD35-A (2001).
6. M. Lenzlinger and E. H. Snow, "Fowler-Nordheim Tunneling into Thermally Grown SiO_2," Journal of Applied Physics vol. 40, p. 278 (1969).
7. C. H. Stapper, "On Yield, Fault Distributions, and Clustering of Particles," IBM Journal of Research and Development vol. 30, p. 326 (1986).
8. J. H. Stathis, "Percolation Models for Gate Oxide Breakdown," Journal of Applied Physics vol. 86, p. 5757 (1999).
9. R. Singh and A. R. Hefner, "Reliability of SiC MOS Devices," Solid State Electronics vol. 48, p. 1717 (2004).
10. I. H. Chen, S. E. Holland, and C. Hu, "Electrical Breakdown in Thin Gate and Tunneling Oxides," IEEE Transactions on Electron Devices vol. 32, p. 413 (1985).
11. M. G. Pecht, Prognostics and Health Management of Electronics, John Wiley & Sons Inc., Hoboken, NJ (2008).
12. P. A. Tobias and D. C. Trindade, Applied Reliability, Second Edition, Chapman & Hall / CRC, Boca Raton (1995).
13. J. W. McPherson and H. C. Mogul, "Underlying Physics of the Thermochemical E Model in Describing Low-Field Time-Dependent Dielectric Breakdown in SiO_2 Thin Films," Journal of Applied Physics vol. 84, p. 1513 (1998).
14. D. K. Schroder, Semiconductor Material and Device Characterization, Second Edition, John Wiley & Sons, New York (1998).
15. M. J. Marinella, D. K. Schroder, T. Isaacs-Smith, A. C. Ahyi, J. R. Williams, G. Y. Chung, J. W. Wan, and M. J. Loboda, "Evidence of Negative Bias Temperature Instability in 4H-SiC Metal Oxide Semiconductor Capacitors," Applied Physics Letters vol. 90, pp. 253508-1-3, (2007).

16. D. Alok, P.K. McLarty, and B.J. Baliga, “Electrical properties of thermal oxide grown using dry oxidation on p-type 6H-silicon carbide,” Journal of Applied Physics vol. 65, p 2177 (1994).
17. M. J. Marinella, D. K. Schroder, T. Isaacs-Smith, J. R. Williams, G. Y. Chung, and M. J. Loboda, "Carrier Generation Lifetimes in 4H-SiC MOS Capacitors," IEEE Transactions on Electron Devices vol. 57, p. 1910 (2010).

DISTRIBUTION

1	MS1033	Stanley Atcitty	6336 (electronic copy)
1	MS 1084	Richard Dondero	1748 (electronic copy)
10	MS 1084	Robert J. Kaplar	1748
10	MS 1084	Matthew Marinella	1748
10	MS1188	Mark A. Smith	6342
1	MS1188	Bruce M. Thompson	6342 (electronic copy)
1	MS 0899	Technical Library	9536 (electronic copy)
1	OE-10	Office of Electricity Delivery & Energy Reliability Attn: Imre Gyuk U.S. Department of Energy 1000 Independence Avenue, SW Washington, DC 20585	