CONF-951156--1
SAND95-0624C

To be presented at the International Symposium for Testing and Failure Analysis
Santa Clara, CA, November 6-10, 1995

Future Technology Challenges for Failure Analysis

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Abstract

Failure analysis is a critical element in the integrated circuit manufacturing industry. This paper explores the challenges for IC failure analysis in the environment of present and future silicon IC technology trends, using the 1994 National Technology Roadmap for Semiconductors as a technology guide. Advanced failure analysis techniques that meet the challenges of state-of-the-art IC technology are described and their applications are discussed. New paradigms will be required for failure analysis to keep pace with future advancements in IC technology.

FAILURE ANALYSIS IS A CRITICAL ELEMENT for all phases of the integrated circuit (IC) product cycle (1). The goal of failure analysis (FA) is to determine the root cause of a failure or parameter excursion so that corrective action can be taken. In the broadest sense, FA includes support of fabrication tool development, processing development, technology development, manufacturing, testing, and field return analysis of ICs. A broad definition of FA includes physical material analysis as well as electrically oriented defect localization. FA is performed on unpatterned test wafers, short loop monitor wafers, test circuits on completely processed wafers, IC die, and packaged ICs. Because of the level of complexity of current IC technologies, test structures are often substituted for ICs during development to facilitate yield analysis. In this case, the surrogate test structures must dependably predict effects that will be manifested in the IC.

As IC technology advances, FA technology must keep pace if it is to provide the needed level of support (2). A clear roadmap of where IC technology is headed is a prerequisite for guiding the research and development activities needed to provide the matching advancements in FA technology. The 1994 National Technology Roadmap for Semiconductors (NTRS) (3) provides a 15 year projection of technology trends for leading edge ICs. Table I shows selected technology characteristics from the NTRS for the years 1995 and 2001. A six year projection is a reasonable point of comparison and provides an appropriately advanced technology target as a driving force for the development of advanced FA techniques. Other relevant technology characteristics are the increasing use of completely planarized surfaces and the utilization of upper wiring levels as power distribution planes. The NTRS also addresses trends toward higher density packaging technologies including flip chips, ball grid arrays, and multichip modules (MCMs). MCM technology introduces a host of challenges for FA, but we address only the impact of flip chip die attach technology in this paper.

Table I. Selected technology characteristics from the NTRS (3).

Characteristic	1995	2001
wafer size	200 mm	300 mm
die size (DRAM)	250 mm^2	360 mm^2
feature size	0.35 µm	0.18 µm
wiring levels	4 - 5	5 - 6
bits/chip (DRAM)	64 M	1 G
clock frequency	150 MHz	300 MHz
operating voltage	3.3 V	1.8 V
chip I/Os	900	2000

In this paper we review developments in failure analysis tools and techniques that help meet the challenges presented by state-of-the-art IC and packaging technologies. These techniques may enable analysis of circuits where, for example, additional interconnection levels, power distribution planes, or flip chip packaging completely eliminate the possibility of employing standard optical or voltage contrast failure analysis techniques without destructive deprocessing.

The focus of this paper is primarily on defect localization using techniques based on advanced imaging and on the interaction of various probes with the electrical behavior of devices and defects. The challenges that technology advancement poses for detailed material characterization using physical, chemical, and optical techniques are not discussed here since they have been reviewed thoroughly elsewhere (4).

New paradigms for failure analysis will be needed to meet the challenges posed by the billion transistor ICs that are anticipated by the NTRS. This paper discusses some of these new thrusts: failure analysis using only electrical test data, design for FA, networking of FA equipment, FA information systems, and multimedia training for failure analysts.

Imaging Techniques for ICs

Optical Microscopy. Optical microscopy techniques are able to locate many physical defects and have been a mainstay in FA for years. However, smaller feature sizes are pushing optical microscopy towards its resolution limit, around 0.2 - 0.3 μm using visible light. Other technology trends that have a large impact on optical microscopy include additional interconnection levels, power distribution planes, and flip chip packaging. Obviously, an optical image from the top of an IC reveals few features deep in the structure if there are many interconnection levels and power distribution planes that obscure a large percentage of the IC surface. Scanning optical microscopy (SOM) provides improved image resolution and contrast compared to conventional optical microscopy. The use of IR lasers extends the usefulness of the SOM by permitting observation through the wafer, because silicon is transparent to IR. Images of the active regions of an IC can be obtained using reflected IR microscopy from the back of the die with a resolution of resolution about 0.6 μm. This circumvents problems caused by additional interconnection levels, power distribution planes, and flip chip packaging, but the spatial resolution may be insufficient for future technologies.

Scanning Electron Microscopy. As IC feature sizes decrease and defects of smaller size become more important, imaging techniques with higher resolution than optical microscopy are required. For the 0.18 μm technology in year 2001, the maximum allowable particle defect size is 0.06 μm (3). SE Secondary electron (SE) imaging in a field emission scanning electron microscope (FESEM) generates a high resolution (2-5 nm depending on beam energy), large depth of field image that depicts the surface topography of an IC. FESEMs have excellent spatial resolution at low beam energies, allowing nondestructive imaging of in-process wafers and high resolution imaging of insulating layers without charging problems.

Although SE imaging in the FESEM will not have difficulty resolving features the size of future lateral IC dimensions, the increasing use of planarization techniques negates the effectiveness of SEM imaging. Unless deprocessing approaches are employed, SEM images of planarized surfaces will provide little information. The features that must be imaged in cross section have already decreased to near the FESEM resolution limits, and defects that can cause failure in these films may be smaller yet. Detailed root cause analysis may require the use of a transmission electron microscope (TEM), which provides resolution down to the sub-nanometer scale.

Scanning Probe Microscopy. Scanning probe microscopy (SPM) is a rapidly growing field that is just beginning to have an impact in the FA of ICs. Samples are imaged in an SPM by scanning a sharp probe tip in close proximity to the sample surface and detecting the interactions between the tip and the sample. Scanning probe instruments provide an entirely new capability for topographical imaging of submicron structures, extending spatial resolution well beyond the limits of optical tools. Scanning tunneling microscopy (STM) provides topographic imaging of conductive surfaces with resolution to the atomic level. Atomic force microscopy (AFM) provides a topographical map of conducting or insulating surfaces with resolution also to the atomic level. AFM has recently been used to image IC cross sections with nanometer resolution, better than that obtainable with optical microscopy or SEM (5). Scanning near-field optical microscopy (SNOM) combines optical and scanning probe technologies and can image surfaces on a scale well beyond the classical diffraction limit (6).

Focused Ion Beam Techniques. The capabilities of focused ion beam (FIB) systems are rapidly becoming critical for FA of submicron technology ICs. FIB systems use a focused beam of Ga^+ ions for imaging, milling, etching, and deposition of metals and dielectrics. No other tools provide these capabilities with sufficient spatial control to effectively support technologies with 0.18 μm feature sizes.

FIB system ion milling and imaging enables in situ cross sectioning, an effective approach for analyzing the root cause of a failure. Sequential cross sections can be made through a feature of interest. Upper layers of an IC may be milled away to expose underlying layers for mechanical or electrical analysis, and conductors may be cut to isolate interconnections and devices.

FIB systems also can be used to precisely deposit conductors and dielectrics, enabling local modification of electrical interconnections and deposition of additional contact areas that can be used to probe circuit functions and measure voltages on functioning ICs (7).

Failure Analysis Techniques for Powered ICs

Larger IC die sizes and higher integration levels have made FA impossible using purely physical techniques. There is simply too much circuitry to analyze. Even for test circuits and short loop monitors, it is not cost effective to apply only physical analysis techniques. Powerful FA techniques based on the application of internal IC probing using electron beam, optical beam, and scanning probe techniques combined with electrical stimulation of the IC inputs have enabled dramatic improvements in rapid defect localization. In many cases the level of integration of the IC is not an important factor in quickly isolating the defect, since the signal from the defect can be observed even at magnifications low enough to image the entire IC. Subsequent high magnification observation then allows the defect signal to be correlated with circuit features.

Technology trends that have a significant impact on FA techniques using electrical stimulation are higher clock frequencies, lower operating voltages, and increased I/O pin counts. These trends dictate the use of higher performance test equipment and enhancement of the electrical interconnections between the tester and the FA apparatus.

Light Emission. Light emission (LE) analysis, also known as photoemission microscopy, is often the primary tool for localizing many types of common IC defects on large die with small feature sizes and high integration levels. LE is effective in identifying gate oxide shorts, degraded *pn* junctions, and MOS transistors in saturation due to interconnection shorts and open circuit defects (8). LE performed while employing extensive test vector sets enables rapid localization of all light emitting defects on an IC at low magnification, independent of feature size. Because the emitted photons have energies in both the visible and near IR wavelengths, LE can be observed from the backside of the die. This circumvents optical obstruction caused by additional interconnection levels, power distribution planes, and flip chip packaging. Figure 1 shows a low magnification light emission image of a double metal, 32-bit microprocessor with four gate oxide shorts (highlighted by the four white boxes). The image was acquired while dynamically exercising the IC with a functional test vector set.

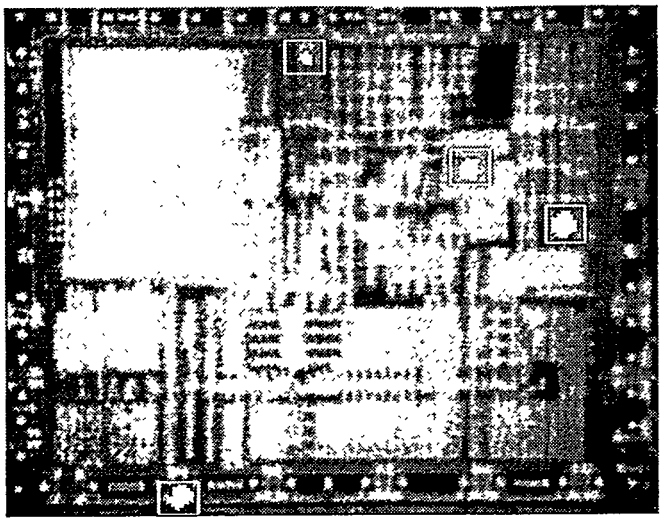

Fig. 1. Low magnification light emission microscopy image showing four gate oxide shorts (bright areas in the four boxes) on a 32-bit microprocessor.

Voltage Contrast. Electron beam voltage contrast (VC) techniques, also known as electron beam testing, have an important role in FA since they provide nondestructive methods for observing internal IC operation and the electrical effects of defects. Advanced electron beam test systems provide integration of CAD databases and permit comparison of control and failing devices through image processing. Software tools are available that reduce the time to locate and analyze logical faults through an automated backtracing approach (9). Evolutionary improvements in electron beam test equipment will continue, providing better voltage, timing, and spatial resolution as well as more powerful software control. However, there are fundamental limitations imposed by advances in IC technology that must be addressed in order for VC to remain useful.

The most obvious challenge is simply dealing with the complexities introduced by larger die sizes, smaller feature sizes, and higher integration levels. Advances in software for navigation, test point selection, and data analysis will be needed. The decreasing feature sizes also result in more interference from adjacent conductors in the VC measurements. Higher clock frequencies and lower operating voltages will necessitate development of faster electron beam gating and more sensitive SE energy spectrometers. Perhaps the most difficult challenge is posed by the increasing number of interconnection levels and the use of the upper metallization level or levels as power planes. The shielding effect of these wiring levels will render VC analysis ineffective on fully processed ICs without deprocessing. Solutions to this problem include designed-in internal test points on the uppermost metallization layer and the use of a FIB system to open vias to lower levels or create probe pads at the point of interest. Flip chip packaging will render VC useless without disassembly It appears that a design for FA philosophy will be necessary in order to maintain the utility of VC for analyzing the circuits of the future.

Resistive Contrast Imaging. Resistive contrast imaging (RCI) is a SEM technique that generates a relative resistance image of the conductor path between two test nodes (10). RCI enables rapid localization of abrupt resistance changes, such as open or short circuits. The main advantage of RCI is that no deprocessing is needed, since overlying conductors and dielectrics do not prevent imaging of structures underneath. The primary application of RCI is analyzing multilevel IC test structures such as electromigration structures and via chains. Figure 2 shows a low magnification RCI image of a test structure with four metal-1 to metal-2 via chains Three via chains are defect free and show a gradual resistance change along the conductor (gradual bright to dark contrast), while the via chain on the right has an open via which is easily identified by the abrupt contrast change.

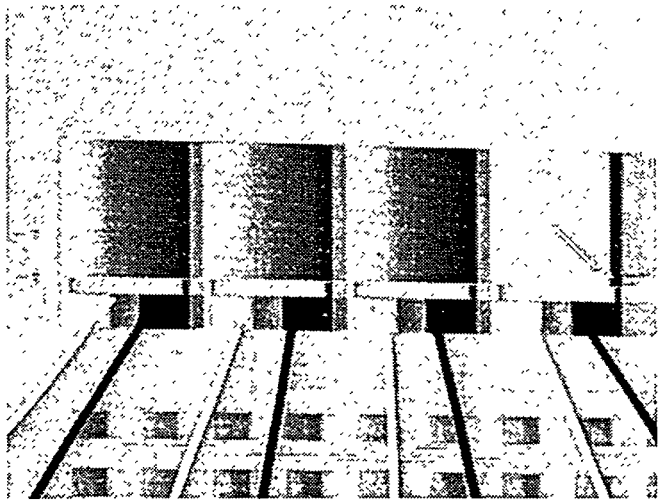

Fig. 2. RCI image of four via chains. The chain on the right has an open via at the location of the abrupt contrast change.

Charge-Induced Voltage Alteration and Light-Induced Voltage Alteration. Charge-Induced Voltage Alteration (CIVA) (11) and Light-Induced Voltage Alteration (LIVA) (12) are techniques that provide a fast, simple method for locating open conductors and contact, via, and junction defects. Open circuit defects traditionally have been very difficult to localize in complex ICs since the failure signature often is not obvious. CIVA and LIVA simplify localization of these defects on an entire IC in a single, low magnification image, independent of feature size, with the ability to zoom in and correlate the defect site to circuit features. Both techniques employ the same electrical approach but use different probes: CIVA employs an electron beam while LIVA uses a photon (laser) beam.

CIVA analysis circumvents many of the challenges of IC technology advancement. CIVA may be performed through multiple layers of dielectrics and metals by increasing the electron energy, but care must be exercised to avoid irradiation damage to the IC. Figure 3 shows an example of low magnification CIVA imaging of a 1 µm, passivated, double metal gate array with an open metal conductor. The CIVA image (bright white lines) of the conductor network with an open circuit is superimposed on a secondary electron image.

CIVA may be performed nondestructively on fully processed ICs using low electron beam energies. This technique is called low energy CIVA (LECIVA) (13). Figure 4 shows a low magnification LECIVA image of the conductor network connected to an open metal-2 to metal-3 via on a 0.8 µm, triple metal technology Intel 486 microprocessor. Application of LECIVA is subject to the same limitations that apply in VC, since lower conductor levels may be analyzed only if they are not completely covered by other metal layers.

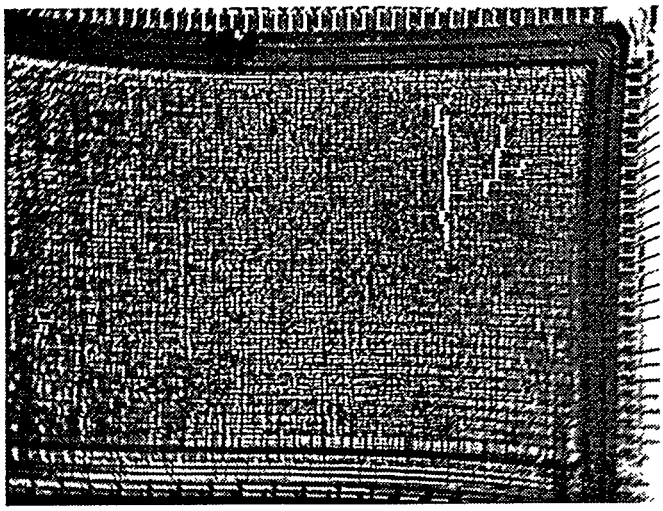

Fig. 3. Low magnification CIVA image of an open conductor network (bright white) superimposed on a secondary electron image of a gate array IC.

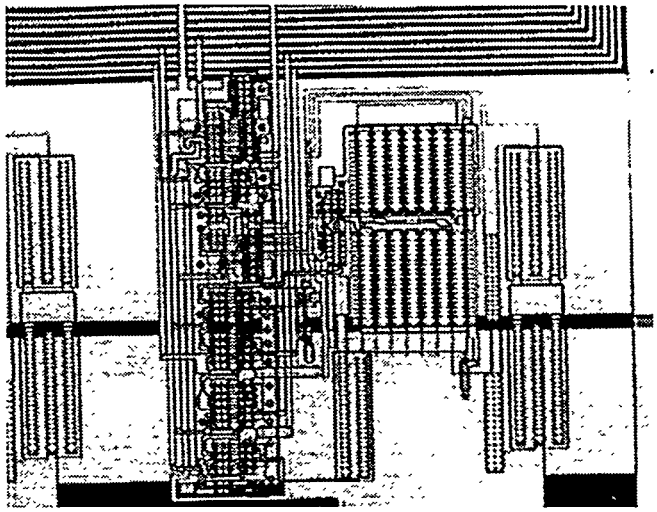

Fig. 5(a). Backside IR SOM image of an I/O port on a microcontroller.

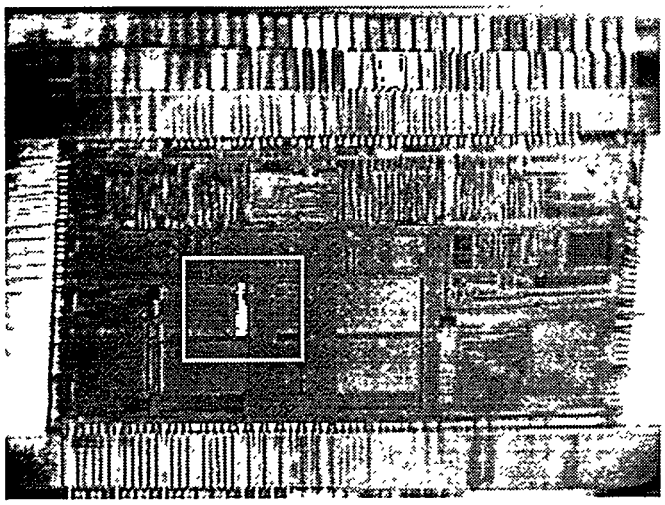

Fig. 4. Low magnification LECIVA image of conductors connected to an open via (bright area in box) superimposed on a secondary electron image of an Intel 486 microprocessor.

Fig. 5(b). Backside LIVA logic state image of the I/O port shown in Figure 5(a).

LIVA uses a SOM to quickly localize either defective *pn* junctions or biased junctions that are electrically connected to defects such as open circuits. LIVA can also identify the logic states of transistors with much greater sensitivity than other optical techniques. LIVA analysis is performed from the front of an IC die using a visible laser or from the back of the die using an infrared laser. Figure 5(a) shows a backside IR SOM image of an I/O port region of a 1.25 µm, double metal technology microcontroller, and Figure 5(b) shows the backside LIVA logic state image when the port is in the "1" state. The dark contrast areas indicate *p*-channel transistors that are "off". The "fuzziness" of the image results from the diffusion length of the optically generated electrons and holes. Note that the transistors in the image are completely covered by metal-2, so no front side imaging or logic state analysis is possible.

Scanning Probe Microscopy Techniques. In addition to imaging, SPM techniques have been used to measure internal voltages and currents on ICs. Charge force microscopy (CFM) can perform potentiometry within ICs with submillivolt sensitivity and has also been applied to develop an AFM-based voltage contrast technique for measuring voltage waveforms up to 20 GHz (14) Magnetic force microscopy (MFM) uses a magnetized tip to detect magnetic force gradients. MFM current contrast imaging can analyze internal IC currents with a sensitivity of ~ 1 mA dc and ~1 µA ac (15). The combination of CFM and MFM in a single instrument may enable simultaneous measurement of internal IC voltages and currents. CFM will experience technological limitations similar to those discussed for VC analysis, while MFM will suffer lower spatial resolution due to the long range of magnetic forces. However, MFM is capable of detecting currents on conductors located beneath other conductors for the same reason.

Focused Ion Beam Techniques. If electrical feedthroughs are provided in the FIB chamber, in situ electrical measurements may be used to extend the capabilities of FIB techniques (16). For example, electrical monitoring of circuit operation can provide end point determination for IC modification operations such as conductor cutting and deposition. Voltage contrast imaging using the positive ion beam (analogous to electron beam VC) may be employed to determine the potentials of circuit elements.

Thermal Imaging. Thermal imaging techniques are helpful in defect localization when there are no obvious detectable symptoms such as light emission or CIVA/LIVA signals. Thermal imaging techniques rely on detecting a defect in an operating IC through a local temperature increase caused by increased power dissipation. These techniques are generally unaffected by feature size, integration level, number of interconnection levels, and planarization. However, thermal conductivity may cause a somewhat diffuse "hot spot" and the spatial resolution of the imaging system may not be the limiting factor in defect localization.

Liquid crystal techniques are commonly used for "hot spot" detection. The spatial resolution and temperature resolution of this technique are relatively poor and there is no temperature mapping capability. Infrared thermography provides a temperature map of the IC surface with good temperature resolution. However, the spatial resolution is relatively poor. Fluorescent microthermographic imaging (FMI) uses the temperature dependent fluorescence quantum yield of a rare earth chelate to provide a direct, quantitative measurement of surface temperature (17). This technique has excellent spatial and temperature resolution, and research to improve the technique is ongoing (18).

New Failure Analysis Paradigms

Failure Analysis Using Only Electrical Testing. Abandoning traditional FA approaches and embracing automatic defect analysis using only electrical testing at the IC I/Os is indeed a paradigm shift. The NTRS identifies the need for improvements in defect modeling, automatic test vector generation, utilization of I_{DDQ}, boundary scan and full scan techniques, and incorporation of built-in-self-test (BIST) in order to realize this goal.

Recently, a new defect class strategy has been developed that inherently links to the circuit architecture and moves away from the classic stuck-at fault model that postulated abstract representations of defects (19,20). This strategy also provides guidance for maximum defect coverage with a minimum of test vectors. Parametric testing techniques for CMOS IC diagnosis are becoming more ubiquitous. In addition to increased defect and fault coverage, I_{DDQ} testing enables rapid identification and physical localization of many design, layout, and fabrication problems (21). Software tools have been written that relate I_{DDQ} test vectors to logic fault and physical defect localization (22,23).

Design for Failure Analysis. Circuit designers must consider testability early in the product concept stages. The risks of missing critical time to market deadlines and product failures make design for testability necessary. Design for FA is an equally critical process as IC technology continues to advance. Design for FA benefits include reduced time and cost for analysis and faster feedback of corrective action throughout the product cycle. Concepts for design for FA include designing to facilitate I_{DDQ} testing, incorporating scan and BIST, circuit partitioning, laying out test points for VC analysis (as discussed earlier), building in fiduciary marks for navigation, providing TEM test structures, and fabricating test circuits and surrogate ICs during the new technology development phase.

Networking of Failure Analysis Equipment. Larger die, higher integration levels, completely planarized surfaces, additional interconnection levels, and power distribution planes all create navigation difficulties while performing FA. CAD navigation software is typically provided on electron beam probe systems and can be installed on focused ion beam systems and other FA equipment. This software links layout and schematic information from the CAD database with images and internal probe data from the FA tools. Linkage assists in positioning probes at the point of interest and correlating the defect site to its physical and electrical location. However, full integration throughout the FA laboratory is uncommon. Further utilization of the CAD database, such as providing cross section diagrams of any location on the IC, will greatly assist the failure analyst. Ultimately, networking of all FA tools in the laboratory and linking with the design and test databases may be required for effective FA.

Failure Analysis Training and Information Systems. FA is a multidisciplinary activity. The effective failure analyst must understand circuit design, IC architecture, semiconductor device physics, IC processing, and IC testing. This broad set of skills takes years to acquire, perhaps through rotational assignments in different departments of a company, while constant advances in technology further complicate the process. Analyst training is usually accomplished on the job and through conference attendance, since few universities provide directly applicable laboratory experience. There are several short courses and seminars that provide useful general information, but the depth of coverage may be insufficient to provide immediate help in the workplace. FA books also have broad applicability, but rapidly become dated as technology advances.

A new paradigm for training failure analysts is the use of failure analysis databases, hypertext help systems, and expert systems. These software products also add value by preserving the knowledge of experienced failure analysts, which is usually lost through retirement or job change. A large "smart database" has been described that uses all of a company's FA records to prediction failure mechanisms and propose FA activities (24). Interactive FA expert systems have been implemented to help train inexperienced analysts as well as guide and assist experienced analysts (25). One limitation is the time and effort necessary to test and debug these systems. Because of this limitation, researchers have begun to look at other ways to deliver FA information. The World Wide Web (a graphical, hypertext view of the Internet) is one option under development that will provide up-to-date, comprehensive multimedia information and training to analysts at their work locations.

As computer technology continues to evolve and network bandwidth increases, multimedia training will become more prevalent. Failure analysts will be able to receive audio instructions for FA procedures. For example, the analyst can have the computer audibly dictate instructions on how to perform a wet chemical etch. The analyst will not have to type on a keyboard or read a computer screen while the etch is being performed. Failure analysts will also watch computerized video clips that describe such procedures as deliding an IC or adjusting the electron beam parameters on a new scanning electron microscope.

Conclusions

FA in today's IC industry is squeezed between the need for very rapid analysis to support manufacturing and the exploding complexity of IC technology. A number of advanced techniques and tools have been developed that enable FA to keep pace with IC technology. However, the technology roadmap for the future poses such large challenges that new paradigms for FA must be realized.

Acknowledgment

The authors thank Daniel L. Barton, Ann N. Campbell, and Edward I. Cole Jr. of Sandia National Laboratories for their contributions and review. This work was performed at Sandia National Laboratories and supported by the U. S. Department of Energy under contract DE-AC04-94AL8500.

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