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Perspective

Roadmap to 100 GW_{DC}: Scientific and supply chain challenges for CdTe photovoltaics

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CONTEXT & SCALE Photovoltaics are expected to be deployed worldwide at the 10s of TW scale by mid-century, with hundreds of GWs in the United States. CdTe photovoltaic modules represent 16% of the solar power generation portfolio in the United States and are poised to find increased deployment globally in the coming years. CdTe photovoltaics have advanced significantly in photoconversion efficiency and are particularly effective in hot and humid climates, where they benefit from higher energy yield than comparable Si modules. Previously considered niche with limited room for growth due to the availability of Te, the manufacturing capacity has grown rapidly, maintaining an average compounded annual growth rate of 37% since 2017. This roadmap discusses the specific scientific research and Te supply chain challenges that must be addressed to enable the CdTe photovoltaics industry to continue to expand with the goal of reaching a manufacturing capacity of 100 GW_{DC}/year by 2030.

SUMMARY

This roadmap highlights pathways to expand the CdTe module manufacturing capacity per year to 100 GW_{DC} by 2030 by improving Te extraction from existing supply chains, minimizing Te usage in modules by leveraging thinner absorbers, and focusing research efforts in key areas to improve module efficiencies. Both scientific and supply chain innovations will be necessary to maintain the high compound annual growth rate of the CdTe photovoltaic (PV) industry and cement its role as a key technology for multi-TW-scale PV deployment.

INTRODUCTION

Photovoltaics (PVs) are growing rapidly as the world's need for energy increases. Projections for growth in PV have fallen short of actual market development due to greater than expected cost reduction and systems deployment flexibility in terms of both location and installation size. Thus, targets and expectations are repeatedly shifted upward.[1] In 2024, the average module price decreased to 0.22 USD/W_{DC}, and global installed capacity surpassed 2 TW_{DC}.[2–4] Thin-film cadmium telluride PV is the only PV technology besides silicon that is currently manufactured at GW scale, with about 20 GW_{DC} of annual production capacity globally and 10 GW_{DC} of annual production in the United States (US). CdTe PV is used almost exclusively in utility-scale deployments. While CdTe PV modules comprise ~5% of the global PV market, which is dominated by Si PV modules, they represent 16% of the total solar power generation portfolio in the US and 40% of US utility-scale deployment.[5]

CdTe has been growing disproportionately in the US and the US utility-scale market due to a combination of policy and technology factors. Trade policy has protected US PV manufacturing by imposing tariffs on imported cells and modules and enforcing anti-dumping and countervailing duties.[6] Additional tax credits also became available in 2022 for US-based manufacturing

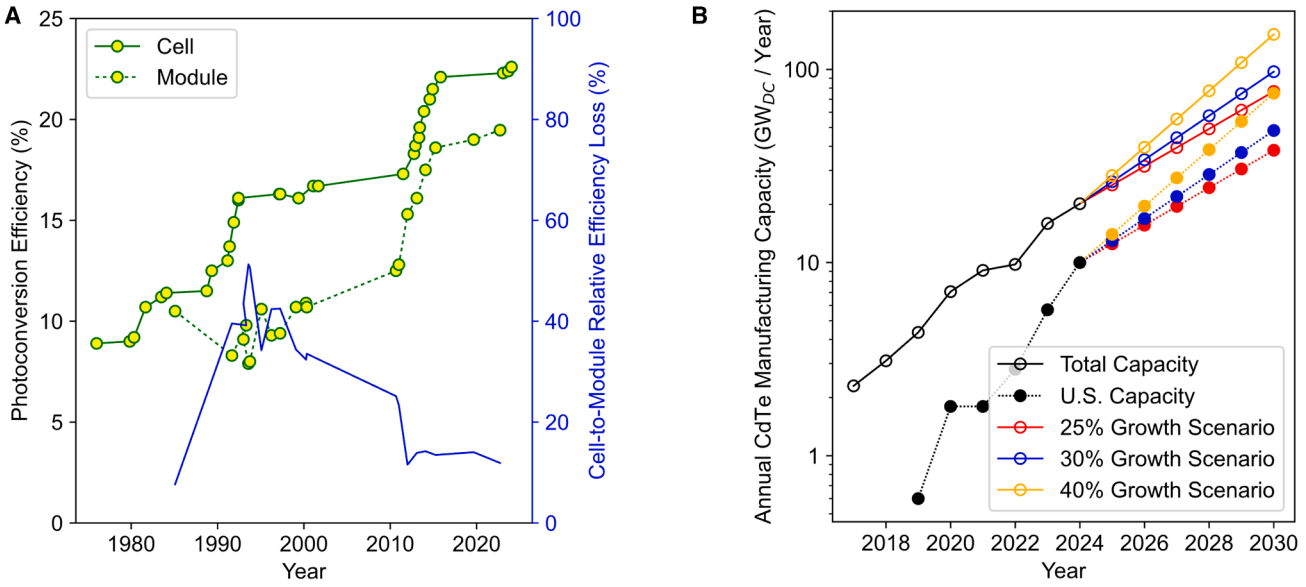

Figure 1. Trends in CdTe photoconversion efficiencies and manufacturing capacity

(A) NLR-certified record cell and module efficiencies for CdTe PV. The blue line and right axis show the gap between cells and module relative efficiency. Since 2010, this difference has been almost entirely due to monolithic integration and the edge-delete that is required to provide voltage isolation. With advances in scribing and packaging, the cell-to-module gap has been nearly constant, with modules foregoing about 15% efficiency of the record cell through this photoinactive area.

(B) US and global CdTe manufacturing capacity from 2017 to 2024 with an average compounded annual growth rate (CAGR) of 37%. CAGR projections of 25%, 30%, and 40% are shown, with 30% CAGR achieving 100 GW by 2030.

and US-sourced module content. As a GW-scale PV technology with a high fraction of US content and a strong US manufacturing base, CdTe has benefited from this incentive structure.

In addition to a competitive cost per watt, growth of CdTe in the US utility-scale market can also be traced to predictable performance and energy yield (EY) advantages (*vide infra*), all of which contribute to bankability. Studies appearing in 2014 showed that early CdTe modules had an excellent performance ratio in comparison to crystalline Si modules available at that time.[7,8] Surprisingly, there are very few studies that compare the performance of different technologies side-by-side. Long-term performance data from fields deployed with prototype CdTe technology in 1995 and series 2 CdTe technology in 2003 show degradation rates of −0.42% per year and −0.24% per year in 2025, after 30 and 22 years of operation, respectively.[9] Both of those systems are still operating on NLR's campus and have completed more than 25 years of testing (Note S1). Results from these long-term experiments enabled CdTe PV manufacturer First Solar to increase the length of its warranty from 25 to 30 years.[10] These early versions of CdTe PV used Cu doping and other module technology that is relatively unsophisticated in comparison with today's technology.[11]

The cost and performance of CdTe modules have continued to improve due to advances in research, development, and manufacturing. After several years of little improvement, the record efficiency for CdTe cells began to move upward in 2023 as group V (Gr-V) dopants were introduced. Four new cell efficiency records were certified at NLR over a 15-month period. The certified record CdTe cell, produced by First Solar, now stands at 23.1% in photoconversion efficiency (*PCE*) through leveraging Gr-V-doping technology of a Cd(Se,Te) alloyed absorber[12] (Figure 1A). Notably, the open-circuit voltage of the record cell is now above 900 mV. Improvements in J_{SC} have been driven by remarkable engineering, but the V_{OC} and fill factor (*FF*) deficits are more difficult to solve due to scientific knowledge gaps and the complexity of the device. Production modules currently use Cu-doped $CdSe_xTe_{1-x}$ absorber layers, but a manufacturing transition to Gr-V doping is presently underway. As market demand has grown, module manufacturing capacity has also expanded. Figure 1B shows how the global (total) and US manufacturing capacity for CdTe PV modules has grown with time. The manufacturing capacity for CdTe PV has been growing at a compound annual growth rate (CAGR) of 37% since 2017. Projecting this rate into the future suggests that a manufacturing capacity of 100 GW_{DC}/year should be possible by 2030, enabling multi-TW_{DC}-scale deployment by mid-century.

This roadmap describes the pathways and challenges to reaching 100 GW_{DC}/year by 2030. In the first section, "CdTe in the PV market," the role of CdTe PV is given context by comparing the technology with market-leading silicon PV. The next section, "Te supply pathways for scaling to 100 GWDC/year," examines historical and projected Te supply and proposes specific developments to improve Te supply. Finally, in "key device research areas," we discuss specific scientific work that will enable cross-cutting improvements in device voltage, efficiency, and tellurium utilization. This roadmap is intended to provide direction and stimulate work within the CdTe

PV community to address key challenges to enable 100 GW-scale CdTe module production with higher *PCE*, lower Te intensity, and improved bifaciality.

CdTe IN THE PV MARKET

CdTe PV competes with other technologies available in the marketplace. Si PV is the obvious measuring stick as the market-leading technology. Key metrics for comparison include EY, capital and operational expenditures (CapEx and OpEx, respectively), and embodied carbon.

The largest manufacturer of CdTe modules is First Solar. Their series 7 module is 2.8 m^2 in area and generates up to 540 W of power under AM1.5G standard test conditions (STCs) with a total-area *PCE* of up to 19.7%. The efficiency of the series 7 module is 20% below that of premium silicon heterojunction (SHJ) modules (24.8%) but only 10% below the more widely manufactured, lower-cost, passivated-emitter rear contact (PERC) modules (21.7%) and 15% below tunnel oxide passivated contact (TOPCon) modules (23.2%). While SHJ modules account for only ~2% of the global PV manufacturing capacity due to high manufacturing costs, many PERC manufacturing lines are compatible with retrofits to enable TOPCon module manufacturing.[13] Nameplate *PCE*s provide one point of comparison, but PCEs are based on measurements under STCs that deployed modules rarely, if ever, experience. Namely, "one sun" (1 kW/m^2) of a standard reference spectrum (e.g., AM1.5G) at 25°C.

The EY of a PV system, instead, offers a better performance metric. Measured in kWh/kW_P, where W_P is the power output under STC. The EY varies based on deployment location and is geographically dependent on variations in irradiance, temperature, and humidity. Systems with lower nameplate *PCE* can generate higher EY under conditions that differ from STC. Si is an indirect band-gap semiconductor with a relatively low band gap of 1.12 eV. Thus, Si PV is much more sensitive to changes in the infrared portion of the irradiance than is CdTe PV, which has a tunable band gap between 1.39 and 1.5 eV depending on the amount of Se that is alloyed to form the Cd(Se,Te) semiconductor. This difference in sensitivity to infrared makes CdTe less sensitive to spectral variations in more humid climates.

Temperature also plays an important role in EY. First Solar's current series 7 modules have a smaller temperature coefficient (−0.32%/°C) than industry-leading PERC modules (−0.34%/°C), providing an advantage in hotter climates. TOPCon modules have an improved temperature coefficient, as low as −0.29%/°C, while more expensive SHJ modules have demonstrated an even smaller temperature coefficient of −0.21%/°C. The temperature coefficient for First Solar's series 4 module, the last series to be fabricated without any alloyed Se at the front interface, had a temperature coefficient of −0.29%/°C. The introduction of Se led to a slight increase in the temperature coefficient, presumably due to the slightly smaller band gap. However, temperature coefficients as low as −0.23%/°C have been demonstrated in next-generation Gr-V-doped CdSeTe absorbers in the lab.[14] This result is in line with expectations based on more classical substitutional doping, as compared with recombination processes associated with Cu and Cl defect complexes that are at play in the Cu-doped versions of CdTe technology.[15] Module efficiency and temperature coefficient data can be found in the supplemental information (Note S2).

As noted earlier, there are surprisingly few experimental studies that compare the long-term performance of different PV technologies side-by-side. Consequently, this analysis relies on NLR's system advisory model (SAM) to compare the EY for similar nameplate size deployments of CdTe and Si modules using data from locations with different climates: Phoenix, AZ, USA (hot and dry climate); Frankfurt, Germany (temperate climate); and Kuala Lumpur, Malaysia (hot and humid climate). The results of these modeled behaviors of modern systems are consistent with the published data of systems from roughly a decade ago. Beyond allowing more modern comparisons, modeling also allows one to deconvolute some of the contributions to the overall EY.[7,8] SAM leverages weather and system data to model PV systems containing a string of Si and CdTe modules in series to evaluate the EY of a system. It is an effective tool for assessing the location-specific effects of weather, such as ambient temperature and wind speed, on module performance.

However, SAM does not adequately capture location-specific effects on module current. In calculating current, SAM leverages an empirical spectral mismatch correction based on a fourth-order polynomial with coefficients that were extracted from measurements performed on a set of crystalline silicon modules.[16,17] Note that this does not account for changes to the spectral shape due to local atmosphere variations. A second set of models leveraging plane-of-array (PoA) irradiance generated by the FARMS-NIT algorithm implemented in the National Solar Resource Database (NSRDB) allows for a spectral mismatch coefficient to be calculated for CdTe and Si panels individually, accounting for this spectral loss effect.[18] The mismatch coefficient calculated in this work leverages recorded Si and CdTe module spectral responses.[19,20]

To enable comparison of how well CdTe and Si modules perform in real-world conditions relative to their nameplate ratings, we defined comparative figures of merit (CFoMs) for both V_{OC} and J_{SC} in Equations 1 and 2, respectively.

$$V_{OC}\ CFoM = \frac{V_{OC,CdTe,field}}{V_{OC,CdTe,nameplate}} - \frac{V_{OC,Silicon,field}}{V_{OC,Silicon,nameplate}} \quad \text{(Equation 1)}$$

$$J_{SC}\ CFoM = \frac{J_{SC,CdTe,field}}{J_{SC,CdTe,nameplate}} - \frac{J_{SC,Silicon,field}}{J_{SC,Silicon,nameplate}} \quad \text{(Equation 2)}$$

The field data for the two technologies can be calculated using spectral and temperature data for various locations, while the nameplate parameters are measured at STC at the factories. In this formulation, a positive value for a CFoM indicates a relative advantage for the CdTe module in terms of performance normalized to its nameplate values, meaning that the CdTe module would be maintaining a higher percentage of its datasheet rating for that parameter. More details on the approach, SAM, and spectral mismatch calculations are available in the supplemental information (Notes S3 and S4). Note that monofacial modules are being considered in this comparison. The impact of bifaciality will be discussed later.

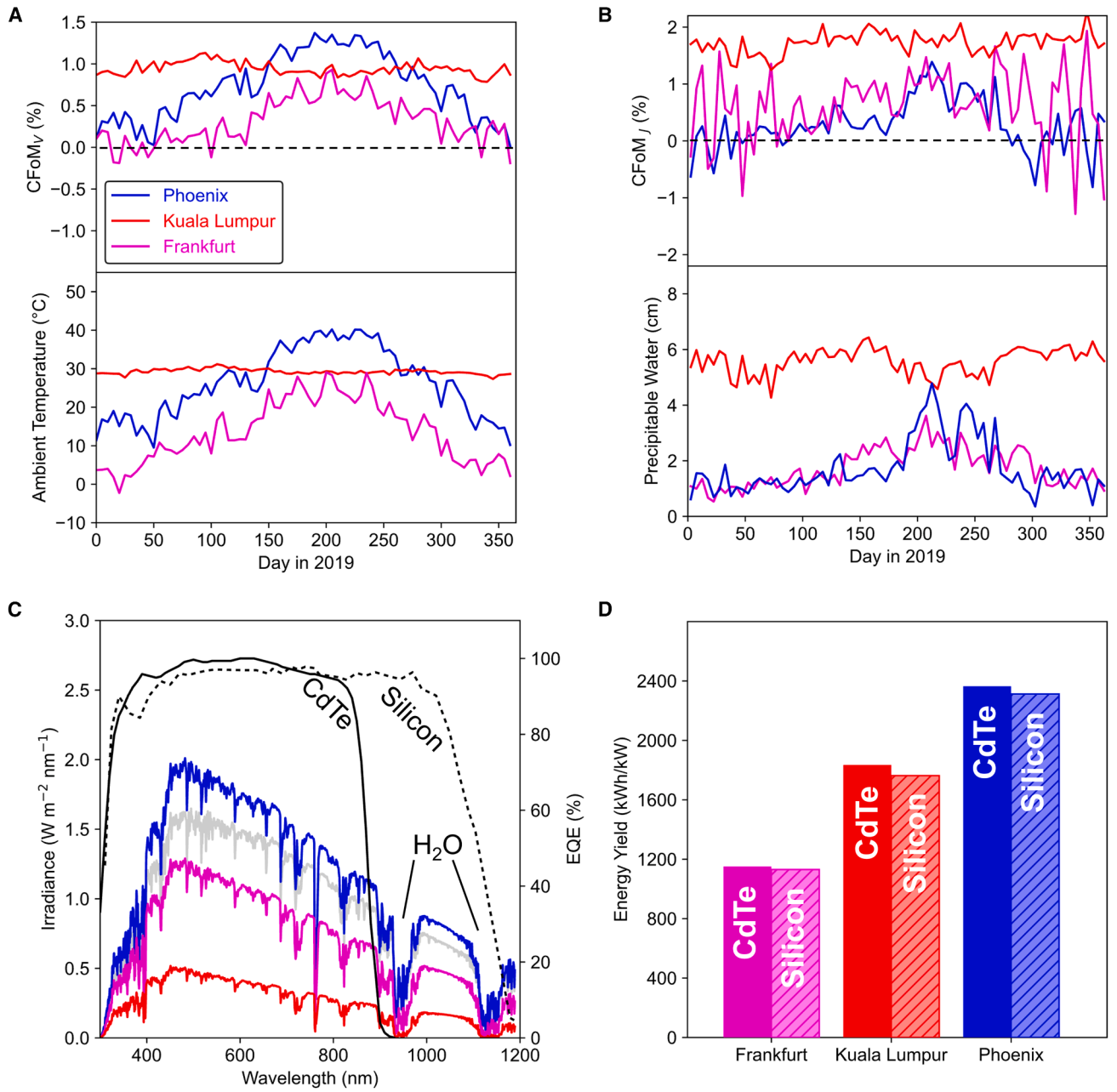

Figure 2. Comparison of factors impacting energy yields for CdTe and Silicon PV arrays in representative locations

(A) Upper: comparative figure of merit (CFoM) for V_{OC} (see text) plotted as a 5-day moving average for the year of 2019 using data from Phoenix, Frankfurt, and Kuala Lumpur. A positive value indicates a relative performance advantage for CdTe. Lower: 5-day moving average temperature for the locations. Note the strong correlation between temperature and the CFoM for V_{OC}, indicating a performance advantage for CdTe in hot climates.

(B) Upper: CFoM for J_{SC} (see text). Lower: atmospheric precipitable water content. Data in both panels are plotted for a 5-day moving average in 2019 at the three locations. Here, a strong correlation is noted between atmospheric precipitable water content, indicating a performance advantage for CdTe in humid climates.

(C) Irradiance spectra as calculated at the summer solstice in 2019 in the three locations. The EQE of the record CdTe and Si modules is also shown. Absorption by water is seen to occur at wavelengths below the CdTe band gap.

(D) Energy yield for a new PV system (i.e., with no module degradation) in each of the three locations. The representative CdTe system has a higher EY than that of the Si system.

Figure 2A shows that CdTe modules have a comparatively higher *Voc* year-round in Kuala Lumpur and during the summers in Frankfurt and Phoenix. During the colder months, however, the CFoM for V_{OC} approaches zero, showing no advantage for either technology. Figure 2B shows that the effects of the atmosphere on the incident spectrum, as modeled by the FARMS-NIT

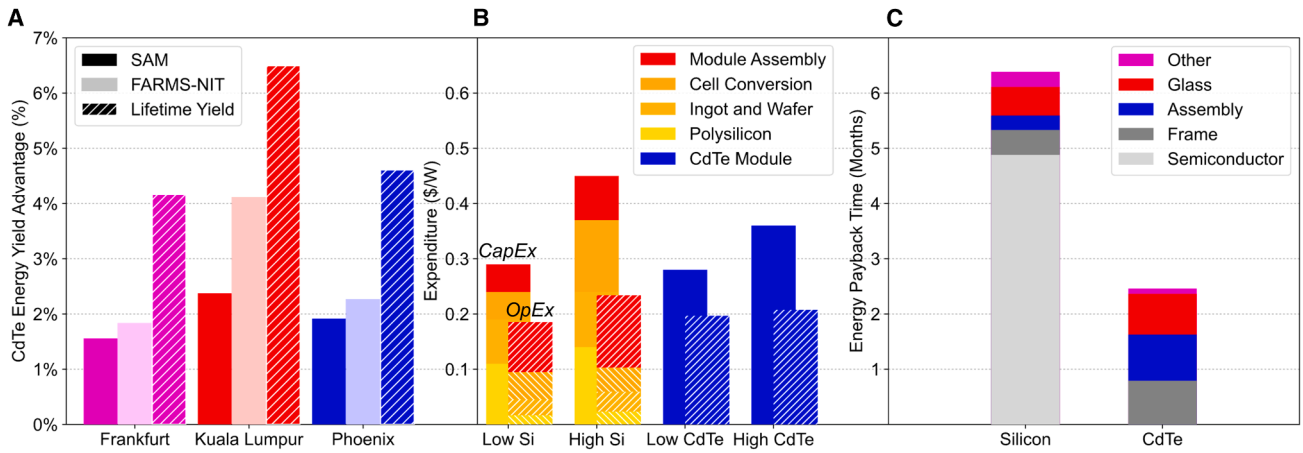

Figure 3. Comparison of CdTe and Silicon PV energy yield, expenditure, and energy payback time

(A) EY advantage for CdTe PV systems in three representative locations. First bar is 1-year advantage from SAM. Second bar is 1-year advantage from SAM modified with FARMS-NIT spectral calculations. Third bar shows 30-year advanage with SAM + FARMS-NIT. EY advantage is defined as EY_{CdTe}-EY_{Si}/EY_{Si}. Lifetime CdTe EY is higher by 4.2%, 6.5%, and 4.6% in Frankfurt, Kuala Lumpur, and Phoenix, respectively. See text for details.

(B) CapEx and OpEx for CdTe and Si module production. Si production is split into four categories typically not collocated, while CdTe module fabrication from raw materials to module is completed in a single facility. Data adapted from Basore and Feldman.[5]

(C) Energy payback time for CdTe and silicon modules in months, broken down by category. Data reproduced with permission from Wikoff et al.[21] Notably, state-of-the-art CdTe modules have transitioned to a frameless design since this 2022 analysis.

algorithm, affect the CFoM for J_{SC}. In conditions with a higher precipitable water content (e.g., Kuala Lumpur), CdTe modules are expected to have a relative boost in J_{SC} as compared with Si modules. Notably, the difference in J_{SC} does not correspond with cloud coverage, which causes scattering events that depress irradiance in both the long- and short-wavelength regions roughly equally, but is instead due to the water content in the ambient, which will preferentially absorb light in the infrared. Figure 2C shows example spectra generated from the NSRDB for each location and the external quantum efficiency (EQE) curves of record CdTe and silicon modules. Here, it can be seen that absorptions due to water vapor are above the band-gap energy of Si and below that of CdTe. These simulations suggest that CdTe modules perform at a slightly higher efficiency than equivalently rated silicon modules in hot and humid climates.

Figure 2D compares the total annual EYs for the year 2019. The representative CdTe system has an EY that is higher than the Si system in each of the locations (*vide infra*). The impact is largest in Kuala Lumpur, which is both hot and humid. The SAMS + FARMS-NIT approach allows considerations of the relative spectral losses and shows that the EY for a particularly humid climate (Kuala Lumpur) is higher than that predicted by SAM alone by about 1.6%.

While to this point our EY modeling has assumed zero degradation, the bankability of PV module systems relies on long-term EY predictions. CdTe modules hold the lowest warranted annual degradation rate of any leading PV technology (−0.3%/year), lower than PERC Si modules (−0.45%/year), TOPCON modules (−0.4%/year), and SHJ modules (−0.35%/year). Accounting for module degradation over a 30-year lifetime, the modeled CdTe PV system EY advantage is extended by 2.5% compared with a similarly sized monofacial PERC silicon system (Figure 3A). A low temperature coefficient, improved spectral response in the presence of atmospheric moisture, and reduced module degradation rate enable CdTe modules to outperform similarly sized Si deployments in all of the climates modeled here.

A detailed comparison of the EY for bifacial CdTe versus Si modules is beyond the scope of this effort, as the performance of bifacial modules is highly system dependent. Inclusion of bifaciality in SAM could perturb the EY results by as much as 4%–11%, according to previous SAM studies comparing monofacial and bifacial silicon modules, with the impact scaling with the degree of bifacality.[22,23] While Si products have been produced with bifaciality of ∼80%–90%, the first bifacial CdTe modules have a bifaciality of 15%. The market for bifacial modules has expanded and is expected to represent 90% of the PV market by 2030.[24] For CdTe to remain competitive, it will be necessary to achieve both higher module *PCE* and bifaciality. The "research goals" section below describes work that will help to meet these challenges.

Previous studies have shown that CdTe modules also have a smaller embodied carbon and energy footprint compared with Si, driven by the difference in techniques by which the semiconductor absorber is processed.[21] Wikoff et al. used data from the First Solar series 6 module and found that CdTe modules have an energy payback time approximately 1/3 that of Si modules (Figure 3C). Notably, the series 6 modules used an aluminum frame, which accounted for about 30% of the embodied energy. Series 7 modules do not use a frame but instead use steel struts, which results in a lower embodied energy. Several studies show that the CapEx for CdTe production per GW_{DC} is comparable to that of TOPCON and lower than that for next-generation heterojunction solar cells (Figure 3B), while OpEx are roughly equal.[5,25] Location-dependent EY, energy payback time, and CapEx make

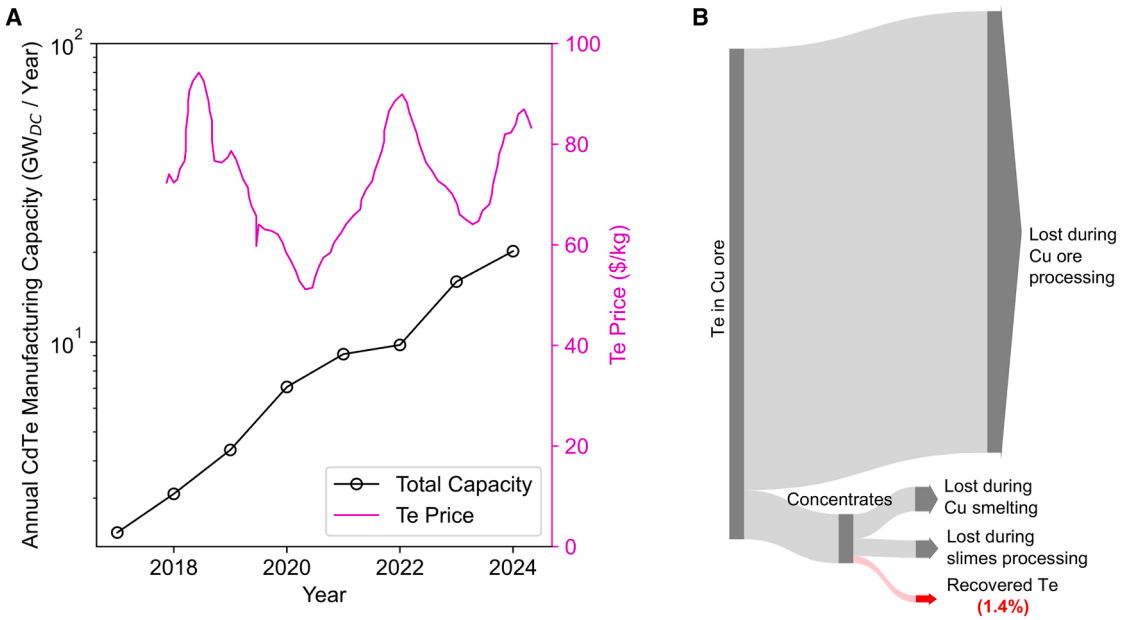

Figure 4. CdTe manufacturing capacity expansion and Te price and Te sourcing from the Cu refining process

(A) Annual global CdTe manufacturing production rate capacity from 2017 to 2024 (black) and the New York tellurium price per kilogram. Over the long term, Te price has fluctuated around $80/kg on average, while manufacturing capacity, which is plotted on a log scale, has increased by an order of magnitude, suggesting that Te availability has not historically been a limiting factor in the industry.

(B) Sankey diagram indicating the flows of Te at different processing steps during the Cu production process that starts with mining and ends with the electrolytic refining of Cu. A significant portion of mined Te is lost during the mineral processing of copper ore before smelting and refining. Adapted from Nassar et al. under creative commons CC-BY license.[29]

it likely that CdTe will reach multi-TW scale as PV deployment continues to scale.

TE SUPPLY PATHWAYS FOR SCALING TO 100 GW$_{DC}$/YEAR

Past projections for the growth of CdTe PV placed ceilings on the ultimate production capacity based on reported Te availability. DOE's report titled *Solar Photovoltaics: Supply Chain Deep Dive Assessment* estimated that the size of the global CdTe PV market would be capped at 20 GW$_{DC}$/year, suggesting that CdTe PV would only be a niche technology in the long term.[5] However, global production is already at that level and First Solar's currently announced capacity expansions for 2026 exceed the 20 GW$_{DC}$ cap by 25%. There are also other emerging players in CdTe (including Advanced Solar Power and CTF/CNMB Solar), which may also contribute at the GW scale. Evidence for tellurium supplies not currently being a limiting factor is suggested by the market price for Te, which has not been correlated with the expansion of CdTe PV manufacturing capacity. Figure 4A shows the price of tellurium on the open market over the same time period as the expansion in nameplate manufacturing capacity, and increasing Te prices would be expected if demand was outstripping supply. The long-term availability of Te is important to consider; however, since only tellurium availability and cost have the potential to truly limit the growth of CdTe PV.[26] Growth in other parts of the supply chain (e.g., glass, wire, inverters, fuses, polymers, framing, junction boxes, tracking, etc.) will also be important, but these components have no fundamental limits, and their availability is expected to grow in response to the growth of the overall PVs industry.[27] Cd, for example, is readily available as a byproduct of the Zn mining industry and will not limit production capacity. Module manufacturing capacity can ramp up quickly when conditions warrant expansion, with turnkey factories being deployed by First Solar and CTF within one year from greenfield to production-ready.[28]

It is estimated that 90%–95% of today's Te supply is a byproduct of Cu mining and refining processes,[29,30] and there are also several other Te sources that could be tapped at a larger scale in the future (i.e., Ag, Au, and Pb byproducts). Nassar et al. examined Te recovery from Cu refining in 2022 and concluded that only about 10% of the Te content in the mined Cu ore is conveyed into the "concentrates" and entrained in the electrolytic-refining process (Figure 4B).[29] The vast majority of the Te is lost to tailings. Another lossy step was the electrolytic-refining stage, where only 29% of the available Cu anode slimes were being sent to Te recovery lines. Recent developments suggest that improving the refining capacity of Te from this stream is possible. Through a collaboration between Rio Tinto and 5N Plus, a 2.9M USD Te recovery line was added to the existing copper refinery at the Kennecott Cu mine to extract 20 metric tons (mT) of Te in 2022.[31] By subsuming Te-refining costs in the CapEx for CdTe PV production, this represents a very small increment to the cost of manufacturing (~0.001 USD/W$_{DC}$). The Kennecott example demonstrates that the CapEx to secure Te availability

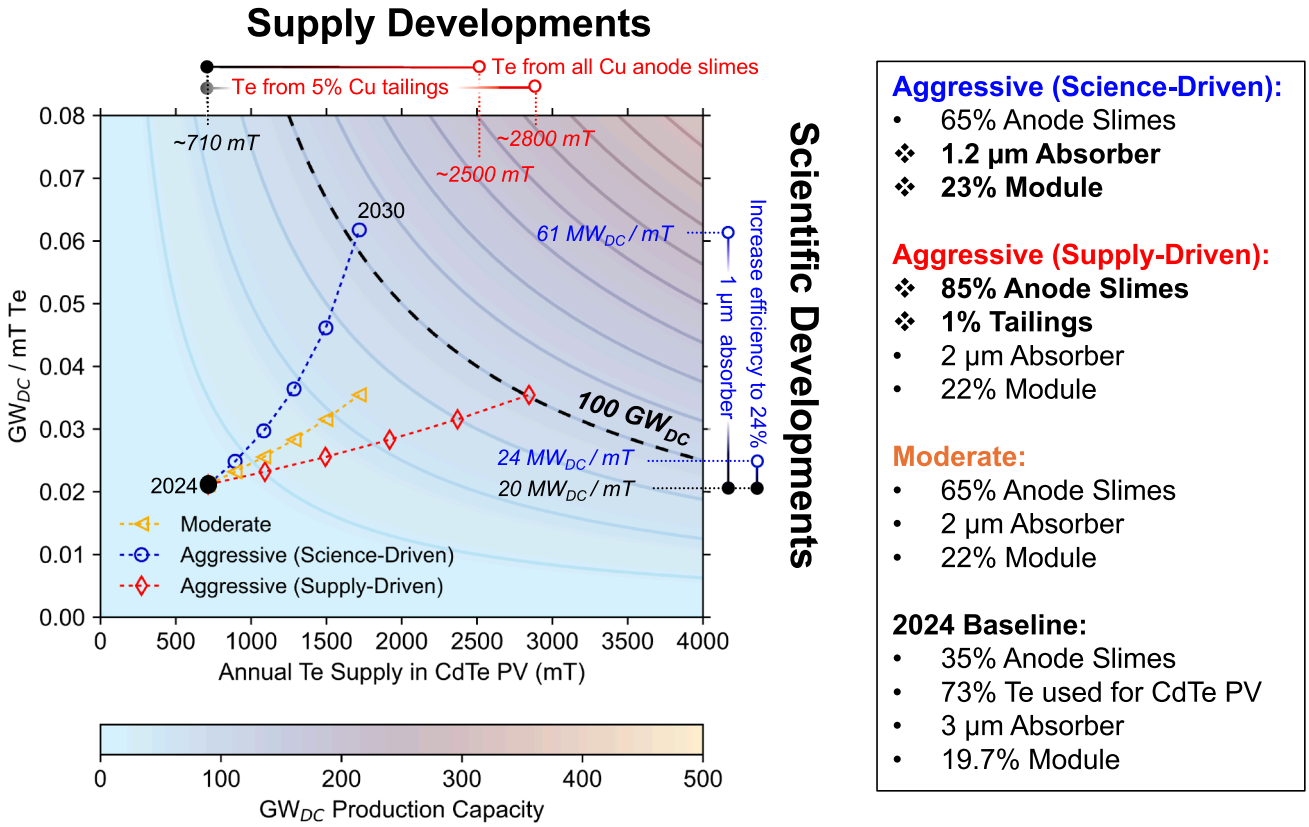

Figure 5. Potential growth scenarios for CdTe PV manufacturing capacity based on assumptions regarding Te supply expansion and the efficiency of turning refined Te into GW_{DC} of modules

Open circles represent years from 2025 to 2030. Assumptions for 2030 supply chain and module milestones for each scenario ("2024 baseline," "moderate," "aggressive science," and "aggressive supply") are described in the right-side panel. Potential Te resources available in anode slimes and tailings from 2024 Cu refining are shown above the chart. Modifications to GW_{DC} per metric ton (mT) of Te, assuming particular module developments are shown to the right of the chart. Contour lines are in 25 GW_{DC} increments.

is orders of magnitude below the CapEx required for the remainder of CdTe PV production. Alternative refining streams to Cu, primarily Au mines, have also been demonstrated, such as at the Kankburg Åkulla Ostra Au mine, which produced 37 mT of metallurgical-grade Te in 2023.[32] Te is also recovered during lead refining and from flue dusts generated during smelting of bismuth and lead-zinc ores.[33] Primary Te resources (such as the Klondike Te property in CO, USA, or the Dashuigou Te deposit on the Tibetan plateau) may provide a significant source of Te in the future.[34,35]

The United States Geological Survey (USGS) estimated that the annual global production of Te in 2024 was 980 mT/year, with 60% of the supply used in CdTe PV and 40% used for other technologies. Assuming a 19% module and a 3 µm absorber of pure CdTe (no selenium alloying), 49 mT Te is presently needed per GW_{DC} of CdTe PV. At these rates, a CdTe PV production capacity of 12 GW_{DC} would be supported based on this 2024 estimate. It is interesting to note, however, that the actual amount of CdTe PV manufactured in 2024 was considerably greater than that amount at ~15.1 GW_{DC} (Figure 5). The USGS estimate can be considered as an approximate, lagging indicator of Te availability. This is not surprising considering that CdTe PV companies and Te suppliers are, understandably, not open to discussing sensitive business information. The discrepancy in the 2024 Te supply data might also be attributed to the Cu market being much larger than reported or the percentage of Te diverted to CdTe production being larger than 60% of the total Te supply. It is also possible that improvements in extraction of Te through the copper supply chain are already being made, or that Te is now being obtained in significant proportion from other sources, such as from Cu tailings or from Au- or Ag-refining streams. All of these markets are opaque, with Te refining from Cu occurring primarily in China. Solid data on the details of extraction and refining occurring in remote locations is lacking, and the productivity of the mines depends on the specifics of the mineralogy and the processing, which can vary strongly from mine to mine. At the market level, however, the available data indicate that the Te supply is growing and not currently limiting the rapid expansion of CdTe PV production.

Figure 5 demonstrates four potential growth scenarios for CdTe nameplate capacity, which consider additional Te only from the Cu supply chain. The two axes show dimensions by which CdTe production capacity may be improved. The

horizontal axis represents annual Te supply in mT (metric tons, i.e., 1,000 kg), and the vertical axis plots the GW_{DC} of CdTe panels that can be produced from a mT of Te. The two axes offer different ways to increase CdTe production capacity, with CdTe device research and development impacting the vertical axis. The baseline case for 2024 assumes a 3 μm absorber of pure CdTe, a 19% module, and that 35% of Te-bearing Cu anode slimes are being refined for Te. The baseline case for Te supply is adjusted by assuming that the percentage of Te that is diverted to CdTe production is slightly higher at 73%, harmonizing the actual production rate in 2024 (15.1 GW_{DC}) to the value estimated from USGS's report at 60% (12.0 GW_{DC}). The "moderate" scenario assumes that modules will reach 22% efficiency, be thinned to 2 μm, and that ultimately 65% of Cu anode slimes will be refined for Te. In this scenario, CdTe manufacturing capacity will reach ~60 GW_{DC}. The combination of moderate module improvements and typical refining practices on a larger percentage of Cu anode slimes enables an annual production capacity of 60 GW_{DC} by 2030. An "aggressive (science-driven)" scenario assumes significant scientific and manufacturing development, allowing module efficiencies to reach 23% *PCE* at 1.2 μm thickness, the minimum thickness to optically absorb 99.9% of incoming solar radiation on a single pass.[36] Te supply values are attainable and equivalent to those presented in the moderate scenario, corresponding to improved collection of anode slimes. Alternatively, the "aggressive (supply-driven)" scenario considers only moderate panel improvements and aggressive Te supply chain development by extracting just 1% of Te in Cu tailings and 85% of Te in Cu anode slimes. Assuming a linear increase from the baseline values, the 100 GW_{DC} threshold would be crossed in early 2030 for either "aggressive" scenario. These scenarios illustrate that it will be necessary to develop several module technologies and the Te market improvements in parallel to reach a goal of 100 GW_{DC} per year, but that there are several viable pathways to that target.

Challenges

Historically, there have not been strong incentives for Cu refineries to improve global Te-refining capacity. Additionally, the metallurgical Cu supply chain from which Te-bearing anode slimes are produced is heavily concentrated in China. The Te price (USD/kg) has fluctuated around 80 USD from 2018 to 2024, corresponding to about 3 USD/kW_{DC} for contemporary 3 μm absorbers. Refined copper cathode may not have a Te concentration higher than 2 ppm under the ASTM B115-00 Copper Specification. To achieve this specification, operational care is given during the refining process to ensure Te reports to the anode slimes. During the processing of slimes, the most valuable metals (gold and silver) are the primary focus.[37] Tellurium is recovered to ensure that it does not interfere with the production of these commodities or return to the refining process. During copper concentrate production, tellurium is lost due to the depression of iron sulfides during flotation.[38,39] The identification and extraction of Te-rich ore with Te as a sole primary mineral resource has historically not been economic, although several particularly Te-rich sites have been identified. Effective mining and extraction of Te-rich ore has been made possible by mining with other metals such as Au.

Research goals

The supply chain for Te will need to be expanded to accommodate a larger manufacturing capacity. Estimates indicate that ample Te resources are available in waste streams from Cu refining. Thus, the most critical developments in the supply chain would target the following.

(1) Improve the recovery of tellurium from copper anode slimes.
(2) Develop a process to utilize pyrite to encourage its recovery during copper mineral processing and capture Te presently lost to copper tailings.
(3) Examine resource potentials for deposits that contain Te enrichments with other metals than copper (e.g., Au, Pb, and primary Te).

In copper anode slime processing, tellurium is lost because of the intentional operation focus on more profitable slime constituents like silver and gold. Tellurium remains in slimes after leaching to minimize silver losses. Recovery from pyrometallurgical slags produced in many operations is challenging and unprofitable. The deportment of tellurium in process residues and slags has not been studied adequately. Greater understanding of the phases containing tellurium would assist in developing recovery processes. Increasing the tellurium recovery during decopperization or processing slags/residues could increase tellurium by a factor of two without significant capital investment as compared with opening a new mine.

In both Cu ore tailings and in ore from Au-Te-Ag hydrothermal deposits, Te is predominantly found as inclusions in low-value pyrite (FeS) grains. The extraction of Te from pyrite is complicated by its low concentration and the small size of the Te inclusions (10s of μm), although weight percent can reach as high as 1.5% in some As-bearing pyrite.[38] Even in deposits where Te is recovered as a primary mineral (i.e., Kankberg, SE; Dashiguou, CN), processing of pyrite grains is uncommon, as recovery of the Te inclusions would require additional grinding and targeted recovery technology for successful Te extraction. Pyrite is largely only refined for the production of sulfuric acid, rather than for its metallic content, limiting economic interest in recovery. Researchers have found that the incentives to process pyrite in Cu tailings to refine Te may be improved by co-extraction with precious metals such as Au and Ag, and that 77% of Te was recovered during gravity separation and froth flotation.[39] Identifying means to obtain value from pyrite could unlock the economic viability of Te recovery from copper tailings.

Assisting Cu producers to create more value by increasing Te production will ensure adequate Te supply for a scaling CdTe PV industry. The increased attention that other critical minerals are receiving may also help to increase Te supply further.

KEY DEVICE RESEARCH AREAS

While First Solar reports a 64 GW backlog for module delivery through 2030 at current module efficiencies,[40] there is substantial headroom for improvements to cell voltage and efficiency that would further increase market demand for the technology. The certified record CdTe cell, produced by manufacturer First

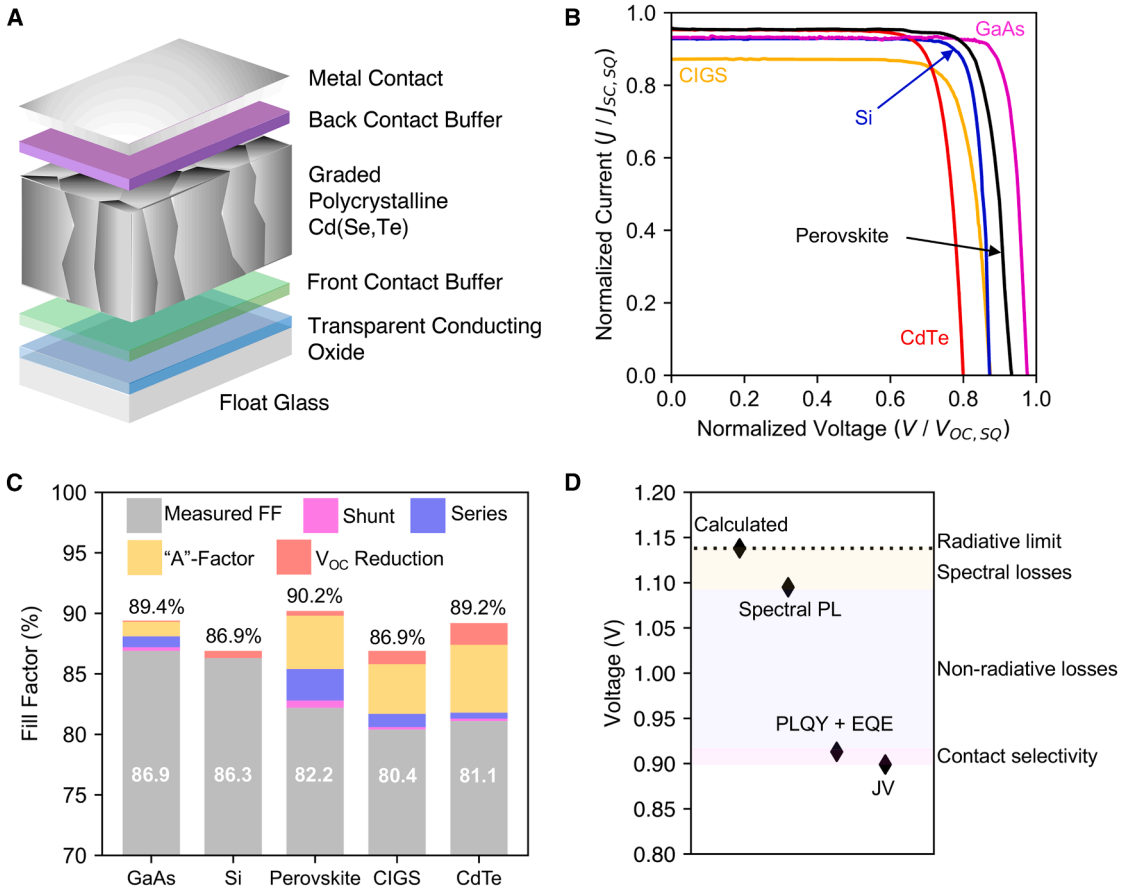

Figure 6. Identifying performance losses in contemporary Cd(Se,Te) devices

(A) Material stack in high-efficiency Cd(Se,Te) PV devices.

(B) Comparison of the highest-efficiency *JV* curves adjusted for band gap for five technologies.

(C) *FF* losses for each technology extracted from the *JV* curve: ideal values are at the top, and those achieved are in white.

(D) Breakdown of V_{OC} losses via PL, EQE, and *JV* measurements in 22.3% Cd(Se,Te) device.

Solar, now stands at 23.1% with a Gr-V-doping technology and a Cd(Se,Te) alloyed absorber[12] (Figure 2B). Notably, the open-circuit voltage of the record cell is now above 900 mV. While short-circuit current (J_{SC}) is within 5% of the theoretical limit, *FF* and open-circuit voltage (V_{OC}) have larger deficits that present significant headroom to improve the overall efficiency of CdTe cells and modules. The V_{OC} of the record CdTe module is 905 mV, 18% below the 1,103 mV V_{OC} theoretically achievable for a 1.38 eV band-gap absorber.[41] The 80.6% *FF* of the record cell lags the theoretical 89.2% maximum value. In comparison, epitaxial-grown GaAs and metal-halide perovskite thin-film devices (*vide infra*) have shown a voltage deficit of only 1% relative to the radiative limit.[42] If CdTe were to reach similar values of entitlement, the V_{OC} would be 1,092 mV. Improvements in J_{SC} have been driven by remarkable engineering, but the V_{OC} and *FF* deficits are more difficult to solve due to scientific knowledge gaps and the complexity of the device.

The history of CdTe PV up to 2024 can be viewed through the lens of a series of critical innovations that have enabled higher *PCE*s to be reached. The first generation of devices used an n-type CdS window layer in contact with Cu-doped p-type CdTe. Innovations at the rear contact improved cell efficiencies by introducing a ZnTe buffer layer. The CdS window layer was eventually replaced with a graded Cd(Se,Te) layer, with Se incorporation significantly improving carrier lifetime in cells. More recently, a shift to Gr-V doping (i.e., N, P, As, Sb, and Bi) has necessitated the development of new dopant activation processes but has offered new pathways to high-performing devices with stability even better than previous-generation Cu-doped devices (Figure 6A). Scarpulla et al. cover the history of CdTe development in-depth.[43]

The remaining key physics, materials science, and chemistry questions revolve around challenges relating to doping control, front and back-contact interface passivation, reduced electronic disorder, increased diffusion length, new alloys, and the construction of both front and back-surface fields, challenges which are complicated by the fact that commercial production methods yield polycrystalline materials. Concerted advances in all these areas will enable the development of a laterally uniform device structure that can produce a large separation of the electron and hole Fermi levels at the front and back contacts, in which recombination is governed only by the bulk recombination

limit of an absorber with a large non-radiative recombination lifetime (τ_{SRH}). Overall, the near-term research needed to pursue the voltage and tellurium utilization goals set out in this roadmap can be grouped into six areas, as described below.

Quantifying and attributing losses in devices

Challenges

Although the community's knowledge base has advanced tremendously over the past decade, there is still considerable debate over exactly where losses occur in the device. The answer to this relatively simple question is complicated by the fact that state-of-the-art CdTe devices are very thin and polycrystalline and may have lateral inhomogeneities.[44–47] In addition, many species that comprise the device are mobile, and their distribution is affected as processing proceeds through manufacturing.[48,49] Moreover, in certain configurations, light- and heat-induced metastabilities must be addressed during evaluation.[50]

To put the CdTe record-efficiency cell in context with other technologies, it is useful to overlay the current-voltage (*JV*) curves and examine their differences. Figure 6B does this for the five most promising commercial technologies.[42] Since each absorber has a different band gap and associated metrics, the *JV* curves here are normalized to their radiative limit values. Two features stand out for the CdTe curve: the current achieved for its band gap compares very favorably with the other technologies, but the normalized voltage is clearly the lowest. Less obvious in Figure 6B, the *FF*s of the two single-crystal technologies are quite close to their ideal, whereas those for the three thin-film polycrystalline technologies show significantly higher losses. These losses can be broken down and quantified as shown in Figure 6C. Of note, the large difference in *FF* loss between the single-crystal and thin-film cells is primarily in the diode quality factor ("A"-factor) related to recombination, corresponding to multiple recombination mechanisms "turning on" over the voltage range near the maximum power point.[51] The most obvious difference between single and polycrystalline devices is the presence of grain boundaries, making these an immediate suspect. In addition to grain boundary recombination, low intergrain mobility may also be a contributing factor.[52] Single-crystal systems have also historically had extremely high-quality interfaces relative to most polycrystalline thin-film devices. Improvements in any of these areas should also improve voltage losses.

The metric of implied V_{OC} (iV_{OC}) obtained from external radiative efficiency (ERE) measurements is increasingly invoked to attribute V_{OC} loss mechanisms in CdTe. Spectrally corrected photoluminescence (PL) quantum yield (PLQY) and EQE measurements enable the calculation of different voltage metrics, including the ideal V_{OC} and implied V_{OC}.[53] Figure 4D shows the breakdown of voltage losses in the 22.3% record described in Mallick et al.[12] The ideal V_{OC} takes into account sub-band-gap states and the effective lowering of band gap (spectral losses in Figure 4D). The implied V_{OC} relates to the intensity of the PL emission ERE and related recombination that can modulate this (non-radiative losses in Figure 6D). The implied V_{OC} has been particularly helpful for absorber development in the presence of poor selectivity contacts, enabling parallel development of absorber and contact processes. For such an analysis to be valid, it is critical that sub-band-gap states are probed (as they can artificially inflate the integrated PL emission), necessitating the use of narrow band-gap PL detectors (i.e., InGaAs).

Buried in the *JV* metrics of V_{OC} and *FF* are several device- and material-level properties that are difficult to quantify. Accessing the electrical and optical parameters that control *JV* performance in a full device stack is not straightforward, often requiring several supplementary measurements and simplifying assumptions to extract useful information. For example, time-resolved PL (TRPL) contains information regarding carrier dynamics and recombination processes, but accessing individual lifetimes associated with certain recombination pathways (such as τ_{SRH}) is complicated by the convoluted presence of electric fields, near-band trap states, distributions of species, and interfaces.[54] Temperature-dependent *JV*, JV*(T)*, is frequently used to identify contact barriers or extrapolate dominant recombination processes, but parameter sets that fit data may not be unique. Some high-impact parameters, such as hole and electron mobility, have not been directly probed in $CdCl_2$-treated polycrystalline CdTe since the introduction of Se to the front interface. Recent work indicates that mobility values in polycrystalline thin films are much lower than values seen in single crystals and often used in models.[55]

It is often valuable to combine or compare measurements with numerical drift-diffusion models to evaluate difficult-to-access parameters. While SCAPS and other 1D modeling software have been used extensively and have provided significant value in the past, different approaches are being pursued throughout the community to capture the 2D and 3D aspects of dopant segregation, grain boundaries, and lateral optoelectronic non-uniformities. Dynamic models that incorporate the evolution of the system over time are particularly helpful for probing time-dependent measurements such as TRPL.

Research goals

Facile access to critical device and materials parameters will be essential to guide process development. Surface recombination velocity for the front and back surfaces, band offsets at the front and back surfaces, transversely varying band-gap and dopant/defect concentration, SRH lifetime, and mobility are of particular interest. Combining multidimensional measurements (i.e., JV*(T)*, frequency-dependent capacitance-voltage [*CV*], and fluence-dependent TRPL) with numerical modeling will be necessary to fully quantify these parameters. In analyzing the effects of processing changes, the measurements of critical parameters must be done with statistically significant device populations, ideally leveraging the design of experiments.

Modeling and simulation would need to include sensitivities to both transverse and lateral non-uniformities and would likely need to be done at multiple scales (the impacts of lateral non-uniformities are discussed in-depth in a later section). For example, the energetic distribution of defect states may be generated via density functional theory (DFT) and defect equilibria studies, then used as inputs for other, larger-scale models. Identifying and proliferating an up-to-date baseline model should be a goal of the community. Machine learning and materials discovery should be implemented to predict new research and development directions with a strong connection to

experimental results, ideally generated and collected using high-throughput approaches.

Optimizing a graded polycrystalline absorber

Challenges

Polycrystalline Cd(Se, Te) absorbers are quite complex, with transverse gradients of Se, dopants and associated defects, columnar (and sometimes lateral) grain boundaries, and segregated species in grain boundaries that impact critical device properties. Contemporary Cd(Se, Te) absorbers are generally deposited onto the transparent conductive oxide (TCO) by physical vapor deposition, with the most prevalent approach at scale being vapor transport deposition (VTD), enabling rapid polycrystalline absorber growth (on the order of μm/min). The resultant films leverage a graded Se alloy from the front interface to control band-gap and other optoelectronic properties, while Gr-V dopants are typically incorporated *in situ*.[56,57] Grain sizes in absorbers immediately following deposition are between 200 nm and 1 μm and are smaller in the graded region of the device. Films are annealed with $CdCl_2$ to form a (Cd, Te, Se, Cl) eutectic, which recrystallizes the film into larger (often columnar) grains, typically limited in size to the thickness of the absorber, with chlorine and Se segregated into grain boundaries.[48,58] The presence of O has been shown to further lower the eutectic point. Se diffuses into Se-poor regions of the device, particularly along grain boundaries, while dopant migration is limited. However, Gr-V dopant "pile-up" at the front interface of the device (~10–20 nm) has been observed even in state-of-the-art devices.[12,59] The resulting absorber is a complex system both for characterization and modeling, requiring careful analysis to extract useful process-property relationships.

Transverse variation of Se concentrations introduces fields at the front interface through band-gap grading, although defect chemistry from V_{Se} or Cl_{Te} has been attributed to strong n-type behavior in Se alloys, which may induce a second-order effect on fields in devices.[60] Evidence for a buried junction has been found in Cd(Se,Te) devices leveraging *ex situ* Cu doping, although such a junction has not been reported for Gr-V doped samples.[50,59,61] The high density of sub-band-gap states in commonly used (20%–40% Se) alloys also presents a potential challenge for devices, as sub-band-gap states may impede carrier mobility through capture-reemission events.[62]

Grain boundaries play an outsized role in the optoelectronic properties of CdTe. Under different processing conditions or dopant chemistries, grain boundaries have been found to be either n-type or p-type relative to grain interiors. Grain boundaries in as-deposited CdTe and Cd(Se,Te) have been found to introduce a high density of mid-gap defect states. Interstitial Cl (Cl_i) is highly mobile in grain boundaries and passivates these mid-gap defects, removing the defect states from the band-gap and enhancing efficiency.[63] Passivation of grain boundaries and interfaces by $CdCl_2$ species is a well-documented effect. However, the presence of Cl_i in grain interiors may be responsible for compensating complexes with other species, the effect of which remains to be elucidated.[15,64] Trap states or detrimental fields in grain boundaries may be responsible for limiting the mobility of free carriers in polycrystalline samples, as much smaller mobilities are required to fit drift-diffusion models of Gr-V doped devices (~2 cm^2/Vs) than have been measured in Gr-V doped single crystals.[65] In polycrystalline Gr-V doped samples, an order of magnitude lower mobility has been recently observed.[55] Typically, grain boundaries are columnar, spanning the absorber thickness from the TCO to the back contact, but the presence of horizontal grain or twinning boundaries may be responsible for large grain-to-grain variations, which ultimately impact device performance.

Crystallographic strain induced in the absorber is frequently overlooked in academic literature but is a scientific frontier ripe for improvements in CdTe. Due to the high temperatures reached in CdTe thin-film processing, strain is difficult to avoid in the absorber layers, which are deposited and annealed at high temperatures. Polycrystallinity can help relax strain, but that process may create additional defects. Quantification of strain fields is possible using X-ray diffraction techniques as well as at a more microscopic level through kernel average misorientation (KAM) measurements derived from electron backscatter diffraction (EBSD).[66] The coefficient of thermal expansion for CdTe is ~4.9 ppm/°C, which is lower than that of the soda-lime glass upon which the absorber is typically coated (8–10 ppm/°C), resulting in an absorber that is under compressive strain (desirable for electronic materials). Although $CdCl_2$ anneals tend to relax the overall stress in films, going too high in temperature while attempting to improve Gr-V dopant activation can result in a weakening of the front interface and delamination due to the accumulation of $CdCl_2$, which is a 2D material. Due to grain boundaries being a natural location to relieve the strain between grains, there is a propensity to concentrate strain-induced defects at the boundaries.

Research goals

Understanding the transversely varying chemical environments in polycrystalline Cd(Se,Te) absorbers is critical to enabling high-efficiency cells. Efforts to quantify cross-sectional properties in state-of-the-art devices by various microscopies, such as Kelvin probe force microscopy (KPFM), scanning spreading resistance microscopy (SSRM), and cathodoluminescence (CL), will help direct future process development.

Investigating single-crystal model systems can help to provide foundations for understanding of the more complex polycrystalline material. By generating and studying samples with large domains of controlled crystal structure, composition (e.g., Se/(Se+Te)), and defects (e.g., GR-V dopants), limitations related to the semiconductor bulk can be separated from the effects of grain boundaries and interfaces. Using these foundational systems can also enable more advanced analysis of polycrystalline material. Advanced SSRM is one example of this, where single crystals with known properties can be used to produce calibration curves to convert resistance to carrier concentration, thus enabling carrier concentration to be mapped on polycrystalline absorbers.[67]

Direct probing of mobility in single-crystal and polycrystalline samples (with known grain boundary densities and properties) as well as alloy compositions will elucidate challenges in bulk and grain-boundary-limited mobility, enabling higher efficiencies to be reached with the currently reported carrier lifetimes and concentrations. Direct and regular measurement of mobilities has been generally lacking in the community, and a

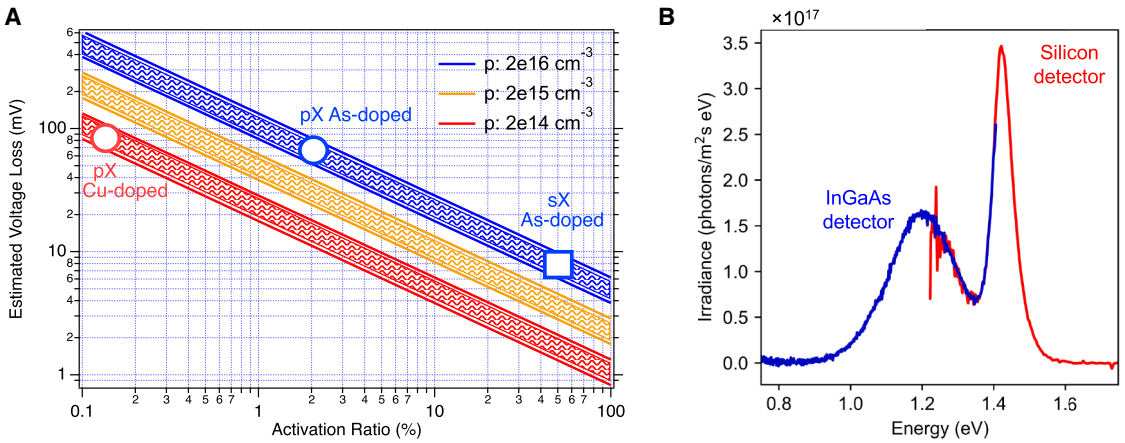

Figure 7. The impact of sub-bandgap defect states on Cd(Se,Te) device performance

(A) Estimated voltage loss vs. activation ratio.

(B) Spectral PL for Cd(Se,Te) doped with As. Direct band emission occurs at 1.4 eV, while sub-band-gap features at lower energy are visible. Quantification of sub-band-gap states exceeds the range of a Si detector (red), necessitating the use of a low-energy detector such as InGaAs (blue).

high-throughput procedure to understand the effects of composition and processing on mobility would be of significant benefit. Strain analysis at various stages in absorber preparation may also be critical in reducing defects in devices at higher temperatures. Synchrotron experiments such as X-ray absorption near edge spectroscopy (XANES) have been performed in a small number of samples and appear to be a useful way to probe the local electronic defects throughout the thickness of a device.[68,69]

Dopant activation and compensation

Challenges

While doping to high carrier concentration (10^{16} cm^{-3}) has been achieved with different Gr-V dopant species by a variety of *in situ* approaches, the degree of activation—the fraction of incorporated dopant atoms to the electrically active carriers—is still only on the order of a few percent in record cells.[70,71] Increasing the activation ratio and understanding the interplay between the competing factors that govern dopant incorporation, activation, and overall device behavior is a key area of research. As and P are the most fully developed of the Gr-V dopants, having both been used to achieve 23% efficient cells.[72] Gr-V dopants are ideally incorporated at the anion (tellurium/selenium) lattice position, where they act as shallow acceptors.[73] However, much remains to be known about how Gr-V dopants are incorporated and activated, how and when they migrate, the degree to which dopant clusters form at various processing stages, and the associated impact on the electronic landscape within the solid.

Figure 7A shows a distillation of the analysis by Moseley et al., in which the densities of randomly distributed As_{Te} acceptors fluctuate spatially and all inactive dopants are treated as compensating donors.[74] In this worst-case scenario, increasing the activation ratio of As from 2% to 20% at a net acceptor level of 2×10^{16} should allow V_{OC} to be increased by 40–65 mV.[74] As net acceptor densities increase, a cell becomes more sensitive to the activation ratio because inactive dopants are much closer to each other. If V_{OC} were to be increased by 50 mV in the most recent record cell while all other parameters are maintained, the cell efficiency would increase by over one percent absolute to 24.3%. Questions revolve around absorber deposition requirements for high activation, such as Cd-overpressure, growth rate, activation kinetics, temperature, and the process sensitivity to species such as chlorine, oxygen, and trace impurities. The system is further complicated in the presence of Se gradients, grain boundaries, and contact processing. While a remarkable amount of dopant atoms appear to oxidatively segregate to the front interface ("pile-up" levels are detectable at the atomic percent level by X-ray photoemission spectroscopy on samples cleaved at the oxide/absorber interface),[12,75] the chemical state, precise distribution, and role of the rest of the inactive dopants are still open questions.

The appearance of sub-band-gap states in spectral PL measurements is also affected by dopant species. Figure 7B shows an exemplar sub-band-gap emission peak, seen below the band-gap emission at 1.4 eV, typical of an arsenic-doped absorber. The intensity of this sub-band-gap emission is accentuated at lower temperatures, indicating a high density of near-band states that excited carriers may relax into from the conduction band minimum.[55] Although present in undoped Cd(Se,Te), these states appear to be sensitive to dopant species and incorporation.[60,62,76] In absorbers doped with Sb, the intensity of this sub-band-gap emission is increased, while the emission in P-doped absorbers is somewhat mitigated compared with undoped samples.[77–79] The nature of this sub-band-gap peak and the associated defects, complexes, or spatial fluctuations are yet to be fully elucidated.

Many of the processing steps in CdTe PV manufacturing introduce species suspected of compensating the dopant chemistry of CdTe. The effects of the Cl introduced during the ubiquitous $CdCl_2$ anneal have immense benefits through grain growth and boundary passivation,[49] but Cl_{Te} (and potentially Cl complexes) can lead to carrier compensation, which may appear as band tails.[60,80,81] Oxygen, a persistent impurity potentially introduced

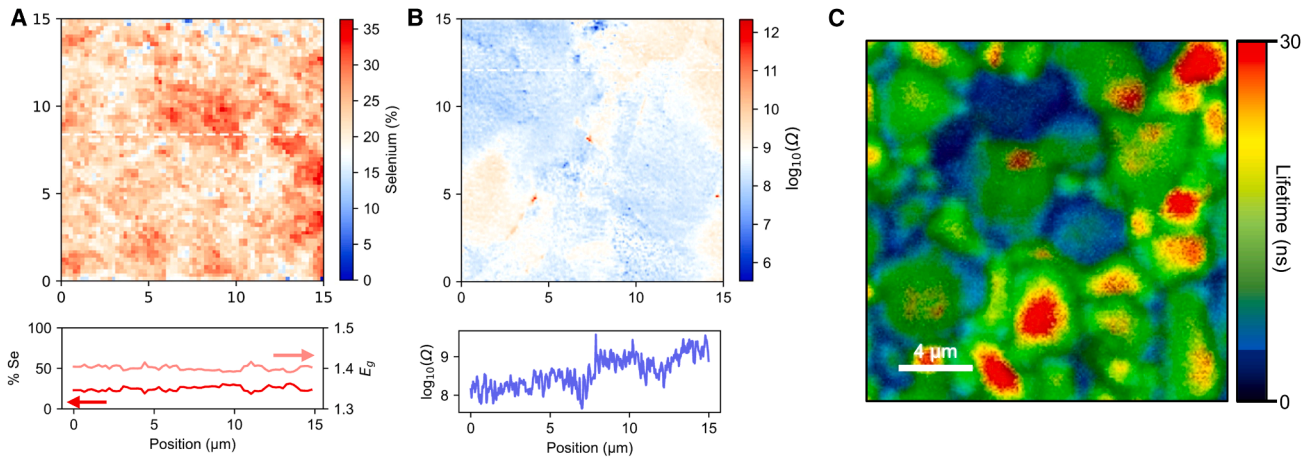

Figure 8. Examination of lateral non-uniformities in Cd(Se,Te) devices

(A) Se distribution at the cleaved front interface.

(B) Scanning-spreading resistance microscopy shows variations in carrier concentration between grains.

(C) Spatially and time-resolved PL shows that carrier lifetime varies between the grain boundaries and interiors and between grains. Some grains show a particularly low lifetime.

during absorber growth or from contacts, may also form detrimental complexes.[82,83] Although the recent record cell had bulk oxygen levels ~5× below the Gr-V dopant concentration, oxygen concentrations were significantly elevated at the front and back interfaces. Recent DFT studies have also highlighted the potential of highly mobile Cd_i to form a compensating donor complex with As_{Te}.[84,85] Some thermodynamically unstable compensating complexes involving arsenic interstitials may be kinetically stabilized to not only compensate the chemistry but also introduce deep defects that accelerate SRH recombination.[86]

Research goals

Measurement of activation ratios is typically a destructive process, requiring either sputtering to achieve depth profiles via dynamic secondary ion mass spectrometry (DSIMS) or digestion of films to access the low Gr-V dopant concentration via inductively coupled plasma mass spectrometry (ICP-MS). Techniques enabling cross-sectional characterization of arsenic concentrations would be valuable for deriving activation ratios. Robust kinetic and DFT models should be developed to characterize complexes formed by Cl, O, Cd, Te, Se, and Gr-V dopants. These models should be supported by experiments that identify which specific defects are present in devices (and where), their concentrations, energy levels, and spectroscopic signatures. Again, such work might leverage model systems (e.g., single crystals), generating a more limited number of defect types that might be measured with techniques such as PL, deep-level transient spectroscopy (DLTS), and XANES. Efforts to improve Gr-V incorporation control (very low levels are required, but Gr-V dopants have low vapor pressure relative to the Cd(Se,Te) matrix) and activation ratios will need to be understood and communicated to the broader CdTe community. *Ex situ* doping with Gr-V dopants such as Bi has demonstrated remarkable device performance while stubbornly having low carrier concentration.[87] This suggests that Gr-V dopants may be able to improve devices through more than one mechanism, which should be understood.

Measurement and effect of lateral non-uniformities

Challenges

The polycrystalline nature of the various layers used in the CdTe device architecture, coupled with the many species introduced during processing (e.g., Cl, Se, dopants, organics, and various inorganic contacting materials), can lead to locally varying chemical and electric potentials.[45] Species participate in many different bonding environments, terminations, defects, and defect complexes, resulting in substantial through-film and lateral non-uniformities. Some heterogeneities introduced by design, such as Se-concentration gradients, may impact local non-uniformities as well.

Macroscopic characterizations such as *JV*, *CV*, EQE, ERE, spectral PL, and TRPL are all examples where standard setups average over many grains or the entire device, such that the specific source of inhomogeneity cannot be distinguished.[88] Spectral PL and EQE show bandtails (sub-band-gap features), which indicate an effective change in the band gap that lowers voltage that is often described by the Urbach energy, E_u.[89] This might result from several mechanisms, including low activation and defects/defect complexes associated with anion vacancies or Cl-compensation (discussed above), inhomogeneous activation, and spatial variations in Se composition leading to band-gap variations. The heterogeneity in the optoelectronic properties related to non-uniform doping and, presumably, non-uniform activation can be readily seen in actual polycrystalline samples. Variations in Se concentration as visualized by auger emission microscopy (AEM) correlate to band-gap variations (Figure 8A). Se concentration varies from grain to grain at the front interface. SSRM indicates that local carrier concentrations can vary by *orders of magnitude* from grain to grain (Figure 8B), which at times correlates to Se concentrations from AEM. Macroscopic indications of recombination, such as ERE and TRPL, may also be influenced by non-uniformity, such as variations in passivation, impurities and recombination centers, grain boundaries, and interface variations. Figure 8C shows the spatial variation in the

TRPL signals, with some regions showing very short lifetimes while lifetimes in other regions are fairly long. The degree of non-uniformity is striking, with grain boundaries and some full grains appearing "dark."

Device simulations that compare a spatially mixed lateral carrier concentration varying from 10^{14} to 10^{17} cm^{-3} versus a constant 10^{16} cm^{-3} value indicate that a 2% absolute boost in efficiency (up to >24%) might be obtained if 2D heterogeneity were removed and the optoelectronic properties could be fixed at the preferred values. This effect is illustrated by a conducting plane (i.e., a metal contact) laid down over a variety of grains with different surface and bulk optoelectronic properties, and the high photovoltage from grains with preferred characteristics will be reduced by the grains with poor characteristics. Counterproductive band offsets (i.e., a back contact barrier) can exacerbate the detrimental effects of lateral inhomogeneities by further biasing photovoltage characteristics toward those of grains with poor performance.[46]

Research goals

To develop a detailed physical understanding of materials or interfaces, researchers need information on local-scale environments that may control macroscopic properties. This includes nanometer-scale depth profiles with high composition resolution for both intentional and unintended impurities, atomic-resolution microscopy to document the nature and distribution of crystalline defects and local compositional variations (especially near grain boundaries and interfaces), and luminescence measurements with high spatial resolutions. Samples may be imaged in cross-section by fabricating bevels via focused ion beam or by thermal cleaving at specific interfaces but should remain as close to full-stack devices as possible and minimize sample damage from the method used to expose the analysis surface. 2D and quasi-3D models will likely be required to understand the sensitivity of different effects, and detailed models will also be helpful in interpreting various microscopic characterizations of real devices.

Interfaces and band alignments

Challenges

As the bulk absorber of the device is improved and thinned, the interfaces have a larger impact on device performance. Advances in the efficiency of CdTe devices from 17% to near 22% took place from 2012 to 2016 primarily due to improvements at the front interface. The current was increased by reducing parasitic absorption by eliminating CdS and including Se, and the conduction band offset at the front interface was made tunable through the introduction of front contact buffer layers such as Mg_xZn_yO. Several modeling efforts have highlighted the benefit of a small spike in the conduction band offset to reduce the concentration of minority carriers and surface recombination at the interface.[90]

The back contact remains a source of loss in the state-of-the-art device that impacts both V_{oc} and FF. State-of-the-art devices leverage highly doped ($\sim10^{19}$ cm^{-3}) ZnTe layers and proprietary buffer layers, resulting in a contact with fairly high hole selectivity (Figure 4A). Due to the high ionization energy of CdTe, it is challenging to produce a low-resistance contact with favorable band bending to reduce minority carrier recombination.[91] High acceptor doping in the absorber pushes the Fermi level deeper, which makes forming an effective back contact even more challenging, as "downward" band bending will induce the collection of minority carriers at the rear interface, increasing local recombination and reducing the device V_{OC}. The interface is further complicated by the presence of both charged and neutral defect states, which may pin the Fermi level of the surface relative to the bulk of the absorber, inducing counterproductive band bending that cannot be screened even when the individual materials have good energy alignment prior to contact. Interface states may be modified by various treatments prior to contact deposition (i.e., etching and wet treatments) or during contact deposition due to interfacial chemistry.[92]

Analysis of interfacial properties is particularly challenging in devices. Access to surfaces and interfaces has historically been limited to partially completed devices or test structures generated specifically for the measurement, although with bifacial contacts becoming more mainstream, low-energy optical measurements such as TRPL are increasingly feasible.[93–95] JV(T) measurements can be used to make estimates of barrier heights, and, in conjunction with other measurements, sample sets, and modeling, may be used to assign parameter values to particular interfaces. In the past several years, a thermomechanical delamination technique has been developed and utilized to reveal the buried front oxide/non-oxide interface, which has enabled a wealth of information to be discovered through detailed characterization of real-world devices.[96]

Band alignments (ΔE_C, ΔE_V), band bending ($E_{V,surface} - E_{V,bulk}$), and surface defect chemistries are particularly helpful for directing contact development. X-ray photoemission spectroscopy (XPS) can be implemented to survey the exposed surface's chemistry and electronic structure with a ~10 nm information depth. For example, the redox-induced changes of tellurium's core electron's energy spectrum are easily detected and can monitor the amounts of Te^{4+}, Te^0, and Te^{2-} participating in Te-O bonds, elemental Te, and Te-Cd bonds, respectively. On the other hand, cadmium's energy spectrum is not so easily modified but does produce a potentially underutilized cadmium-modified Auger parameter whose value can be correlated to a compound (e.g., CdTe, CdSe, and CdO).[92] The sensitivity to most elements yields a non-destructive screening procedure for impurities remaining in the absorber after processing steps like wet etching. The surface sensitivity can be further utilized in careful angle-resolved studies, which have proven useful for investigating the formation of two-dimensional $CdCl_2$ sheets post-absorber deposition.[97] Both Te and Cd core peak positions can in some cases be used to extract built-in fields in the device, enabling band bending at the interface to be extracted. TRPL is often used to estimate surface passivation and is particularly helpful in trends between like devices, but care must be taken to ensure that bulk parameters do not change between samples.[98] Raw surface recombination velocities are typically not feasibly extracted, as additional assumptions regarding optoelectronic properties (band offset, mobility, bulk trap density, etc.) are required for interpretation.

Research goals

The construction of a band diagram for a system in which several optoelectronic properties are transversely varying in the device

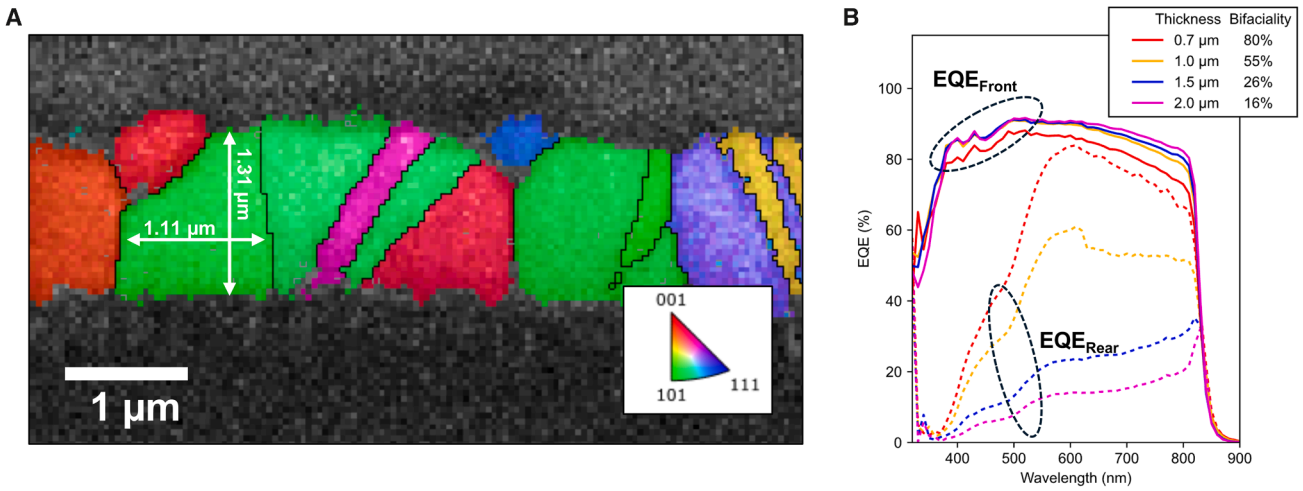

Figure 9. Microsctructure and performance implications of thinning Cd(Se,Te) absorbers

(A) EBSD image of a cross-section in a thin Cd(Se,Te) device. Grain sizes are approximately equal to the film thickness.

(B) EQE measures from the front ("sunny") side of the film stack and from the rear ("film") side of the device for thicknesses varying from 0.7 to 2 µm. The bifaciality increases as the device is thinned due to a larger proportion of the incident light being collected at the field-affected front interface during rear illumination.

(e.g., band-gap and dopant density) is very challenging. Combining cross-sectional measurements such as CL, energy-dispersive spectroscopy (EDS), AEM, KPFM, and SSRM in devices with XPS-generated band alignments in congruent test structures would allow such band diagrams to be created and areas for improvement identified. Cross-sections would need to be generated with minimal damage to the analysis interface, such as by cryogenic focused ion beam (cryo-FIB). Single-crystal model systems may be leveraged here to determine the expected behavior of bulk interfaces and orientation-dependent properties that may impact performance.

Identification of new material compositions and methods for doping control at the front interface will be necessary to induce stable and productive band bending in the absorber. Ideally, the densities of interface defects and the related surface recombination velocity would be low. The ideal front interface would enable lossless collection of minority carriers and have an appropriate band gap or band-gap grading. Any proposed changes must be compatible with subsequent processing (e.g., $CdCl_2$ and doping). Chemical reactions such as oxidative segregation should also be limited. While many useful scientific discoveries have been made leveraging Cu-doped absorbers, the coupling between interfacial and bulk absorber properties necessitates that ongoing interfacial studies leverage Gr-V or undoped absorbers to maximize transferability to contemporary cells.

Several strategies are considered for fabricating an improved rear contact. A thin passivating layer, perhaps comprised of wide band-gap amorphous material, might be able to coordinate with dangling bonds to reduce the surface state population and the related recombination velocity. Evidence for such an approach was demonstrated in Al_2O_3-passivated samples, which had remarkably high lifetimes and implied V_{OC}, although the passivating layers were too resistive to make an effective contact.[99] It is difficult to achieve both passivation and adequate conductivity simultaneously, and for this reason approaches based on point-contact geometries, where regions of carrier collection and surface passivation are laterally dispersed, either artificially (through lithography) or naturally (through facet-specific reactivity), are being pursued.[100,101] Alternatively, states for hole transfer at the right energy level, either in the passivating layer itself or in an adjacent layer, could transport holes in an adequately thin (~5–10 nm) layer.

Thin and bifacial devices

Challenges

As discussed previously, thinning the absorber could directly enable higher CdTe manufacturing capacity with the existing Te supply and potentially reduce processing time and CapEx expenditure related to deposition and high-temperature processing. Additionally, use of a thinner absorber would also provide additional benefits associated with a higher degree of bifaciality. One challenge is the coupling between grain sizes and absorber thickness. As an EBSD image of a Cd(Se,Te) device fabricated by the University of Toledo using close-space sublimation shows (Figure 9A), the aspect ratio of grain height to width is approximately 1:1. Thus, thinner devices have a higher concentration of grain boundaries and microstructures in the absorber. This 675-nm-thick Cu-doped Cd(Se,Te) device prepared on a TEC12D substrate exhibited an efficiency of 16.8% as compared with 17.7% for a 4 µm absorber.

As shown in Figure 9B, First Solar's best-performing device with a 2 µm thick Cd(Se,Te) absorber has over 20% efficiency, indicating high efficiency can be achieved with thinner absorbers. Still, improvements in both back contact passivation and the absorber lifetime remain critical for full efficiency entitlement. 80% of the sunny-side current has been realized under backside illumination with a 0.7 µm CdTe absorber, and 55% for 1.0 µm. Significant loss near the back contact remains with low film-side EQE for the near-blue wavelengths at all absorber thicknesses. Better absorber lifetime/mobility (both contributing

to longer diffusion length) and long-wavelength light management would also help with better carrier collection and device performance, judged by the reduced film-side EQE in the red region.

The barrier to reaching full efficiency entitlement in thin devices and a high bifaciality in bifacial devices is the highly defective and poorly energy-aligned hole contact.[102–105] In both thin and bifacial devices, the concentration of electrons generated within or diffusing into the depletion width of the Schottky barrier at the rear contact is higher than in a standard cell, inducing a reduction in the quasi-Fermi level splitting at the rear interface and subsequently the extractable voltage. Inducing upward band bending to deplete electrons at the interface or minimizing the density of interfacial defects would reduce back surface recombination and help to minimize the voltage deficit. Lateral non-uniformities in the absorber are likely to also lead to spatially varying back-surface band bending and interfacial defect distributions that sum to control the performance of the contact.[106]

Ultra-thin bifacial devices (<1 μm) require additional light management to retain high J_{SC} entitlement. Long-wavelength light in devices with opaque metallic contacts benefits from a reflection at the back contact, allowing for additional collection. This is particularly beneficial at long wavelengths that are only effectively absorbed in a Se-rich low-band-gap region at the front interface. Fabricating transparent hole contacts that allow ingress of short-wavelength light and the internal reflection of long-wavelength light would make the most of a bifacial configuration.

Research goals

Creating thin and bifacial devices requires the development of an improved back contact. Focused studies to develop a hole contact that is band-aligned, relatively defect-free, transparent, conductive, and compatible with device processing will facilitate improved bifacialities and thinner devices. Optimizing absorber growth by managing grain size and alloying is also of concern. Light management strategies at the rear contact, either through optically engineered reflectors or through down-conversion layers capable of red-shifting rear-side incident light, will enable higher front-side and bifacial currents as the device is thinned. Improved performance of the electrical and optical properties of the back contact for thin devices may also be required for future application of CdTe-related materials in tandem devices.[107–109]

SUMMARY

Below, we highlight several supply chain and scientific development areas that must be addressed concurrently to improve the CdTe PV manufacturing capacity that was discussed in detail above. This growth will require collaboration between research scientists, engineers, PV manufacturers, and mineral refiners and must also be supported with sufficient resources.

Supply chain development needs

The supply chain for Te will need to be grown to accommodate a larger manufacturing capacity. Estimates indicate that ample Te resources are available in waste streams from Cu production. Thus, the most critical developments in the supply chain would target the following.

1. Improve the recovery of tellurium from copper anode slimes.
2. Develop a process to utilize pyrite to encourage its recovery during copper mineral processing and capture Te presently lost to copper tailings.
3. Examine resource potentials for deposits that contain Te enrichments with other metals than copper (e.g., Au, Pb, and primary Te).

Scientific development needs

Scientific developments need to target improving module efficiencies and decreasing Te intensity (g Te/W_{DC}) of existing module manufacturing. Developments that improve the efficiency will improve the competitiveness of CdTe modules with respect to standard silicon modules. Efforts to thin absorbers allow a smaller quantity of Te to be used per W_{DC} of power, effectively growing the available manufacturing capacity for a constrained Te supply as Te-refining ramps to higher production. Reducing non-radiative recombination both in the bulk and at interfaces will be key for both efforts. Specific efforts identified to improve device efficiency and Te intensities are listed below.

(1) Develop robust techniques for combining multidimensional measurements (i.e., JV*(T)*, frequency-dependent *CV*, and fluence- and temperature-dependent TRPL) with numerical modeling for access to sub-*JV* parameters.
(2) Develop and proliferate multiscale optoelectrical models of state-of-the-art Cd(Se,Te) devices.
(3) Develop robust kinetic and DFT models characterizing the complexes formed by Cl, O, Cd, Te, Se, and Gr-V dopants and their activation.
(4) Develop models and measurement techniques that capture physics associated with nano- and micron-scale fluctuations in electrical and chemical environments.
(5) Develop and proliferate a high-throughput procedure for the direct and regular measurement of inter-grain and intra-grain mobilities in polycrystalline devices.
(6) Develop an improved rear contact with lower surface recombination velocity and improved band alignment to enable thin and bifacial devices.

OUTLOOK

Despite being a mature and multi-GW PV technology, CdTe PV has tremendous potential for growth both in the material supply chain and in module efficiencies. The fact that it has demonstrated success at this scale with production modules less than 2/3 of its detailed balance limit indicates significant room for future growth. This roadmap highlighted pathways to 100 GW_{DC} in module production per year by 2030 by improving Te extraction from existing supply chains, minimizing Te usage in modules by leveraging thinner absorbers, and by improving device efficiencies. The scientific developments necessary to address these challenges were discussed to focus the efforts of the research community, and the barriers to improving Te supply were discussed. Both scientific and supply chain innovations will be necessary to maintain the high CAGR of the CdTe PV

industry and cement it as a key part of the pathway to multi-TW-scale PV deployment.

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DECLARATION OF INTERESTS

R.G.D. has 10% ownership in Solarscape.

SUPPLEMENTAL INFORMATION

Supplemental information can be found online at https://doi.org/10.1016/j.joule.2025.102235.

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