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ABSTRACT

Negative differential resistance (NDR), where the device current decreases with increasing bias voltage, is a representative phenomenon where quantum mechanics induces counterintuitive physical behavior and offers promising applications such as high-frequency oscillators, amplifiers, and multilevel logic circuits. While the NDR behavior has been extensively studied in various materials and devices, the role of surface properties in NDR, particularly in InAs-based diodes, remains underexplored. In this work, we report the observation of NDR in vertically structured InAs p^+n diodes that exhibit a peak-valley current ratio of ~6, which is suitably high for applications. Circumference-normalized current–voltage characterization revealed that the NDR originates from band-to-band tunneling between the valence band of p^+-InAs and the conduction band of an n^+-InAs surface, where the n^+ surface is due to surface states on otherwise n^--InAs. In addition, by comparing devices with various surface passivation methods (without intentional passivation, benzocyclobutene polymer, and silicon nitride), we found that the surface termination significantly affects the NDR characteristics. We present an equivalent circuit model to explain the observed device behavior. These findings offer insights into surface-enabled NDR phenomena and present new knobs for engineering NDR devices.

I. INTRODUCTION

Negative differential resistance (NDR) is a phenomenon where the current flowing through an electronic device decreases as the bias voltage across the current leads increases in a certain voltage range. This counterintuitive effect possesses significant potential for numerous device applications, including high-frequency oscillators,[1,2] amplifiers,[3,4] and multilevel inverters.[2,5] Since the demonstration of NDR in germanium pn junctions by Esaki in 1957,[6] there have been many studies on the various mechanisms of NDR and their implementation in semiconductor electronic devices such as the Esaki diode,[6,7] resonant tunnel diode (RTD),[8,9] Gunn diode,[10,11] impact ionization avalanche transit time diode,[12,13] as well as NDR circuitries employing active components.[14,15] Among these, the Esaki diode, which utilizes band-to-band tunneling (BTBT) in heavily doped pn junctions, is of great interest as it can be realized by simply exploiting heavy doping in a semiconductor, even in a homojunction. Esaki diodes have been demonstrated in a variety of materials and their combinations, such as silicon,[7,16] germanium,[6,17] gallium arsenide (GaAs),[18] gallium nitride (GaN),[1,19] two-dimensional (2D) materials,[20,21] and their heterojunctions.[22,23]

Indium arsenide (InAs) is a III–V compound semiconductor material that has a small direct bandgap of 0.35–0.42 eV, high electron mobility in the range of 10^4, and strong spin–orbit coupling.[24–26] These features can be advantageous for the tunneling process as the small direct bandgap provides a low effective tunneling barrier and high electron mobility, resulting in increased tunneling probability.[27,28] Therefore, these properties can lead to high peak tunneling current and high-frequency operation compared to other materials, which is beneficial for the applications noted above.[1–5] For that reason, there have been several reports on InAs-based tunnel diode NDR. NDR in InAs has been attributed to trap-assisted tunneling through bulk trap levels[29] and BTBT through bulk p-i-n structures.[30] InAs exhibits heavily doped n-type surface layers because of Fermi level pinning related to the surface donor-like states.[31–33] The presence of this n-type surface can present complications in device design and material processing for electronic device fabrication in terms of undesirable doping profiles and as a source of leakage current. However, the effects of the n-type surface layer of InAs on the NDR behavior have so far been relatively unexplored.

In this letter, we present the observation of NDR in the current–voltage (I–V) characteristics of vertically structured InAs p^+n diodes and show that the NDR is closely related to the surface property of the device sidewalls. Specifically, the NDR originates from the BTBT between the valence band of the p^+ layer and the conduction band of the surface of the sidewalls of the n layer. This relation is evidenced by the circumference-normalized I–V characteristics near the NDR regime. In addition, three types of devices with different surface passivation methods are compared: no intentional passivation, benzocyclobutene (BCB), and SiN. We observe that the NDR behavior is sensitive to the surface passivation. To explain the observed NDR, we present an effective circuit consisting of bulk and surface pn diodes in parallel, where the overall current in the device in the NDR regime is dominated by the current through the surface pn diode. Our findings on surface-dominated NDR not only elucidate the origin of NDR in InAs p^+n junctions but also suggest an interesting approach to engineering NDR for improving device performance by tailoring the device geometry and surface passivation so that the NDR current can be maximized with low area cost in highly scaled integrated circuits. This work provides insight into surface NDR phenomena and their potential use in future electronic applications.

II. SAMPLE PREPARATION AND METHODOLOGY

A. Sample preparation

An optical microscope image of an array of vertically structured InAs p^+n diodes is presented in Fig. 1(a) and a schematic drawing of its cross-section is illustrated in Fig. 1(b) with the designed doping profiles. For the experiment presented in this work, the material stack was grown via molecular beam epitaxy with standard effusion cells for Al, In, Si, and Be, and valved cracker cells for As and Sb. Growth began with 200 nm of n^+-InAs at a doping density of 2×10^{18} cm^{-3}, followed by 1200 nm of n^--InAs at a doping density of 5×10^{15} cm^{-3}. The p-type region of the junction was doped to 1×10^{18} cm^{-3} and comprised 25 nm p-InAs, then 100 nm of lattice-matched p-AlAsSb, and finally 150 nm of p-InAs. The final 50 nm of the p-InAs layer had the doping graded up to 1×10^{19} cm^{-3} to improve contact resistivity. Here, active doping densities were calibrated by measuring the Hall effect on a series of GaAs samples grown with varying dopant fluxes. In addition, it is worthwhile to mention that the n^--InAs layer is sufficiently thick to prevent tunneling between the p^+- and n^+-InAs layers, and the AlAsSb electron barrier layer suppresses electron diffusion current.[34] After epitaxy, diodes were fabricated in a cleanroom using standard photolithographic techniques. First, devices were isolated by etching mesas with a solution of 100:55:5:3 deionized (DI) H_2O:$C_6H_8O_7$:H_3PO_4:H_2O_2, followed by a rinse in deionized water and drying with N_2 gas. Devices receiving passivation were either spin-coated with BCB and cured in an oven or coated with SiN by plasma-enhanced chemical vapor deposition. Vias were opened through the passivation layer using a reactive ion etch. The samples were immersed in 1:1 HCl:H_2O immediately prior to depositing Ti/Pt/Au Ohmic contacts through electron beam evaporation and subsequent lift-off. As a result, three kinds of circular diodes with different passivation statuses were fabricated: without intentional passivation, BCB passivated, and SiN passivated. Furthermore, we designed diodes with several different diameters (150, 300, 500, and 1000 μm) to delineate bulk and surface current components.

B. Electrical characterization

A closed-cycle He cryostat was used for temperature-dependent I–V measurements from 2 to 300 K. The sample was

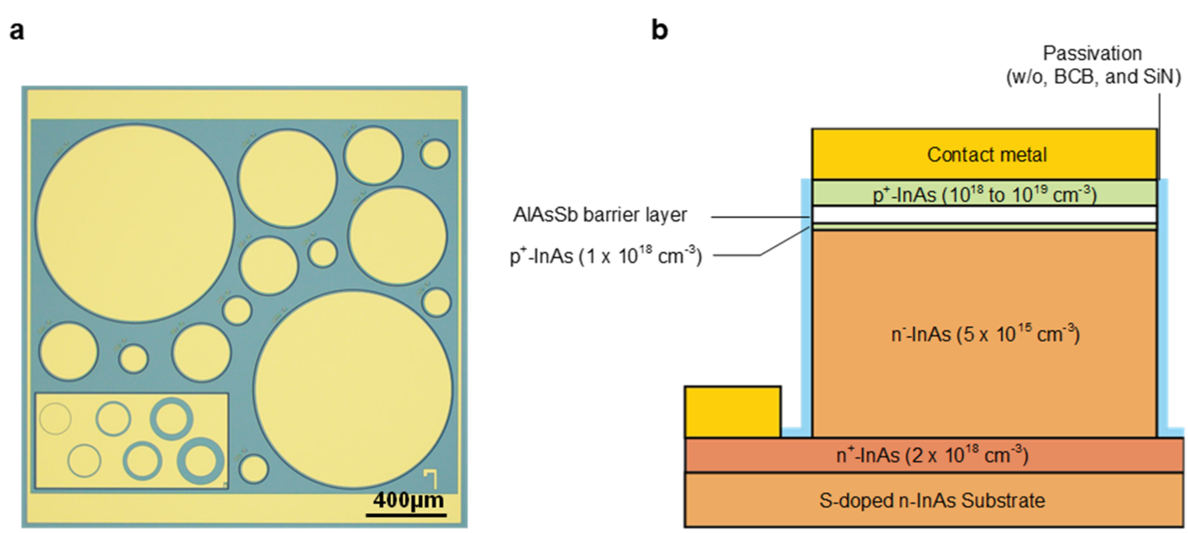

FIG. 1. (a) An optical microscope image and (b) a schematic cross-section of the vertical InAs pn diode.

mounted on a printed circuit board on a custom probe equipped with semi-rigid coaxial cables for I–V measurements in the cryostat. The sample temperature was controlled with a Lakeshore 336 temperature controller from 2 to 300 K, and the I–V characteristics were obtained using Keithley 2400 source measure units.

III. RESULTS AND DISCUSSION

A. Current–voltage characteristics and observation of NDR

Figure 2(a) shows the measured temperature-dependent I–V characteristics from the device without intentional surface passivation in the small forward bias voltage regime between 0 and 0.4 V. Clear NDR behavior between 0.05 and 0.2 V is observed over the temperature range from 2 to 275 K, and the NDR disappears as the temperature increases over 275 K. Above this temperature, the thermionic current, which arises from carriers overcoming the pn junction potential through thermal excitation, becomes dominant. There is a shift in both voltage and current at the NDR peak position as temperature varies [Figs. 2(c) and 2(d)]. The peak current initially increases with increasing temperature, reaching a maximum of about 86 μA at 140 K, and decreases as the temperature further increases. On the other hand, the bias voltage at the NDR peak monotonically diminishes with increasing temperature. Several factors affect the tunneling coefficient in BTBT, such as bandgap, effective mass, carrier concentration, and thermal distribution of carriers. Each of these factors has a different dependence on temperature. We attribute the shift in NDR peak current, with the peak at 140 K, to the change in the tunneling rate due to those competing mechanisms. For example, the decrease in bandgap with increasing temperature can increase the BTBT rate at high temperatures.[35,36] On the other hand, a smeared Fermi–Dirac distribution of carriers at high temperatures can reduce the NDR peak current.[37] The monotonic decrease in the peak voltage with temperature can be explained as the effect of lower series resistance in the n-region at higher temperature, consequently reducing the bias voltage required for NDR. Influenced by those factors, the peak-to-valley current ratio (PVCR), which is a representative figure of merit in NDR devices, shows a similar change with temperature, and the maximum PVCR is measured to be 6 at 140 K [Fig. 2(b)]. It is worthwhile to point out that the PVCR value satisfies the requirement for applications, PVCR > 5.[38] A similar NDR behavior is observed in the two devices with intentional surface passivation (BCB and SiN), and their temperature-dependent I–V characteristics are presented in supplementary material Fig. S1. Their detailed characteristics will be discussed in Sec. III B.

B. Current path and surface sensitivity of NDR

To assess the contributions from bulk and surface currents to the observed NDR, we normalize the NDR current to two diode dimensions—area and circumference. The surface current density as a function of bias voltage for non-passivated devices with

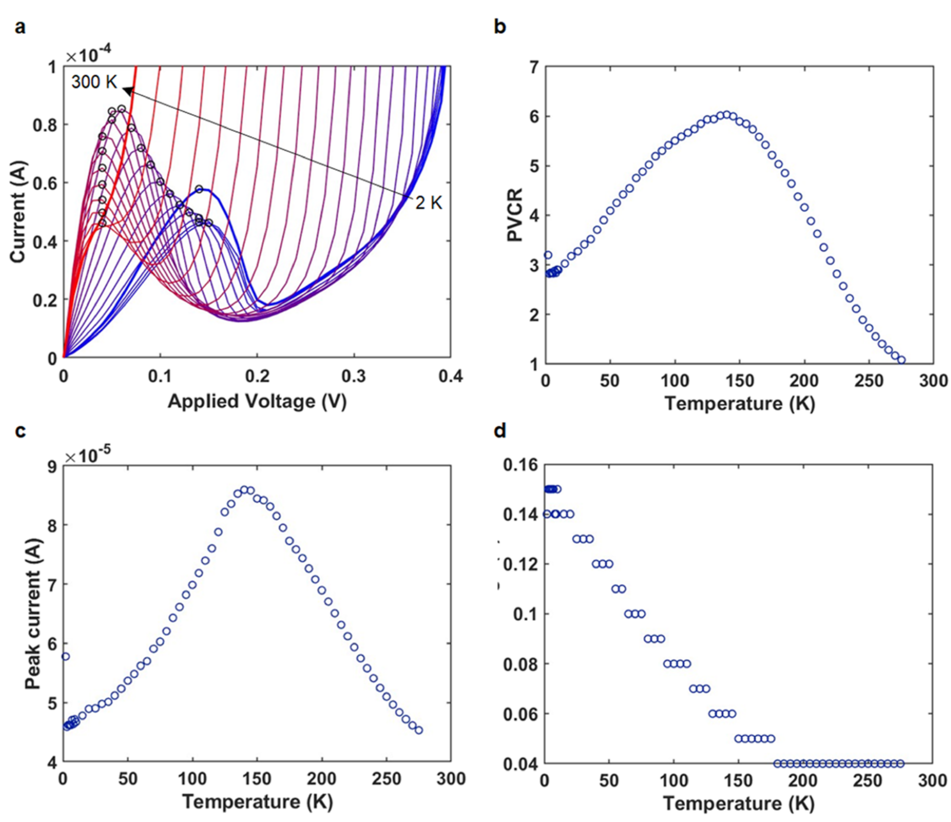

FIG. 2. Electrical characteristics of a 500-μm-diameter InAs diode without passivation. (a) Temperature-dependent current–voltage characteristics from 2 to 300 K with NDR. The data for the lowest and highest temperatures (2 and 300 K) are represented as thick blue and red lines, respectively, and the peak positions at each temperature are represented as black dots. (b) The PVCR, (c) peak current, and (d) the bias voltage where the peak current appears under various temperatures. The staircase behavior is due to a voltage step size of 0.01 V used in our voltage sweeps.

diameters of 300 and 500 μm at four different temperatures of 2, 100, 200, and 300 K is presented in Fig. 3(a). In the plot, the surface current density curves from the two devices with different diameters, as grouped by line types, overlap well at each temperature. This strongly suggests that the overall current in this regime is dominated by conduction along the sidewall surface. The ratios between the NDR peak currents from the 300 and 500 μm devices are calculated and plotted in Fig. 3(b). The ratio is much closer to the circumference length ratio between the two diodes (5/3) rather than the device area ratio (25/9) throughout the whole measurement temperature range. In addition, the peak current from BCB-passivated devices shows good linear dependency in device diameter as presented in supplementary material Fig. S2, proving that the tunneling current is dominantly conducted through the sidewall. Therefore, the NDR behavior itself is also related to the surface. In addition, we found that the NDR is sensitive to surface passivation. In Fig. 3(c), the PVCRs from 500 μm diameter devices with different surface passivation methods are presented. Both the magnitude and temperature dependence of the PVCR strongly depend on the surface passivation state. The device without intentional passivation has the highest PVCR value among the devices throughout the measurement temperature range. The BCB-passivated device shows that the PVCR stays relatively constant up to 150 K and decreases at high temperatures as the thermionic current overrides the tunneling current. In the case of SiN-passivated diodes, the overall trend is similar to the non-passivated device, but the magnitude of PVCR is lower than the non-passivated one. The diodes exhibit significant differences in the overall shape of the I–V characteristics in the NDR regime depending on the surface passivation. The non-passivated diode has the smallest peak voltage with the largest PVCR. The BCB-passivated device shows the highest peak current in the NDR regime, but also the highest valley current, resulting in a small PVCR. Interestingly, there is a significant difference in the NDR behavior of the SiN-passivated device. The I–V characteristics from this device show two abrupt kinks in the NDR region rather than a smooth decrease in current. This behavior is similar to the NDR reported by Krier and Huang for InAs-based p-i-n diodes, where they explained the NDR through carrier tunneling mediated by bulk defect states in InAs.[29] This distinct behavior of the SiN-passivated diode may come from plasma-induced damage during SiN deposition or stronger chemical bonds between InAs and SiN than BCB. As SiN does not passivate the defects on the etched surface,[39,40] the damage on the etched

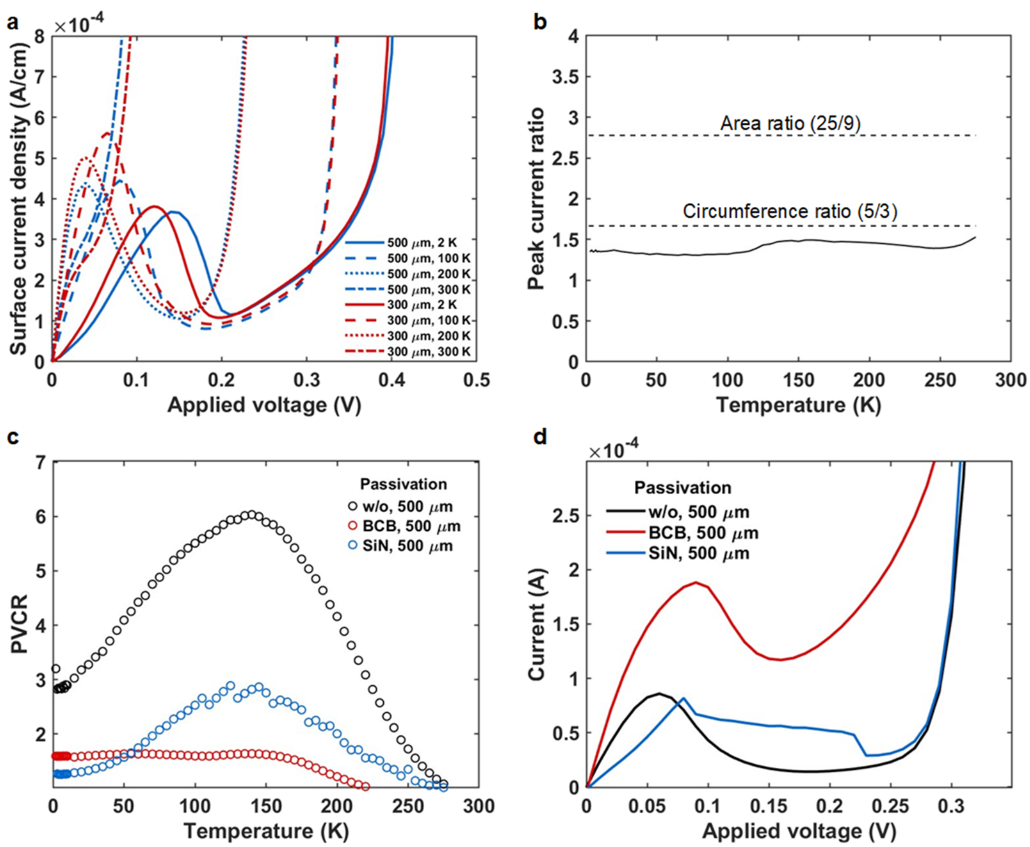

FIG. 3. Circumference dependency and surface sensitivity of NDR in InAs vertical diodes. (a) Circumference-normalized current–voltage characteristics from the device without intentional passivation and (b) NDR peak current ratio between 300 and 500 μm diameter devices. Dashed lines represent the reference line for area and circumference ratio of the devices. (c) Temperature dependence of PVCR vs temperature plot and (d) current–voltage characteristics at 140 K for different surface passivation methods.

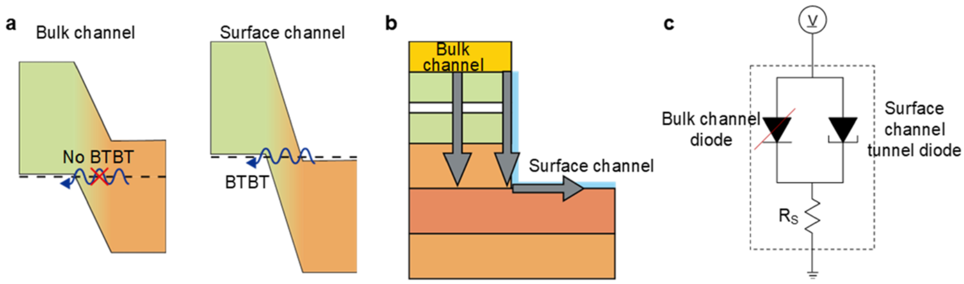

FIG. 4. NDR mechanism through a surface channel in an InAs vertical diode. (a) Energy band diagram for bulk and surface channels. BTBT can occur in the surface channel due to the heavy electron doping from surface defect states, whereas it is forbidden in the bulk channel. (b) Cross-sectional schematic with two possible channels for conduction represented by arrows. (c) Equivalent circuit diagram for two-channel InAs vertical diode where the conduction through the surface channel is dominant.

sidewall can induce similar defect-mediated tunneling behavior. The results above on the circumference dependence and surface sensitivity of the NDR in these devices indicate that the observed NDR is closely tied to conduction along the sidewalls of the mesa.

C. Mechanism and equivalent circuit

The clear NDR characteristics observed in these InAs p^+n devices indicate BTBT across the pn junction. Representative band diagrams are shown in Fig. 4(a). In the bulk, the doping of the n-InAs layer is low (5×10^{15} cm^{-3}), and the Fermi level is within the bandgap. Therefore, no electron states are available for BTBT under zero or weak positive bias conditions. However, the situation on the sidewall surface is quite different. It is well known that the surfaces of etched InAs sidewalls pin the Fermi level in the conduction band and lead to a surface accumulation layer of n-type charge.[32,33] A p^+n^+ junction can therefore exist at the sidewall surface, enabling BTBT there.

The InAs vertical diode can be understood as a composite diode with two parallel current paths: a bulk p^+n diode without BTBT and a surface p^+n^+ diode with BTBT as shown in Fig. 4(b). With this model, the circumference dependence of the BTBT current is understandable. Since conduction through the surface channel occurs at the p^+n^+ junction, its effective width is proportional to the circumference of the device. In addition, the BTBT characteristics are expected to change significantly with surface passivation, as the passivation modifies or passivates the pinning of the sidewall surface. This is consistent with the observed surface passivation sensitivity of the NDR behavior in Figs. 3(c) and 3(d). In addition, as the AlAsSb layer reduces the diffusion through the bulk channel, the circumference length dependency can be found in the thermionic current regime as well. This dependency can be seen in full-range I–V characteristics from all three devices under room temperature in supplementary material Fig. S3.

Here, we compare the performance of our tunnel diode with InAs/GaSb heterojunction tunnel diodes, which are representative Esaki diodes using InAs. In a study by Hou *et al.*,[41] a peak current density of 9 MA/cm^2 was achieved with an InAs/GaSb heterojunction Esaki diode. Although it is difficult to directly compare our device, as our tunnel diode has the tunnel current through the sidewall, our InAs homojunction diode shows a surface peak current density of 0.368 mA/cm, which becomes 29.4 mA/cm^2 when it is converted into current density for our 500 μm diameter device—much lower than the InAs/GaSb case due to a poor surface-to-volume ratio. If our diode were scaled down to a 100 nm diameter, which is similar to the above-mentioned InAs/GaSb device, we would expect that a current density of 147 A/cm^2 could be achieved. In addition, the InAs/GaSb tunnel diode shows a maximum PVCR of 1.7, which is much smaller than our maximum PVCR of ~6. Another study on a 10 nm scale InAs/GaSb tunnel diode[42] shows an average peak current density of 1 MA/cm^2 and a maximum PVCR of 3.6, also showing a higher current density and lower PVCR than our diodes. A summary of the figures of merit of these diodes is provided in supplementary material Table S1.

This surface-dominant NDR device may find use in maximizing the performance of NDR applications by adapting the device geometry. Compared to bulk devices where the device current scales with the device area, surface-dominated NDR devices can preserve the large current even with scaling by exploiting appropriate geometry design such as a zigzag wave pattern that maximizes surface area while minimizing the total footprint of the device. This characteristic is advantageous in several practical applications such as NDR oscillators and NDR-based logic circuits, which require a significant current level for stability and reliability.[43,44] The surface sensitivity serves as a knob for engineering the NDR through choices of material processing and surface passivation methods. The surface sensitivity also presents a mechanism for chemical sensing.[45,46] As chemical species bind to and chemically dope the sidewall surface, the tunnel junction characteristics are expected to exhibit corresponding changes.

IV. CONCLUSIONS

In summary, we investigated the NDR behavior observed in the I–V characteristics from vertically structured InAs p^+n diodes with different sizes and surface passivation. The NDR is shown to be dominated by conduction along the sidewall surface and is sensitive to the surface passivation method. This surface-dependent NDR originates from the etched InAs sidewall, which is heavily doped with electrons due to the Fermi level pinning in the conduction band at the surface of InAs. The resultant heavily doped p^+n^+ junction at the surface enables BTBT, leading to surface-dependent NDR with a PVCR of ~6, which is suitably high for applications. Our study provides the understanding of this NDR mechanism in InAs and the potential use of the phenomenon in the highly scaled system.

SUPPLEMENTARY MATERIAL

The supplementary material includes the temperature-dependent I–V characteristics of BCB- and SiN-passivated tunnel diodes, a description of the NDR current analysis where the NDR current was fitted as a function of diameter to determine the bulk and surface channel contributions to the total current, the full-range current density–voltage and surface current density–voltage characteristics at room temperature from three different passivation samples, and a comparison table between previously reported InAs/GaSb tunnel diodes and the tunnel diode investigated in this study.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Sungjae Hong: Conceptualization (equal); Data curation (lead); Formal analysis (lead); Investigation (equal); Methodology (equal); Validation (equal); Visualization (lead); Writing – original draft (lead); Writing – review & editing (equal). **Aaron J. Muhowski**: Data curation (supporting); Formal analysis (supporting); Investigation (supporting); Resources (supporting); Writing – review & editing (equal). **Victor J. Patel**: Data curation (equal); Investigation (equal); Methodology (equal); Resources (equal); Writing – review & editing (equal). **Evan M. Anderson**: Conceptualization (supporting); Funding acquisition (lead); Investigation (supporting); Project administration (lead); Supervision (supporting); Visualization (supporting); Writing – review & editing (equal). **Tzu-Ming Lu**: Conceptualization (equal); Data curation (supporting); Formal analysis (equal); Investigation (equal); Methodology (equal); Resources (equal); Supervision (lead); Validation (equal); Visualization (supporting); Writing – original draft (supporting); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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