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High Mobility and Electrostatics in GeSn Quantum Wells With SiGeSn Barriers

Christopher R. Allemang, David Lidsky,* Peter Sharma, Shang Liu, Jifeng Liu, Yunsheng Qiu, Shuiqing Yu, and Tzu-Ming Lu*

GeSn is an emerging material with potential applications in next-generation integrated optoelectronics and quantum information processing. While GeSn/SiGeSn quantum wells exhibit promising optical properties, their electrical transport characteristics and governing electrostatics in gated structures remain unexplored. Heterostructure field-effect transistors are fabricated using GeSn/SiGeSn quantum wells and electronic transport properties of 2D holes are characterized. At 2 K, heterostructure field-effect transistors with well/barrier compositions of $Ge_{0.945}Sn_{0.055}/Si_{0.03}Ge_{0.93}Sn_{0.04}$ and $Ge_{0.9}Sn_{0.1}/Si_{0.017}Ge_{0.927}Sn_{0.056}$, show peak mobilities of 9000 and 19 000 cm^2/Vs, respectively, the latter setting a record for the highest mobility reported for GeSn quantum wells with a Sn concentration around 6 % or greater. Remarkably, at low carrier densities, devices with a SiGeSn barrier exhibit mobilities several times higher than previously reported for GeSn quantum wells with a Ge barrier. This higher mobility contrasts with the expectation that alloy scattering from the barrier would reduce carrier mobility. Two mechanisms based on atom probe tomography data analyses are proposed: i) unintentionally improved SiGeSn/GeSn interface and/or ii) reduced alloy scattering from short-range order. Significant current–voltage hysteresis is observed, with the effective threshold gate voltage shifting by more than 5 V, attributed to non-equilibrium trapped charge at various interfaces within the SiGeSn heterostructure.

1. Introduction

Silicon has led the semiconductor industry for decades, resulting in the development of a wide range of electronic devices and digital computing. Silicon-germanium (SiGe) alloys brought new opportunities with strain engineering for higher mobilities and bandgap engineering in heterostructures for quantum wells (QW). Building on this foundation, adding Sn to Group-IV alloys and heterostructures brings new potential to silicon-based photonics,[1–9] electronics,[10–15] spintronics,[15] and quantum information science (QIS).[16] Within QIS, there is particular interest in the ability to perform both quantum computation and transmit quantum information in the same system, and a SiGeSn material system provides a promising platform to do this.

Toward the goal of a system that can compute and transmit quantum information, spin-photon coupling is an important milestone to provide quantum transduction from spins, where computation is performed, to photons for transmission.[17–20] Single spin-to-photon coupling has been realized with III-V QWs.[21] However, QIS based on III-V QWs is limited by challenges including material quality and compatibility with silicon processing and integration.[22] Direct spin-photon transduction cannot be performed in Si because of its indirect bandgap. Therefore, there is a desire for a high quality spin system based in a material that provides a direct bandgap and is compatible with silicon processing and integration.

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SiGeSn has compatibility with silicon integration and processing and progress has been made for both spin computation and photon transmission. There are a variety of opportunities in SiGe heterostructures where, in particular, many advances have been made using hole quantum dots confined in a Ge QW as qubits, leveraging their strong spin-orbit coupling.[16,23] Recently, interest in Ge QWs in GeSn have gained interest because of their potential for quantum computation using light-holes and access to a a direct band gap GeSn system.[24] Furthermore, adding Sn to Ge provides an additional knob for controlling spin-orbit coupling[25] and the GeSn material platform allows incorporating nuclear spins of Sn, which have been proposed as qubits with long coherence times.[26]

Realizing a SiGeSn-based quantum computation and transmission platform requires understanding both the optical and electrical properties of a SiGeSn-based system. There is ongoing work to understand complementary metal-oxide-semiconductor (CMOS)-compatible group-IV-based optoelectronic devices including GeSn lasers,[4–7] photodetectors,[8] and modulators[9] and significant progress has been achieved by leveraging Sn composition and strain.[27–35] While n-type metal–oxide–semiconductor[10,11] and p-type metal-oxide-semiconductor (PMOS)[12–15] GeSn transistors have been demonstrated, where it is understood mobility can be enhanced by strain and limited by surface roughness scattering at the well boundaries,[36] none of these works investigated the impact of the quantum well barriers. Understanding the impact of barrier layers on carrier transport and scattering mechanisms is desirable for electronic devices and for high-speed optoelectronic devices[37,38] toward the envisioned QIS platform.

Toward understanding the impact of QW barrier material on electrical properties, in this work, we study the electrical behavior of 2D holes in GeSn/SiGeSn QWs that previously demonstrated strong photoluminescence (PL) and excellent promise in optoelectronic devices.[39] We demonstrate a record hole mobility of 19 000 cm^2/Vs at 2 K in GeSn QWs with a Sn concentration on the order of 6 % for both the wells and barriers. Interestingly, at low carrier densities, devices with a SiGeSn barrier exhibit mobilities several times higher than previously reported for GeSn QWs with a Ge barrier, in contrast to the expectation that alloy scattering from the barrier would reduce carrier mobility. This is a significant outcome as low-density mobility is a critical figure of merit for QIS systems.[40] Two mechanisms, based on atom probe tomography data analyses, are proposed for this improved performance: i) un-intentionally improved SiGeSn/GeSn interface and/or ii) short-range order (SRO) reduced alloy scattering.

2. Results and Discussion

We focus on two samples in this study: one is $Ge_{0.9}Sn_{0.1}/Si_{0.017}Ge_{0.927}Sn_{0.056}$ and has the designation 01; the other is $Ge_{0.945}Sn_{0.055}/Si_{0.03}Ge_{0.93}Sn_{0.04}$ and has the designation 02. 01's epitaxial stack, from top to bottom, consists of a Ge cap (<10 nm), an upper SiGeSn barrier (42 nm), a GeSn QW (12 nm), a lower SiGeSn barrier (45 nm), and a Ge buffer (700 nm) on top of a Si substrate, Figure 3. The stack in 02 is similar, with differences in stoichiometry determined by atomic probe tomography (APT), to be discussed Section 2.1.2. This paper focuses on data from 01, which has the higher QW Sn content of the two samples, therefore when figures have no sample designation it should be understood the sample is 01. Qualitatively similar measurements of 02 are presented in the Supporting Information. In Section 4, the mobilities of 01 and 02 will be compared with samples that have simple monatomic Ge barriers. Sample 01's material properties were characterized by transmission electron microscopy (TEM), PL, and APT.

2.1. Material Analysis

2.1.1. Transmission Electron Microscopy

Cross-sectional TEM images of sample 01 are shown in **Figure 1** and were acquired using an FEI Titan with an accelerating voltage of 300 kV. In Figure 1a, misfit dislocations that form half-loop Lomer dislocations can be seen and are confined between the Ge buffer and the Si substrate.[41] Such features prevent threading dislocations (from lattice mismatch) from propagating to the QW layers and enhance strain relaxation on the top surface, which is attributed to a sufficiently thick Ge buffer. A high-angle annular dark-field TEM image is shown in Figure 1b. Sharp boundaries between each epi-layer are observed with gradient contrast, indicating the compositional transition between each layer. In Figure 1c, transitional boundaries at the interfaces of the cap, barriers, and well are shown, perpendicular to the [001] direction. The boundaries are only a few atomic layers thick, and energy dispersive X-ray spectrometry (not shown) indicates the boundaries originate from the change of Si/Sn incorporation. While a relatively low-density of defects in the QW is epxected, the 30°/60° dislocations formed by stacking faults are still observed throughout the entire QW.[42,43]

2.1.2. Atom Probe Tomography

APT was used to quantify the composition and SRO in the samples[44–46] and was acquired at the University of North Texas using a LEAP 5000XS with 20 pJ laser pulse energy, 355 nm wavelength, 250 kHz pulse frequency and 30 K base temperature. APT data of sample 01 is shown in **Figure 2a**. The composition profile in Figure 2b confirms a $Ge_{0.9}Sn_{0.1}$ QW sandwiched between SiGeSn barriers with 1.7 at.% Si and 5.6 at.% Sn on average. Interestingly, very thin (~2 nm thick) unintentional $Ge_{0.95}Sn_{0.05}$ barriers without Si are also observed between SiGeSn and $Ge_{0.9}Sn_{0.1}$ on both sides of the QW, consistent with the high-resolution TEM image in Figure 1c. Si-Si SRO in the SiGeSn barrier layers was analyzed using the Poisson-KNN method developed by Liu *et al.*[45] The degree of SRO was quantified using the parameter α^{KNN}_{Si-Si}, defined as P^{KNN}_{Si-Si}/x_{Si}, where P^{KNN}_{Si-Si} is the probability for a Si atom to have another Si atom as its Kth nearest neighbor (KNN), while x_{Si} is the Si composition in the same region. An α^{KNN}_{Si-Si} larger than 1 means preference for Si-Si KNN. The analysis of α^{KNN}_{Si-Si} was performed in each $10\times 10 \times 10$ nm^3 nanocube, and the histograms of α^{1NN}_{Si-Si} and α^{2NN}_{Si-Si} are presented in Figure 2c,d. The mean value of α^{1NN}_{Si-Si} and α^{2NN}_{Si-Si} are 1.11 ± 0.02 and 1.07 ± 0.01, respectively, both larger than 1. This result indicates a notable SRO in terms of preference for Si–Si 1NN and 2NN in the SiGeSn barriers, consistent with our previous work.[47] Notably, the SRO in the lower SiGeSn

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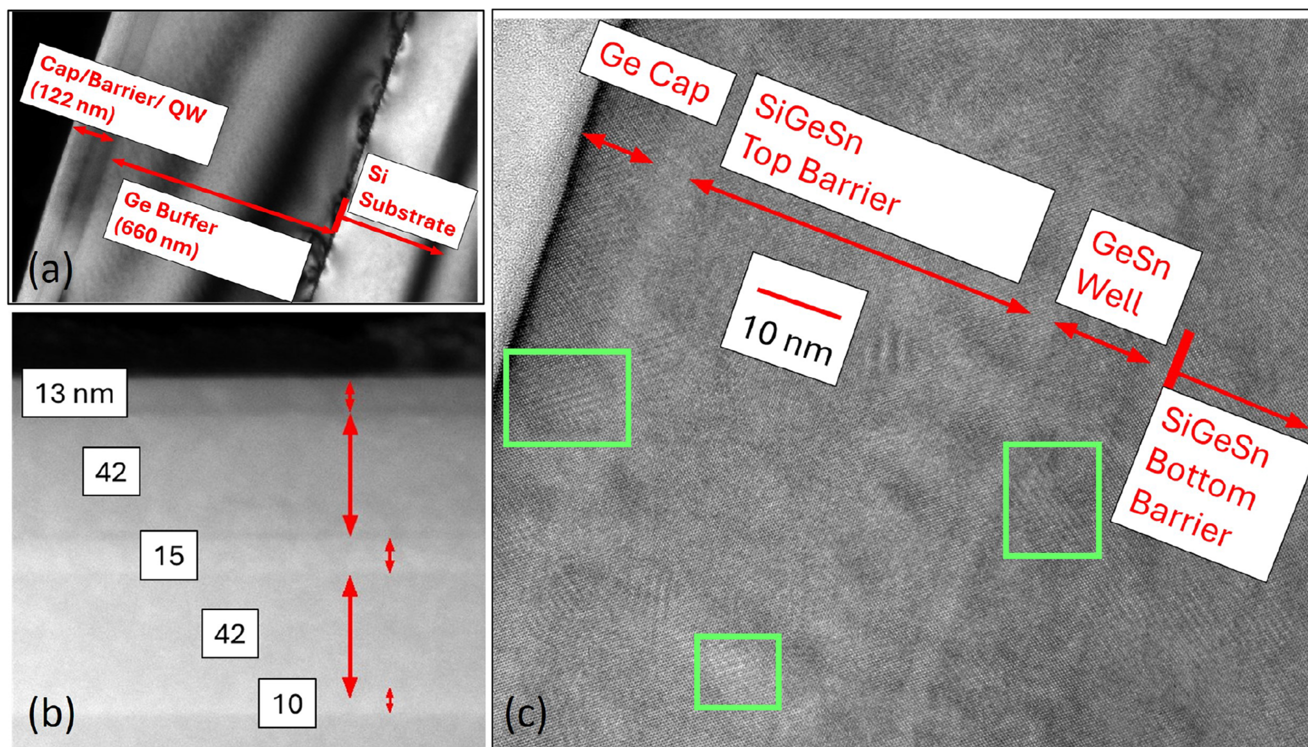

Figure 1. a) Bright field, b) High-angle annular dark-field, and c) High-resolution cross-sectional TEM images of sample 01. Examples of 30°/60° dislocations are enclosed by green boxes.

barrier layer may impact the atomic ordering in the GeSn QW grown on top of it.

2.1.3. Photoluminescence

PL spectra under various excitation conditions were compared in an earlier work.[39] The most relevant results are summarized here. The SiGeSn barriers provide type-I band alignment with the GeSn well and enhance carrier confinement. Under a 1550 nm pump laser at 10 K, the GeSn/SiGeSn heterostructure consisting of a ~10 nm GeSn QW and two 40 nm SiGeSn barriers shows a direct emission peak at 2127 nm. The peak intensity exceeds that of a GeSn bulk sample with the same ~90 nm total thickness by more than 10 % with a 1550 nm pump laser and 30% with a 532 nm pump laser. The increased intensity can be attributed to a barrier height of 284 meV in the GeSn quantum well at the Γ point in the conduction band. At low temperatures, photon-excited electrons are confined in the GeSn active layer by the SiGeSn barriers and have a higher probability of radiative recombination in the direct-bandgap transition, resulting in a higher intensity peak than the GeSn bulk sample, which has weak carrier confinement by the Ge buffer.

2.2. Electrostatics and Transport

A color-coded cross-sectional illustration of the Hall bar used in our transport experiments is shown in **Figure** 3a and an optical microscope image is shown in Figure 3b. The channel is 800 μm long and 40 μm wide. A schematic cross-section of the layers is shown in Figure 3. The pure Ge cap layer of the device was partially consumed during processing and is less than the 10 nm of the original heterostructure.

2.2.1. Current- and Capacitance–Voltage Characteristics and Qualitative Electrostatics

Small-signal drain-source current and gate-contact capacitance, as a function of gate-voltage, are shown in **Figure 4**. The raw data included a 79.0 nF/cm^2 parasitic capacitance from the measurement apparatus. This parasitic capacitance has been subtracted from the displayed data, so that the minimum capacitance is zero and is consistent with capacitance–voltage (C-V) measurements using shielded coax cables, causing the parasitic capacitance to approach zero.

There are three plateaus in capacitance, labeled as C_1, C_2, C_3 in Figure 4b. From the structure and the dielectric constants of the semiconductor layers, we determine that C_1 is the capacitance of the Al_2O_3 layer, C_2 is the capacitance of the Ge cap and top SiGeSn barrier in series with C_1, and C_3 is the capacitance of the well, bottom SiGeSn barrier, and Ge buffer, in series with C_2. There are up to four conductive layers within these effective capacitors. Listing them in order from top to bottom: 1) metal gate, 2) Ge cap and the top of the top barrier or effectively the Ge/SiGeSn cap, 3) GeSn quantum well, and 4) interface between 700 nm germanium buffer and silicon substrate. Only the metal gate is

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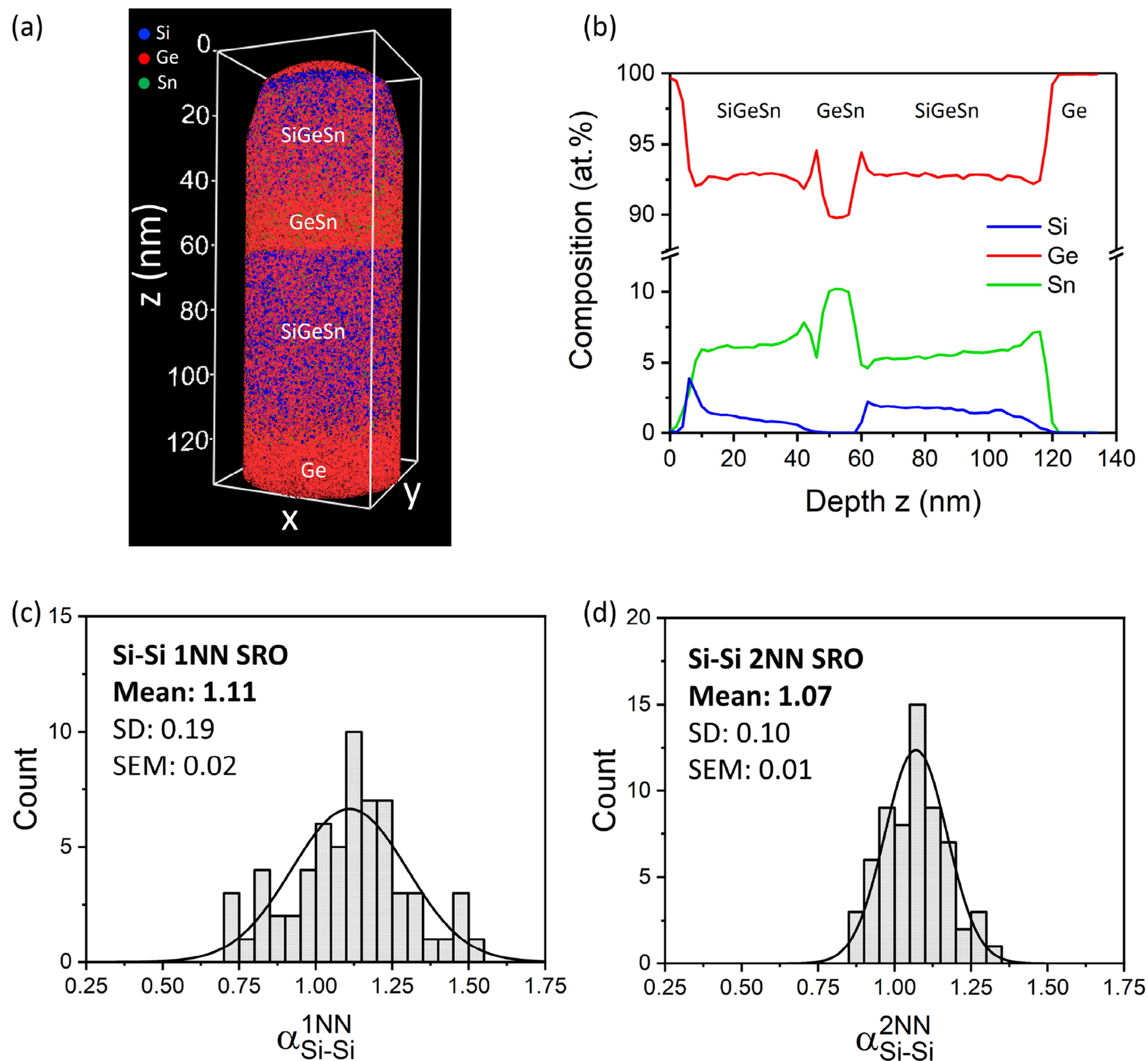

Figure 2. a) APT data of sample 01. b) Composition profile derived from (a). c) Histogram of α^{1NN}_{Si-Si} in SiGeSn barriers. d) Histogram of α^{2NN}_{Si-Si} in SiGeSn barriers. Overall, 63 nanocubes were analyzed. The error bars of mean α^{1NN}_{Si-Si} and α^{2NN}_{Si-Si} represent the standard error of mean (SEM), which equals the standard deviation (SD) divided by the square root of the number of the nanocubes analyzed.

conductive at all gate voltages. The other three layers have a mobile charge only under certain gate voltages and sweep directions. The measured and modeled values of C_1, C_2, C_3 are given in **Table 1**. Previously, we measured the dielectric constant of ALD-grown Al_2O_3 to be 7.5.[49] Knowing the dielectric constant and the 90 nm thickness of Al_2O_3, we obtain the value of the capacitance of the oxide shown in column three of the row for C_1, which agrees well with the measured value in column four. The experimentally measured values of C_2 and C_3 agree well with the modeled values obtained from the measured layer thicknesses and linear interpolation of the dielectric constants of the three constituents: Si (11.7), Ge (15.8), and Sn (24).[50,51]

To understand the capacitance- and current-voltage (I-V) trends, we created qualitative band diagrams, based upon the

Table 1. Layer Capacitances.

Effective capacitance	Capacitance by linear interpolation of known dielectric constants (nF/cm^2)	Capacitance from Figure 4b (nF/cm^2)
C_1	73.8	74[48,52]
C_2	58.6	58.3
C_3	14.1	14

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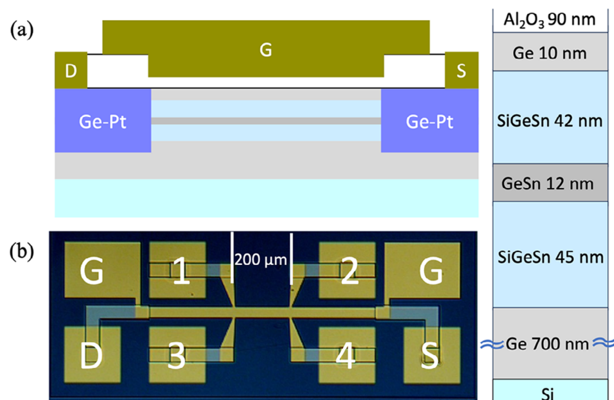

Figure 3. a) Illustrative sample cross section, with labeled drain (D), gate (G), and source (S). (Right) Cross-sectional schematic with layer thicknesses from gate oxide to the substrate, not to scale. b) Optical microscope image of the Hall bar, identifying the gate, source, drain, and Hall contacts 1-4. The longitudinal segment for Hall measurements is 200 µm long between the parallel white lines. All pads except for the gate electrically contact the semiconductor stack through Ge-Pt. Hidden in this top view, the gate and Ge-Pt are electrically isolated from one another by the oxide layer, as sketched in cross-section in (a).

current and capacitance measurements (Figure 4 and Table 1), shown in **Figure 5**, with a schematic of the relevant layers and thicknesses in the upper left. These band diagrams are qualitative illustrations intended to provide physical insight into the charge distribution and carrier accumulation at different bias conditions. The capacitance measurements in this work provide quantitative validation of the layer structure. Specifically, the excellent agreement between measured and calculated capacitance values in Table 1 (within 2% for all three capacitance plateaus) confirms our understanding of the dielectric layers and charge distribution, supporting our qualitative interpretation of carrier accumulation shown in the band diagrams.

Figure 5 presents the complete progression of charge states through a full gate voltage cycle, illustrating how the non-equilibrium trapped charge may evolve during device operation. The sequence a to d shows the downsweep (off to on) while d to g to a completes the hysteretic cycle on the upsweep.

At 10 V (Figure 5a and bias point A in Figure 4), the device is fully off, very little current flows and the capacitance is

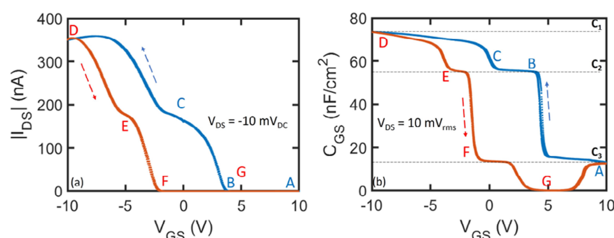

Figure 4. a) Drain current and b) capacitance as a function of V_{GS}. The blue curve (ABCD) corresponds to a voltage sweep from positive (off) to negative (on). Sweep directions are also indicated by arrows. The red curve (DEFGA) corresponds to a voltage sweep from negative (on) to positive (off). The bias points (ABCDEFG) are (10,4,0,–10,–5,–2,5)V. The values of the three plateaus of capacitance, C_1, C_2, C_3, are compared with theoretical values in Table 1.

12.6 nF/cm^2. At this bias point, we infer from the current–voltage measurements that there are no mobile carriers for lateral transport and from (C-V) that the relevant interface is between the Si substrate and Ge buffer. The charge accumulating at the Ge/Si interface has a low enough resistance to contribute to the finite capacitance at 1 kHz, but a high enough resistance that it is not seen in lateral transport. Here, we expect electron traps are filled.

When V_{GS} decreases to 4 V (Figure 5b and bias point B), the trapped charge at the Si/Ge interface is slow to respond, maintaining a non-equilibrium negative charge distribution. There is also negative trapped charge at the oxide/semiconductor interface, which behaves as an effective negative gate voltage resulting in a shift of the threshold voltage. The shift in the threshold voltage allows holes in the well even with a positive gate voltage. Therefore, mobile holes enter the GeSn well at 4 V (bias point B) and lateral drain-source current starts to flow. The capacitance barely increases on the downsweep from 10 to 4 V, until it jumps to a new plateau of 55 nF/cm^2 at 4 V (bias point B), justifying the observed jump in lateral drain-source current at bias point B and the proposed band diagram.

Reducing the voltage further to 0 V (Figure 5c and bias point C), the drain-source current increases to 200 nA. At this point, most of the current flows through the GeSn well. Going to more negative V_{GS}, the Ge/SiGeSn cap channel starts to fill, as revealed by the beginning of the rise in capacitance. The current in the Ge/SiGeSn cap starts to flow when V_{GS} decreases to about –2 V.

Sweeping the voltage down to –10 V (Figure 5d and bias point D), the capacitance increases to 73.6 nF/cm^2, while the drain-source current increases to 350 nA. While the device is fully on, with parallel currents flowing through both the well and the Ge/SiGeSn cap, we note that between –5 and –10 V, the slope changes sign, meaning the transconductance becomes negative as in **Figure 6**b. This is explained by magnetotransport measurements (Section 3.2) where we observe that Ge/SiGeSn cap and upper barrier have more charge than the well, as evidenced by **Figure 7**a and 8a, but lower mobility (Figure 7b and 8b), resulting in the decrease in the effective mobility (Figure 7b). Here, we also expect that hole traps at the oxide/semiconductor interface and in the oxide are filled and that there are hole traps at the Si/Ge interface.

The residual trapped positive charge shifts the threshold gate voltage to a more negative value, causing hysteresis in both capacitance and current where the values on the downsweep differ from the values on the upsweep. Relative to the upsweep, the threshold voltage is about 5 V higher on the downsweep. Similarly, the capacitance is higher on the downsweep. Nevertheless, the capacitance plateaus have the same (vertical) values in both directions; only the (horizontal) voltages shift.

Analyzing the downsweep, we we start at V_{GS} = –10 V (Figure 5d and bias point D) and sweep to more positive voltages. The capacitance decreases and then reaches a plateau of 55 nF/cm^2 at –5 V (Figure 5e and bias point E), where the 175 nA current has an inflection point. Here the Ge/SiGeSn cap is depleted of mobile charge, as seen by a decrease in current and capacitance, but current continues to flow through the well.

Increasing the voltage to –2 V (Figure 5f and bias point F), the capacitance drops precipitously to 12.6 nF/cm^2, and the device has turned off with negligible lateral current flowing. The device

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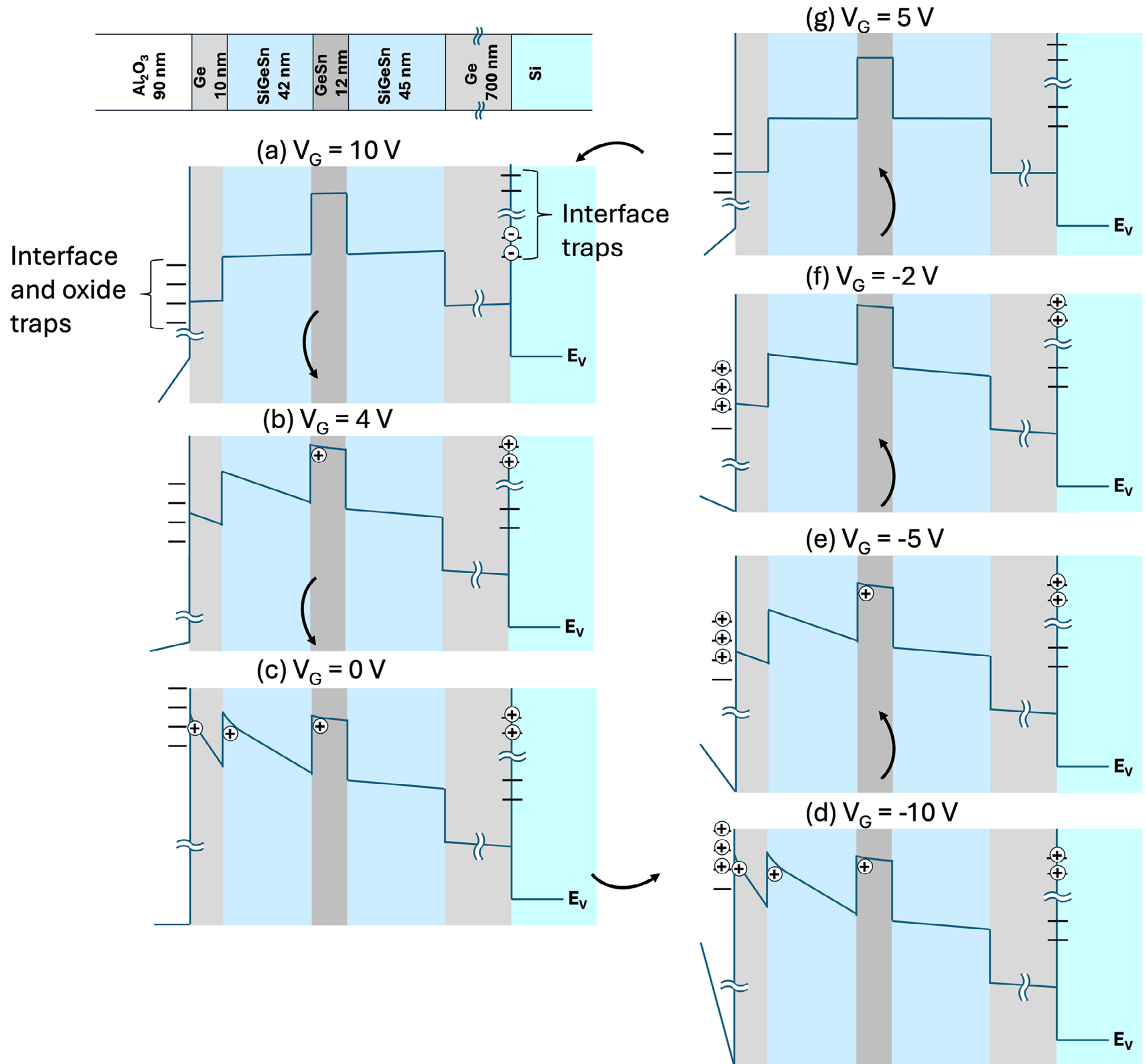

Figure 5. Qualitative valence band energy diagrams and charge distribution at each of the bias points A-G in Figure 4. The colored bands correspond to the layer structure shown in the top left. The progression from (a) to (g) illustrates how trapped charge at various interfaces influences the threshold voltage and creates the observed hysteresis in transport and capacitance measurements.

is off at this bias, even though it was on during the upsweep, because of non-equilibrium positive charge at the Si/Ge interface, which makes it energetically favorable for mobile holes to leave the well. This trapped charge also results in the measured non-zero capacitance.

Increasing the voltage from −2 V to +2 V, the capacitance stays constant, but then drops to a plateau of zero, centered at 5 V (Figure 5g bias point G). The vanishing of capacitance implies the stack lacks charge that can respond fast enough for capacitance measurement. Increasing the voltage to 10 V (bias point A), the capacitance rises again to 12.6 nF/cm^2. The increase in capacitance between G and A is due to negative charge accumulation at the substrate interface (Figure 5a).

Large-signal DC current and transconductance, $g_m = \frac{\partial I_{DS}}{\partial V_{GS}}$, are shown in Figure 6a,b,c, for the gate voltage swept from positive to negative such that the device goes from off to on. The transconductance shows two peaks, at gate voltages 4 V and −3 V, corresponding to the well and to the Ge/SiGeSn cap, respectively. The threshold voltages are more positive in Figure 6a,b,c than when the gate voltage is swept in the opposite direction in Figure 6d,e,f, due to the influence of trapped charge, as discussed previously. On the upsweep, the transconductance shows two peaks, at gate

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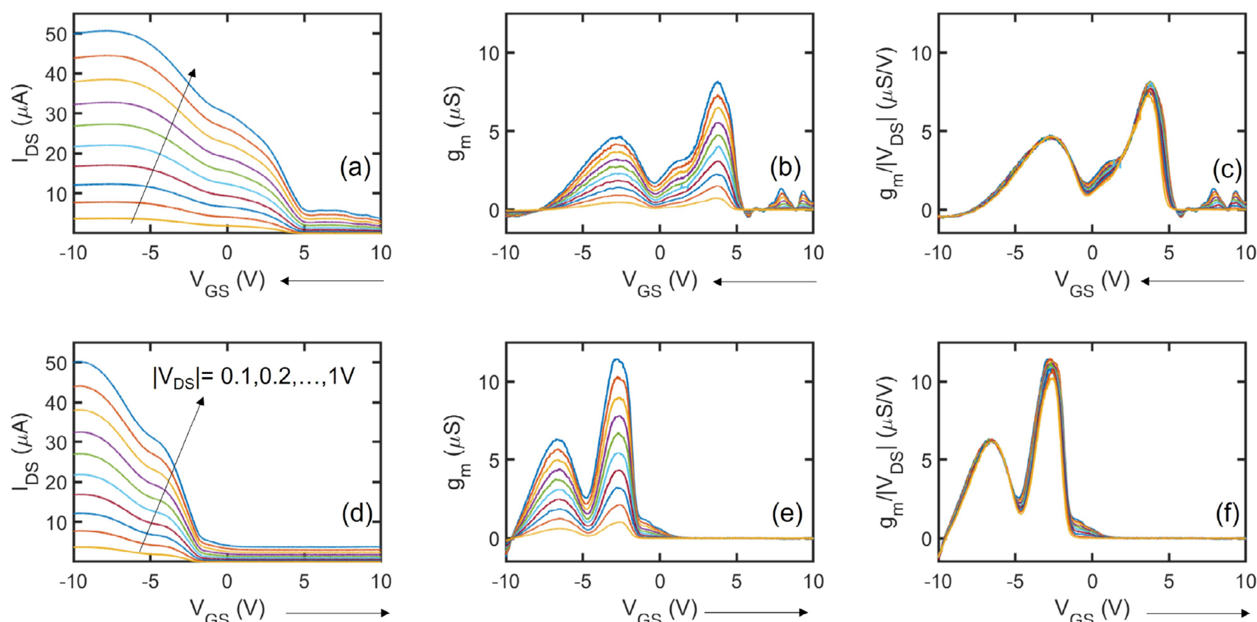

Figure 6. a) Drain current, b) transconductance, and c) transconductance divided by drain voltage as a function of V_{GS}, swept from high to low. From the bottom curve to the top curve, $|V_{DS}|$ increases from 0.1 to 1 V in increments of 0.1 V. Curves (d), (e), (f) have V_{GS} swept from low to high. The presence of positive trapped charge shifts the threshold voltage more negative relative to (a), (b), (c).

voltages –7 V and –3 V, corresponding to charge transport in the Ge/SiGeSn cap and the well, respectively. The maximum value of the transconductance is 8 μS on the downsweep and 11 μS on the upsweep. Similarly, the maximum values of g_m/V_{DS} are 8 μS/V and 11 μS/V, respectively. When both the well and the cap are populated, the transconductance is linear in V_{DS} (Figure 6c,f). Sub-threshold, the current and transconductance are nonlinear functions of V_{DS}. This may be due to modulation of the germanide-GeSn Schottky barrier height as previously reported for Ge Schottky barrier metal-oxide-semiconductor field-effect transistors (MOSFETs).[49]

2.2.2. Magnetotransport

The effective Hall hole density, p_H, and mobility, μ_H, as a function of V_{GS} are measured at 2 K and shown in Figure 7a,b. These quantities were obtained from magnetotransport measurements with a sinusoidal drain-source voltage of 5 mV_{rms}, with the B-field scan ranging from −0.5 T to +0.5 T. Downsweeping the gate voltage, starting from a high of +10 V, the carrier density starts to be measurable at +4 V. As V_{GS} decreases, the carrier density rises until it has an inflection point at –2 V. The slope steepens and then levels off as V_{GS} is swept down to –10 V. On the voltage upsweep, the inflection point occurs at a more negative voltage, relative to the downsweep. The carrier density stops being measurable at about –3 V. The mobility peaks at a gate voltage of –1 V on the downsweep, but at –6 V on the upsweep. The blue and red lines in Figure 7b do not coincide for most gate voltages, but they coincide near –10 V.

We acknowledge that the significant hysteresis observed in our *I–V* and *C–V* measurements (Figure 4) indicates a high density of interface states and/or mobile charges in the dielectric layer. While this hysteresis affects the gate voltage required to achieve

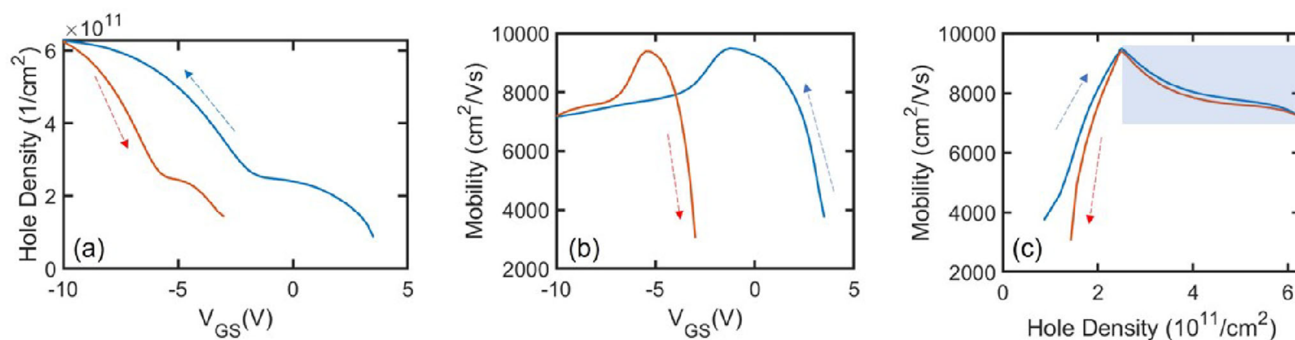

Figure 7. a) Hole density vs. V_{GS}. Dashed-line arrows indicate the direction of voltage sweep. b) Mobility vs. V_{GS}. c) Mobility vs. density. The shaded area corresponds to an equilibrium charge distribution in the semiconductor stack. Measurements were performed at T = 2 K. In all cases, the experimental data (both density and mobility) are extracted from Hall (magnetotransport) measurements.

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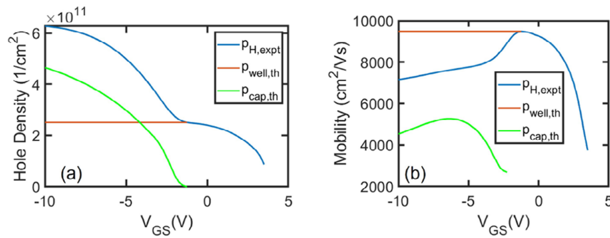

Figure 8. a) Hole density vs. V_{GS}. The theoretical hole density in the well $p_{well,\,th}$ is assumed to saturate at the value of p_H at the inflection point. b) Mobility vs. V_{GS}. The theoretical mobility in the well $\mu_{well,\,th}$ is assumed to saturate at the maximum value of μ_H. Only the voltage downsweep data are shown. In all cases, the experimental data (both density and mobility) are extracted from Hall (magnetotransport) measurements.

a given carrier density, it does not directly impact the Hall mobility extraction, which is determined from magentotransport measurements of the actual carriers present in the channel. At all but the most negative voltages, the trapped charge in the oxide is out of equilibrium and hysteretic as discussed previously, and the mobility depends on the voltage sweep direction. However, between –7 V and –10 V, the mobility is approximately independent of sweep direction, indicating equilibrium charge distribution in the semiconductor stack and near the oxide/semiconductor interface.[53] When the mobility is plotted as a function of carrier density (Figure 7c), the hysteresis nearly disappears, especially at high carrier densities. Our record mobility of 9000 cm^2/Vs corresponds to a carrier density of approximately $2.5\times 10^{11}/cm^2$, where the hysteresis largely disappears when plotted versus carrier density (Figure 7c). This indicates that the peak mobility value represents the intrinsic transport properties of the quantum well rather than an artifact of the hysteretic gate response.

The experimentally measured p_H and μ_H may be expressed in terms of the unknown hole concentrations and mobilities in the quantum well (p_{well}, μ_{well}) and the Ge/SiGeSn cap (p_{cap}, μ_{cap}):

$$p_H = \frac{(p_{well}\mu_{well} + p_{cap}\mu_{cap})^2}{(p_{well}\mu_{well}^2 + p_{cap}\mu_{cap}^2)} \tag{1}$$

$$\mu_H = \frac{p_{well}\mu_{well}^2 + p_{cap}\mu_{cap}^2}{p_{well}\mu_{well} + p_{cap}\mu_{cap}} \tag{2}$$

To solve for the four unknowns using these two equations, we assume that for voltages above about –1 V, near the inflection point of p_H, the cap channel is off, so that $p_{cap} = 0$, $\mu_{cap} = 0$, $p_{well} = p_H$, and $\mu_{well} = \mu_H$. This is the first guess in the iteration that leads to a self-consistent solution when all four equations are used.[53] The voltage at the inflection point is close to the voltage at bias point C in Figure 4. The assumption that p_{cap} equals zero at inflection point C is consistent with the measured capacitance there, corresponding to a dielectric region of oxide, Ge/SiGeSn cap, and top barrier. The inflection of the (total) current at C may be understood as the well charge reaching maximum capacity before the cap starts to fill. p_H, p_{well}, and p_{cap} are plotted together in Figure 8a. μ_H, μ_{well}, and μ_{cap} are plotted together in Figure 8b. At large negative voltages, the carrier density in the cap exceeds the carrier density in the well. The mobility in the well always

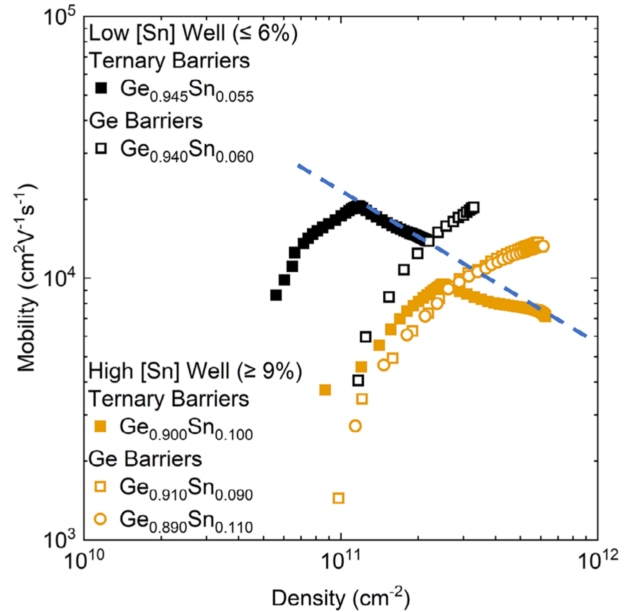

Figure 9. Mobility comparison of five different samples: $Ge_{0.945}Sn_{0.055}/Si_{0.03}Ge_{0.93}Sn_{0.04}$, $Ge_{0.9}Sn_{0.1}/Si_{0.017}Ge_{0.927}Sn_{0.056}$, $Ge_{0.94}Sn_{0.06}$/Ge, $Ge_{0.89}Sn_{0.11}$/Ge, and $Ge_{0.91}Sn_{0.09}$/Ge.[15] The legend identifies the stoichiometry in the well, and the composition of the barrier: pure Ge or ternary. The dashed line qualitatively shows the limiting trend of surface-dominated scattering in the Ge/SiGeSn cap. In all cases, the experimental data (both density and mobility) are extracted from Hall (magnetotransport) measurements.

exceeds the mobility in the cap. The mobility of the Ge/SiGeSn cap adjacent to Al_2O_3 is expected to be lower than the mobility of a quantum well adjacent to epitaxially grown smooth barriers, because of oxide surface roughness,[54–56] the extremely thin Ge cap layer, and alloy scattering in the SiGeSn ternary alloy barrier. It is the combination of both low mobility and increasing carrier density in the cap that makes the apparent mobility of the device decrease at large negative voltages.

2.3. Comparison of GeSn Quantum Wells

A comparison of the mobilities of the GeSn QW samples with SiGeSn barriers studied in this work to the GeSn QW samples with Ge barriers reported in our previous work[15] is shown in **Figure 9**. We first note that the samples with a SiGeSn barrier show a clear drop in mobility at high carrier densities. The decrease in mobility at higher concentrations has two possible causes (see also Figure 8). First, in addition to the well, at high carrier densities, current also flows through the thin Ge cap and SiGeSn barrier layer, which has strong alloy scattering. Additionally, it is known that the mobility of a germanium MOSFET decreases at high carrier densities due to surface roughness scattering.[49] In the case of the germanium MOSFET, the peak mobility is approximately 500 cm^2/Vs at a density of $2.5\times 10^{12}/cm^2$ and is roughly consistent with the observed trend here.

For the two samples with Sn content around 6%, at *low carrier densities*, the mobility is higher with the SiGeSn barrier than it is with Ge. The peak low-density mobility of the sample with the

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SiGeSn barrier is 19 000 cm^2/Vs, while at the same carrier density the mobility of the sample with the Ge barrier is more than four times smaller. For the samples with Sn content greater than 9%, the mobility of the sample with a SiGeSn barrier is also higher at *low carrier densities*, although the difference is not as drastic as in the former case. An improved low-density mobility is desired for QIS applications.[40] We also note that the mobilities of the samples with low Sn content are in general higher than the mobilities in the samples with higher Sn content.

The difference in mobility in the low-density range is likely related to the alloy composition in the QW and alloy scattering. There are at least two possible causes for this difference: 1) Background impurity and structural defect levels and/or 2) Atomic ordering in the barrier. For 1) the synthesis conditions are quite different between the two sets of samples grown by different growers. The variation in synthesis conditions could lead to differences in impurity and defect levels, which are also affected by alloy content. Higher impurity and defect levels can scatter carriers more effectively, reducing mobility. Whereas for 2), the atomic ordering in the barrier could play a role in the growth of the GeSn QW, which in turn affects the carrier mobility. We have evidence of SRO, in Figure 2, in the SiGeSn layers of the samples studied in this work. During chemical vapor deposition, for a thin GeSn quantum well, it is plausible that the SRO of the bottom SiGeSn barrier can transfer to the GeSn well, creating a templating effect through epitaxial registry, where the locally ordered Si–Si pairs in the SiGeSn barrier create a non-random template for subsequent Ge and Sn atom positions during GeSn growth. Ordered alloys have higher mobilities than disordered alloys[57,58] because of reduced alloy scattering. Therefore, a $Ge_{1-x}Sn_x$ QW with higher SRO has a higher mobility than a $Ge_{1-x}Sn_x$ QW with lower SRO, even though the macroscopic ratio of constituents is the same. Given the observations and the presence of SRO in the SiGeSn layers, it is likely that atomic ordering in the barrier plays a significant role in the observed difference in mobility.

3. Conclusion

In summary, we have experimentally demonstrated that the mobility of a cryogenic GeSn/Ge heterostructure MOSFET may be improved by replacement of the Ge barrier with SiGeSn. The high mobility indicates a high-quality well-barrier interface, which would reduce sources of noise for semiconductor-based qubits and single photon emitters. This is a positive development for the future of GeSn based quantum devices, with monolithic integration of quantum optical and quantum electronic function.

4. Experimental Section

Hall Bar Fabrication: The as-received epitaxially grown sample was cleaned with a six-step process 1) Acetone, methanol, then isopropanol rinse 2) 5-minute oxygen plasma exposure at 150 °C 3) Soak in a 1:3 volume:volume solution of HCl:H_2O for 5 minutes 4) Rinse in de-ionized water 5) Soak in a buffered oxide etch (BOE, 6:1 volume ratio of 40% NH_4F in water to 49% HF in water) for 1 minute 6) Rinse in de-ionized water. Immediately following cleaning, a 2 nm thick aluminum oxide (Al_2O_3) layer was deposited for passivation using atomic layer deposition (ALD) at 150 °C. After passivation, the sample was exposed to oxygen plasma for two minutes. Then, ohmic contact was made to the quantum well using platinum germanide. The platinum germanide process used standard photolithography to create a photoresist mask exposing Al_2O_3 in regions where the germanide was desired. Then, a 20-second dip in BOE etched down to the Ge-cap. Immediately after the BOE dip, 100 nm of platinum was deposited by evaporation and patterned by lift-off. The germanide was then formed by a vacuum anneal at 250°C for 3 hours. The annealing promotes reaction between platinum and germanium, creating ~300 nm deep platinum germanide (Ge-Pt), necessary for the electrical contacts.[49] Between Pt metal deposition and the germanide anneal, the sample was patterned for mesa etching, necessary for electrical isolation, and etched with a target depth of 100 nm, sufficient to etch past the quantum well. Using the same ALD process, 90-nm of Al_2O_3 was deposited forming the gate dielectric layer. After depositing the gate dielectric, the sample was exposed to oxygen plasma for 5-minutes. Standard photolithography was used to create a photoresist mask for vias to the source and drain. The vias were formed with a 205-second dip in BOE and filled with a 5 nm Ti adhesion layer followed by 90 nm Au to contact the Ge-Pt. Bond pads and the gate electrode were created with a blanket layer of 5 nm/90 nm Ti/Au and a back etch using standard photolithography and ion milling. Finally, the sample was soaked overnight in acetone to remove the photoresist mask.

Electrical Characterization: To perform electrical characterization, the device was wire bonded to a printed circuit board and measured in a variable-temperature system with a base temperature of 2 K. Measurements were performed at 2 K to freeze out unintentional current leakage paths and evaluate the material at cryogenic temperatures relevant for quantum information sciences. For Hall measurements, standard lock-in techniques at 13 Hz were employed, with the DC gate voltage supplied by a Keithley 2400 or 2401 source-measure unit. For large-signal DC I-V characterization, source-measure units were used. CC-V measurements were performed with an Agilent 33500B arbitrary waveform generator (AWG) and Fempto DHPCA-100 transimpedance amplifier, using an AC excitation of 10 mV_{rms} at 1 kHz. The AWG has a total (AC + DC) voltage range of +/−10 V.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflicts of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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