

Nonvolatile Electrochemical Memory at 600 °C Enabled by Composition Phase Separation

Jingxian Li^{*1}, Andrew J. Jalbert¹, Sang Yong Lee¹, Leah S. Simakas¹, Noah J. Geisler¹,
Virgil J. Watkins¹, Laszlo A. Cline¹, Elliot J. Fuller², A. Alec Talin², Yiyang Li^{*1}

¹Materials Science and Engineering, University of Michigan, Ann Arbor, MI, 48109, USA

²Sandia National Laboratories, Livermore, CA, 94550, USA

*Corresponding authors: jxli@umich.edu; yiyangli@umich.edu

Lead contact: Yiyang Li; yiyangli@umich.edu

Contact information:

Jingxian Li, jxli@umich.edu

Andrew Jalbert: jalberta@umich.edu

Sangyong Lee: sangylee@umich.edu

Leah Simakas: lsimakas@umich.edu

Noah Geisler: geislern@umich.edu

Virgil J. Watkins: virgiljw@umich.edu

Laszlo Cline: lzcline@umich.edu

Elliot J. Fuller: ejfull@sandia.gov

A. Alec Talin: aatalin@sandia.gov

Yiyang Li: yiyangli@umich.edu

Summary

CMOS-based microelectronics are limited to ~150°C and therefore not suitable for the extreme high temperatures in aerospace, energy, and space applications. While wide bandgap semiconductors can provide high-temperature logic, nonvolatile memory devices at high temperatures have been challenging. In this work, we develop a nonvolatile electrochemical memory cell that stores and retains analog and digital information at temperatures as high as 600 °C. Through correlative scanning transmission electron microscopy, we show that this high-temperature information retention is a result of composition phase separation between the oxidized and reduced forms of amorphous tantalum oxide. This result demonstrates a memory concept that is resilient at extreme temperatures and reveals phase separation as the principal mechanism that enables nonvolatile information storage in these electrochemical memory cells.

Introduction

Conventional Si-based digital electronics are typically limited to 150°C due to the rise in the intrinsic carrier concentration with temperature¹. This limitation precludes high-temperature needs² including in aerospace and automotive engines (150-600°C), interplanetary exploration such as Venus (550°C), and the extraction of petroleum and geothermal energy from deep wells (300-600°C)¹. Logic and memory form the foundation for modern computing. While high-temperature logic can be developed using wide bandgap semiconductors like Silicon Carbide (SiC)^{3,4} and Gallium Nitride (GaN)⁵, as well as emerging technologies like carbon nanotubes⁶, the development of memory units for such extreme temperatures has been more challenging. Presently, the only re-writeable memories^{7,9} that have retained nonvolatile information above 500°C are nanogap resistive memory⁸ and nitride-based ferroelectric memory^{10,11}; these emerging technologies exhibit limitations including large cycle-to-cycle variations, destructive read, and/or high switching voltages.

Electrochemical Random-Access Memory (ECRAM) has recently emerged as a promising solution for analog computing¹²⁻¹⁶. ECRAM is a three-terminal memory device that stores and switches information through ion migration and the resulting change in valence and electronic conductivity. ECRAM research primarily focused on three types of ions: Li⁺¹⁷⁻²¹, H⁺²²⁻²⁶, and O²⁻²⁷⁻³⁷; other ions like Cu⁺³⁸ and Mg²⁺³⁹ have also been studied. Oxygen-based ECRAM operates by electrochemically transporting oxygen ions (or vacancies) between two mixed ionic and electronic conducting (MIEC) metal oxides with a solid electrolyte. This mechanism allows ECRAM to switch resistance states by modulating the oxygen concentration in the MIEC metal oxides. Early demonstrations of oxygen ion ECRAM based on titanium²⁸ or tungsten²⁷ oxides achieved a high density of analog states but suffered from poor state retention times (<1 day at room temperature). Recently, it was shown that tungsten oxide-based ECRAM can yield ~24 hours of retention at 200°C under short circuit⁴⁰, which projects to over 10 years at 85°C. However, this device was constructed on single-crystal yttrium stabilized zirconia (YSZ) crystal substrate and therefore not CMOS compatible. Moreover, there is no clear pathway for operations above 200 °C.

In this work, we developed a high-temperature stable ECRAM device utilizing amorphous TaO_x deposited on a Si/SiO₂ substrate that is capable of recording and retaining binary and multi-level analog conductance states at temperatures up to 600 °C. Importantly, we obtain over 24 hours

of retention at short circuit at 600°C, a notable advancement in the resilience of electrochemical memory devices. We propose that these findings are a result of amorphous phase separation between the Ta and TaO_{1.9}^{41,42} which have been shown to facilitate information retention in TaO_x-based resistive memory devices⁴². Our correlative transmission electron microscopy shows clear evidence of this phase separation. Our results demonstrate a promising path towards the realization of high-temperature analog and binary resistive memory.

Results

TaO_x-based ECRAM as High-Temperature Nonvolatile Binary Memory

The structure of our TaO_x-ECRAM cells consists of a 20 nm reservoir layer of tantalum, a 140 nm electrolyte layer of yttria stabilized zirconia (YSZ) electrolyte, and a 20 nm channel layer of amorphous oxygen-deficient tantalum suboxide (TaO_x) deposited on SiO₂ (500 nm)/Si substrates using sputtering (Fig. 1a, Fig. S1). Three Pt current collectors are sputtered using shadow masks to serve as the gate, source, and drain electrodes. Finally, a passivation layer of SiN_x is deposited to protect the tantalum oxide from moisture and oxygen in the environment.

We switch this device by applying either a positive or a negative gate voltage (V_G), typically +2V to increase (SET) or -2V to decrease (RESET) the channel conductance. This applied electrochemical voltage moves oxygen ions between the gate and the channel, which change the channel conductance. The channel conductance depends on the Coulombs of ions transferred, which is given by the time integral of the current; this makes the channel conductance strongly hysteretic and therefore dependent on the voltage applied over time. As a result, ECRAM's switching mechanism is different from that of a three-terminal field-effect transistor, where the channel current depends on the presently applied gate voltage without substantial hysteresis. During retention measurements, we ground the gate by applying 0 V, short-circuiting it to the channel. No switch or selector was used in these experiments. All fabrication was conducted at room temperature with a 1 hour anneal 400°C to improve the crystallinity of the YSZ but still maintain thermal compatibility with back-end-of-line processes. More details are in the experimental section.

We initially assess the binary switching behavior. Fig. 1b illustrates the SET process, showcasing a >100 on/off ratio differentiating between the high resistance state (HRS) and low resistance state (LRS) with $\pm 2V$ for 1 second at $350^{\circ}C$. This SET/RESET switching is reproducible with minimal cycle-to-cycle variation (Fig. 1c). Moreover, the write endurance exceeds 10000 pulses at $400^{\circ}C$ (Fig. 1d). The read speed is as short as $1 \mu s$, while the read endurance exceeds 10^6 pulses (Fig. S2). Fig. S3 shows that resistance switching could be effectively obtained across a broad temperature range of $200^{\circ}C$ to $600^{\circ}C$, rendering this technology adaptable for diverse high-temperature applications. To assess the temperature-dependent switching, we further conducted a comprehensive examination of temperature's influence on switching behavior by utilizing a consistent $2V$, $1s$ pulse across a temperature span from $300^{\circ}C$ to $550^{\circ}C$ (Fig. S4). Our findings reveal that the highest on/off ratios (>100) are obtained for temperatures ranging between $350^{\circ}C$ and $400^{\circ}C$ (Fig. S5). However, at temperatures below $300^{\circ}C$, the sluggish oxygen diffusivity in our metal oxides impedes sufficient ion migration needed for higher on/off ratios. At temperatures above $450^{\circ}C$, the HRS conductance increases due to an increase in the electronic conductivity of TaO_2 with temperature, and thus reduces the on/off ratio. The overall switching speed is fairly slow due to the high Arrhenius activation energy of oxygen ($>1 eV$); however, as seen in Fig. S3, the speed increases at higher temperatures due to the increased oxygen mobility with higher thermal energies²⁸.

We tested the retention of the device under short circuit at temperatures between $400^{\circ}C$ to $600^{\circ}C$. These results show less than 12% change in the conductance after 24 hours over these temperatures (Fig. 1e, Fig. S6). Fig. 1f shows a comparative analysis of the retention times between our TaO_x -ECRAM and other high-temperature memory technologies (Fig. 1f). At $600^{\circ}C$, our ECRAM cell has similar temperature performance to Pt-nanogap ReRAM⁸ and $Al_{0.7}Sc_{0.3}N$ ferroelectric capacitors¹⁰; a comparative analysis of these devices will be given in the discussion section. ECRAMs utilizing TiO_x ²⁸ and WO_x ⁴⁰ show substantially reduced retention compared to the TaO_x ECRAM device shown here. Likewise, filament-based ReRAM devices using similar materials⁴⁴ yield substantially lower retention compared to the TaO_x ECRAM cell (Fig. 1f). We note that these measurements were conducted in an inert Ar environment with ~ 3 ppm O_2 ; in an oxidizing, the ~ 60 nm SiN_x barrier layer is not sufficient to prevent the TaO_x layers from oxidation (Fig. S7). Additional oxygen diffusion barriers would be necessary for high-temperature operations in more oxidizing environments.

Direct Visualization of Phase Separation in TaO_x ECRAM

To shed light on the mechanism of the above resistive switching and retention behaviors in TaO_x-based ECRAM, we performed Scanning Transmission Electron Microscope (STEM) on cross-sectioned devices. Fig. 2a depicts high-angle annular dark field (HAADF) and energy dispersive spectroscopy (EDS) mapping at the Ta K edge and O K edge from a pristine Ta/YSZ/TaO₂ device. Although the EDS atomic ratios are not fully quantitative, they are consistent with a metallic Ta ion reservoir and a TaO₂ channel based on our deposition recipes. Next, we consider a device after switching to the LRS in Fig. 2b. On the channel side, we observe a ~5 nm reduced Ta-rich layer at the electrolyte/channel interface and a corresponding ~15nm oxidized TaO_x at the reservoir/electrolyte interface. These results are consistent with the migration of oxygen ions from the channel layer through the electrolyte in response to the applied electric field, ultimately reaching the Ta reservoir. The reduced Ta-rich layer at the channel is consistent with the increased conductance of the low-resistance state. Furthermore, electrical measurements of the LRS channel resistance as a function of the temperature in Fig. S8 show very little temperature dependence, consistent with a metallic Ta-rich region observed in the STEM (Fig. 2b). In contrast, the HRS shows substantial temperature dependence, which is consistent with an oxidized channel consisting of a metal oxide semiconductor or insulator shown in Fig. 2a and again later in Fig. 2d.

The increased thickness of the reservoir may be attributed to the volumetric expansion due to the oxidation of the Ta to TaO_x, while the reduced channel undergoes slight contraction due to the loss of oxygen ions. Our STEM results provide direct microscopic evidence to show the electrochemical migration of oxygen in ECRAM devices.

We next investigate retention by imaging a different LRS device after 12 hours of short circuit at 400°C (Fig. 2c). The tantalum and oxygen distribution remains essentially unchanged compared to that observed in the LRS device without this high-temperature annealing (Fig. 2b). This observation is consistent with the stability of the electrical resistance over this time (Fig. 1d). We attribute this stability to the phase separation of the tantalum and oxygen within the device, which appears to play a crucial role in retaining the chemical state and, by extension, the electrical properties under thermal stress (Fig. 1e). Specifically, within the miscibility gap, the oxygen chemical potential of all compositions of Ta and O is equal (Fig. S9), which is discussed in detail our previous work⁴². For this reason, the coexistence of oxidized and reduced layers in both the

channel and the reservoir is a stable configuration; it will not revert to a single homogeneous film over time. For the same reason, the oxygen chemical potential in the reservoir and channel are equal regardless of the thickness of the reduced Ta-rich layer in the channel. As a result, oxygen has no preference to migrate from the gate to the channel or vice versa, resulting in the retention stability of the device in Fig. 1d. In other words, the long retention of our ECRAM device at high temperatures under short circuit is enabled by the absence of any chemical driving forces to move the oxygen ions between the reservoir and channel.

In Fig. 2d, we image the high-resistance state after resetting the device. The channel composition resembles the pristine device in Fig. 2a, but with a slight increase in the Ta concentration. This likely accounts for the higher conductance seen in HRS ($\sim 3 \mu\text{S}$ at 400°C) relative to the pristine configuration ($< 0.1 \mu\text{S}$). Conversely, the HRS shows a reduced Ta layer at the reservoir-electrolyte interface and an oxidized layer above it, distinguishing it from both the pristine and the LRS state. We hypothesize that there is a net transfer of oxygen from the YSZ electrolyte to the metallic Ta reservoir during the initial heating process, thereby making the reservoir in the HRS more oxidized than in the pristine device. However, this oxidation process is expected to be self-limiting because there is a finite amount of excess oxygen in the YSZ electrolyte. Fig. S10 shows that the Ta metal conductance increases when annealed at 500°C for 100 hours. This suggests that the Ta film remains metallic over this timeframe, and the increase in the conductance is likely a result of increased crystallinity upon annealing.

To further illustrate the role of phase separation, we conduct cyclic voltammetry between the reservoir/gate and the channel (Fig. 3a). The results show clear oxidation and reduction peaks corresponding to the SET and RESET of the device. When a positive voltage is applied to the gate, the positive gate current indicates that negatively charged oxygen ions are moved from the channel to the ion reservoir. This results in the formation of a reduced Ta-rich layer in the channel, increasing the channel conductance (Fig. 3c). However, upon further increase of the voltage, the gate current decreases substantially, which most likely suggests a depletion of oxygen from the channel. A similar behavior is observed upon reversing the voltage, whereby a negative current implies that oxygen moves from the gate to the channel (Fig. 3a), reducing the channel conductance (Fig. 3b). This result is largely repeatable from one cycle to the next.

The total integrated charge is about 170 micro-Coulombs in each direction, or 5.3×10^{14} oxygen ions. With an estimated channel volume of $1.7 \times 10^{13} \text{ nm}^3$ ($500 \text{ }\mu\text{m} \times 1750 \text{ }\mu\text{m} \times 20 \text{ nm}$), our results suggest that 30 oxygen ions are transferred for every $(\text{nm})^3$ of device volume. Crystalline Ta_2O_5 has about 50 oxygen ions per $(\text{nm})^3$ based on a density of 7.8 g cm^{-3} and a molar mass of 442 g mol^{-1} . If the amorphous TaO_2 channel has a similar volume density of oxygen as bulk crystalline Ta_2O_5 , the total charge transferred in the cyclic voltammetry suggests that most of the available oxygen has been transferred between the channel and ion reservoir. In contrast, our STEM images only show a partial reduction of the channel (Fig. 2b) because the switching was only conducted for 1 second.

The cyclic voltammetry sweeps also help us understand retention mechanisms, which show clear hysteretic behavior in Fig. 3d. According to Fig. 3b, there is no electrochemical gate current at 0V, regardless of whether the channel was previously reduced (SET) or oxidized (RESET). This result indicates that there is no migration of oxygen between the gate and the channel at 0V and is consistent with the nonvolatility observed at high temperatures (Fig. 1). This result is again consistent with phase separation whereby the chemical potential of the channel and reservoir are equal, thereby resulting in no electrochemical current when the voltage equals 0. In contrast, previous cyclic voltammetry on a TiO_2 ECRAM device shows a more capacitive profile whereby there exists a substantial current at 0V (Fig. 3c). This nonzero current reverses the oxygen migration forced at positive and negative voltages, thereby resulting in a loss of information over time.

Analog Multilevel Switching

In addition to binary switching, our TaO_x -ECRAM cells exhibit analog switching characteristics, which align with the traits observed in previous room-temperature ECRAM cells¹². This device attains and sustains 100 analog states through sub-millisecond pulses at 400°C , as illustrated in Figure 4a. These properties mirror those found in other ECRAM and highlight the device's ability for analog matrix multiplications for in-memory computing. Moreover, our devices show reproducible switching consistent with previous oxygen-based ECRAM cells^{27–29,45}. Fig. 4b and Fig. S11 shows the ECRAM device manifests analog behavior across different resistance values spanning from the micro-Siemens to milli-Siemens range. This reliability and consistency

further substantiate the device's potential for dependable analog data manipulation in various computational tasks.

In probing the analog switching behavior across pulse widths ranging from 500 μs to 4 ms at 8V (Fig. S12a), we observe linear dependence of analog switching with pulse width. A similar behavior has been observed with a negative pulse (Fig. S12b). This indicates that the device's conductance can be finely tuned by altering the duration of the applied pulses. Similarly, Fig. S13 reveals that the conductance change is also linearly proportional to the pulse amplitude, consistent with previous reports in ECRAM²⁸.

Finally, we conduct data retention tests for the analog states, summarized in Fig. 4c. These tests show that the analog states ranging from 20 μs to over 800 μs maintained stable resistances after 12 hours at 400°C. The observed phase separation within our device contributes to establishment of multiple equilibrium resistance states.

Discussion

Our study presents a non-volatile ECRAM device concept based on amorphous, phase separating TaO_x, demonstrating record ECRAM state retention in both binary and analog switching modes at temperatures as high as 600°C. The high-temperature performance is substantially better than commercial floating-gate memory (<150°C). It is also significantly better than all previously reported ECRAM types, which are limited to 200°C. Its temperature performance is comparable to that of recently demonstrated nitride-based ferroelectric memory¹¹ and Pt nanogap memory⁸. Compared to nitride ferroelectric memory, TaO_x ECRAM uses lower voltages (2V vs >15V), can provide analog multi-level states, and has a higher on/off ratio (100 vs 3 at 400°C, 3 vs 1.5 at 600°C). Furthermore, its resistance information state can be “read” without disturbing the device. Compared to the nanogap memory, ECRAM has lower voltages (2V vs 6V) and analog multi-level state capability (Fig. 4), which can result in a higher density of information states. We note that these three emerging memory technologies utilize very different switching and information retention mechanisms; each device has its advantages and disadvantages, and are all viable candidates for high-temperature nonvolatile memory.

One weakness of our ECRAM cell is the high write temperatures above 250°C. For low-temperature operations, we envision that it will be necessary to integrate a localized Joule heater

as recently demonstrated for other oxygen-based ECRAM devices^{46,47}. Additionally, while the on/off ratio is diminished at 600°C, this is a result of an increased conductance of the channel layer and could be mitigated by making the channel more oxidized initially. Further research is also needed to decrease the size of the device. Recent research has successfully shown micron- and nano-sized ECRAM devices based on proton^{24,26} or oxygen ion²⁹ insertion into tungsten oxide using lithography processes. We anticipate a similar process can be used to scale the tantalum oxide devices in this work.

Our STEM and electrochemical results are consistent with an amorphous phase separation mechanism to explain the long-term retention in the TaO_x ECRAM. This design rule of using composition phase separation can also be used to engineer other types of ECRAM, such as protonic ones which have fast speed but limited retention under short circuit^{24,48}. While our previous work also postulated that phase separation enables information retention in WO_x ECRAM⁴⁰, this work both showed direct evidence of phase separation using STEM (Fig. 2) as well as much higher operations (600°C vs 200°C). Moreover, the persistent coexistence of the Ta-rich and oxygen-rich regions provides additional evidence of phase separation in amorphous tantalum oxide within the device. This characterization result is consistent with our previous Auger depth profile measurements which show that a Ta-rich and oxygen-rich bilayer film would not mix⁴²; however, unlike the previous work, the two layers in this work were electrochemically created in situ during device operation, rather than directly deposited from vapor. This work also shows how phase separation can be harnessed in three-terminal ECRAM devices for high temperature information storage, just as they can be used to store information in two-terminal resistive memory based on tantalum oxide⁴² and on lithium titanium oxide^{49,50}.

Finally, we speculate on the possible ultimate switching temperature of this device. Tantalum oxide is also known to crystallize around 650°C⁵¹; this could represent the upper temperature limit. However, if we can make ECRAM using crystalline tantalum oxide, then it could point to much higher operational temperatures. According to the Ta-O phase diagram⁵², the miscibility gap extends to the melting temperature that exceeds 1500°C. In this regime, the functionality of the other components, such as the SiN_x oxygen diffusion barrier, may limit the ultimate temperature limit.

Conclusion

We present a nonvolatile electrochemical memory that switches and retains information at 600°C for over 24 hours. Our electrochemistry and transmission electron microscopy results suggest that phase separation occurs in the amorphous tantalum oxide channel, and this phase separation is responsible for the high temperature stability of this device. This work shows new concepts that can be used to engineer nonvolatile memory for extreme environments.

Experimental Procedures

Fabrication of TaO_x ECRAM Cells

The ECRAM devices comprising thin-film YSZ were fabricated using an AJA Orion 8 DC/RF sputter system (baseline pressure <5 e-7 torr) using shadow masks on a 1 cm die of Si with 500 nm of thermal oxide (University Wafers). The first shadow mask (Fig. S1a) defines the bottom Pt electrode, which contains 5 nm of Ta adhesion layer and 20 nm of Pt. The Ta adhesion layer was DC sputtered at 100W on a 3-inch Ta target (99.95% purity; Plasmaterials Inc) under pure Ar (6N purity). The Pt layer was DC sputtered at 100W on a 2-inch Pt target (99.99% purity, AJA) under pure Ar. The sputter gas pressure was 3 mtorr.

The second shadow mask (Fig. S1b) defines the three successive oxide layers: the TaO_x channel, the YSZ electrolyte, and the Ta reservoir layer. The channel, or switching layer, consists of 20 nm of TaO_x and was DC sputtered at 100 W with the 3-in. Ta target and a sputter gas mixture of Ar (6N):O₂ (5N) at a 37:3 ratio regulated by mass flow controllers. The sputter gas pressure was maintained at 5 mtorr, with a substrate-to-target distance of approximately 15 cm. The 140 nm YSZ electrolyte was grown by RF sputtering on a 3-in. YSZ target (8 mol% Y₂O₃ in ZrO₂, 99.9% purity, Plasmaterials Inc) using a sputter power of 150 W and 5 mtorr of pure argon. The 20 nm Ta gate layer was grown by DC sputtering on a 3-in. Ta target at a sputter power of 100 W in 5 mtorr of pure argon.

The third shadow mask (Fig. S1c) was used to define the top gate contacts. It consists of 30-nm-thick gate Pt current collectors sputtered using the same process as the bottom contact, except without an adhesion layer. No additional annealing was performed during the room temperature sputtering process. Finally, for environmental protection against oxidation, a 60 nm

silicon nitride layer was deposited on the ECRAM device's channel side using plasma-enhanced chemical vapor deposition (PECVD) at 200°C in the Lurie Nanofabrication Facility via a Plasmatherm 790. The SiN_x above the current collectors were etched using reactive ion etching used a gaseous CF₄/O₂ mixture at a ratio of 95:5. The final devices are given in Fig. S1d,e. A 400°C anneal at 1 hour was conducted in inert Ar to improve the crystallinity and ionic conduction of the YSZ electrolyte.

Device Measurements

Following fabrication, the cell was tested in a six-probe Nextron MPS-Ceramic Heater CHH750 probe station, where the two channel electrodes made direct contact with Rh probes. Three of the probes were used to contact the top electrode and the two bottom electrodes. The environment was further regulated by flowing 5N ultra high-purity Ar at a controlled rate of 87 standard cubic centimeter per minute (sccm) using an Omega mass flow controller. A Swagelok check valve maintained the chamber pressure at \approx 50 torr above ambient, further preventing air backflow. Monitoring with a Zirox ZR5 oxygen sensor indicates that the oxygen gas concentration in the chamber is about 3 parts per million (ppm). Notably, the flowing Ar formed a more effective thermal contact between the heater and chip compared to testing the device in ultra-high vacuum.

Retention, cyclic voltammetry, and switching measurements for 1 second or longer were conducted using a Bio-logic SP300 bipotentiostat. For switching, we applied a +/- 2V gate pulse for 1 second or longer; for retention, we applied 0 V on the gate. To measure the channel resistance, we applied a continuous 0.01 V voltage across the channel. Switching measurements with a duration of less than 1 second were conducted using a National Instruments Data Acquisition Device (DAQ-6358) system from previous work²⁸. For switching, we applied a square wave between 2 and 8 V for between 0.8 to 50 ms. The read pulses consisted of 0.1 V pulses applied for 0.1 seconds after the write pulse. As shown in Fig. S8, the current-voltage response of the channel is largely linear, so the resistance does not depend on the applied voltage. The switching voltage and duration for each measurement are included in the figure. The read speed and endurance measurements (Fig. S2) were taken using a Keithley 4200A Semiconductor Parameter Analyzer with a Pulse Measure Unit.

STEM Measurements

STEM analyses were carried out using a Thermo Fisher Talos F200X G2, a 200 kV FEG scanning transmission electron microscope operating in STEM mode. Acquisition of STEM images and EDS data employed Velox software. STEM specimens were prepared utilizing a Thermo-Fisher Helios G4 Plasma FIB, with the final beam condition set at 12 keV 10 pA for liftout polishing.

Resource Availability

Lead Contact: Requests for further information and resources should be directed to and will be fulfilled by the lead contact, Yiyang Li, yiyangli@umich.edu

Materials Availability: This work did not generate new unique reagents or materials.

Data and Code Availability: The data that support the findings of this study are publicly available at Materials Commons 2.0 repository at <https://doi.org/10.13011/m3-pmdj-mz08>. This paper does not report original code.

Acknowledgements

The work at the University of Michigan was supported by the National Science Foundation under grant no. ECCS-2106225 and CCF-2235316, and by a Sandia University Partnership Network (SUPN) program. Part of the fabrication of the devices was conducted at the University of Michigan Lurie Nanofabrication Facility. The authors acknowledge the University of Michigan College of Engineering for financial support and the Michigan Center for Materials Characterization for use of the instruments and staff assistance. We thank Dr. Kai Sun for assistance with the TEM sample preparation and measurements.

The work at Sandia National Laboratories was supported by the Laboratory-Directed Research and Development (LDRD) program. Sandia National Laboratories is a multi-mission laboratory managed and operated by National Technology and Engineering Solutions of Sandia, LLC, a

wholly-owned subsidiary of Honeywell International Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA-0003525.

Author Contributions

J.L., A.A.T., E.J.F., and Y.L. conceived the idea. J.L. designed the experiments. J.L., A. J. J., S.Y.L., L.S., N. J. G., V. W., and L. C. fabricated ECRAM devices and performed device measurements. J.L. conducted transmission electron microscopy experiments. Y.L. supervised the project. All authors contributed to writing or revising the manuscript.

Declarations of Interest

The authors have filed a patent based on this work to the US Patent and Trademark Office, application number 18/ 775896

References

1. Neudeck, P.G., Okojie, R.S., and Chen, L.-Y. (2002). High-temperature electronics - a role for wide bandgap semiconductors? *Proc. IEEE* *90*, 1065–1076. <https://doi.org/10.1109/JPROC.2002.1021571>.
2. Cressler, J.D., and Mantooh, H.A. (2017). *Extreme Environment Electronics* (CRC Press).
3. Neudeck, P.G., Spry, D.J., Chen, L., Prokop, N.F., and Krasowski, M.J. (2017). Demonstration of 4H-SiC Digital Integrated Circuits Above 800 °C. *IEEE Electron Device Lett.* *38*, 1082–1085. <https://doi.org/10.1109/LED.2017.2719280>.
4. Kaneko, M., Nakajima, M., Jin, Q., and Kimoto, T. (2022). SiC Complementary Junction Field-Effect Transistor Logic Gate Operation at 623 K. *IEEE Electron Device Lett.* *43*, 997–1000. <https://doi.org/10.1109/LED.2022.3179129>.
5. Yuan, M., Xie, Q., Niroula, J., Isamotu, M.F., Rajput, N.S., Chowdhury, N., and Palacios, T. (2022). High Temperature Robustness of Enhancement-Mode p-GaN-Gated AlGaIn/GaN HEMT Technology. In *2022 IEEE 9th Workshop on Wide Bandgap Power Devices & Applications (WiPDA)*, pp. 40–44. <https://doi.org/10.1109/WiPDA56483.2022.9955304>.
6. Jo, E., Kang, Y., Sim, S., Lee, H., and Kim, J. (2023). High-Temperature-Operable Electromechanical Computing Units Enabled by Aligned Carbon Nanotube Arrays. *ACS Nano* *17*, 13310–13318. <https://doi.org/10.1021/acsnano.3c01304>.
7. Suga, H. (2024). High-temperature non-volatile memory technology. *Nat. Electron.* *7*, 330–331. <https://doi.org/10.1038/s41928-024-01172-6>.

8. Suga, H., Suzuki, H., Shinomura, Y., Kashiwabara, S., Tsukagoshi, K., Shimizu, T., and Naitoh, Y. (2016). Highly stable, extremely high-temperature, nonvolatile memory based on resistance switching in polycrystalline Pt nanogaps. *Sci. Rep.* 6, 34961. <https://doi.org/10.1038/srep34961>.
9. Pradhan, D.K., Moore, D.C., Francis, A.M., Kupernik, J., Kennedy, W.J., Glavin, N.R., Olsson, R.H., and Jariwala, D. (2024). Materials for high-temperature digital electronics. *Nat. Rev. Mater.* 9, 790–807. <https://doi.org/10.1038/s41578-024-00731-9>.
10. Drury, D., Yazawa, K., Zakutayev, A., Hanrahan, B., and Brennecke, G. (2022). High-Temperature Ferroelectric Behavior of Al_{0.7}Sc_{0.3}N. *Micromachines* 13, 887. <https://doi.org/10.3390/mi13060887>.
11. Pradhan, D.K., Moore, D.C., Kim, G., He, Y., Musavigharavi, P., Kim, K.-H., Sharma, N., Han, Z., Du, X., Puli, V.S., et al. (2024). A scalable ferroelectric non-volatile memory operating at 600 °C. *Nat. Electron.* 7, 348–355. <https://doi.org/10.1038/s41928-024-01148-6>.
12. Huang, M., Schwacke, M., Onen, M., del Alamo, J., Li, J., and Yildiz, B. (2023). Electrochemical Ionic Synapses: Progress and Perspectives. *Adv. Mater.* 35, 2205169. <https://doi.org/10.1002/adma.202205169>.
13. Talin, A.A., Li, Y., Robinson, D.A., Fuller, E.J., and Kumar, S. (2023). ECRAM Materials, Devices, Circuits and Architectures: A Perspective. *Adv. Mater.* 35, 2204771. <https://doi.org/10.1002/adma.202204771>.
14. Fuller, E.J., Li, Y., Bennet, C., Keene, S.T., Melianas, A., Agarwal, S., Marinella, M.J., Salleo, A., and Talin, A.A. (2019). Redox transistors for neuromorphic computing. *IBM J. Res. Dev.* 63, 9:1-9:9. <https://doi.org/10.1147/JRD.2019.2942285>.
15. Kwak, H., Kim, N., Jeon, S., Kim, S., and Woo, J. (2024). Electrochemical random-access memory: recent advances in materials, devices, and systems towards neuromorphic computing. *Nano Converg.* 11, 9. <https://doi.org/10.1186/s40580-024-00415-8>.
16. Nikam, R.D., Lee, J., Lee, K., and Hwang, H. (2023). Exploring the Cutting-Edge Frontiers of Electrochemical Random Access Memories (ECRAMs) for Neuromorphic Computing: Revolutionary Advances in Material-to-Device Engineering. *Small* 19, 2302593. <https://doi.org/10.1002/smll.202302593>.
17. Fuller, E.J., Gabaly, F.E., Léonard, F., Agarwal, S., Plimpton, S.J., Jacobs-Gedrim, R.B., James, C.D., Marinella, M.J., and Talin, A.A. (2017). Li-Ion Synaptic Transistor for Low Power Analog Computing. *Adv. Mater.* 29, 1604310. <https://doi.org/10.1002/adma.201604310>.
18. Nguyen, N.-A., Schneegans, O., Salot, R., Lamy, Y., Giapintzakis, J., Mai, V.H., and Oukassi, S. (2022). An Ultralow Power Li_xTiO₂-Based Synaptic Transistor for Scalable Neuromorphic Computing. *Adv. Electron. Mater.* 8, 2200607. <https://doi.org/10.1002/aelm.202200607>.

19. Li, Y., Fuller, E.J., Asapu, S., Agarwal, S., Kurita, T., Yang, J.J., and Talin, A.A. (2019). Low-Voltage, CMOS-Free Synaptic Memory Based on Li_xTiO_2 Redox Transistors. *ACS Appl. Mater. Interfaces* *11*, 38982–38992. <https://doi.org/10.1021/acsami.9b14338>.
20. Wan, Q., Rasetto, M., Sharbati, M.T., Erickson, J.R., Velagala, S.R., Reilly, M.T., Li, Y., Benosman, R., and Xiong, F. (2021). Low-Voltage Electrochemical Li_xWO_3 Synapses with Temporal Dynamics for Spiking Neural Networks. *Adv. Intell. Syst.* *3*, 2100021. <https://doi.org/10.1002/aisy.202100021>.
21. Tang, J., Bishop, D., Kim, S., Copel, M., Gokmen, T., Todorov, T., Shin, S., Lee, K.-T., Solomon, P., Chan, K., et al. (2018). ECRAM as Scalable Synaptic Cell for High-Speed, Low-Power Neuromorphic Computing. In 2018 IEEE International Electron Devices Meeting (IEDM), p. 13.1.1-13.1.4. <https://doi.org/10.1109/IEDM.2018.8614551>.
22. van de Burgt, Y., Lubberman, E., Fuller, E.J., Keene, S.T., Faria, G.C., Agarwal, S., Marinella, M.J., Alec Talin, A., and Salleo, A. (2017). A non-volatile organic electrochemical device as a low-voltage artificial synapse for neuromorphic computing. *Nat. Mater.* *16*, 414–418. <https://doi.org/10.1038/nmat4856>.
23. Fuller, E.J., Keene, S.T., Melianas, A., Wang, Z., Agarwal, S., Li, Y., Tuchman, Y., James, C.D., Marinella, M.J., Yang, J.J., et al. (2019). Parallel programming of an ionic floating-gate memory array for scalable neuromorphic computing. *Science* *364*, 570–574. <https://doi.org/10.1126/science.aaw5581>.
24. Onen, M., Emond, N., Wang, B., Zhang, D., Ross, F.M., Li, J., Yildiz, B., and del Alamo, J.A. (2022). Nanosecond protonic programmable resistors for analog deep learning. *Science* *377*, 539–543. <https://doi.org/10.1126/science.abp8064>.
25. Yao, X., Klyukin, K., Lu, W., Onen, M., Ryu, S., Kim, D., Emond, N., Waluyo, I., Hunt, A., del Alamo, J.A., et al. (2020). Protonic solid-state electrochemical synapse for physical neural networks. *Nat. Commun.* *11*, 3134. <https://doi.org/10.1038/s41467-020-16866-6>.
26. Cui, J., An, F., Qian, J., Wu, Y., Sloan, L.L., Pidaparthy, S., Zuo, J.-M., and Cao, Q. (2023). CMOS-compatible electrochemical synaptic transistor arrays for deep learning accelerators. *Nat. Electron.* *6*, 292–300. <https://doi.org/10.1038/s41928-023-00939-7>.
27. Kim, S., Todorov, T., Onen, M., Gokmen, T., Bishop, D., Solomon, P., Lee, K.-T., Copel, M., Farmer, D.B., Ott, J.A., et al. (2019). Metal-oxide based, CMOS-compatible ECRAM for Deep Learning Accelerator. In 2019 IEEE International Electron Devices Meeting (IEDM), p. 35.7.1-35.7.4. <https://doi.org/10.1109/IEDM19573.2019.8993463>.
28. Li, Y., Fuller, E.J., Sugar, J.D., Yoo, S., Ashby, D.S., Bennett, C.H., Horton, R.D., Bartsch, M.S., Marinella, M.J., Lu, W.D., et al. (2020). Filament-Free Bulk Resistive Memory Enables Deterministic Analogue Switching. *Adv. Mater.* *32*, 2003984. <https://doi.org/10.1002/adma.202003984>.
29. Noh, K., Kwak, H., Son, J., Kim, S., Um, M., Kang, M., Kim, D., Ji, W., Lee, J., Jo, H., et al. (2024). Retention-aware zero-shifting technique for Tiki-Taka algorithm-based analog deep learning accelerator. *Sci. Adv.* *10*, eadl3350. <https://doi.org/10.1126/sciadv.adl3350>.

30. Langner, P., Chiabrera, F., Alayo, N., Nizet, P., Morrone, L., Bozal-Ginesta, C., Morata, A., and Tarancòn, A. (2024). Solid-State Oxide-Ion Synaptic Transistor for Neuromorphic Computing. Preprint at arXiv, <https://doi.org/10.48550/arXiv.2408.01469>
<https://doi.org/10.48550/arXiv.2408.01469>.
31. Freidzon, D., Wachtel, E., Cohen, H., Houben, L., Kossoy, A., Brontvein, O., Varenik, M., Frenkel, A.I., Ehre, D., and Lubomirsky, I. (2024). A Gd-doped ceria/TiO_x nanocomposite as the active layer in a three terminal electrochemical resistivity switch. *Solid State Ion.* *411*, 116572. <https://doi.org/10.1016/j.ssi.2024.116572>.
32. Marinella, M.J., Bennett, C.H., Zutter, B., Siath, M., Spear, M., Vizkelethy, G., Xiao, T.P., Fuller, E., Hughart, D., Agarwal, S., et al. (2024). Heavy-Ion-Induced Displacement Damage Effects on WO_x ECRAM. *IEEE Trans. Nucl. Sci.* *71*, 579–584. <https://doi.org/10.1109/TNS.2024.3360409>.
33. Fang, R., Li, X., Ren, K., Zhang, W., Xu, H., Wang, L., and Shang, D. (2024). Improved dynamic characteristics of oxide electrolyte-gated transistor for time-delayed reservoir computing. *Appl. Phys. Lett.* *124*. <https://doi.org/10.1063/5.0185402>.
34. Chen, P., Liu, F., Lin, P., Li, P., Xiao, Y., Zhang, B., and Pan, G. (2023). Open-loop analog programmable electrochemical memory array. *Nat. Commun.* *14*, 6184. <https://doi.org/10.1038/s41467-023-41958-4>.
35. Lee, J., Nikam, R.D., Kwak, M., and Hwang, H. (2022). Strategies to Improve the Synaptic Characteristics of Oxygen-Based Electrochemical Random-Access Memory Based on Material Parameters Optimization. *ACS Appl. Mater. Interfaces* *14*, 13450–13457. <https://doi.org/10.1021/acsmi.1c21045>.
36. Nikam, R.D., Kwak, M., and Hwang, H. (2021). All-Solid-State Oxygen Ion Electrochemical Random-Access Memory for Neuromorphic Computing. *Adv. Electron. Mater.* *7*, 2100142. <https://doi.org/10.1002/aelm.202100142>.
37. Porzani, M., Ricci, S., Farronato, M., and Ielmini, D. (2024). Programming Characteristics of Electrochemical Random Access Memory (ECRAM)—Part I: Experimental Study. *IEEE Trans. Electron Devices* *71*, 3240–3245. <https://doi.org/10.1109/TED.2024.3376309>.
38. Kang, H., and Woo, J. (2021). Cu-ion-actuated three-terminal neuromorphic synaptic devices based on binary metal-oxide electrolyte and channel. *Appl. Phys. Lett.* *119*, 072103. <https://doi.org/10.1063/5.0059697>.
39. Schwacke, M., Žguncs, P., Del Alamo, J., Li, J., and Yildiz, B. (2024). Electrochemical Ionic Synapses with Mg²⁺ as the Working Ion. *Adv. Electron. Mater.* *10*, 2300577. <https://doi.org/10.1002/aelm.202300577>.
40. Kim, D.S., Watkins, V.J., Cline, L.A., Li, J., Sun, K., Sugar, J.D., Fuller, E.J., Talin, A.A., and Li, Y. (2023). Nonvolatile Electrochemical Random-Access Memory under Short Circuit. *Adv. Electron. Mater.* *9*, 2200958. <https://doi.org/10.1002/aelm.202200958>.
41. Skowronski, M. (2023). Material instabilities in the TaO_x-based resistive switching devices (Invited). In *2023 IEEE International Reliability Physics Symposium (IRPS)*, pp. 1–5. <https://doi.org/10.1109/IRPS48203.2023.10117796>.

42. Li, J., Appachar, A., Peczonczyk, S., Harrison, E., Ievlev, A.V., Hood, R., Shin, D., Yoo, S., Roest, B., Sun, K., et al. (2024). Thermodynamic origin of nonvolatility in resistive memory. *Matter*. <https://doi.org/10.1016/j.matt.2024.07.018>.
43. Choi, S., Lee, J., Kim, S., and Lu, W.D. (2014). Retention failure analysis of metal-oxide based resistive memory. *Appl. Phys. Lett.* *105*, 113510. <https://doi.org/10.1063/1.4896154>.
44. Lee, M.-J., Lee, C.B., Lee, D., Lee, S.R., Chang, M., Hur, J.H., Kim, Y.-B., Kim, C.-J., Seo, D.H., Seo, S., et al. (2011). A fast, high-endurance and scalable non-volatile memory device made from asymmetric Ta₂O_{5-x}/TaO_{2-x} bilayer structures. *Nat. Mater.* *10*, 625–630. <https://doi.org/10.1038/nmat3070>.
45. Kwak, H., Lee, C., Lee, C., Noh, K., and Kim, S. (2021). Experimental measurement of ungated channel region conductance in a multi-terminal, metal oxide-based ECRAM. *Semicond. Sci. Technol.* *36*, 114002. <https://doi.org/10.1088/1361-6641/ac25c8>.
46. Lee, J., Nikam, R.D., Kwak, M., and Hwang, H. (2022). Improved Synaptic Characteristics of Oxide-Based Electrochemical Random Access Memory at Elevated Temperatures Using Integrated Micro-Heater. *IEEE Trans. Electron Devices* *69*, 2218–2221. <https://doi.org/10.1109/TED.2022.3151306>.
47. Nikam, R.D., Lee, J., Choi, W., Kim, D., and Hwang, H. (2022). On-Chip Integrated Atomically Thin 2D Material Heater as a Training Accelerator for an Electrochemical Random-Access Memory Synapse for Neuromorphic Computing Application. *ACS Nano*, acsnano.2c02913. <https://doi.org/10.1021/acsnano.2c02913>.
48. Melianas, A., Quill, T.J., LeCroy, G., Tuchman, Y., Loo, H. v., Keene, S.T., Giovannitti, A., Lee, H.R., Maria, I.P., McCulloch, I., et al. (2020). Temperature-resilient solid-state organic artificial synapses for neuromorphic computing. *Sci. Adv.* *6*, eabb2958. <https://doi.org/10.1126/sciadv.abb2958>.
49. Gonzalez-Rosillo, J.C., Balaish, M., Hood, Z.D., Nadkarni, N., Fraggedakis, D., Kim, K.J., Mullin, K.M., Pfenninger, R., Bazant, M.Z., and Rupp, J.L.M. (2020). Lithium-Battery Anode Gains Additional Functionality for Neuromorphic Computing through Metal–Insulator Phase Separation. *Adv. Mater.* *32*, 1907465. <https://doi.org/10.1002/adma.201907465>.
50. Tian, H., and Bazant, M.Z. (2022). Interfacial Resistive Switching by Multiphase Polarization in Ion-Intercalation Nanofilms. *Nano Lett.* *22*, 5866–5873. <https://doi.org/10.1021/acs.nanolett.2c01765>.
51. Min, K.-H., Sinclair *, R., Park, I.-S., Kim, S.-T., and Chung, U.-I. (2005). Crystallization behaviour of ALD-Ta₂O₅ thin films: the application of in-situ TEM. *Philos. Mag.* *85*, 2049–2063. <https://doi.org/10.1080/14786430500036546>.
52. Garg, S.P., Krishnamurthy, N., Awasthi, A., and Venkatraman, M. (1996). The O-Ta (Oxygen-Tantalum) system. *J. Phase Equilibria* *17*, 63–77. <https://doi.org/10.1007/BF02648373>.

Figure 1. Binary switching and high-temperature retention of TaO_x ECRAM devices. (a) Schematic depicting the structure of the ECRAM device, featuring a stacked configuration of TaO_x/YSZ/Ta. This design utilizes an electric field to facilitate the movement of oxygen ions through the YSZ electrolyte, effectively modulating the oxygen concentration in the TaO_x channel oxide to enable the storage of information through the creation of varying resistance states in the device. (b) Binary switching behavior from HRS to LRS with one pulse (2V, 1s) at 350°C shows an on/off ratio of more than 100. (c) 50 cycle switching between LRS and HRS with minimal cycle-to-cycle variation. (d) Write endurance measurements at 400°C shows operations for greater than 10,000 write pulses; the read endurance is given in Fig. S2. (e) The retention measurements of two resistance states at 400°C and 600°C for 24 hours. At 400°C, the LRS conductance decreased by 5%, and the HRS conductance decreased by 10% after 24 hours; at 600°C, the LRS conductance increased by 5% while the HRS conductance decreased by 12% after 24 hours. (f) Retention times of various memory devices including our ECRAM with TaO_x, Pt nanogap devices⁸, Al_{0.7}Sc_{0.3}N ferroelectrics^{10,11}, ReRAMs based on TaO_x⁴³, and ECRAMs utilizing TiO_x²⁸ and WO_x⁴⁰.

Figure 2. Scanning Transmission Electron Microscopy (STEM) of cross-sectioned ECRAM devices. The top row is the high-angle annular dark field (HAADF) mapping, while the bottom row is energy dispersive spectroscopy (EDS) mapping. The Ta at% is plotted as a function of the depth. (a) Pristine devices fabricated using a Ta ion reservoir and a TaO₂ channel; this sample was not annealed at 400°C after fabrication. (b) In the low-resistance state (LRS), the ion reservoir is partially oxidized while a reduced Ta-rich, O-poor layer is formed at the channel. (c) The LRS device maintains its metal and oxygen distribution even after short-circuiting the device for 12 hours at 400°C. This coexistence of oxidized and reduced TaO_x compounds over time in both the reservoir and the channel is consistent with the composition phase separation of the material and the nonvolatile information retention of the device. (d) The HRS state shows that the channel is again oxidized, while a reduced Ta-rich layer forms at the reservoir layer.

Figure 3: Cyclic Voltammetry Analysis of ECRAM device. (a) Cyclic voltammetry was conducted by cycling the voltage at a rate of 20 mV s^{-1} while maintaining a constant read voltage of 0.01 V across the channel. (b) The gate current during the cyclic voltammetry shows clear redox peaks during SET and RESET. There is no electrochemical current at 0V , consistent with the absence of an oxygen chemical potential difference between the reservoir and the channel. (c) The channel current as measured with a 10-mV potential taken concurrently with the gate cyclic voltammetry. During switching (SET or RESET), the channel current is affected by the electrochemical gate current from (a). (d) A plot of the channel current against the gate voltage shows a clear hysteresis between the HRS and the LRS after switching, consistent with its role as a nonvolatile memory. (e) Cyclic voltammetry data for a volatile TiO_2 -based ECRAM devices from previous work²⁸ shows a substantial negative current at 0V after SET, thereby resulting in information loss through an electrochemical self-discharge process. This contrasts with the TaOx ECRAM in (b).

Figure 4. Analog switching and retention characterizations of the ECRAM. (a) Linear and symmetric conductance update in an ECRAM using a series of SET/RESET pulsing cycles of different pulse widths at 400°C (100 pulses, ± 8 V, 800 μ s). (b) Small amplitude analog switching around the many conductance states of the device. The switching alternates between 100 pulses of +2V and 100 pulses of -2V. (c) Retention test of >10 analog states over a wide switching window.

Supplemental Figures

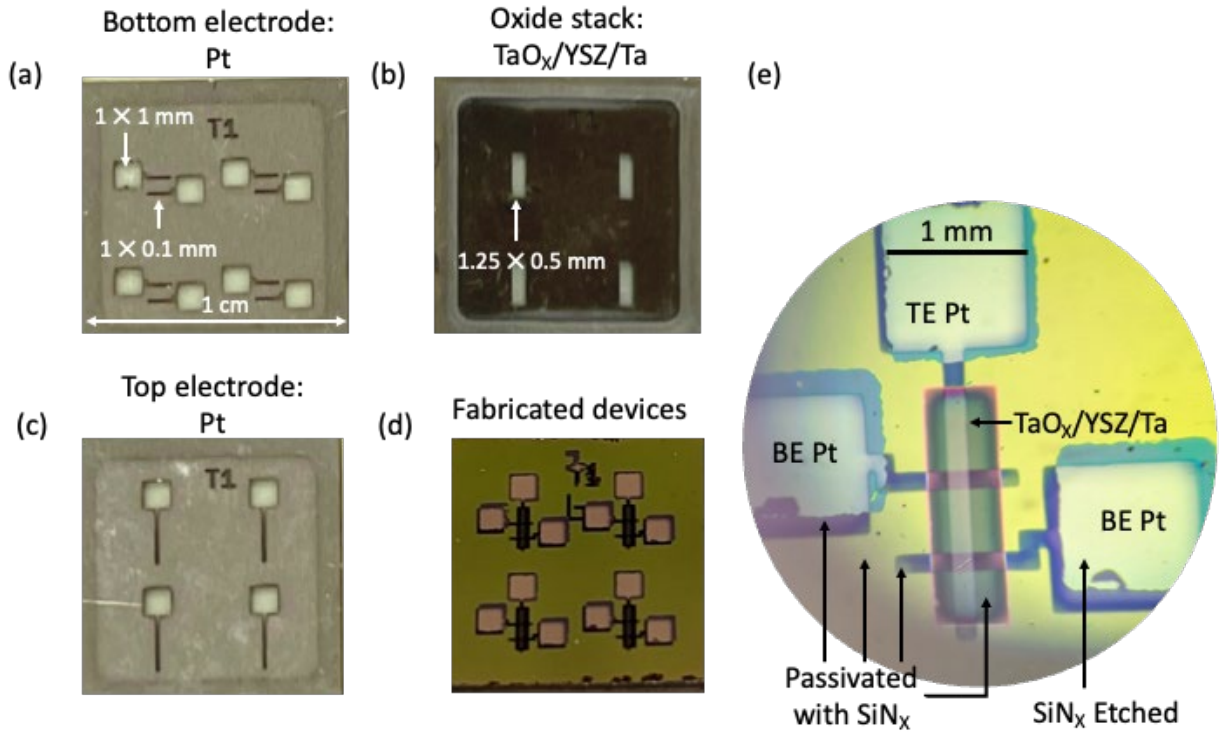


Figure S1. Images of the shadow masks and the ECRAM devices. (a-c) The three shadow masks used to fabricate the device. (d) Image of the fabricated device. (e) Low-resolution optical micrograph of a device. The chip was passivated with SiN_x except that the Pt electrodes were to ensure contact.

Figure S2: Read speed and endurance of the channel in a low-resistance state. (a) Square voltage pulses of different widths were applied across the channel. (b-c) The read current stabilized within $1 \mu\text{s}$ of the voltage pulse. (d) Read endurance of the channel exceeds 10^6 read pulses. In set shows the shape of each voltage pulse, which consists of both a positive and negative voltage. The positive current was used to compute the channel conductance. These read endurance measurements were taken using a Keithley 4200A semiconductor parameter analyzer with a 4225 pulse measure unit.

Figure S3: Switching between LRS and HRS with minimal cycle-to-cycle variation across a wide temperature range. Note the differences in the switching time at different temperatures.

Figure S4: Switching between LRS and HRS with $\pm 2V$, 1s pulses at different temperatures. The device operated at 350-400°C shows the largest on/off ratio.

Figure S5: On/off ratios at different temperatures. (a) The obtained conductance ranges for the HRS and LRS from Fig. S4. (b) The devices operating at 350-400°C show the largest on/off ratio.

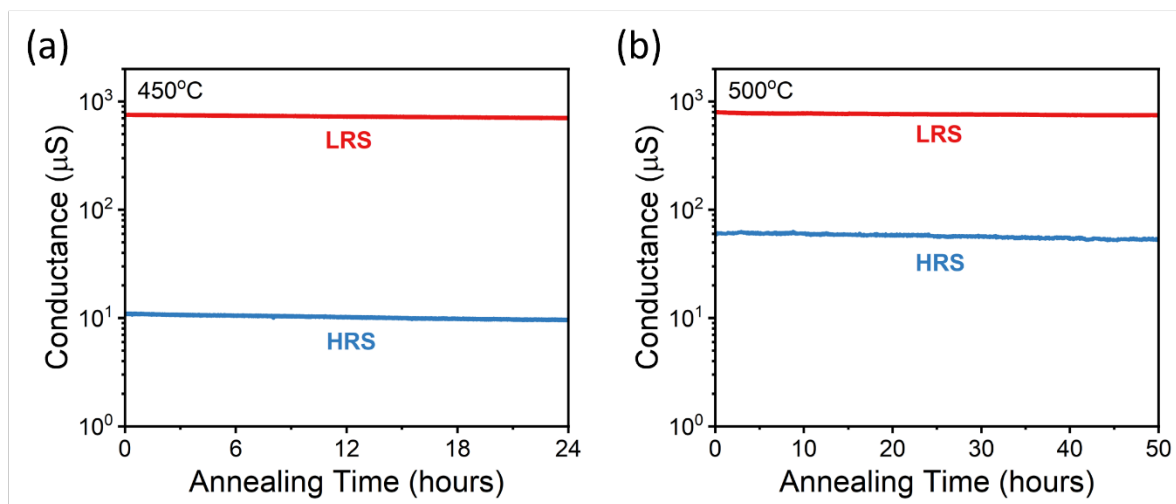


Figure S6: Retention test over 24 hours at 450°C (a) and 500°C (b). No significant change in conductance was observed in both LRS and HRS.

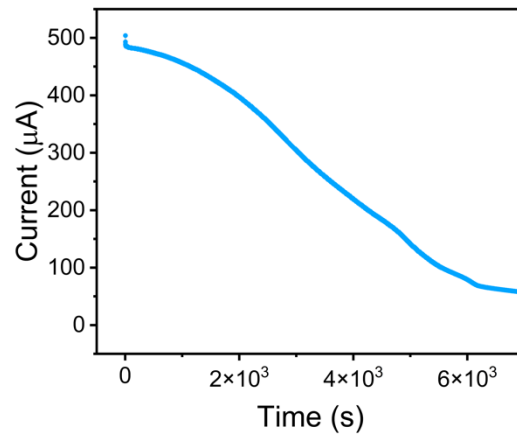


Figure S7: The ECRAM device rapidly oxidizes in air. Thicker and/or improved oxygen diffusion barriers would be necessary for operations in air.

Figure S8: Temperature-dependent conductance and current-voltage readings of an ECRAM device.

We first switched this device to the LRS or the HRS at 400°C, and subsequently changed the temperature while applying a +/- 0.5V voltage sweep across the channel. (a) plots the conductance, while (b) and (c) show the current-voltage readings at different temperatures for the LRS and HRS, respectively.

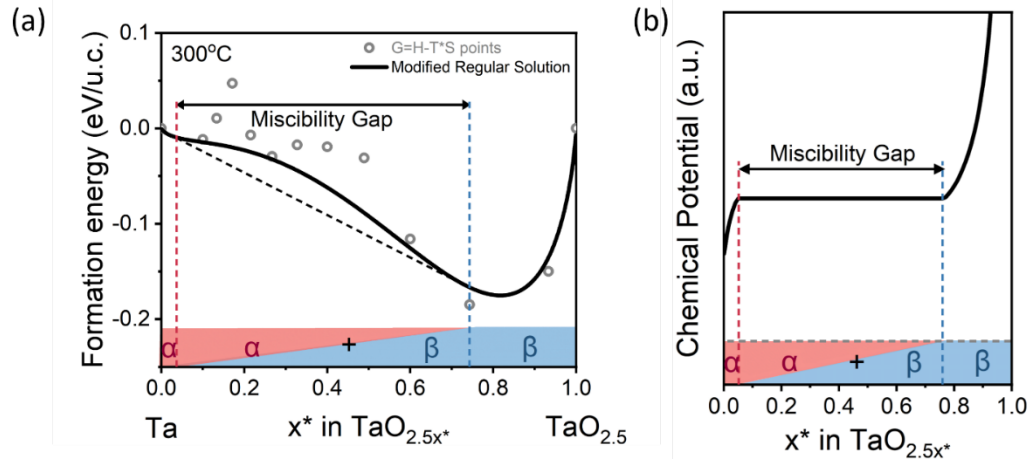


Figure S9: Computed formation energy and chemical potential of amorphous tantalum oxide from our previous work^{S1}. (a) Free energy curve fitted from DFT free energy points at 300°C and (b) corresponding oxygen chemical potential. $\sim\text{Ta}$ (α) and $\text{TaO}_{1.9}$ (β) are identified as two stable phases in the amorphous tantalum-oxygen system.

Fig. S10: Ta reservoir conductance over time. The conductance of the Ta reservoir in a modified ECRAM geometry increases over the first 90 hours at 500°C, likely a result of the increased crystallization of the metal over time upon annealing.

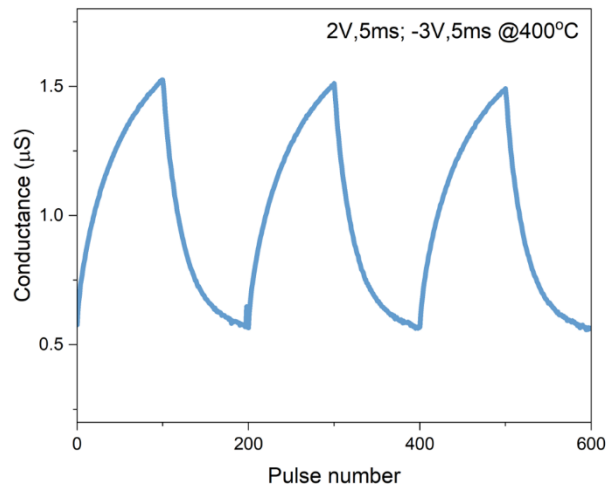


Figure S11: Analog switching at approximately 1 microsiemens (μS) conductance.

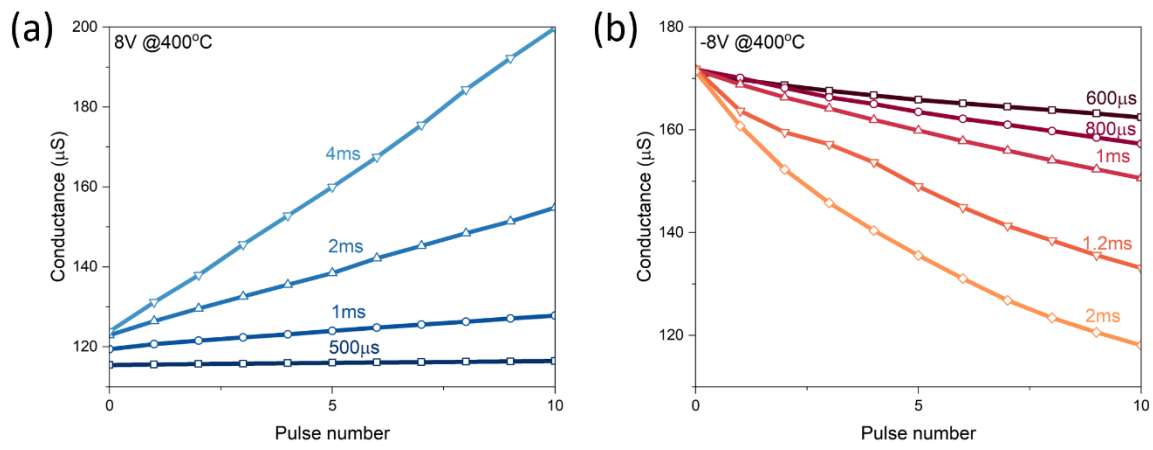


Figure S12: Analog switching with different pulse widths at +/- 8V. The conductance can be tuned by the applied pulses with different pulse widths.

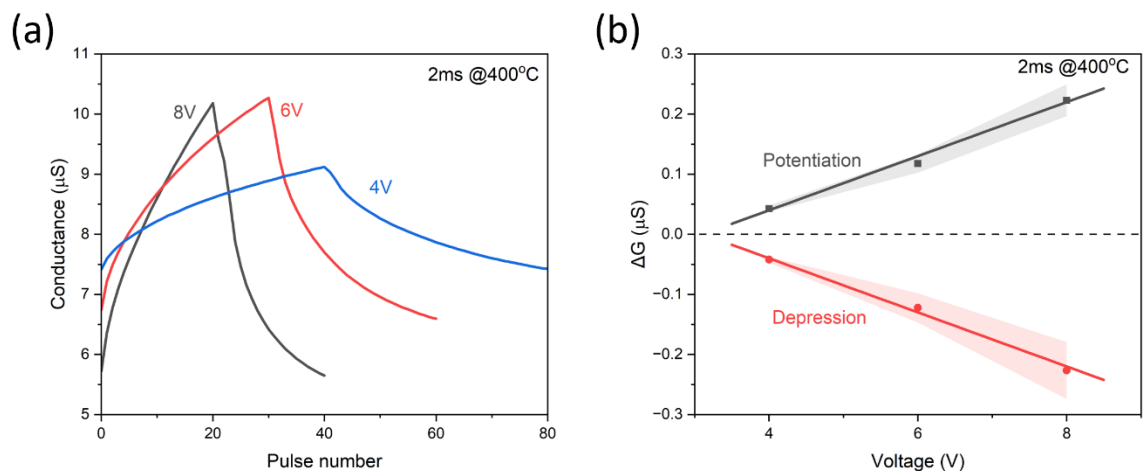


Figure S13: Analog switching with different pulse amplitudes. (a) Analog switching data with different pulse amplitudes. (b) Our results show that the conductance change is linearly proportional to the pulse amplitude

Supplemental References

[S1] Li, J., Appachar, A., Peczonczyk, S., Harrison, E., Ievlev, A.V., Hood, R., Shin, D., Yoo, S., Roest, B., Sun, K., et al. (2024). Thermodynamic origin of nonvolatility in resistive memory. *Matter*. <https://doi.org/10.1016/j.matt.2024.07.018>.