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To cite this article: Cameron J Kopas *et al* 2024 *Mater. Quantum. Technol.* **4** 045101

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IOP Publishing Mater. Quantum Technol. 4 (2024) 045101 https://doi.org/10.1088/2633-4356/ad88cc

Materials for Quantum Technology

OPEN ACCESS

RECEIVED
30 July 2024

REVISED
25 September 2024

ACCEPTED FOR PUBLICATION
18 October 2024

PUBLISHED
5 November 2024

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PAPER

Enhanced superconducting qubit performance through ammonium fluoride etch

Cameron J Kopas[1,*], **Dominic P Goronzy**[2], **Thang Pham**[2], **Carlos G Torres Castanedo**[2], **Matthew Cheng**[2], **Rory Cochrane**[1], **Patrick Nast**[1], **Ella Lachman**[1], **Nikolay Z Zhelev**[3,4,5], **André Vallières**[6,7], **Akshay A Murthy**[7], **Jin-su Oh**[8], **Lin Zhou**[8], **Matthew J Kramer**[8], **Hilal Cansizoglu**[1], **Michael J Bedzyk**[2,4], **Vinayak P Dravid**[2,9], **Alexander Romanenko**[7], **Anna Grassellino**[7], **Josh Y Mutus**[1], **Mark C Hersam**[2,10,11] and **Kameshwar Yadavalli**[1]

[1] Rigetti Computing, Berkeley, CA, United States of America
[2] Department of Materials Science and Engineering, Northwestern University, Evanston, IL, United States of America
[3] Center for Applied Physics and Superconducting Technologies, Northwestern University, Evanston, IL, United States of America
[4] Department of Physics and Astronomy, Northwestern University, Evanston, IL, United States of America
[5] Department of Physics, University of Oregon, Eugene, OR, United States of America
[6] Graduate Program in Applied Physics, Northwestern University, Evanston, IL 60208, United States of America
[7] Fermi National Accelerator Laboratory, Batavia, IL, United States of America
[8] Ames National Laboratory, U.S. Department of Energy, Ames, IA, United States of America
[9] Northwestern University Atomic and Nanoscale Characterization Experimental Center (NUANCE), Northwestern University, Evanston, IL, United States of America
[10] Department of Chemistry, Northwestern University, Evanston, IL, United States of America
[11] Department of Electrical and Computer Engineering, Northwestern University, Evanston, IL, United States of America
[*] Author to whom any correspondence should be addressed.

E-mail: ckopas@rigetti.com

Keywords: superconducting qubits, two-level systems, fabrication, interfaces

Supplementary material for this article is available online

Abstract

The performance of superconducting qubits is often limited by dissipation and two-level systems (TLS) losses. The dominant sources of these losses are believed to originate from amorphous materials and defects at interfaces and surfaces, likely as a result of fabrication processes or ambient exposure. Here, we explore a novel wet chemical surface treatment at the Josephson junction-substrate and the substrate-air interfaces by replacing a buffered oxide etch (BOE) cleaning process with one that uses hydrofluoric acid followed by aqueous ammonium fluoride. We show that the ammonium fluoride etch process results in a statistically significant improvement in median T_1 by $\sim 22\%$ ($p = 0.002$), and a reduction in the number of strongly-coupled TLS in the tunable frequency range. Microwave resonator measurements on samples treated with the ammonium fluoride etch after niobium deposition and etching also show $\sim 33\%$ lower TLS-induced loss tangent compared to the BOE treated samples. As the chemical treatment primarily modifies the Josephson junction-substrate interface and substrate-air interface, we perform targeted chemical and structural characterizations to examine materials differences at these interfaces and identify multiple microscopic changes that could contribute to decreased TLS losses.

1. Introduction

In the growing field of quantum information sciences, quantum computing is a likely complement to state-of-the-art classical high performance computing systems, and efforts to integrate these two computing architectures are already promising [1–3]. There are several potential quantum computing platforms, including superconducting, ion-trap, photonic, neutral atom, spin and topological approaches [4–9]. Each of these platforms has strengths and trade-offs in terms of performance, reliability, scalability, and complexity. Superconducting qubits are one of the leading approaches that are commonly researched for quantum

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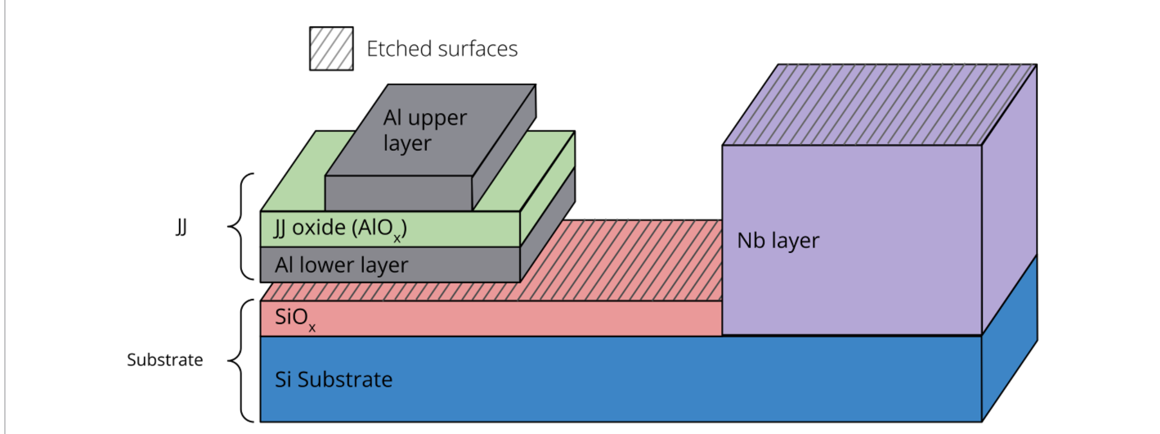

Figure 1. Cross-section schematic of the qubit devices, where the hashed surfaces are those treated during the wet chemical etch processing used in this study. The aluminum does indeed overlap the Nb, but it is not shown for clarity. The SiO_x shown is the native oxide formed on a bare Si surface, it is included because the oxide removal etch is the focus of this experiment.

computing [10]. The ability to achieve an addressable quantum system in micron-scale circuits, which can be fabricated by the well understood techniques and processes developed by the CMOS, MEMS, and superconducting electronics industries, as well as the ability to control interactions by purely electronic means have been drivers for the development of the superconducting quantum computing platform over the last two decades [11]. Furthermore, the use of commonly available fabrication techniques enables the possibility of scaling the qubit count [12–15] while being able to correct for device variation using post-processing techniques [16, 17].

Performance of superconducting qubits is impacted by decoherence through various loss channels. It is well known that dielectric loss from two-level states is a major decoherence source in superconducting qubits [18]. While the coherence times of superconducting qubits are known to fluctuate unpredictably [19], by systematic analysis and by measuring large numbers of qubits, one can identify the contribution of fabrication related loss channels [20]. In typical transmon qubits, the interfaces that affect performance include metal-substrate, substrate-air, metal-air, metal-metal, and dielectrics on the various surfaces and at the Josephson junction barrier.

Several approaches have been investigated to address these loss sources and reduce decoherence in superconducting resonators and qubits. Trenched resonators show improved performance [21], due to reduced participation of the substrate-air interface. Furthermore, design changes have been investigated to alter the participation ratio of different interfaces to study their loss contributions [22, 23]. Additionally, loss in superconducting devices fabricated on Si substrates has been shown to be impacted by surface treatments before and after the qubit electrode deposition [23, 24]. Chemical and/or physical treatments to remove dielectrics from various parts of the device have been shown to help improve device performance partially by removing the native oxide on the Si substrate prior to junction formation [25]. Due to the importance of Si substrate preparation for device performance, we looked into testing different pre-cleaning solutions prior to Josephson junction fabrication. Aqueous fluoride solutions are known to provide either a rough surface or a smooth one for Si(100) wafers based on the pH of the solutions [26]. Earlier work has shown that an ammonium fluoride etch on a Si(111) surface can form an atomically defined and oxidation resistant monohydride surface [27]. Superconducting Nb films deposited onto these smooth passivated surfaces show improved properties, but it was not known what effect a similar process would have on Si(100) surface or on Josephson junctions deposited on such a treated surface.

In this study we compare two sets of devices fabricated on Si(100) wafers that, after dry etching to define the niobium circuit layer fabrication, were prepared using different surface cleaning etches just before the Josephson junction process steps. See figure 1 for a schematic of the resulting devices and treated surfaces. The first set (referred to as BOE etched from here on) were etched for 2 min in a Buffered Oxide Etch (BOE) that is a 5:1 mixture of NH_4F 40% (aq.): HF 49% (aq.). The second set of devices were etched in HF 2% (aq.) for 1 min, followed by a deionized (DI) water rinse, and then a 2 min etch in NH_4F 40% (aq.), where the wafer was continuously dipped in and out of the NH_4F during the etch process for agitation to avoid accumulation of bubbles on the surface. This set will be referred to as HF $\rightarrow$ NH_4F from here on. After another DI water rinse and dry, the etched wafers are immediately coated with the bi-layer e-beam lithography resist. After e-beam exposure and pattern development, the junctions are fabricated using a double tilt angle deposition technique. This procedure minimizes the time that the Si and Nb surfaces are

exposed to air after resist development. A second lithography and deposition step is used to deposit the patch (or bandage) layer between the Nb circuitry and the junctions [28]. More information about the qubit fabrication process and the double-angle lithography process are described in the Supplementary Information section and in [20, 29]. Throughout this manuscript we use the notation HF $\rightarrow$ NH_4F to indicate the HF followed by NH_4F process steps, where the arrow indicates two sequential processes in time and not a reaction diagram. The sizes of the Josephson junctions used in these test devices range from 0.01 μm^2 to 0.34 μm^2 for each Josephson junction in the SQUID loop. In addition to microwave characterization of resonators and qubits, we performed materials characterization of the affected interfaces using x-ray photoelectron spectroscopy (XPS), time-of-flight secondary ion mass spectrometry (TOF-SIMS), atomic force microscopy (AFM), contact angle measurements, and scanning transmission electron microscopy (STEM). By combining these materials characterizations with extensive device measurements, we demonstrate that an etch process using NH_4F reduces TLS and improves dissipation. We also point to several microscopic properties that could be driving these improvements. This study verifies improved performance for an industry-ready process and provides insights into understanding the sources of TLS at Si interfaces.

2. Results and discussion

The dominant sources of loss in superconducting qubits are generally concentrated at interfaces, but specific microscopic sources are numerous and difficult to pinpoint. Given this challenge to understanding which defects at the silicon-air and silicon-aluminum interfaces are affecting performance in these devices, we use qubit performance as the primary metric to evaluate these etch processes. While qubit performance metrics should be very sensitive to changes at these interfaces, we expect some spread across qubits on a single die, and across different wafers due to fabrication non-uniformities. To ensure good sampling while expecting these variations, we measured multiple dies from multiple wafers, each processed by the etches described earlier. Qubit performance metrics including decoherence are also impacted by design, which affects coupling to the environment and to other devices. To control for design variations, we verify the impact of these etch processes on two separate qubit chip designs; Design 1 is a simple test chip of nominally isolated qubits, while Design 2 is more complex where multi-qubit coupling is employed. Comparing multiple designs also ensures that any improvements carry over to devices useful for potential applications in quantum computing, and not only in test platforms. Both designs use a similar concentric qubit design, while the layouts, qubit-qubit coupling, and surface participation ratios are different. Design 1 consists of 14 flux-tunable qubits and 2 fixed qubits, without any qubit-qubit couplers. Design 2 consists of 32 flux-tunable qubits with fixed couplers to 2 or 3 neighbors in a square-octagon layout (similar to the Aspen-9 lattice described in Li *et al* [30]), where we only measure 24 qubits on each die due to test setup limitations. These 32-qubit devices are flip-chip bonded to a superconducting cap for signal delivery and isolation, and as a result are expected to have different surface participation ratios compared to the simpler device without a cap. The results in figure 2 show decoherence values for both device designs, and confirm that the results are consistent across both die layouts.

For each set and design of devices, we measured multiple chips from the same wafer, as well as from different wafers for each design type, totalling to 102 qubits for the HF $\rightarrow$ NH_4F etch, and 134 qubits for the BOE etch. Qubit measurements show that HF $\rightarrow$ NH_4F etched devices have a median relaxation rate of $\Gamma_1 = 18$ kHz (corresponding to a median $T_1 \approx 55$ μs) with 1st and 3rd quartiles of 15 and 25 kHz, while the BOE etch set of devices have a median $\Gamma_1 = 22$ kHz (corresponding to a median $T_1 \approx 45$ μs) with 1st and 3rd quartiles of 17 and 28 kHz. Since we have a large sample set and nearly-normal distributions with similar skew and variances, we chose the Tukey HSD (honestly significant difference) test to compare these distributions. We find that these are different Γ_1 distributions with $p = 0.002$, and the HSD allows us to estimate that the 95% upper and lower confidence intervals for the significant difference between two means is 1.8 to 8 kHz. A non-parametric Kruskal–Wallis test similarly determines that the medians are not the same across the two groups with $p < 0.01$. We report the median and quartiles here to avoid skewing the results with either high- or low-performing outliers. Despite the wide spread in each set, we can confidently conclude that these distributions are different, and the HF $\rightarrow$ NH_4F set has improved relaxation rate. We do not find any significant differences between the sets for Γ_2 or Γ_ϕ, and since we note that the decoherence and dephasing rates are higher than the relaxation rate, we believe that Γ_2 and Γ_ϕ are limited by external factors (i.e. not limited by relaxation). The same trend holds when comparing coherence results for each chip design individually.

We compare the effects of strongly-coupled TLS in these sample sets by spectroscopically measuring the qubit frequency as a function of flux bias, and fitting any features or avoided crossings to measure the coupling strength. The splitting in the avoided crossing is given by $\sqrt{\Delta_{TLS}^2 + 4g^2}$, where g is the coupling between the TLS and the qubit, and Δ_{TLS} is the difference in frequency between the qubit and the TLS. We

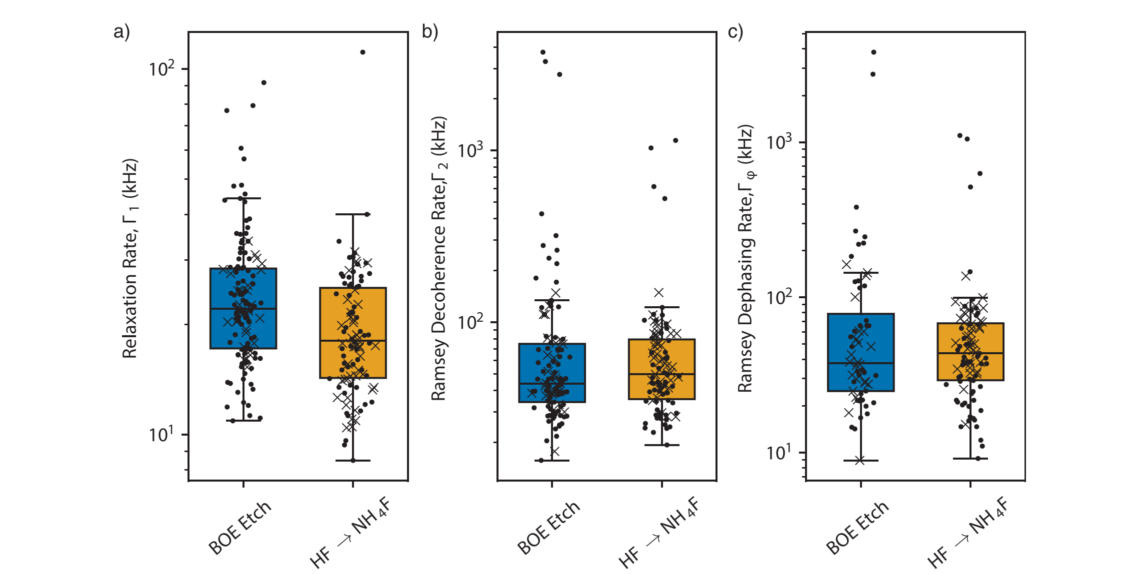

Figure 2. Comparison of measured qubit (a) relaxation rate, (b) Ramsey decoherence rate, and (c) Ramsey dephasing rate for surfaces prepared with a BOE etch (blue, left in each set) and HF $\rightarrow$ NH_4F (orange, right in each set). The $\times$ markers represent qubits with Design 1 (uncoupled qubits), and the dot markers represent qubits with Design 2 (coupled qubits). The y-axes are log scale to show the wide range in measured rates (this visually compresses differences between sample set means).

Table 1. Summary of the strongly-coupled TLS observed in qubits from both sets.

Group	Tunable Qubits	Sum of Qubit Tunable Ranges	Number of TLS	SPI
BOE	73	38.3 GHz	73	0.0095
HF $\rightarrow$ NH_4F	95	63.1 GHz	68	0.0065

find that the HF $\rightarrow$ NH_4F etched devices are improved by having fewer TLS. In terms of number of TLS per tunable range, there are on average $\sim$ 1.1 TLS/GHz in the HF $\rightarrow$ NH_4F set compared to $\sim$ 1.9 TLS/GHz in the BOE etched set.

In addition to the number of TLS, the coupling strength of TLS also affects the proportion of the qubit tunable spectrum where the qubit is useful for gate operations. For example, a tunable qubit with a single weakly-coupled TLS may have more available frequency spectrum than another tunable qubit with a single strongly-coupled TLS. To include this consideration in our TLS metrics, we introduce the SPI (Spectral Pollution Index) metric to track the frequency-normalized effect of strongly-coupled TLS across qubits in an experiment where the qubits may have different tunabilities. SPI is the sum of all TLS coupling g in a set of qubits, normalized by the sum of all the tunable qubit frequency ranges ($f_{\mathrm{max}} - f_{\mathrm{min}}$). We find that the total SPI is reduced in the HF $\rightarrow$ NH_4F set by about 32%, as shown in table 1. To visualize the difference in terms of number and coupling strength of TLS, we include a histogram of coupling g-factors in the supplement figure S-4.

In order to help separate the contribution of losses at the Si-air interface from those at Si-Al interface, we measure the power-dependent loss tangent of ten coplanar waveguide resonators for each etch method. Resonator devices were fabricated on the same wafer with other qubit devices, and were initially processed using a BOE etch. After processing, the devices were stored in a desiccator for about 4 months before the final BOE or HF $\rightarrow$ NH_4F etches were performed on individual chips. After the final etch, devices were stored in air for about 3 days before cooling down in a dilution refrigerator for measurement. We find that there is a significant difference in losses due to TLSs, with the BOE and HF $\rightarrow$ NH_4F treated resonators having $F\delta^0_{\mathrm{TLS}} = 2.5 \times 10^{-6}$ and 1.7×10^{-6} respectively, representing 32% lower TLS losses in the HF $\rightarrow$ NH_4F set, as shown in figure 3(a), consistent with the reduction in SPI measured on the qubits. The power-independent losses for the two etch processes, however, are similar (within 8.5% of each other, with a large spread), with $\delta_{\mathrm{PI}} = 4.7 \times 10^{-7}$ and 4.3×10^{-7} for BOE and HF $\rightarrow$ NH_4F sets respectively, as shown in figure 3(b). Since the power-independent losses are similar between the two sets, we conclude that there is no difference in loss due to hydrogen incorporation in the films [31]. Based on the NbO_x etch rates described in [32] we expect that the short etch times are insufficient to significantly remove the Nb-surface oxide, and so we do not expect any differences in loss from the Nb-air interface. Additionally, we performed TOF-SIMS depth

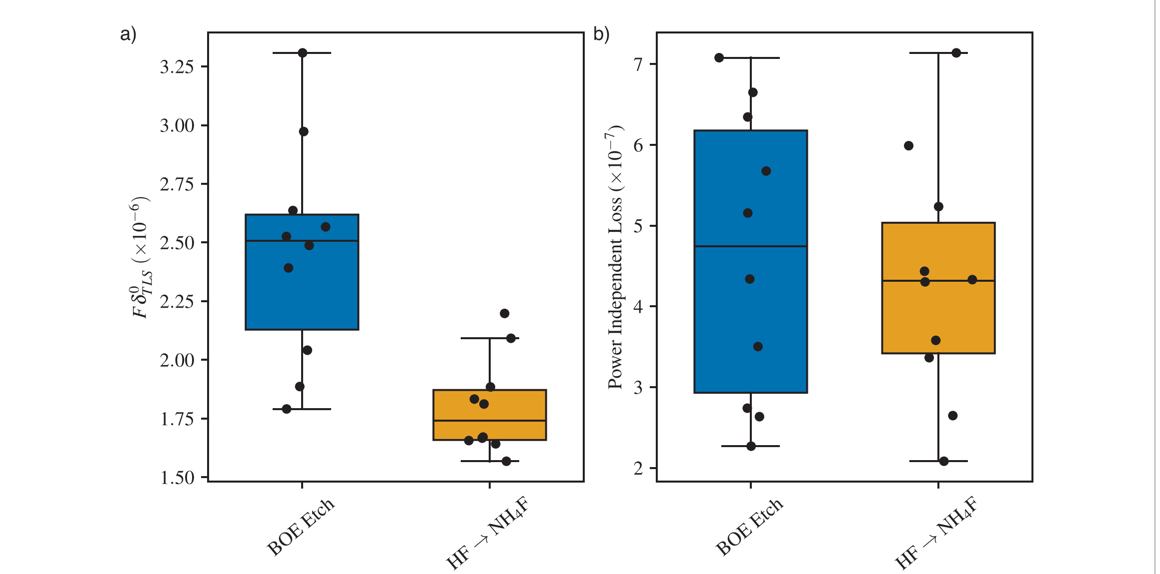

Figure 3. (a) TLS loss and (b) power-independent losses extracted from power-dependence measurements on coplanar waveguide resonators fabricated with both etch methods.

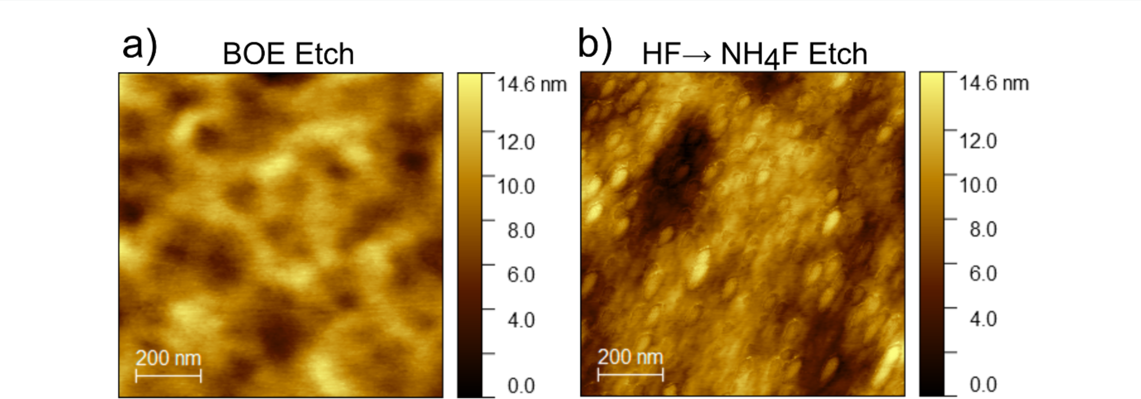

Figure 4. Surface topography of a 1 $\mu m \times 1$ μm area measured by AFM on the Si-area near a JJ within a qubit area. The Si surface was etched first with RIE then with the wet chemical process (a) BOE etch with RMS roughness 1.95 nm, and (b) the HF $\rightarrow NH_4F$ etch treatment with RMS roughness 2.29 nm. Larger area scans are in the supplement figure S-7.

profiles on the niobium layers of resonators treated with different etches and do not find any significant differences in the degree of H incorporation within the Nb film for the two etch methods, nor do we see differences in other impurity concentrations including O, C and F. (see figure S-1 for the results).

Since this short etch process is performed before the Josephson junctions deposition, the most likely location for any microscopic changes that could explain the reduced loss are at the Si surface (Si-air interface, or the Si-Al interface underneath the Josephson junction's lower lead and electrode). We looked into potential changes at the Si-air interface by performing the BOE and HF $\rightarrow NH_4F$ etches on both RIE-etched Si surfaces near the Josephson junction (real devices with the full qubit process), and on bare Si substrates, without any dry etch processes. In both the real devices (figure 4) and on the bare substrates (see figure S-6), we observe that Si substrates etched with HF $\rightarrow NH_4F$ show the presence of some small diameter surface peaks 10 nm high in AFM scans, increasing the roughness over that of the BOE etched surfaces. However, the low-frequency background roughness (presumably from the RIE etch process) visually appears decreased in the HF $\rightarrow NH_4F$ etched samples. We observe that the density of these small peaks is enough that some peaks must be present underneath the JJs, JJ leads, and the bandage layers, but based on qubit measurements we did not resolve any additional losses or TLS from these. We hypothesize that the HF $\rightarrow NH_4F$ etch process may reduce some of the large-scale roughness, but that small peaks are created during the HF process step in the HF $\rightarrow NH_4F$ etch process. This is consistent with the conclusions in Aldinger *et al* [26] and with the observation that Si substrates etched with NH_4F only (skipping the HF etch) do not show this additional roughness (see figure S-6).

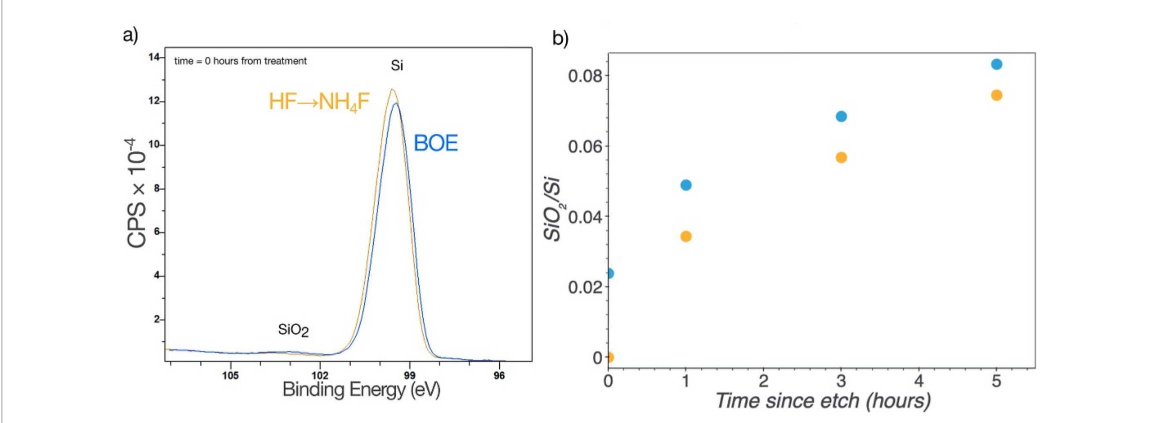

Figure 5. Re-oxidation of Si surfaces in atmosphere after receiving a BOE etch or a HF $\rightarrow$ NH_4F treatment, as measured by XPS. (a) shows an overlay of the measured XPS Spectra at time = 0 h , and (b) shows the ratio of $SiO_2$to Si peak intensities over time. Uncertainties in the SiO_2/Si ratio are $< 2.5\%$.

To further interrogate the Si surfaces, we measured the contact angle, where we also observe differences between the two treatments. The contact angle on the HF $\rightarrow$ NH_4F treated Si shows a higher angle, indicating a more hydrophobic surface. More hydrophobic surfaces may be caused by more H-passivation on the Si surface, which further suggests that the surface has less Si oxide. See data in the supplement figure S-8.

We used x-ray photoelectron spectroscopy (XPS) to examine the chemical nature of the Si surface immediately following treatment by both etch methods and also observe the rate of regrowth of oxide following etching. As shown in figure 5(a), XPS of the Si 2p region taken on Si samples immediately following etching with both methods show a prominent peak at approximately 99.4 eV, consistent with elemental Si. However, only the BOE treated sample shows signal in the range of 102–104 eV, consistent with the presence of Si oxide. Furthermore, we used XPS to track the growth of the Si oxide signal for up to 5 h of ambient exposure following etching (See figure S-2). We compare the re-oxidation of the Si surface for both etch methods by looking at the ratio of the peak area of the Si oxide signal to the elemental Si signal (figure 5(b)) and observe that while the regrowth of SiO_x occurs at similar rates for both conditions, the HF $\rightarrow$ NH_4F etch treatment provides an initial resistance to oxidation, with less oxide regrowth seen at all time points compared to the BOE treated samples. These results suggest that the HF $\rightarrow$ NH_4F etch treatment could be improving the interface between the Josephson junction and the Si substrate by preventing Si oxide re-growth in the short time between surface cleaning and Josephson junction deposition.

To evaluate this hypothesis, we further characterized the interface between the Al bottom electrode and the Si substrate using scanning transmission electron microscopy (STEM) imaging and spectroscopy. Figures 6(a),(c) display an overview of our Josephson junction by high-angle annular dark field (HAADF) STEM, showing the main components of our device: two polycrystalline Al electrodes with approximately 40–50 nm thickness, and a thin (1–2 nm) AlO_x tunnel barrier. The interface between the Al bottom electrode and the Si substrate is shown in atomic-resolution STEM images (figures 6(b),(d) for both BOE and HF $\rightarrow$ NH_4F treated Si substrates. The Al-Si interface in both cases is amorphous, and its width ranges from 2–4 nm. From these atomic-resolution images we do not find any significant differences in the surface oxide thickness or structure at the substrate-JJ interface.

We further employed energy dispersive spectroscopy (EDS) to investigate the chemistry of the aluminum-silicon interfaces. Figure 7 shows the chemical distribution of oxygen (O) and of all observed elements (Al, Si, O) displayed in a combined map for a BOE etched (figures 7(a),(c)) and a HF $\rightarrow$ NH_4F etched (figures 7(b),(d)) device, respectively. As expected, O concentrates at the AlO_x barrier between the two Al electrodes. Additionally, EDS mapping shows a significant amount of O at the Al-Si interface for both sample types. We quantify and plot the interfacial O for eight devices, in which four were fabricated with the BOE etch treatment, while the other four with the HF $\rightarrow$ NH_4F etch treatment, selecting two high T_1 -and two low T_1 devices from each set. Overall, the devices that received the HF $\rightarrow$ NH_4F etch show lower O concentration, 7.36 ± 2.66 at%, compared to the devices that received the BOE etch treatment, with 9.54 ± 2.90 at% O. However, when we compare the measured T_1 of each specific qubit to the EDS-measured average O concentration at the Josephson junction's Al-Si interface, we do not see a clear trend, as shown in figure 7(e).

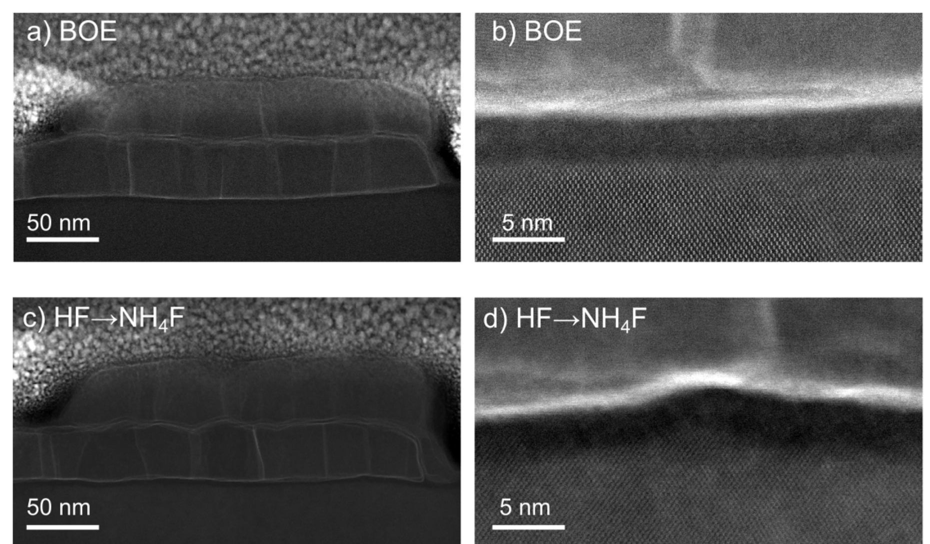

Figure 6. Structural characterization of Josephson junctions. (a), (c) Low-magnification STEM images of two representative Josephson junctions with: (a) BOE and (c) HF → NH_4F substrate cleaning treatments. (b), (d) Atomic resolution STEM images showing the amorphous interface between the Si substrate and the Al bottom electrode.

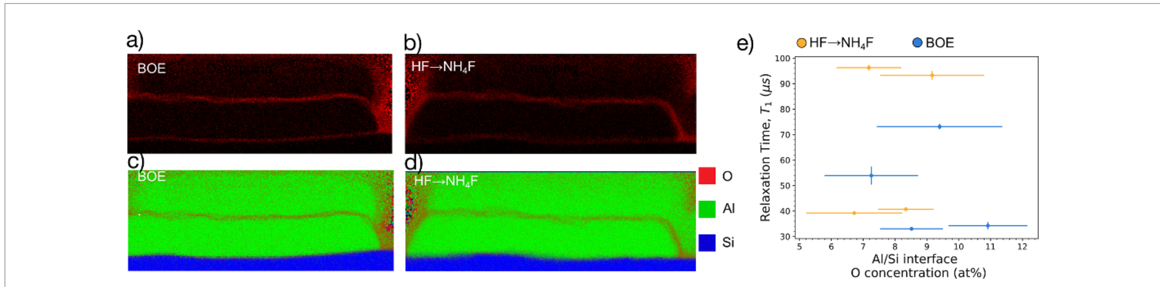

Figure 7. Chemistry of the Al-Si interface. Oxygen chemical mapping and an overlay of all chemical element (O, Al, Si) distribution for BOE etched sample (a), (c) and HF → NH_4F sample (b), (d), respectively. (e) Quantification of O concentration at the Al-Si interface for eight devices, four using BOE and four using the HF → NH_4F method. Error bars in (e) represent the standard error of the mean.

3. Conclusion

We show that a chemical change to the surface treatment of the Si substrate, prior to Josephson junction deposition, can result in a significant and reproducible improvement to dissipation properties (T_1) and a reduction in the number of TLS per tunable frequency span. We sought to correlate these changes in dissipation and TLS with physical and chemical changes at the silicon-aluminum interface through surface analysis, quantitative electron microscopy, and TOF-SIMS techniques. We observed that qubits treated with HF → NH_4F show on average less O at the Al-Si interface across the population, but on an individual-device basis this did not deterministically predict T_1 values. Because we observe a similar reduction in TLS loss in resonator power-dependence and in the incidence of strongly-coupled TLS observed in qubit measurements, and given that the resonators do not have a substrate-Josephson junction interface, we infer that many TLS may be localized on the Si-air interface, and are not necessarily exclusive to the substrate-Josephson junction interface. This is an unexpected result since the Si-air interface is exposed to uncontrolled atmosphere, forms a native oxide, and the main difference we found at this interface is that the HF → NH_4F (with fewer TLS) has additional roughness on the Si surface. TEM imaging of the Si-Josephson junction interface did not observe any significant differences, but this is because TLS losses are likely to be specific localized defects, which are difficult to image or pinpoint with characterization techniques that only analyze a small fraction of the device area. The difficulty in correlating qubit relaxation with microscopic materials properties highlights the significance of performing careful measurements on a large numbers of qubits, compared against a control group before making conclusions on the impacts of fabrication process changes. Despite the high decoherence rates and large populations of TLS in the test qubits studied here, the consistency of the results across three device types (coupled qubits, uncoupled qubits, and coplanar waveguide resonators), indicates to us that these improvements should carry over to state-of-the-art coherence-optimized qubits. This study

targets the specific substrate-air and substrate-Josephson junction interfaces, so dissipation benefits should similarly apply to device designs, experiment setups, and fabrication processes addressing other loss channels. Our findings demonstrate that the HF → NH_4F etch process improves qubit dissipation and TLS properties and can be easily incorporated into production fabrication processes.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

Acknowledgments

This material is based upon work supported by the U.S. Department of Energy, Office of Science, National Quantum Information Science Research Centers, Superconducting Quantum Materials and Systems Center (SQMS) under contract no. DE-AC02-07CH11359. This work made use of the Rigetti Fab-1 facilities. This work made use of the EPIC and Keck-II facilities of the Northwestern University NUANCE Center, which has received support from the SHyNE Resource (NSF ECCS-2025633), the IIN, and the Northwestern MRSEC program (NSF DMR-2308691). This work also made use of the QSET facility of the Northwestern University Center for Applied Physics and Superconducting Technologies (CAPST), which has received support from SQMS. The Ames National Laboratory is operated for the U.S. Department of Energy by Iowa State University under Contract No. DE-AC02-07CH11358.

ORCID iDs

Cameron J Kopas https://orcid.org/0000-0002-6184-2987
Dominic P Goronzy https://orcid.org/0000-0003-2856-4732
Carlos G Torres Castanedo https://orcid.org/0000-0002-4505-7970
Nikolay Z Zhelev https://orcid.org/0000-0002-5344-6298
André Vallières https://orcid.org/0000-0003-0769-8432
Akshay A Murthy https://orcid.org/0000-0001-7677-6866
Jin-su Oh https://orcid.org/0000-0002-7462-3142
Lin Zhou https://orcid.org/0000-0003-2286-6510
Matthew J Kramer https://orcid.org/0000-0002-9097-6730
Michael J Bedzyk https://orcid.org/0000-0002-1026-4558
Mark C Hersam https://orcid.org/0000-0003-4120-1426

References

[1] Möller M and Vuik C 2017 On the impact of quantum computing technology on future developments in high-performance scientific computing *Ethics Inf. Technol.* **19** 253–69
[2] Britt K A and Humble T S 2017 High-performance computing with quantum processing units *ACM J. Emerg. Technol. Comput. Syst.* **13** 1–13
[3] Humble T S, McCaskey A, Lyakh D I, Gowrishankar M, Frisch A and Monz T 2021 Quantum computers for high-performance computing *IEEE Micro* **41** 15–23
[4] Arute F *et al* 2019 Quantum supremacy using a programmable superconducting processor *Nature* **574** 505–10
[5] Moses S A *et al* 2023 A race-track trapped-ion quantum processor *Phys. Rev.* X **13** 041052
[6] Madsen L S *et al* 2022 Quantum computational advantage with a programmable photonic processor *Nature* **606** 75–81
[7] Graham T M *et al* 2022 Multi-qubit entanglement and algorithms on a neutral-atom quantum computer *Nature* **604** 457–62
[8] Veldhorst M, Eenink H G J, Yang C H and Dzurak A S 2017 Silicon CMOS architecture for a spin-based quantum computer *Nat. Commun.* **8** 1766
[9] Aguado R and Kouwenhoven L P 2020 Majorana qubits for topological quantum computing *Phys. Today* **73** 44–50
[10] Ichikawa T 2022 Bibliometric analysis of topic structure in quantum computation and quantum algorithm research (arXiv:2201.01911 [physics, physics:quant-ph])
[11] Clarke J and Wilhelm F K 2008 Superconducting quantum bits *Nature* **453** 1031–42
[12] Vahidpour M *et al* 2017 Superconducting through-silicon vias for quantum integrated circuits (arXiv:1708.02226 [physics, physics:quant-ph])
[13] Yost D R W *et al* 2020 Solid-state qubits integrated with superconducting through-silicon vias *npj Quantum Information* **6** 1–7
[14] Foxen B *et al* 2017 Qubit compatible superconducting interconnects *Quantum Sci. Technol.* **3** 014005
[15] Gold A *et al* 2021 Entanglement across separate silicon dies in a modular superconducting qubit device (arXiv:2102.13293 [quant-ph])
[16] Zhang E J *et al* 2022 High-performance superconducting quantum processors via laser annealing of transmon qubits *Sci. Adv.* **8** eabi6690
[17] Pappas D P *et al* 2024 Alternating-bias assisted annealing of amorphous oxide tunnel junctions *Commun. Mater.* **5** 1–7
[18] Martinis J M *et al* 2005 Decoherence in Josephson qubits from dielectric loss *Phys. Rev. Lett.* **95** 210503
[19] Klimov P V *et al* 2018 Fluctuations of energy-relaxation times in superconducting qubits *Phys. Rev. Lett.* **121** 090502

[20] Nersisyan A *et al* 2019 Manufacturing low dissipation superconducting quantum processors (arXiv:1901.08042 [physics, physics:quant-ph])

[21] Vissers M R, Kline J S, Gao J, Wisbey D S and Pappas D P 2012 Reduced microwave loss in trenched superconducting coplanar waveguides *Appl. Phys. Lett.* **100** 082602

[22] Chu Y, Axline C, Wang C, Brecht T, Gao Y Y, Frunzio L and Schoelkopf R J 2016 Suspending superconducting qubits by silicon micromachining *Appl. Phys. Lett.* **109** 112601

[23] Woods W, Calusine G, Melville A, Sevi A, Golden E, Kim D K, Rosenberg D, Yoder J L and Oliver W D 2019 Determining interface dielectric losses in superconducting coplanar-waveguide resonators *Phys. Rev. Appl.* **12** 014012

[24] Quintana C M *et al* 2014 Characterization and reduction of microfabrication-induced decoherence in superconducting quantum circuits *Appl. Phys. Lett.* **105** 062601

[25] Earnest C T, Béjanin J H, McConkey T G, Peters E A, Korinek A, Yuan H and Mariantoni M 2018 Substrate surface engineering for high-quality silicon/aluminum superconducting resonators *Supercond. Sci. Technol.* **31** 125013

[26] Aldinger B S and Hines M A 2012 Si(100) etching in aqueous fluoride solutions: parallel etching reactions lead to pH-dependent nanohillock formation or atomically flat surfaces *J. Phys. Chem.* C **116** 21499–507

[27] Berti G, Torres-Castanedo C G, Goronzy D P, Bedzyk M J, Hersam M C, Kopas C, Marshall J and Iavarone M 2023 Scanning tunneling microscopy and spectroscopy characterization of NB films for quantum applications *Appl. Phys. Lett.* **122** 192605

[28] Dunsworth A *et al* 2017 Characterization and reduction of capacitive loss induced by sub-micron Josephson junction fabrication in superconducting qubits *Appl. Phys. Lett.* **111** 022601

[29] Lecocq F, Naud C, Pop I M, Peng Z -H, Matei I, Crozes T, Fournier T, Guichard W and Buisson O 2011 Novel E-beam lithography technique for in-situ junction fabrication: the controlled undercut *Nanotechnology* **22** 315302

[30] Li A C Y *et al* 2023 Benchmarking variational quantum eigensolvers for the square-octagon-lattice Kitaev model *Phys. Rev. Res.* **5** 033071

[31] Torres-Castanedo C G *et al* 2024 Formation and microwave losses of hydrides in superconducting niobium thin films resulting from fluoride chemical processing *Adv. Funct. Mater.* **34** 2401365

[32] Altoé M V P *et al* 2022 Localization and mitigation of loss in niobium superconducting circuits *PRX Quantum* 3 020312