

PV-BESS DC-Series Integration for Regulated DC Systems

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Abstract—DC-series integration introduces a novel approach to seamlessly integrate a solar photovoltaic (PV) array and a battery energy storage (BES) in series. This system, referred to as the PV-integrated battery energy storage system – DC series (PVBESS-DCS), simplifies integration and enhances power density by leveraging the inherent voltage-source characteristics of batteries and adopting the concept of partial power processing. However, addressing voltage variations of a PV array and a BES under different operational conditions remains a challenge to apply the PVBESS-DCS to a regulated DC system, where the DC bus voltage is fixed. This paper proposes a PVBESS-DCS solution tailored for regulated DC systems. Within this framework, we present a controllable series voltage source compensating for the voltage differences between the PV and BES sources and the DC bus. Thus, the system can perform PV maximum power point tracking and curtailment control while charging and discharging BES and connected to a regulated DC bus. Additionally, we present a single-stage multi-port partial power processing DC-DC converter designed for the proposed PVBESS-DCS. It utilizes a triple active bridge DC-DC converter topology. This paper presents operating principles, control strategies, simulation results, and experimental findings of the proposed PVBESS-DCS for regulated DC systems.

Index Terms—Battery energy storage system (BESS), DC-series integration, partial power processing, regulated dc bus, solar photovoltaic (PV).

I. INTRODUCTION

Integration of solar photovoltaic (PV) generation and battery energy storage system (BESS) can reduce costs of energy and improve energy availability with more efficient energy management [1]. BESSs can also smooth out the variations of PV power and electrical loads and support grid

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stability and resiliency [2], [3]. For the PV-BESS integration, DC microgrids have been considered as suitable applications because of their high energy conversion efficiency, natural DC interface, and reliable power control [4], [5]. For the DC integration, prior works mainly present DC-parallel system architectures [6], [7]. A conventional DC-parallel integration system consists of two DC-DC converters connected in parallel to the point of common coupling, a DC bus, as shown in Fig. 1 (a). The DC-parallel system enables independent power control and flexible system expansion. However, it requires at least two fully rated power electronic converters that lead to bigger system size, higher cost, and more power conversion losses.

DC-series integration shown in Fig. 1 (b) has recently been proposed as a new PV-BESS integration solution [8], referred to as the PV-integrated battery energy storage system – DC series (PVBESS-DCS) in this paper. This integration method directly connects a PV string and a battery in series, and these energy sources are directly connected to a DC bus. A partial power processing DC-DC converter regulates the compensation current at the DC-series coupling node to enable independent current control of the PV string and the battery connected in series. The PVBESS-DCS has several benefits:

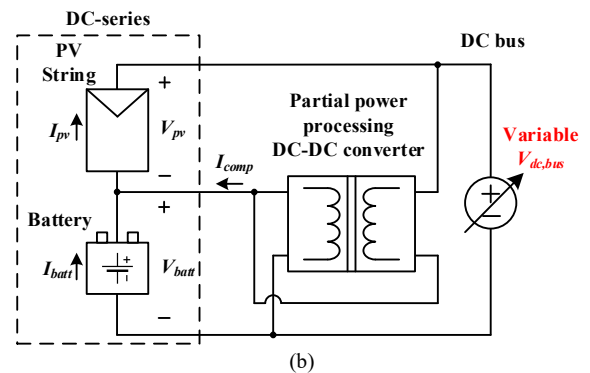
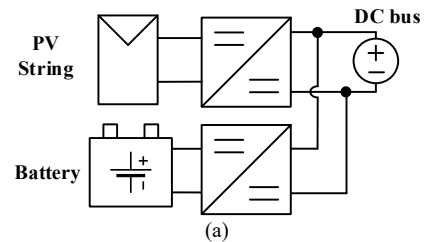


Fig. 1. PV-BESS DC integration: (a) DC-parallel and (b) DC-series.

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- PV voltage support: The battery voltage is added to the PV string voltage so a relatively low-voltage PV string can be connected to the high-voltage DC bus without using a boost converter.
- Reduction of the rated power of power electronic converters: The partial power processing DC-DC converter is the only power electronic converter in the DC power processing loop. Partial power processing [9-11] reduces the required rated power of the power electronic converters. Compared to conventional two fully-rated DC-DC converters, a power electronic converter with a lower-rated power can be used to transfer the same amount of PV power and battery power. Besides, the less processed power, the less power loss.
- Seamless source integration/configuration: PV-only, PV-battery, and battery-only source configurations are available without adding/changing converter circuitry and/or topology.

Although the PVBESS-DCS has many benefits, it has a limitation due to the voltage variations of the PV string and the battery [12]. The PV voltage has to change so the PV string can generate the maximum power, especially when irradiance level and temperature change. The battery voltage changes according to the state of charge (SOC) and the loading condition. Therefore, the voltage of the DC-series terminal—the sum of the PV and battery voltages—has to change, and the DC bus voltage needs to be variable accordingly.

This paper proposes a novel PVBESS-DCS architecture tailored for regulated DC bus systems, such as DC microgrids where the DC bus voltage is generally fixed or slowly changed and independently controlled by the system operator or other power devices. The proposed system adds a controllable series voltage source in between the DC-series circuit and the fixed-voltage DC bus to address voltage discrepancies under varying operating conditions [13]. To realize this approach, we propose a new single-stage multi-port partial power processing DC-DC converter that serves as both the controllable current and voltage sources. This converter is built upon a triple active bridge (TAB) DC-DC converter topology, chosen for its capabilities of bidirectional power flow, galvanic isolation, and multi-port structure.

The paper is organized as follows. Section II introduces the proposed PVBESS-DCS architecture. Section III details the converter circuit topology and control. Section IV presents the simulation and experimental results. Conclusions are discussed in Section V.

II. PV-Integrated Battery Energy Storage System – DC-Series for Regulated DC Systems

A. System Architecture

Fig. 1 (b) illustrates the PVBESS-DCS presented in [8]. A solar PV string and a battery are directly connected in series. The battery supports the PV string as an almost fixed DC voltage bias. The DC-series terminal can be directly connected to the DC bus without voltage amplification devices such as a boost converter. This voltage support function is expressed as

$$V_{pv} + V_{batt} = V_{dc,bus} \quad (1)$$

where V_{pv} is the PV voltage, V_{batt} is the battery voltage, and $V_{dc,bus}$ is the DC bus voltage. Since the battery voltage is determined by the SOC, the PV voltage can be adjusted for maximum power point tracking (MPPT) by controlling the DC bus voltage.

The partial power processing DC-DC converter is working as a controllable current source regulating a compensation current, I_{comp} , which flows into the DC-series coupling node, as shown in Fig. 1 (b). The regulation of the compensation current enables independent battery current control while the PV current, I_{pv} , changes according to the PV string's operating power point. The battery current, I_{batt} , can be determined as

$$I_{batt} = I_{pv} - I_{comp}. \quad (2)$$

The controllable current source also provides a power processing bypass when one of the energy sources is disconnected from the DC-series circuit. Thus, seamless PV-battery integration/configuration is available.

Based on these control principles, the DC bus voltage varies as the PV voltage and the battery voltage change.

In this paper, adding a controllable series voltage source between the DC-series circuit and the regulated DC bus is proposed, as shown in Fig. 2. The series voltage, V_{series} , compensates for the voltage difference, as expressed as

$$V_{dc,bus} = V_{pv} + V_{batt} + V_{series}. \quad (3)$$

The regulation of the series voltage enables the adjustment of the PV voltage while the system is connected to a fixed/regulated-voltage DC bus such as in DC microgrid.

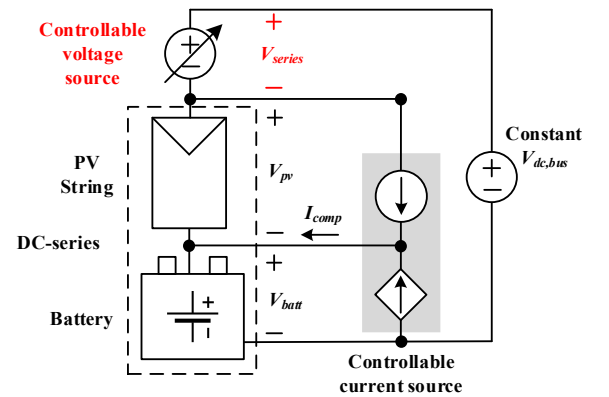


Fig. 2. The proposed PV-integrated battery energy storage system – DC-series for regulated DC systems.

B. Partial Power Processing DC-DC Converter

The controllable current and voltage sources are key components of the proposed PVBESS-DCS. A new single-stage multi-port partial power processing DC-DC converter realizing these two electrical sources is proposed here.

First, the controllable current source can be configured by using the partial power processing DC-DC converter presented in Fig. 1 (b) [8]. It consists of an isolated and bidirectional DC-

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DC converter whose primary side (PS) and secondary side (SS) are connected across the PV string and the battery, respectively. Thus, the converter can be redrawn as shown in Fig. 3 (a)—the PV-battery (PB) converter. The isolation between the PS and the SS and the wiring with the external sources make the partial power processing loop feasible. The PB converter processes only a portion of the resource power according to the partial power processing principle [8]. The rated power of the PB converter, $P_{conv,pb}$, is reduced as

$$P_{conv,pb} = P_{pv} \frac{V_{batt}}{V_{dc1}} - P_{batt} \frac{V_{pv}}{V_{dc1}} \quad (4)$$

where P_{pv} is the PV power, P_{batt} is the battery power, and V_{dc1} is the intermediate DC bus voltage which equals to the sum of the PV voltage and the battery voltage.

The controllable voltage source can be added to the intermediate DC bus in series by using the same partial power processing DC-DC converter topology, but with different source configuration, as shown in Fig. 3 (b)—the series converter. This type of configuration is also called a series-connected boost unit [9] since it can boost the input voltage by adding the series voltage. This configuration is used for solar PV systems [10]. It is also used as an input-parallel-output-series converter in other applications [11]. The PS of the series converter is connected across the intermediate DC bus, and the SS configures the series voltage. According to the partial power processing, the rated power of the series converter, $P_{conv,series}$, is calculated as

$$P_{conv,series} = (P_{pv} + P_{batt}) \frac{V_{series}}{V_{dc2}} \quad (5)$$

where V_{dc2} is the voltage of the output DC bus which is the regulated DC bus in Fig. 2.

Lastly, the PB converter and the series converter are combined, as shown in Fig. 3 (c)—the PV-battery-series (PBS) converter. The intermediate DC bus terminals of the PB converter and the series converter are tied to each other. The PB converter replaces the PS of the series converter. A three-port isolated and bidirectional DC-DC converter is used in Fig. 3 (c). The PS and the SS of the PBS converter work as the PB

converter while they work as the PS of the series converter. Therefore, the PS and the SS of the PBS converter process both the rated powers of the PS converter and the series converter. Since they process the rated power of the series converter together, the power-sharing between the PS and the SS is related to their voltage ratio as

$$P_{conv,pbs,p} = P_{conv,pb} + P_{conv,series} \frac{V_{pv}}{V_{dc1}} \quad (6)$$

$$P_{conv,pbs,s} = P_{conv,pb} - P_{conv,series} \frac{V_{batt}}{V_{dc1}} \quad (7)$$

where $P_{conv,pbs,p}$ and $P_{conv,pbs,s}$ are the rated powers of the PS and the SS of the PBS converter, respectively. The tertiary side (TS) of the PBS converter works as the SS of the series converter since it has not changed. Thus, the rated power of the TS of the PBS converter, $P_{conv,pbs,t}$, is the same as the series converter's rated power.

$$P_{conv,pbs,t} = P_{conv,series}. \quad (8)$$

C. DC Analysis

DC analysis compares system model parameters and rated powers of power electronic converters between the proposed PVBESS-DCS shown in Fig. 3 (c) and the DC-parallel integration method shown in Fig. 1 (a) to study the effectiveness of the proposed system.

TABLE I lists the system model parameters that represent system-level designs of a 380 V and 3 kW residential (load) system with the integration of a 6 kW PV array (200% oversizing rate) and a 3 kW battery—the 200% oversizing rate allows both 3 kW battery charge and 3 kW DC load available under the PV maximum power (MP) condition. This oversizing rate can maximize the usage rate of the PV energy under normal and MP operating conditions. The PVBESS-DCS design has three of 1.88 kW maximum power point (MPP) trackers (the PBS converters) which can connect a single PV string of five 375 W PV panels connected in series. Each MPP tracker can generate PV MP at 171.4 V with the voltage support from the battery (161.5 V) directly connected to the three MPP trackers. On the other hand, the DC-parallel system design has

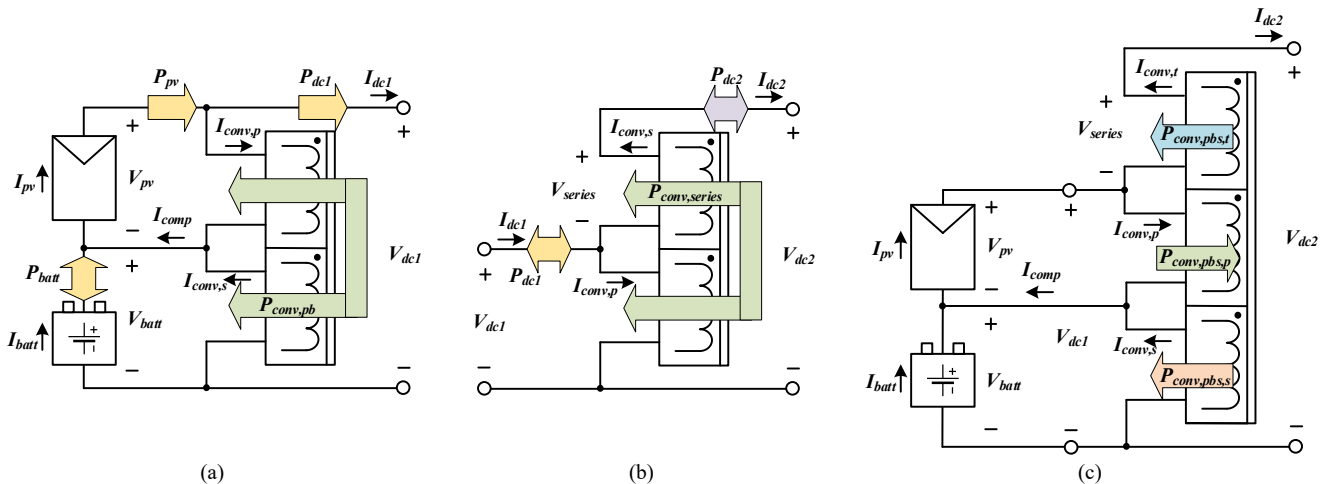


Fig. 3. Partial power processing DC-DC converters: (a) the PV-battery converter, (b) the series converter, and (c) the proposed PV-battery-series converter.

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two 3 kW MPP trackers (DC-DC boost converters) which can connect a single PV string of eight 375 W PV panels connected in series. Each MPP tracker can generate PV MP at 274.2 V. The same battery is used for the DC-parallel system, but it is connected to a separate 3 kW DC-DC boost converter. These system configurations are shown in Fig. 4. The voltage support function from the battery makes the difference between the two system model designs. It can lower the PV string voltage per MPP tracker, which results in more MPP trackers available. The more MPP trackers, the more PV total energy yield with the less partial shading effect.

TABLE I
COMPARISON OF SYSTEM MODEL PARAMETERS BETWEEN THE PROPOSED PVBESS-DCS AND THE CONVENTIONAL DC-PARALLEL INTEGRATION (6 kW PV, 3 kW BATTERY, AND 3 kW LOAD)

Components	Parameter	PVBESS-DCS	DC-Parallel
PV panel	Part number	SPV375-R60JWVG	
PV string @ STC (Single MPP tracker)	Open circuit voltage	207.5 V	332 V
	Short circuit current	11.46 A	
	MPP voltage	171.4 V	274.24 V
	MPP current	10.95 A	
PV array	Maximum power	1.88 kW	3 kW
	# of MPP trackers	3	2
Battery module	Part number	BJ DCB105ZKT	
	Nominal voltage	150 V	
Battery	Rated voltage	161.5 V	
	Rated current	18.6 A	
	Rated power	3 kW	
	Rated power	3 kW	
DC bus	Rated voltage	380 V	
	Rated power	3 kW	

TABLE II
CONTROL MODES OF THE PV-INTEGRATED BATTERY ENERGY STORAGE SYSTEM

#	PV	Battery	DC
1	Curtailment – 100% irradiance (3 kW)	Idle (0 kW)	Load (3 kW)
2	MPPT – 100% irradiance (6 kW)	Charging (-3 kW)	Load (3 kW)
3	MPPT – 10% irradiance (0.6 kW)	Charging (-3 kW)	Source (-2.4 kW)
4	Idle (0 kW)	Discharging (3 kW)	Load (3 kW)

TABLE III
COMPARISON OF THE CONVERTER RATED POWERS BETWEEN THE PROPOSED PVBESS-DCS AND THE CONVENTIONAL DC-PARALLEL INTEGRATION

		PVBESS-DCS	DC-Parallel
Power processed through the converter	Mode 1	1.44 kW (PS) 1.28 kW (SS) 0.16 kW (TS)	3 kW (PV DC-DC) 0 kW (Battery DC-DC)
	Mode 2	4.45 kW (PS) 4.12 kW (SS) 0.33 kW (TS)	6 kW (PV DC-DC) -3 kW (Battery DC-DC)
	Mode 3	1.59 kW (PS) 1.96 kW (SS) -0.37 kW (TS)	0.6 kW (PV DC-DC) -3 kW (Battery DC-DC)
	Mode 4	-1.47 kW (PS) -1.73 kW (SS) 0.25 kW (TS)	0 kW (PV DC-DC) 3 kW (Battery DC-DC)
Converter's rated power		4.45 kW (PS) 4.12 kW (SS) 0.37 kW (TS)	6 kW (PV DC-DC) 3 kW (Battery DC-DC)

To calculate the converter's rated power, four different control modes are considered as listed in TABLE II:

- Mode 1: PV power is the only source providing power to the DC load. 1000 W/m² irradiance is applied. Due to the PV oversizing, PV curtailment control limits the PV power.
- Mode 2: Battery charging command is applied while solar irradiance is 1000 W/m². PV output power is the maximum (6 kW). The PV power provides both the battery charging power and the DC load power.
- Mode 3: Solar irradiance drops to 100 W/m² (10%) while continuing battery charging. The available PV output power is less than the battery charging power. The DC bus provides the remaining battery charging power.
- Mode 4: Battery discharging command is applied when the PV power is not available. The battery provides power to the DC load.

TABLE III presents a comparison of the converter rated powers between the PVBESS-DCS and the DC-parallel system. First, the powers processed through the PS, SS, and TS modules of the PBS converter under the four different control modes are calculated by substituting values in TABLE I and TABLE II for the corresponding variables in the equations (4)-(8). The powers processed through the PV DC-DC and battery DC-DC converters of the DC-parallel system are the same as the PV power and the battery power in TABLE II. The

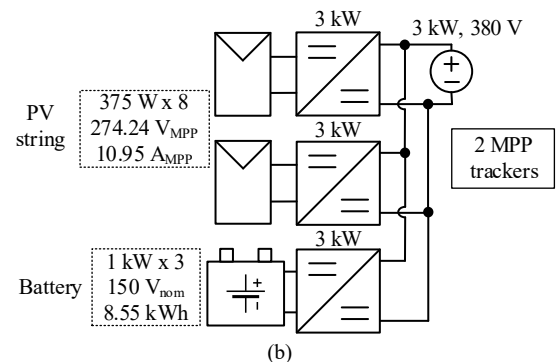
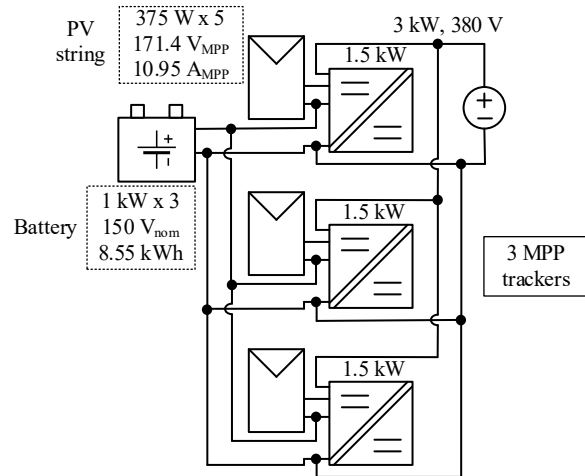


Fig. 4. Modeled system configuration with PV MPP trackers and BESS: (a) Proposed PVBESS-DCS and (b) DC-Parallel.

maximum absolute value of each power is selected as the converter's rated power. Therefore, 4.45 kW PS module, 4.12 kW SS module, and 0.37 kW TS modules are required to handle 6 kW PV, 3 kW battery, and 3 kW DC load. On the other hand, 6 kW PV DC-DC and 3 kW battery DC-DC converters are required to do the same work as the PBS converter does. In summary, owing to partial power processing present in the PVBESS-DCS, only a 4.5 kW three-port DC-DC converter—especially having only a 0.5 kW TS module—is required for the PVBESS-DCS. Therefore, the rated power of the PBS converter is almost 50% lower (4.5 kW / 9 kW) than that of the DC-DC boost converters in the DC-parallel system.

III. CONVERTER TOPOLOGY AND CONTROL

This section describes the circuit topology, passive component design, and the closed-loop control scheme of the proposed PBS converter.

The PBS converter circuit is illustrated in Fig. 5. A TAB DC-DC converter topology is selected since the PBS converter requires capabilities of 1) three DC ports, 2) galvanic isolation, and 3) bidirectional power flow. The TAB converter is composed of three full-bridge (FB) modules, a three-port high frequency (HF) transformer, three leakage inductors, three DC filter capacitors. Besides, two DC filter inductors are added to provide more filtered DC currents to the energy sources. In this work, the single-phase-shift (SPS) control method [14] is used to control power flow through the HF transformer because of its simplicity and wide applications to the dual active bridge converters.

The HF transformer turn ratios are calculated by the DC voltage ratios among the PS, SS, and TS FB modules under the MP condition: PV MPPT & battery charging & DC load (Mode 2 in TABLE II).

$$n_{ps} = \frac{V_{p,mp}}{V_{s,mp}}, \quad n_{pt} = \frac{V_{p,mp}}{V_{t,mp}} \quad (9)$$

where $V_{p,mp}$, $V_{s,mp}$, and $V_{t,mp}$ are the DC voltages of the PS, SS, and TS FB modules under the MP condition. n_{ps} and n_{pt} are the transformer turn ratios of the PS to the SS and the PS to the TS, respectively.

The leakage inductances, $L_{lk,p}$, $L_{lk,s}$, and $L_{lk,t}$, are calculated by the transformer power equation [15] under the MP condition. It is assumed that the magnetizing current is negligible.

$$P_{ps,max} = \frac{n_{ps}V_{p,mp}V_{s,mp}A\varphi_{ps,mp}(1-A\varphi_{ps,mp})}{2f_s(L_{lk,p}+n_{ps}^2L_{lk,s})} \quad (10)$$

$$L_{lk,p} + n_{ps}^2L_{lk,s} = \frac{n_{ps}V_{p,mp}V_{s,mp}A\varphi_{ps,mp}(1-A\varphi_{ps,mp})}{2f_sP_{ps,max}} \quad (11)$$

$$P_{pt,max} = \frac{n_{pt}V_{p,mp}V_{t,mp}A\varphi_{pt,mp}(1-A\varphi_{pt,mp})}{2f_s(L_{lk,p}+n_{pt}^2L_{lk,t})} \quad (12)$$

$$L_{lk,p} + n_{pt}^2L_{lk,t} = \frac{n_{pt}V_{p,mp}V_{t,mp}A\varphi_{pt,mp}(1-A\varphi_{pt,mp})}{2f_sP_{pt,max}} \quad (13)$$

where f_s is the TAB converter's switching frequency, and $P_{ps,max}$ and $P_{pt,max}$ are the MP transferred from the PS to the SS

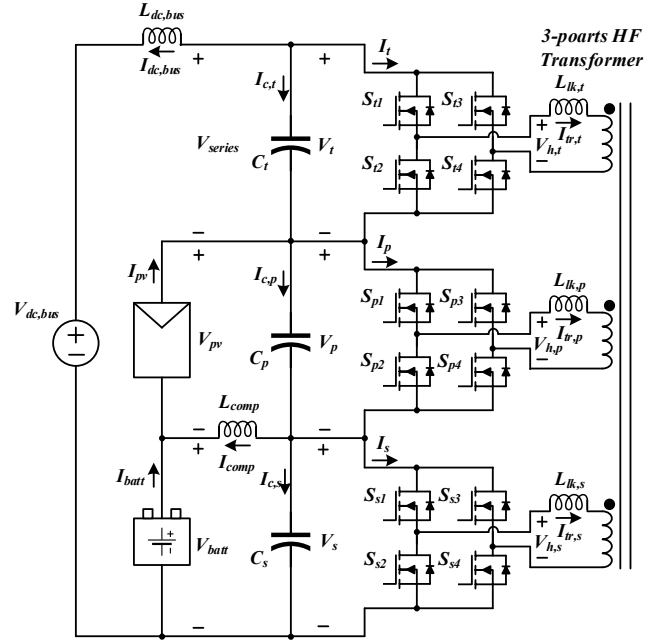


Fig. 5. The PV-battery-series converter circuit.

and from the PS to the TS, respectively. $A_{\varphi_{ps,mp}}$ and $A_{\varphi_{pt,mp}}$ are the phase-shift modulations between the PS and the SS and between the PS and the TS under the MP condition. These phase-shift modulations are calculated as

$$A_{\varphi_{ps,mp}} = \frac{\varphi_{ps,mp}}{\pi}, \quad A_{\varphi_{pt,mp}} = \frac{\varphi_{pt,mp}}{\pi} \quad (14)$$

where, $\varphi_{ps,mp}$ and $\varphi_{pt,mp}$ are the phase angle differences between the PS and the SS and between the PS and the TS under the MP condition, as shown in Fig. 6 (a). The maximum phase angle difference, $\pi/2$, is considered for the calculation.

DC filter capacitors, C_p , C_s , and C_t , decouple the double-switching-frequency current ripple from the FB modules' DC currents, I_p , I_s , and I_t . The PS and SS filter capacitances are calculated under the MP condition that results in the maximum double-switching-frequency current ripple in the PS and SS FB modules' DC currents, as shown in Fig. 6 (a).

$$C_p = C_s = \frac{(I_{tr,p,pk,mp} + I_{p,avg,mp})A_{\varphi_{ps,mp}}}{4f_sV_{p,mp}A_{dv}} \quad (15)$$

where $I_{tr,p,pk,mp}$ is the peak value of the transformer current at the PS under the MP condition, $I_{p,avg,mp}$ is the PS FB module's DC current average, and A_{dv} is the desired DC voltage ripple ratio. The TS filter capacitance is calculated under the zero-power (ZP) condition where the highest voltage across the TS leakage inductor appears due to the PV open-circuit voltage. The PS DC voltage is the maximum, and the TS DC voltage is the minimum, as shown in Fig. 6 (b).

$$C_t = \frac{I_{tr,t,pk,zp}D}{4f_sV_{t,mp}A_{dv}} \quad (16)$$

where $I_{tr,t,pk,zp}$ is the peak value of the transformer current at the TS under the ZP condition, and D is the duty cycle ratio of the PWM signal, which is calculated by dividing the time period

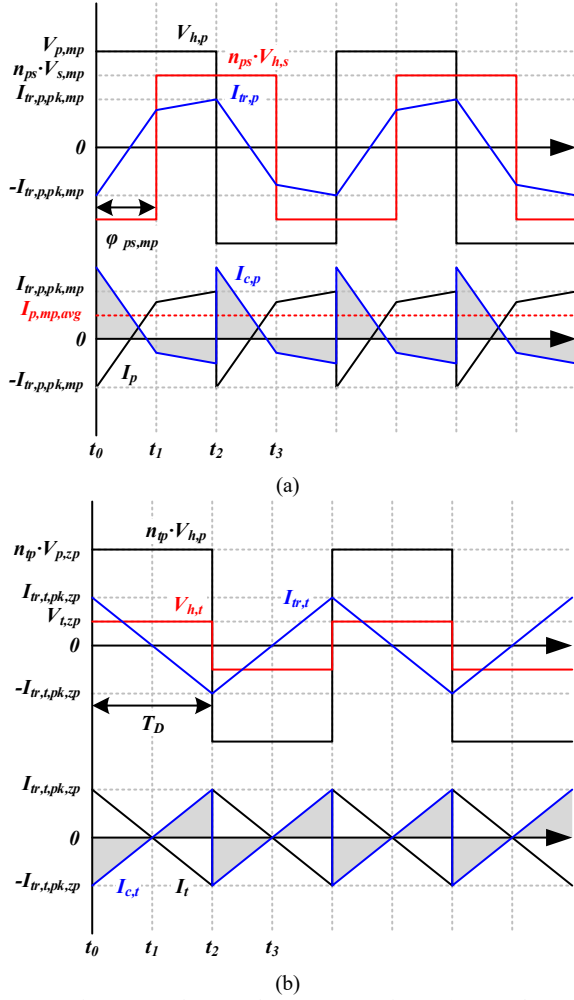


Fig. 6. Transformer's voltage and current waveforms (top) and DC filter capacitor node's current waveforms (bottom): (a) the PS under the MP condition and (b) the TS under the ZP condition.

of the PWM duty cycle, T_D , by the time period of the PWM switching cycle, T_{sw} . In this work, 0.5 duty cycle ratio is applied because of the SPS control mode.

The DC filter inductors, L_{comp} and $L_{dc,bus}$, decouple the HF current ripple further from the FB modules' DC currents. They add HF impedances that are multiple times higher than those of the DC filter capacitors, as shown in Fig. 7 (a). The inductance can be calculated based on the HF ripple attenuation ratio, A_{atten} , expressed as

$$A_{atten} = \frac{I_L}{I_h} \quad (17)$$

$$L_{comp,p} = \left(\frac{1}{A_{atten}} - 1 \right) \frac{1}{\omega_h^2 C_p} \quad (18)$$

$$L_{comp,s} = \left(\frac{1}{A_{atten}} - 1 \right) \frac{1}{\omega_h^2 C_s} \quad (19)$$

$$L_{dc,bus} = \left(\frac{1}{A_{atten}} - 1 \right) \frac{1}{\omega_h^2 C_t} \quad (20)$$

where I_L is the inductor current, I_h is the HF current, ω_h is the angular frequency of the HF current, and $L_{comp,p}$, $L_{comp,s}$, and

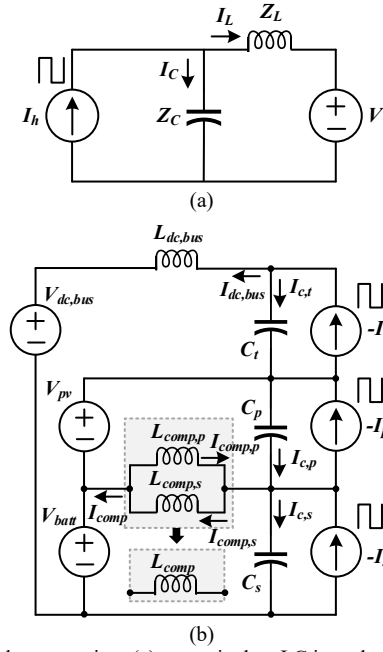


Fig. 7. HF ripple attenuation: (a) an equivalent LC impedance circuit and (b) DC filter inductors added to the proposed converter circuit.

$L_{dc,bus}$, are the DC filter inductances against the PS, SS, and TS DC filter capacitors, respectively, as shown in Fig. 7 (b). $L_{comp,p}$ and $L_{comp,s}$ can be combined in parallel since the $L_{comp,p}$ loop and the $L_{comp,s}$ loop are overlapped because of the DC-series integration.

$$L_{comp} = \frac{L_{comp,p} L_{comp,s}}{L_{comp,p} + L_{comp,s}} \quad (21)$$

where L_{comp} is the total inductance connected to the DC-series coupling node.

Closed-loop control shown in Fig. 8 is developed to determine the phase-shift modulations of the TAB DC-DC converter under varying PV power points and battery charging and discharging conditions. The SPS method generates PWM signals for the three FB modules according to the phase-shift modulations, A_{pps} and A_{pts} , with the base (0.5) PWM duty cycle ratios, D_p , D_s , and D_t . The PS FB module's phase-shift modulation is fixed to zero as the reference. The first PI compensator adjusts A_{pps} to control the battery current. The battery current control reference, $I_{batt,ref}$, is calculated by

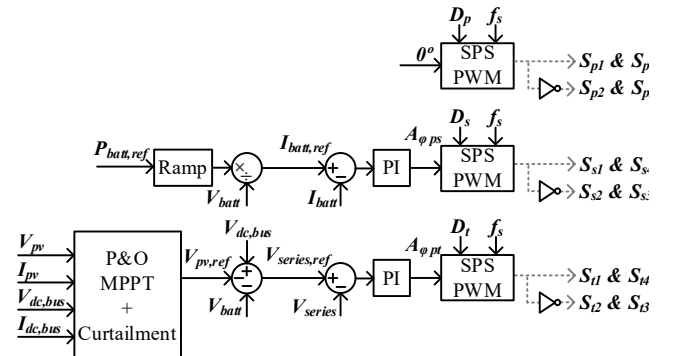


Fig. 8. SPS PWM based closed-loop control including PV MPPT-plus-Curtailment control, and battery charging and discharging power control.

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dividing the battery power control reference, $P_{batt,ref}$, by the battery voltage. The battery power control reference changes with the applied ramp rate. The second PI compensator adjusts A_{opt} to control the series voltage. The series voltage control reference, $V_{series,ref}$, is calculated by

$$V_{series,ref} = V_{dc,bus} - V_{pv,ref} - V_{batt}. \quad (22)$$

where $V_{pv,ref}$ is the PV voltage control reference that is derived from PV MPPT-plus-curtailment control. A conventional P&O MPPT algorithm is used. The curtailment control increases the PV voltage control reference—corresponding to reducing PV output power—if the DC load power is higher than the DC bus rated power [16].

IV. RESULTS

A. Simulation Results

A MATLAB Simulink simulation model including the proposed PBS converter and closed-loop control was developed. In this simulation, only a single MPP tracker for a 2 kW PV string, a 1 kW battery, and a 1 kW DC bus, shown in Fig. 4 (a), was considered. A 1.5 kW PBS converter was modeled, and the converter design parameters calculated by (9)-(21) are listed in TABLE IV. The system model parameters in TABLE I were used for the calculation. To ensure that the phase-shift modulations do not exceed ± 0.5 in the entire control range, 2 kW and 0.2 kW (higher than the rated power) were considered as $P_{ps,max}$ and $P_{pt,max}$, respectively.

Fig. 9 plots the simulation results of the four control modes listed in TABLE II. Fig. 9 (a) shows the system's power,

TABLE IV
CONVERTER DESIGN PARAMETERS OF A SINGLE MPP TRACKER OF THE PBS CONVERTER IN MATLAB SIMULINK SIMULATION (2 kW PV, 1 kW BATTERY, AND 1 kW LOAD)

Parameter	Value	Parameter	Value
$V_{p,mp}$	171.4 V	D	0.5
$V_{s,mp}$	161.7 V	$A_{ops,mp}$ & $A_{opt,mp}$	0.5
$V_{t,mp}$	46.9 V	A_{dv}	0.05 (5%)
$V_{p,zp}$	207.5 V	A_{atten}	0.01 (1%)
$V_{t,zp}$	10.8 V	$L_{lk,p}$ & $L_{lk,s}$	43 μ H
n_{ps}	1	$L_{lk,t}$	79 μ H
n_{pt}	3	L_{comp}	30 μ H
$P_{ps,max}$	2 kW	$L_{dc,bus}$	60 μ H
$P_{pt,max}$	0.2 kW	C_p & C_s & C_t	25 μ F
f_s	20 kHz		

current, and voltage waveforms. Fig. 9 (b) shows the PBS converter's power, current, and phase-shift modulation waveforms. The simulation results validate the feasibility of the controls of the compensation current and the series voltage of the PBS converter, and thereby the PV and battery power regulations. The comparison between the system power and the PBS converter power proves the reduction of the rated power of the power electronic converter with the partial power processing principle.

- Mode 1 (10-40 ms): PV MPPT control started at 10 ms. The PV power increased to 1 kW (the DC bus rated power), and the curtailment control became active. The PBS converter increased the series voltage to 20.5 V (A_{opt} : 0.2) and maintained the 1 kW PV power point (198 V & 5.1 A). To maintain zero battery current, the compensation

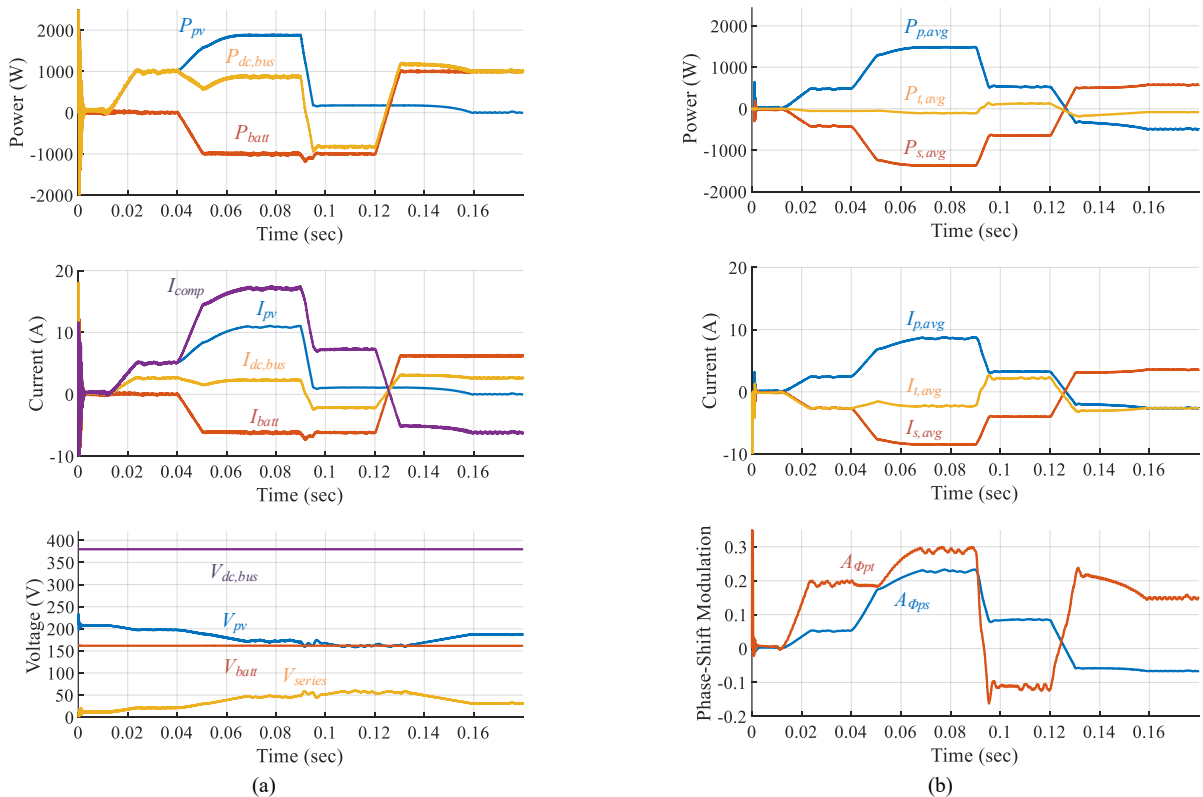


Fig. 9. Simulation results: (a) system's power, current, and voltage waveforms and (b) converter's power, current, and phase-shift modulation waveforms.

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current increased to 5.1 A (A_{ops} : 0.05). The converter processed 0.48 kW (PS), -0.43 kW (SS), and -0.05 kW (TS).

- Mode 2 (40-90 ms): 1 kW battery charging started at 40 ms. The PBS converter increased the compensation current to 17 A (A_{ops} : 0.23) and maintained -6.2 A battery current. The PV curtailment control became inactive as the battery took the PV power, and the series voltage increased to 47.5 V (A_{opt} : 0.3). The 1.9 kW PV MPP was maintained. The DC bus received 0.9 kW. The converter processed 1.5 kW (PS), -1.4 kW (SS), and -0.11 kW (TS).
- Mode 3 (90-120 ms): Solar irradiance dropped to 100 W/m² at 90 ms. The PV power decreased to 0.2 kW, and the PV current decreased to 1.1 A. The PBS converter decreased the compensation current to 7.3 A to maintain the 6.2 A battery charging current (A_{ops} : 0.09). The DC bus sent 0.8 kW to the battery (A_{opt} : -0.12). The converter processed 0.5 kW (PS), -0.65 kW (SS), and 0.13 kW (TS).
- Mode 4 (120-180 ms): 1 kW battery discharging started at 120 ms. The PBS converter decreased the compensation current to -6.2 A (A_{ops} : -0.07) and maintained 6.2 A battery current. The PV curtailment control became active as the battery provided the DC bus rated power (1 kW), and the series voltage decreased to 31.5 V (A_{opt} : 0.15). The PV power decreased to 0 kW. The converter processed -0.48 kW (PS), 0.56 kW (SS), and -0.08 kW (TS).

B. Experimental Results

A 400 W PBS converter hardware prototype was built to demonstrate the proposed system, as shown in Fig. 10. Due to the lab space limitations, a miniaturized version was built to validate the feasibility of the proposed PVBESS-DCS. Therefore, 62.2 V_{MPP} and 340 W PV string, 50 V and 170 W battery module, and 130 V and 170 W resistive DC load are considered, as shown in TABLE V. A FB module having four SiC semiconductor devices (C3M0120090J), gate driving circuits, and a heatsink was designed as a daughterboard. Three

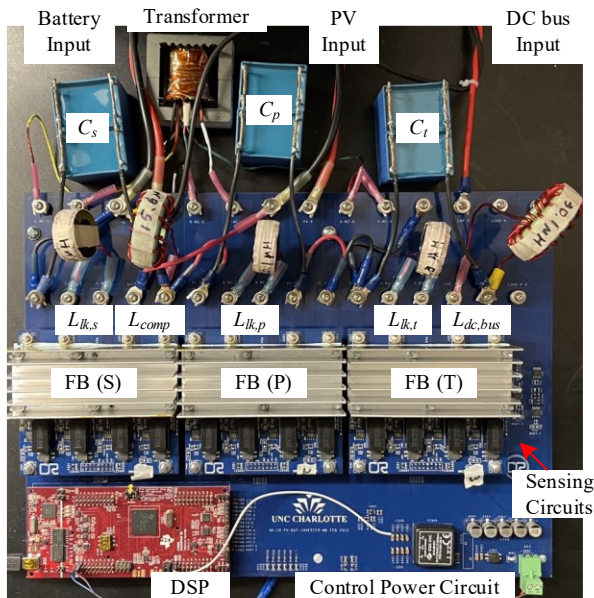


Fig. 10. Hardware prototype of the PBS converter.

TABLE V
SYSTEM CONFIGURATION PARAMETERS AND PASSIVE COMPONENT VALUES USED FOR THE HARDWARE PROTOTPYE OF THE PBS CONVERTER (340 W PV, 170 W BATTERY, AND 170 W LOAD)

Parameter		Value
PV	Open circuit voltage	75.6 V
	Short circuit current	5.6 A
	MPP voltage	62.2 V
	MPP current	5.4 A
	Maximum power	339 W
Battery	Nominal voltage	50.0 V
	Rated current	±3.4 A
	Rated power	±170 W
DC bus	Nominal voltage	130.0 V
	Rated current	±1.3 A
	Rated power	±170 W
FB Converter	f_s	20 kHz
Transformer	Turn ratio	3:3:1 (P:S:T)
	$L_{lk,p}$ & $L_{lk,s}$	23.6 uH
	$L_{lk,t}$	21.7 uH
DC Filter Cap.	C_p & C_s & C_t	58 uF
DC Filter Inductor	L_{comp}	15.6 uH
	$L_{dc,bus}$	30.1 uH

FB daughterboards were mounted on top of the motherboard. The motherboard was designed to have a) reconfigurable power circuits with multiple bushing terminals, b) voltage and current sensors and analog signal conditioning circuits for closed-loop control, and c) a digital micro controller for embedded control interface. The passive components designed for the prototype were connected to the power bushing terminals. The values of the passive components are recalculated according to the system configurations of the hardware prototype. The components are selected/fabricated based on the calculated values. The final values are measured by using an LCR meter and listed in TABLE V. A TI DSP microcontroller board, LAUNCHXL-F28379D, was used to run the SPS PWM generation, the battery current control, and the series voltage control. The PV MPPT-plus-curtailment control and the battery power ramp function were not implemented here to observe the transient responses to the step changes of the control references. The experimental setup was built with AMETEK TerraSAS ETS150 Photovoltaic Simulator, a 50 V DC power supply parallel with a DC electric load, and a 130 V DC power supply parallel with a DC electric load emulating a 340 W PV string, a 170 W battery, and a 170 W regulated DC bus, respectively, as shown in Fig. 11.

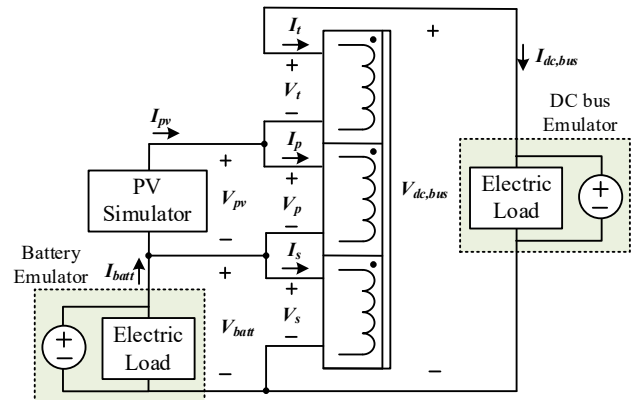


Fig. 11. Experimental setup.

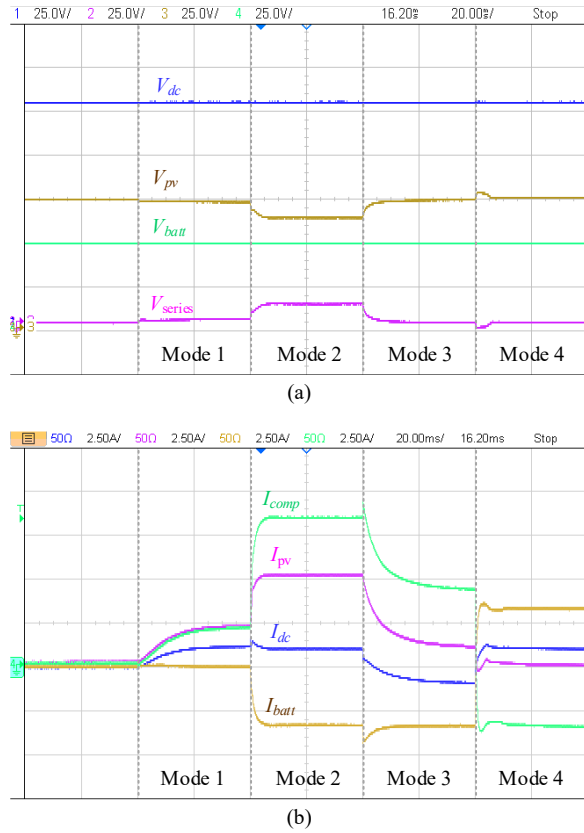


Fig. 12. Experimental results: (a) system voltage waveforms and (b) system current waveforms.

Experimental results are shown in Fig. 12. The voltage and current waveforms validate the operating principle, converter design theory, and simulation results of the proposed PV-BESS-DCS. Like the simulation results, the four control modes were tested. In Mode 3, the PV voltage was increased to reduce the PV output power instead of irradiance drop. The series voltage control reference and the battery current control reference applied for Mode 1-4 were 6.91 V & 0 A, 15.58 V & -3.4 A, 4.90 V & -3.4 A, and 4.90 V & 3.4 A, respectively. The results are summarized below:

- Mode 1: 171 W PV power was generated and transferred to the DC bus. The PV voltage decreased to 73.13 V by increasing the series voltage to 6.55 V. The battery current was maintained as 0.09 A by increasing the compensation current to 2.31 A, equal to the PV current magnitude.
- Mode 2: 336 W PV power was generated and transferred to the DC bus and the battery. The PV voltage decreased to 64.05 V by increasing the series voltage to 15.30 V to generate the maximum PV power. The battery current was controlled as -3.28 A by increasing the compensation current to 8.56 A.
- Mode 3: PV power was dropped to 89 W, and the DC bus provided 110 W to the battery. The PV voltage increased to 74.68 V by decreasing the series voltage to 4.38 V to decrease the PV power. The battery current was controlled as -3.34 A by decreasing the compensation current to 4.50 A.

- Mode 4: 172 W battery power was discharged and transferred to the DC bus. The PV voltage was maintained as 75.63 V. The battery current was controlled as 3.44 A by decreasing the compensation current to -3.28 A.

Current overshoots were observed during the transients of the step changes of the control references. These overshoots occurred due to 1) measurement delay, 2) delay in controlling the PV current from the PV simulator in accordance with the changes of the PV voltage, 3) coupled magnetic path (interaction between A_{ops} and A_{opt}), and 4) slow control response settings (low PI gains). These overshoots can be reduced or almost removed in real-world applications where solar irradiance and temperature change slowly, and battery current ramp rate is limited like our simulation results shown in Fig. 9. In addition, optimal design of closed loop control algorithm such as adding decoupling terms and optimal control gain tuning can improve the control response. At the current stage of the research, a basic and simple control algorithm is employed for the proof-of-concept purpose.

The experimental results verify the feasibility of the independent PV voltage control and battery current control of the proposed system while being connected to a fixed-voltage DC bus or DC microgrid. This independent PV and battery control capability helps users and operators make flexible system operation decisions.

V. CONCLUSION

In this paper, we proposed a novel PV-BESS DC-series integration architecture tailored for voltage-regulated DC bus systems. The key innovation lies in the incorporation of a controllable series voltage source into the DC-series circuit. This series voltage compensates for voltage disparities between the DC bus voltage and the combined PV and battery voltages, allowing dynamic adjustment of the PV voltage to optimize its performance, including PV MPPT and curtailment control. Within the proposed architecture, we employed the concept of partial power processing. A TAB DC-DC converter topology is used. This proposed architecture reduces the rated power of the converter. It enables a 150% power-rated converter to efficiently process 200% power-rated PV string, 100% power-rated battery energy storage, and a 100% power-rated DC load, for 200% oversized PV system. This reduction in rated power can not only shrink the power electronic converter's size but also enhance the overall energy efficiency by reducing the converter power loss. These contributions collectively lead to a more efficient solar-plus-storage system, both in terms of power density and energy yield. To substantiate the feasibility and effectiveness of the proposed PV-BESS-DCS, we provided theoretical analysis, simulation and experimental results that validate its operating principles and practical viability. As the early stage of research, there are many challenges or implications to be solved before the proposed system can be implemented. Future work will present detailed analysis on the enhancement of system efficiency under wide operating range, analysis on control system, and comparison with other converter topology usage.

REFERENCES

- [1] K. Eurek, C. Murphy, W. Cole, W. Frazier, P. Brown, and A. Schleifer, "Representing DC-Coupled PV+Battery Hybrids in a Capacity Expansion Model," Nat. Renewable Energy Lab., Golden, CO, USA, Tech. Rep. NREL/TP-5C00-77917, April. 2021.
- [2] J. Traube et al., "Mitigation of Solar Irradiance Intermittency in Photovoltaic Power Systems With Integrated Electric-Vehicle Charging Functionality," in IEEE Transactions on Power Electronics, vol. 28, no. 6, pp. 3058-3067, June 2013, doi: 10.1109/TPEL.2012.2217354.
- [3] S. Vazquez, S. M. Lukic, E. Galvan, L. G. Franquelo and J. M. Carrasco, "Energy Storage Systems for Transport and Grid Applications," in IEEE Transactions on Industrial Electronics, vol. 57, no. 12, pp. 3881-3895, Dec. 2010, doi: 10.1109/TIE.2010.2076414.
- [4] T. Dragičević, X. Lu, J. C. Vasquez and J. M. Guerrero, "DC Microgrids—Part I: A Review of Control Strategies and Stabilization Techniques," in IEEE Transactions on Power Electronics, vol. 31, no. 7, pp. 4876-4891, July 2016, doi: 10.1109/TPEL.2015.2478859.
- [5] T. Dragičević, X. Lu, J. C. Vasquez and J. M. Guerrero, "DC Microgrids—Part II: A Review of Power Architectures, Applications, and Standardization Issues," in IEEE Transactions on Power Electronics, vol. 31, no. 5, pp. 3528-3549, May 2016, doi: 10.1109/TPEL.2015.2464277.
- [6] T. Dragičević, J. M. Guerrero, J. C. Vasquez and D. Škrlec, "Supervisory Control of an Adaptive-Droop Regulated DC Microgrid With Battery Management Capability," in IEEE Transactions on Power Electronics, vol. 29, no. 2, pp. 695-706, Feb. 2014, doi: 10.1109/TPEL.2013.2257857.
- [7] C. Wang, X. Li, L. Guo and Y. W. Li, "A Nonlinear-Disturbance-Observer-Based DC-Bus Voltage Control for a Hybrid AC/DC Microgrid," in IEEE Transactions on Power Electronics, vol. 29, no. 11, pp. 6162-6177, Nov. 2014, doi: 10.1109/TPEL.2013.2297376.
- [8] N. Kim and B. Parkhideh, "PV-Battery Series Inverter Architecture: A Solar Inverter for Seamless Battery Integration With Partial-Power DC-DC Optimizer," in IEEE Transactions on Energy Conversion, vol. 34, no. 1, pp. 478-485, March 2019, doi: 10.1109/TEC.2018.2873664.
- [9] R. M. Button, "An advanced photovoltaic array regulator module," IECEC 96. Proceedings of the 31st Intersociety Energy Conversion Engineering Conference, Washington, DC, USA, 1996, pp. 519-524 vol.1, doi: 10.1109/IECEC.1996.552937.
- [10] J. -P. Lee, B. -D. Min, T. -J. Kim, D. -W. Yoo and J. -Y. Yoo, "A Novel Topology for Photovoltaic DC/DC Full-Bridge Converter With Flat Efficiency Under Wide PV Module Voltage and Load Range," in IEEE Transactions on Industrial Electronics, vol. 55, no. 7, pp. 2655-2663, July 2008, doi: 10.1109/TIE.2008.924165.
- [11] J. Anzola et al., "Review of Architectures Based on Partial Power Processing for DC-DC Applications," in IEEE Access, vol. 8, pp. 103405-103418, 2020, doi: 10.1109/ACCESS.2020.2999062.
- [12] N. Kim, C. Roy and B. Parkhideh, "A Single-Stage Capacitor-Bridge Boost Converter Topology for PV-Battery Series Integration in Regulated DC Microgrids," 2021 IEEE Applied Power Electronics Conference and Exposition (APEC), Phoenix, AZ, USA, 2021, pp. 2613-2619, doi: 10.1109/APEC42165.2021.9487440.
- [13] N. Kim, "PV-Battery Series Integration for Residential Solar-Plus-Storage Systems," Ph.D. dissertation, Dept. Elect. Eng., Univ. North Carolina, Charlotte, USA, 2022.
- [14] B. Zhao, Q. Song, W. Liu and Y. Sun, "Overview of Dual-Active-Bridge Isolated Bidirectional DC-DC Converter for High-Frequency-Link Power-Conversion System," in IEEE Transactions on Power Electronics, vol. 29, no. 8, pp. 4091-4106, Aug. 2014, doi: 10.1109/TPEL.2013.2289913.
- [15] F. Krismer and J. W. Kolar, "Efficiency-Optimized High-Current Dual Active Bridge Converter for Automotive Applications," in IEEE Transactions on Industrial Electronics, vol. 59, no. 7, pp. 2745-2760, July 2012, doi: 10.1109/TIE.2011.2112312.
- [16] V. Kumar and M. Singh, "Derated Mode of Power Generation in PV System Using Modified Perturb and Observe MPPT Algorithm," in Journal of Modern Power Systems and Clean Energy, vol. 9, no. 5, pp. 1183-1192, September 2021, doi: 10.35833/MPCE.2019.000258.



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