# Modeling The Impacts of Material Properties on Oscillatory Neuron Behavior

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***Abstract*— Neuromorphic computing, which mimics the functions of biological brains, offers improvements in both latency and energy efficiency over typical von Neumann computing architectures. Spiking neural networks can be especially power-efficient because they encode information temporally and can use more sparse electrical inputs [1]. Here, we study the design of volatile memristors (variable resistors with memory) for neuronal devices, with particular consideration toward the feasibility of all-on-chip oscillation using built-in capacitance. We use circuit simulations to model the behavior of oscillator neurons with a range of realistic material properties. We find that energy inputs increase with insulating-phase resistivity, thermal conductivity, and device aspect ratio. However, we also find that the minimum capacitance needed for oscillation decreases with increasing insulating-phase resistivity, which opposes the constraints for power efficiency. Based on published data on $NbO_2$, $VO_2$, and $EuNiO_3$, we find that existing materials can be engineered for all-on-chip spiking using their parasitic capacitance.**

***Index Terms*— memristor, neuromorphic computing, neuronal device, volatility**

## I. INTRODUCTION

With the saturation of Moore's law and increasing demand for computing resources, new computer architectures are necessary [2], [3]. Traditional von Neumann architectures separate data storage from the central processing unit, which is a fundamental limitation on speed and energy. Neuromorphic hardware seeks to mimic biological brains by combining storage and processing [3]. This approach has the same advantages of now-ubiquitous software neural networks in big-data applications, while significantly improving energy efficiency; biological brains are estimated to use one ten-thousandth of the energy of existing hardware [4], [5]. Compared to other next-generation non-von Neumann computational strategies, neuromorphic computing was recently calculated to outperform other technologies, including quantum computing, by at least 10,000-fold in terms of energy per solution [6].

Biomimetic neuromorphic devices fall into two categories: those mimicking synapses by varying their conductance or synaptic weight, and those mimicking neurons by integrating charge and generating a pulse at a certain threshold [7]. Synaptic behaviors have been widely demonstrated in 3-terminal transistors and in 2-terminal memristors, which are dynamic resistors governed by an internal state variable [8]–[10]. Originally theorized by Leon Chua in 1971, the memristor connects flux, the time-integral of voltage, with charge, the time integral of current. Since then, memristive behavior has been identified in many devices [11]. Memristive devices can be nonvolatile, meaning their conductance depends on stimulus but not time, or volatile, meaning their conductance will relax to the initial state over time without a reset stimulus [9], [12].

Here, we focus on neuronal devices, typically implemented as volatile memristive devices, which have received much less attention than synaptic devices. Volatile neuron-like devices can be used for continuous oscillation and implemented in oscillating neural networks, or to emulate more complex biological integration and spiking [1], [13], [14]. Materials with an insulator-metal transition (IMT) are well-suited for this application; previous studies of $VO_2$ and $NbO_2$ have demonstrated multiple neuronal behaviors [13], [15], [16]. Rare-earth nickelates ($R\text{NiO}_3$) are another class of IMT materials that have not been implemented as a volatile neuron devices, despite several studies of nonvolatile memristive behavior [8], [17]–[20]. We include them here because their IMTs span a range of useful temperatures.

The IMT of $VO_2$ is a structural transition that can be driven thermally (occurring around 340 K) or by photoexcitation, and more recent work has shown doping or alloying can raise the temperature up to 390 K [21]. The IMT in these materials can also be electrically driven by leveraging significant Joule heating in the insulating state which dissipates after transition to the metallic state. This electrically driven IMT is characterized by S-type negative differential resistance (NDR) in a current-controlled *I-V* curve or bistable hysteretic *I-V* curves under voltage-control. In $NbO_2$, NDR is first caused by a Poole-Frenkel thermal instability around 400 K and then a sharper NDR is caused by the Mott IMT around 1040 K [22]. Such a high temperature requires more energy per switch, an ideal material would have an IMT around 450 K to reduce energy consumption and prevent environmental switching due to processor heating without active cooling [23]. Therefore, $EuNiO_3$ ($T_{IMT}$  450 K) is included as a potentially useful as a volatile memristive device [24].

In this work, we use circuit simulations to explore the impacts of various measurable properties of IMT materials. A number of mathematical or circuit-level models have been proposed for volatile memristive devices [10], [25]–[27]. Here, we use a physics-based system of equations to define an IMT-based volatile memristive device implemented in LT-SPICE and simulate circuit-level behavior with various realistic material properties.

Experimental implementations of such circuits in $VO_2$ and $NbO_2$ have been successfully modeled with the same equations [13], [15], [16]. This style of oscillator circuit is simple but can be built up into biologically realistic neuristors, simple circuits that mimic the spiking behavior of biological axons [13], [28]. Although local activity modeling is a powerful tool for identifying instability conditions [29], the equations used here are analytically intractable so we take an empirical approach to investigating the impact of material properties on volatile memristor behavior. This approach is widely applicable to any device geometry and any material system with a similar thermally-driven IMT, though it neglects field-driven changes to the conductivity such as ion migration.

## II. MODELS AND METHODS

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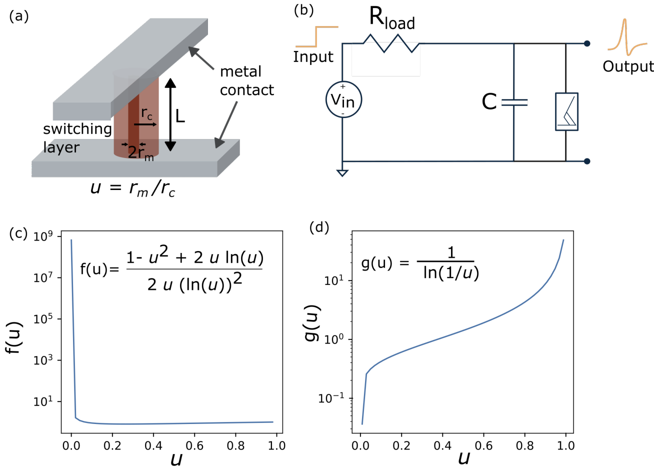


Fig. 1: (a) Schematic of memristor, (b) circuit diagram for Pearson-Anson oscillator, (c) and (d) functions of $u$ included in physics-based model.

### A. Physics-Based Model

The model used here, previously laid out by Pickett and Williams [28], treats the properties of the insulating and metallic phases of the IMT material as temperature-independent. It allows for a general analysis of IMT materials, which can have different underlying conduction mechanisms, and uses commonly measured material properties. The most general form of a memristor relates input current to output voltage by a resistance governed by an internal state variable. In this case, the state variable $u$ represents the ratio of the radius of the metallic-phase channel to the radius of the overall device (Fig. 1(a)). Both are assumed to be cylindrical, such that the metallic phase forms a cylindrical wire within an insulating shell. The governing equation is given by:

$$V = I \cdot R(u). \tag{1}$$

$R(u)$ is found by adding the resistances of the conducting channel and insulating shell in parallel:

$$R(u) = \frac{\rho_{ins} L}{\pi r}\left(1 + \left(\frac{\rho_{ins}}{\rho_{met}} - 1\right)u^2\right)^{-1}. \tag{2}$$

The amount of material in the metallic phase depends on the resistive heating as well as the cooling to the environment. Thus, the rate of change of $u$ is given by

$$\frac{du}{dt} = \left(\frac{d\Delta H}{du}\right)^{-1}(R(u)i^2 - \Gamma(u)\Delta T) \tag{3}$$

Where R(u) is the electrical resistance and $\Gamma(u)$ is the thermal conductivity, given by

$$\Gamma(u) = 2\pi L\kappa\left(ln\left(\frac{1}{u}\right)\right)^{-1}, \tag{4}$$

where $L$ is the device length and $\kappa$ is the thermal conductivity of the insulating phase. $\Delta T$ is the difference between the IMT transition temperature and the ambient temperature—the metallic-phase region is assumed to stay at the transition temperature and the outside of the insulating shell is assumed to be at ambient temperature. Finally, the relationship between the overall device enthalpy $\Delta H$ and state variable $u$ is given by,

$$\frac{d\Delta H}{du} = \pi L r^2\left(\hat{c}_p \Delta T\frac{1 - u^2 + 2u^2 ln(u)}{2u(ln(u))^2} + 2\Delta\hat{h}u\right). \tag{5}$$

Where r is the device radius, $\hat{c}_p$ is the volumetric heat capacity, and $\Delta\hat{h}$ is the volumetric enthalpy of the phase transformation.

In the physical model, $u$ is bounded between 0 and 1, so it can be helpful to understand general trends of $u$ (Fig. 1(c) and (d)). The expression in eqn. 5, $\frac{1-u^2+2u^2 ln(u)}{2u(ln(u))^2}$, which comes from the application of Newton's law of cooling to the temperature assumptions above, makes this system of equations analytically intractable. Additionally, this expression is large ($> 10^2$) for $u < 0.02$, then remains near 1 for $u > 0.1$, which indicates that $\frac{du}{dt}$ is suppressed for small values of $u$. The expression from thermal conductivity (eqn. 4) asymptotically approaches 0 as $u \to 0$ and $\infty$ as $u \to 1$. This means the thermal conductivity is low at high insulating fractions, and the device is more inclined to heat, while the thermal conductivity is very high at high metallic fractions, so the rate of cooling is greater than that of resistive heating.

### B. Quasi-dc Memristor Behavior

The characteristic feature of a volatile S-type memristor *I-V* curve is the region with negative slope, or negative differential resistance, known as the NDR region (Fig. 2(a)) when operated with current control. When current and voltage are low, the memristor has the constant resistance of the fully insulating device; similarly, at high current and voltage, the memristor has the resistance of a mostly metallic device. The region where the memristor switches from high to low resistance is the NDR region. We call the beginning of the NDR region the threshold point, given by $V_{th}$, $I_{th}$, and the end of the NDR region the inflection point, given by $V_{inf}$, $I_{inf}$. The memristor should be biased by setting the input voltage and load resistance so that it operates in its NDR region. The load line, indicated in orange in Fig. 2(a), must intersect the memristor *I-V* curve in the NDR region for the device to oscillate between high and low resistance states. The boundaries for $V_{in}$, $R_L$ constrained by the *I-V* curve in Fig 2(a) are shown in Fig 2(b), which indicates that a higher load resistor (or high line resistance) requires a higher input voltage, and vice-versa.

For increasing current we can assume that before the NDR region begins ($I < I_{th}$), $u$ is low and at the start of the NDR region, $u$ increases rapidly. Assuming $\frac{du}{dt}$ goes from negative (passive cooling overwhelms resistive heating) to positive (resistive heating overtakes cooling) at the threshold voltage ($V_{th}$), it follows that $v^2/R(u \to 0) > \Gamma(u \to 0)\Delta T$. Then a rough approximation can be made:

$$V_{th} = \sqrt{R_{ins}\Gamma(u \to 0)\Delta T}$$

$$= \sqrt{\left(\frac{\rho_{ins} L}{\pi r^2}\right)\left(\frac{2\pi L\kappa}{ln(1/10^{-12})}\right)\Delta T} \approx \frac{L}{r}\sqrt{\rho_{ins}\kappa\Delta T(0.07)} \tag{6}$$

Note that the resistivity in this case is governed by the insulating phase, so the threshold voltage should depend on device radius, transition temperature, and insulating-phase conductivity and resistivity. Also important to note is the fact that we artificially limit $u$ to a low value of $10^{-12}$ to prevent division by 0. In practice, the device might be fully insulating in its ground state, or might oscillate between small and large metallic fractions.

Similarly, the inflection point, at which the metallic phase is large enough to dominate conduction, might occur when $u$ is near 1, or well below it. For example, if a device channel area ($r_c$ in Fig. 1) is large, the value of $u$ need not be high for a sufficient metallic channel area ($r_m$ in Fig. 1) to conduct most of the current. Therefore, relationships intuited from the governing equations are approximate at best, and the remainder of this study focuses on numerical simulation that updates the value of $u$ throughout oscillations.

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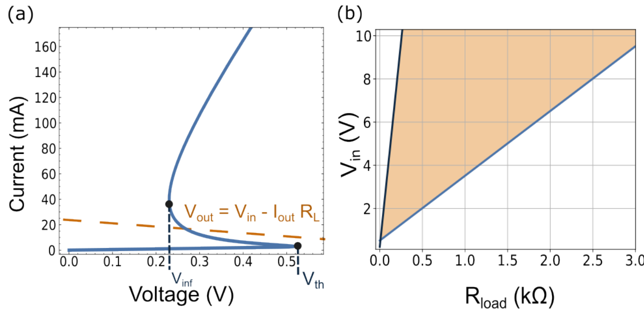


Fig. 2: (a) *I-V* curve of example memristor showing current-controlled negative differential resistance (CC-NDR), two critical points, and load line. (b) Range of input voltage and load resistor for which load line intersects NDR region.

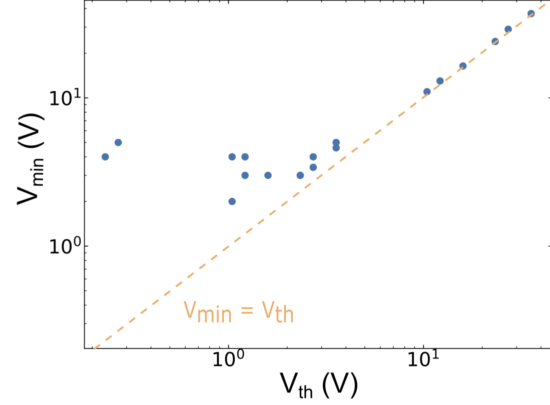


Fig. 3: Minimum voltage input for which oscillations occur in transient simulations vs. threshold voltage from the *I-V* curve.

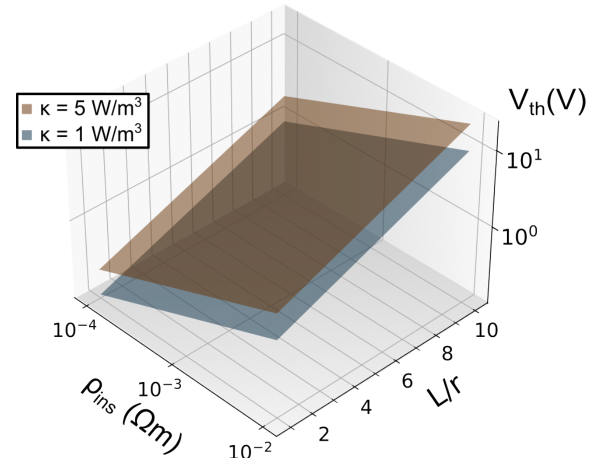


Fig. 4: Threshold voltage vs. insulating-phase resistivity and aspect ratio $L/r$ for both $\kappa = 1$ and $\kappa = 5$

### C. Pearson-Anson Oscillator Circuit

Here, as in previous studies, we focus on the Pearson-Anson oscillator (Fig. 1(b)), as it is both simple and can be leveraged for biologically realistic behavior [15], [28], [30]. A capacitor placed in parallel with the memristor passes most of the current, allowing the memristor to stay insulating, until the capacitor is charged, then it forces current through the memristor, triggering the transition to metallic behavior. When the resistance of the memristor drops, the voltage across the capacitor drops as well, causing it to discharge through the memristor. The timing of this oscillatory behavior is primarily set by the rise time $\tau = R_L C$, where $R_L$ is an additional load resistor, because the falling time as the memristor transitions is generally faster [15]. The time constant must be long enough, however, to allow cooling back to the insulating state between cycles in the case of constant input voltage. Internal capacitances native to IMT devices have been measured in $NbO_2$ and $VO_2$ oscillators and suggest specific area capacitances of 6000 fF/$\mu$m$^2$ and 20 fF/$\mu$m$^2$ respectively. For $\mu$m-scale devices, built-in capacitance is likely limited to 100s of pF, but could be improved by adding a higher dielectric material around the IMT material [31]. If the capacitor is an external component, $\tau$ is easily controlled, however, if the material's built-in capacitance sets C, $R_L$ is the only way to control the time component, adding another constraint besides the biasing regime.

### D. SPICE Model and Statistical Analysis Methods

With so many material parameters involved, we first performed a designed screening experiment to estimate the effect sizes of these parameters on $V_{th}$, estimating how much the dependent variable changes with a change in each independent variable. We chose $V_{th}$ as the dependent variable as an easily-measured proxy for energy consumption. We chose values for real material parameters based on published data, summarized in Table I. Each combination of variables was implemented in the memristor model and its *I-V* curve simulated in LT-SPICE as described elsewhere [28]. We extracted the parameters $V_{th}$, $I_{th}$, $V_{infl}$, $I_{infl}$, and $R_{NDR}$ via numerical differentiation.

Our screening experiment indicated the strongest effect sizes for $\rho_{ins}$, $\kappa$, $r$, $L$, whereas $\Delta T$, $c_p$, $\rho_{ins}/\rho_{met}$, and $\Delta h$ did not have statistically significant effect sizes in this experiment. Importantly, we used $\rho_{ins}/\rho_{met}$ as a variable rather than $\rho_{met}$ to keep with the definition of an IMT material, where $\rho_{met} < \rho_{ins}$. To further reduce the number of variables, we substituted $L/r$ for L and r, based on preliminary simulations that showed minimal change when increasing or decreasing L and r together, keeping $L/r$ constant. We used these three variables in a full-factorial experiment consisting of 8 runs in which each parameter is either the high or low value from its pre-determined range.

For each run, we found the minimum input voltage for sustained oscillation to occur, the minimum capacitance needed at that value. The presence of sustained oscillation in this relaxation oscillator circuit is a useful binarized output value representing device volatility. In order to isolate the roles of input voltage and capacitance, we also identified the minimum capacitance needed for an input of 5 V for all runs where $V_{min} < 5V$.

Although $\rho_{ins}/\rho_{met}$ did not have a statistically significant effect on the *I-V* data, we found that it did impact capacitance values. Therefore we designed an additional experiment in which we held all other variables constant and varied only $\rho_{ins}$ and $\rho_{ins}/\rho_{met}$ to investigate conditions for oscillation. The constant values were $c_p = 1.5{\times}10^6 J/m^3K$, $\Delta h = 2.35{\times}10^8 J/m^3$, $\kappa = 1 W/m{\cdot}K$, and $\Delta T = 50K$. We treated the capacitance as an external component, rather than scaling with the device geometry, so these results apply to both built-in and external capacitors.

## III. Results

First, we find an obvious correlation between $V_{th}$ and the minimum input voltage for $V_{th} > 2V$ (Fig. 3), which supports the use of $V_{th}$ as a predictor of energy consumption. The divergence at low values

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TABLE I: Material properties from literature and range of values used in the model parameter sweeps.

| Parameter | $VO_2$ [13] | $NbO_2$ [28] | $EuNiO_3$ | Model Range |
|---|---|---|---|---|
| $\Delta T$ (IMT temperature - Ambient Temperature 300 K) | 43 K | 800 K | 150 K [24] | 50-500 K |
| $\hat{c}_p$ (volumetric heat capacity) | $3.3\times10^6$ J/m$^3$K | $2.6\times10^6$ J/m$^3$K | $3\times10^6$ J/m$^3$K [32] | 1-$3\times10^6$ J/m$^3$K |
| $\Delta\hat{h}$ (volumetric enthalpy of phase transformation) | $2.4\times10^8$J/m$^3$ | $1.6\times10^8$ J/m$^3$ | $5.8\times10^6$ J/m$^3$ [33] | $2\times10^8$ J/m$^3$ |
| $\kappa$ (thermal conductivity) | 3.5 W/m K | 1.5 W/m K | 5 W/m K[34] | 1-5 W/m K |
| $\rho_{ins}$ (electrical resistivity of insulating phase) | $1\times10^{-2}\Omega$m | $7\times10^{-4}\Omega$m | $1\times10^{-3}\Omega$m [35] | $1\times10^{-4} - 1\times10^{-2}\Omega$m |
| $\rho_{met}$ (electrical resistivity of metallic phase) | $3\times10^{-6}\Omega$m | $1\times10^{-4}\Omega$m | $1\times10^{-5}\Omega$m [36] | $1\times10^{-6} - 1\times10^{-2}\Omega$m |
| Energy/switch (calculated) | $3.8\times10^8$ J/m$^3$ | $2.3\times10^9$ J/m$^3$ | $4.6\times10^8$ J/m$^3$ | |

of $V_{th}$ is due to the line resistance, which is kept at 10 Ω for this study, and could not realistically be reduced in practice.

In the full-factorial experiment, $\rho_{ins}$ had the largest impact on $V_{th}$, while $L/r$ has a slightly smaller impact and $\kappa$ has a much smaller impact, as shown in Fig. 4. Results from runs with different values of $\rho_{met}$ were averaged together in Fig. 4 because the variation due to $\rho_{met}$ was small. The relationships between $V_{th}$ and $\kappa$, $L/r$, and $\rho_{ins}$ are all increasing, as predicted by the intuitive model proposed in eqn. 6. A higher thermal conductivity would compete more with resistive heating and a more resistive device (either higher specific resistivity or larger dimension) would require a higher voltage to pass the same amount of current. For the realistic material parameters used here thermal conductivity plays a much smaller role than the other properties.

However, low $V_{th}$ is not the only figure of merit, compatibility with low capacitance is critical for all-on-chip spiking devices. Across all runs in the full-factorial experiment, we found lower minimum capacitances for $L/r = 10$ than for $L/r = 1$. Although other parameters affected the minimum capacitance, no statistically significant relationships could be extracted, in part because several runs produced no oscillation condition regardless of capacitance. In fact, two devices simulated with different parameters can have identical *I-V* curves (a coincidence of having chosen round numbers for material parameters) but different transient behavior (Fig. 5). As in this example, certain devices with low $L/r$ and low $\rho_{ins}$ had no oscillation conditions.

Because several runs had no oscillation conditions, we performed an additional focused experiment, in which we varied only $\rho_{ins}$ and $\rho_{ins}/\rho_{met}$ and found the minimum capacitance is inversely related to $\rho_{ins}$ and $\rho_{ins}/\rho_{met}$, shown in Fig. 6. The relationship between $C_{min}$ and $\rho_{ins}$ appears linear, while the relationship to $\rho_{ins}/\rho_{met}$ appears to saturate with increasing $\rho_{ins}/\rho_{met}$. The lowest value of $C_{min}$ was approximately 25 fF, while the highest value needed was 60 pF, meaning built-in capacitance is in reach for all the values used. The specific capacitance of $VO_2$ and $NbO_2$ estimated from literature are included in Fig. 6 for comparison.

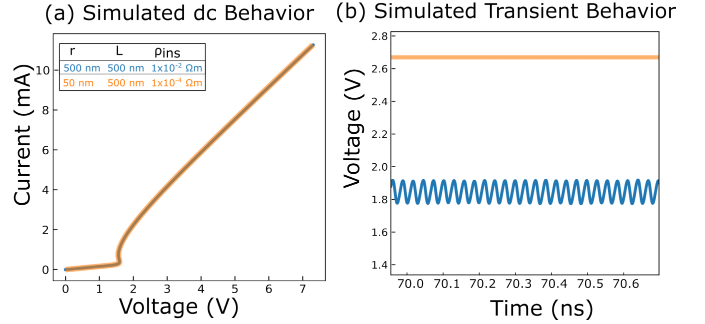


Fig. 5: (a) Simulated dc *I-V* curve for two memristors with different properties, and (b) simulated transient behavior showing one memristor oscillates with an input of 5 V and the other does not.

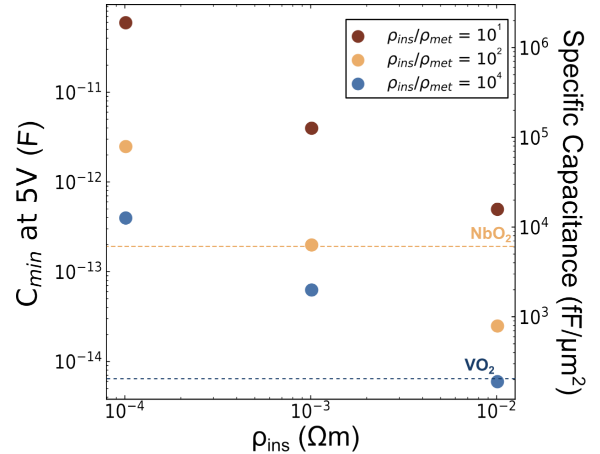


Fig. 6: Minimum capacitance at 5 V and corresponding specific capacitance, along with material values estimated from literature. Other values held constant. [15], [37].

## IV. Discussion

In keeping with the overall goals of energy-efficient neuromorphic computing, low power usage is a key figure of merit for memristors. We focus on the threshold voltage because the input voltage must be at least as large as $V_{th}$, and power is dissipated in the total circuit is proportional to $V_{in}^2$, so it increases faster with $V_{in}$ than with the circuit impedance. We find $\rho_{ins}$ and $L/r$ have larger effect sizes than $\kappa$. However, the device aspect ratio may be the easiest parameter to control when resistivity can vary even between growths in the same study [38], [39].

In addition to low power consumption, we identify whether volatile memristors can function in Pearson-Anson oscillators using their own built-in capacitance. These capacitances are lower than those of typical external components. We find that higher insulating-phase resistivity correlated with lower minimum capacitance for oscillation, in opposition to the low resistivity desired for minimal power consumption. Most of the realistic conditions simulated here were compatible with the best-case built-in capacitance of 500 pF, so balancing these considerations is possible with existing materials.

Using values from literature, $VO_2$ falls at the low end of specific area capacitance, but has a higher resistivity ratio ($10^4$) than $NbO_2$ ($< 10^1$) that allows $VO_2$ devices to operate with lower capacitance. Polymorphs and doped $VO_2$ are approaching the ideal range for $T_{IMT}$, otherwise $VO_2$ devices would require active cooling. $EuNiO_3$ is included in this study despite the lack of previous demonstrations

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due to its near-ideal IMT temperature. Other studies of rare-earth nickelates suggest a high resistvity ratio, but are inconclusive about specific capacitance.

When considering energy per switch, we estimate that all three materials require $10^8$-$10^9$ J/m$^3$ to transition a device from room temperature to its metallic phase (Table I). Despite the lower $\Delta h_{tr}$ of $EuNiO_3$, additional heat required to reach its transition temperature makes the overall energy per switch slightly higher than that of $VO_2$. According to this model for energy use, engineering the IMT transition temperature is a key step in applying these materials to energy-efficient computing.

Further, other circuit parameters impact overall energy use. If $T_{IMT}$ is close to the operating temperature, external cooling may be used and require additional power. The load resistor, which is tuned to each device, also dissipates power while the input voltage is applied. Therefore, we highlight $T_{IMT}$, $\rho_{ins}$, and specific capacitance as important device metrics.

Importantly, this work does not investigate the relationships to neighboring devices. The model we used assumes the exterior of each device remains at 293 K but processors are known to operate well above room temperature (330-350 K) due to resistive heating. Though our models could easily be updated with a smaller $\Delta T$, the expected ambient temperature for a dense array of devices with intentional resistive heating is not obvious. Further, local thermal gradients as some devices switch more than others will add complexity to a system of artificial neurons. The practical considerations of such a system requires further study.

## V. Conclusion

We have systematically studied the impacts of material properties on volatile memristors in Pearson-Anson oscillator circuits. We find that energetic requirements can be modified by material properties–such as thermal conductivity or resistivity–or by device parameters–such as aspect ratio. With the goal of all-on-chip spiking in mind, we also consider how these parameters impact the minimum capacitance that will achieve oscillation. We find that higher insulating-phase resistivity, while correlated with higher power input, allows for lower capacitance, so these goals will have to be balanced. Within this model, we find that resistivity and IMT temperature are critical parameters for implementing both dense and energy-efficient neuronal devices.

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