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A 32-channels readout ASIC for X-ray spectrometry and tracking in the GAPS experiment

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***Abstract*—This work describes the architecture and the experimental results from the characterization of a 32-channels mixed-signal Application-Specific Integrated Circuit (ASIC) developed for the readout of the lithium-drifted silicon, Si(Li), detectors of the General AntiParticle Spectrometer (GAPS) experiment dedicated to searching for dark matter. The instrument is designed for the identification of antiprotons, antideuterons and antihelium nuclei from cosmic rays during an Antarctic balloon mission scheduled for late 2024. A full custom integrated circuit, named SLIDER32 (32-channels Si-LI DEtector Readout) ASIC, has been produced in a commercial 180 nm CMOS technology. The ASIC is comprised of 32 low-noise analog readout channels featuring dynamic signal compression to comply with the wide input range, an 11-bit SAR ADC and a digital back-end section which is responsible for channel setting and for sending digital information to the data acquisition system (DAQ). The circuit design criteria and the experimental results are discussed in the paper.**

***Index Terms*—Low-noise, front-end, CMOS, dynamic signal compression.**

I. Introduction

THE General Antiparticle Spectrometer (GAPS) instrument is a balloon-borne experiment designed to conduct a dark matter search by measuring low-energy (<0.25 GeV/n) antiprotons, antideuterons and antihelium nuclei from cosmic rays. Using a novel detection approach which relies on exotic atom formation and decay, the GAPS program will deliver a high-statistics antiproton spectrum in an unexplored low-energy range, a sensitivity to antideuterons two orders of magnitude better than the current best limits, and a leading sensitivity to low-energy cosmic antihelium nuclei [**?**], [**?**].

The GAPS instrument consists of a precision-timing, large-area time-of-flight (ToF) system [**?**] surrounding a 10-plane tracker with >1000 large area Lithium-drifted Silicon (Si(Li)) detectors and dedicated ASIC readout. These detectors have a diameter of about 10 cm, a thickness of 2.5 mm, and are segmented in 8 strips each. Once biased at -250 V, they can operate at a relatively high temperature (-35 to -45 °C) with a strip capacitance of about 40 pF and a typical leakage current of about 5 nA/strip [**?**], [**?**]. For the readout of these detectors, a full custom 32-channels front-end integrated circuit, named SLIDER32 (32-channels Si-LI DEtector Readout) was designed and fabricated in a commercial 180 nm CMOS technology. This ASIC is the final result of an R&D activity that started in 2018 with the submission of the first 8 channels prototype. The chip includes 32 low-noise analog readout channels to process signals delivered by four 8-strip sensors, an ADC, and a digital back-end. For the correct behavior of the circuit some functional IP blocks are also included. A microphotograph of the die, which has an area of around 10 mm^2, is shown in Fig. **??**. 600 samples of the ASIC were produced in 2021, each included in a 128 pin Plastic Thin Quad Flat Pack (TQFP128) package that covers an area of 14×14 mm^2.

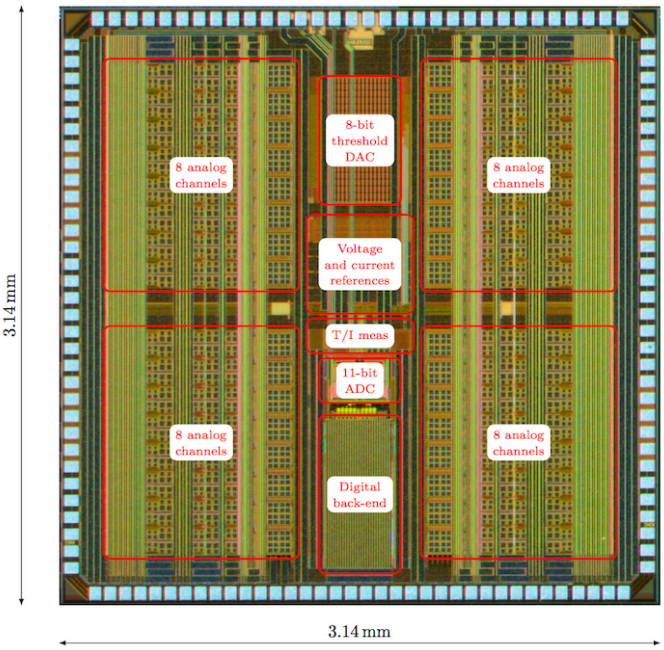

Fig. 1. Microphotograph of the SLIDER32 die. The ASIC takes an area of around 10 mm^2.

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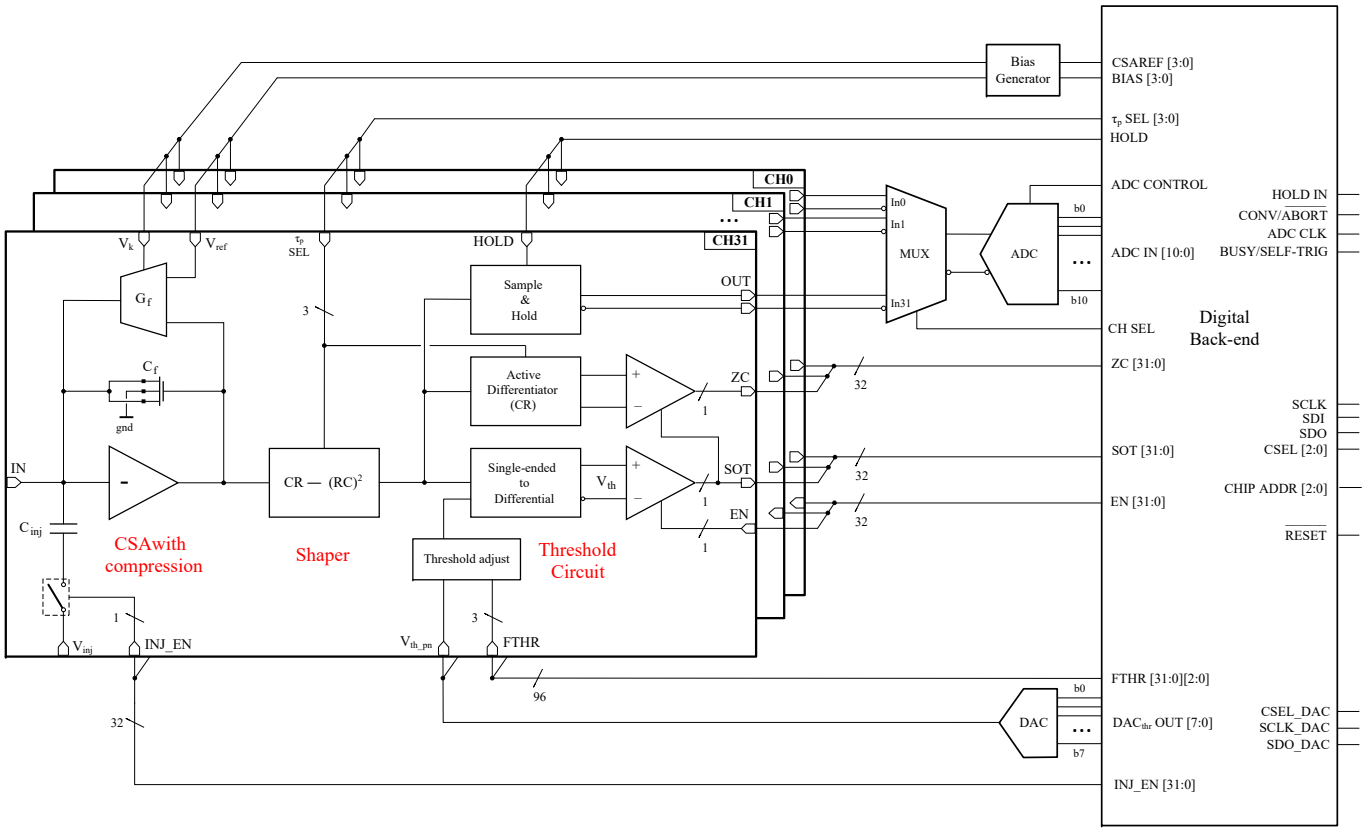

Fig. 2. Simplified block diagram of the SLIDER32 ASIC.

This paper will focus on describing the chip architecture and on the results obtained from the experimental characterization. It is organized in two sections. In Section **??** all the details concerning the architecture of the ASIC are discussed together with the constraints and the requirements determined by the application. In Section **??** the experimental results are discussed with an emphasis on the main analog performance parameters of the front-end. GAPS is currently being prepared for the first balloon flight scheduled in late 2024 from the McMurdo Station in Antarctica. Two follow-up flights are also planned.

II. Chip Description

A. Chip Specifications and Architecture

The SLIDER32 ASIC is mainly comprised of an analog front-end section with 32 low-noise analog readout channels, a digital back-end and additional IP blocks, among which is an 11-bit hybrid Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC). To save space, only one ADC per ASIC is used and an analog 32:1 multiplexer, controlled by the digital back-end, is used to connect the output of each channel to the converter. A simplified view of the ASIC block diagram is shown in Fig. **??**. The following sections provide a brief description of each block.

B. Analog Front-End

A low-noise charge-sensitive amplifier (CSA) integrates the current signal delivered by each strip of the Si(Li) detectors. To comply with the wide input dynamic range, while preserving good resolution at low energies, a non-linear n-channel MOS capacitor (C_f) featuring dynamic signal compression is used in the amplifier feedback loop [**?**], [**?**]. Charge restoration is achieved by a continuous-time Krummenacher network that allows the preamplifier to operate at detector leakage currents up to 10 nA per strip [**?**]. The amplifier is followed by a time invariant filter, which implements a second-order CR-$(RC)^2$ semi-Gaussian weighting function with 8 selectable peaking times (τ_p sel) tunable from 0.25 µs to 1.6 µs. After the amplifier and the filter, a single-ended to differential sample-and-hold (S&H) stage stores the peak value of the signal at the filter output and feeds it to the subsequent differential 11-bit SAR ADC for digitization (OUT). Depending on the operating mode, the sampling signal (HOLD) can be provided either from outside or inside the ASIC. In flight, the chip will be operated in *external-trigger mode* with the sampling signal generated by the ToF system. During calibration, instead, a *self-trigger mode* will be adopted. In this latter configuration, the time at which the signal peak occurs is detected by differentiating the signal at the shaper output, and by driving a zero-crossing discriminator with it. The zero-crossing discriminator output signal (ZC) is then fed to the sample-and-hold. To avoid spurious triggering due to noise, this discriminator is armed only when a signal over threshold is detected. To this purpose, the signal at the shaper output is also converted from single-ended to differential, and then is compared to a preset

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differential threshold (V_{th_pn}) of a discriminator which may generate a Signal-Over-Threshold (SOT) pulse. A 3-bit binary weighted DAC for fine threshold trimming (FTHR) is available in each channel. The comparator output of noisy channels can be disconnected by a programmable "kill mask" (EN). All channels are also equipped with an individual charge injection circuit for test and calibration purposes. The circuit consists of an injection capacitance (C_{inj}=1.18 pF) and an injection voltage (V_{inj}) provided from the outside by a commercial 16-bit DAC. The channels to be injected with a test pulse can be selected by a programmable "inject mask" (Inj_en). A detailed discussion of the channel architecture and performance was provided in [**?**].

To be suitable for application in the GAPS experiment, the analog front-end must comply with the main requirements reported in Table **??**. The readout channel must be able to resolve both X-rays in the range of 20 to 100 keV and charged particles with energy depositions up to 100 MeV. In the X-ray detection region, a resolution <4 keV FWHM for a 40 pF detector capacitance is required to clearly distinguish X-rays from antiprotonic or antideuteronic exotic atoms. The readout electronics of the ASIC, which is expected to run at a temperature of about -40 °C, has to comply with a detector leakage current in the order of 5-10 nA per-strip. The power dissipation should be limited to less than 10 mW/channel to be compatible with the balloon nature of the experiment.

C. Analog-to-Digital Converter

SLIDER32 is provided with an analog-to-digital converter that makes it possible to keep sensitive analog signals within the chip and to minimize external components on the front-end PCB. ADC requirements include a bit size corresponding to about 1 keV in the X-ray energy range, a full scale of 11 bits, a power consumption of the order of 1 mW, and a conversion time of the order of 1 µs. Because of the high grade of nonlinearity of the analog front-end and its resolution of about 1.7 keV RMS for X-rays, a linearity close to 10 bits is adequate to calibrate the transfer function without worsening the double peak identification capability of the tracker. Since the ADC is shared between all channels, its footprint on the power budget per channel is negligible, while the conversion time needs to be fast enough to have no impact on the dead time of the instrument.

TABLE I
FRONT-END ELECTRONICS REQUIREMENTS

Channels per ASIC	32
Nominal operating temperature	-40 °C
Power dissipation	≤10 mW/ch
Signal polarity	electrons
Dynamic range	10 keV-100 MeV
Analog Resolution (@ C_D=40 pF)	4 keV (FWHM)
ENC (@ C_D=40 pF)	480 e^- rms
detector capacitance	40 pF
Threshold	20 keV
Detector leakage current	5 nA
Event rate	100 Hz

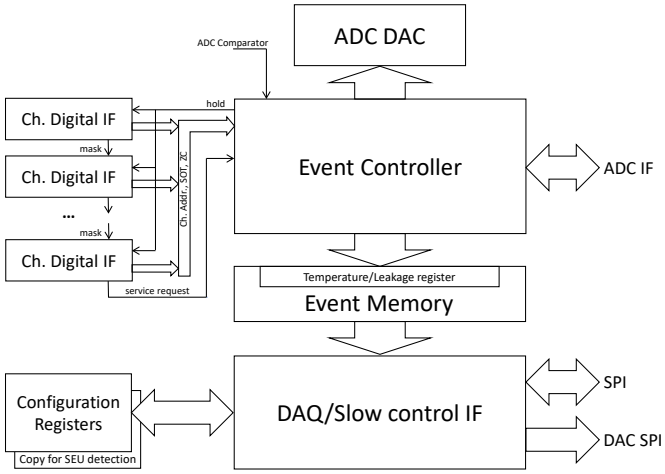

Fig. 3. Simplified block diagram of the Digital Back-End circuit.

The ADC was realized in a differential, capacitive-resistive hybrid SAR architecture [**?**] that makes it possible to fulfill the specifications without resorting to the use of calibration circuitry. Both capacitive and resistive DACs have a resolution of 5 bits (the MSB being determined by the sign of the sampled differential input), and the input capacitance (∼3 pF) was minimized to reduce the load to the S&H buffers. The input range is from -1.8V to +1.8V, and the power consumption of the analog core (including the digital buffers controlling the DAC switches) is 330 µW on average with a clock of 20 MHz and a full swing sinusoidal input, while the peak power consumption of the resistive DAC is 480 µW for code '10000'. The static power of the ADC is due to the comparator differential preamplifier, which is always active, and amounts to 210 µW. Lastly, the digitization of each channel requires fifteen clock cycles, the first three are used to allow S&H buffer settling during the sampling phase, eleven cycles are required to perform the A-to-D conversion, and the last one is used to store the result on the event memory. Details about the design and the performance of the ADC will be reported in another article.

D. Digital Back-End

The digital back-end circuit is responsible for the ASIC configuration, the event and housekeeping parameter digitization, the self-trigger handling, and the event data transfer to the tracker data acquisition (DAQ) system. It also makes it possible to control an external 16-bit calibration DAC for V_{inj} generation by means of a dedicated SPI port (CSEL_DAC, SCLK_DAC, SDO_DAC). Its simplified block diagram is shown in Fig. **??**. The main requirements for its design are to provide a minimal interface with the DAQ, which is to be shared between six ASICs controlled by the same acquisition channel to reduce routing needs, and to operate at a clock frequency of at least 10 MHz to keep the dead time of the tracker manageable. All digital signals interfacing SLIDER32 with the DAQ (ten in total) are differential CMOS to minimize the charge injection at the channel inputs due to stray capacitive coupling. Differential CMOS signaling was

also chosen over LVDS (Low Voltage Differential Signaling) to avoid the large static power consumption of the line drivers.

The back-end circuit is divided into two sections. The first one, that controls the event acquisition and digitization, is composed of the digital interfaces with the analog channels (SOT and ZC signals, channel address), the event controller that manages the analog multiplexer (Ch sel), the DAC controlling the SAR ADC (ADC Control), and the event memory, which is implemented as a FIFO. A HOLD signal issued by the DAQ samples the channel outputs and latches the SOT signals, while the subsequent CONV/$\overline{\text{ABORT}}$ signal activates the ADC control block, which is otherwise forced to a reset state when this signal is not active. An external ADC clock, also provided by the DAQ, advances the event digitization while the ASIC provides an open-drain BUSY feedback to notify the DAQ when operations are completed. According to the ASIC configuration, the event acquisition can convert all channels (full acquisition mode) or just the ones whose output is above the threshold (SOT active, zero-suppression acquisition mode). In any case, after all relevant channels are read out, the selected housekeeping parameter (external temperature sensor or leakage current of a given channel) is digitized and stored in a dedicated register before releasing the BUSY signal. The last digitized value of the housekeeping parameter can then be read out from the ASIC whenever it is required. The ZC signals from the channels are masked according to the discriminator configuration, OR'ed and then used to trigger a D-type flip-flop that is enabled when the self-trigger mode is active. Since they are temporally separated, the BUSY and self-trigger outputs share the same differential pins to reduce the number of external connections.

The second section of the digital back-end circuit takes care of the slow controls and data communication protocols with the DAQ. It comprises a slave SPI interface (SCLK, SDI, SDO) that incorporates a command interpreter, the ASIC configuration registers (implemented in dual redundancy to detect Single Event Upset (SEU) events for potential application in space missions), and a master SPI to control the external calibration DAC. The ASIC slave SPI is selected using three address bits (CSEL) that allow for six individual devices to be controlled by the DAQ channel plus a broadcast address (address '111') for common register writing, while the remaining code is used as the reset state of all the connected SPIs. The configuration registers are set and read individually, and include the acquisition mode, the trigger mode, the shaper time constant, the global and fine energy thresholds adjustments for each channel, the discriminator mask, the calibration mask, the housekeeping parameter selection, and the bias trimming. The event data command provides error codes if no data is available in zero-suppression mode (all SOT are not active) or if data is requested when an event acquisition is not active. The ASIC SPI and interpreter state machines are kept in a reset state when the ASIC address is not selected. The SPI output is a three-state output to allow other ASICs in the chain to communicate with the DAQ.

The two digital back-end sections were optimized, considering corner models of the digital libraries both at room temperature and at -40°C, for clock frequencies up to 50 MHz with power consumption of the order of 1 and 2 mW respectively. To minimize interference on the analog section by the digital circuitry, the latter was integrated inside a deep N-well and surrounded by a grounded guard ring.

E. IP Blocks and bias

Beside the aforementioned structures, the SLIDER32 chip also includes some IP blocks that are necessary to the operation of the ASIC.

For the proper bias of the blocks in the analog readout channel, a fixed current of 5 μA is generated starting from a precise Bandgap Voltage Reference (BGR). Because there is inevitably some variation in the current due to mismatch in devices of the V-to-I converter, a 3-bit DAC has been introduced for reference current trimming.

An 8-bit D/A Converter based on a current steering architecture has been designed. This IP block is responsible for setting the amplitude of a differential voltage, V_{tp}-V_{tn}, used by the threshold generator to generate the Signal-Over-Threshold (SOT) comparator threshold voltage. In addition to this global threshold setting, which is common to all the 32 channels, a 3-bit-DAC is available in each channel for individual channel fine threshold trimming.

To work properly, the ASIC must be biased with the following voltages: AVDD=1.8 V for analog core, DVDD=1.8 V for digital core, DVDD/IO=1.8 V for digital I/O pads and 3V3DVDD/IO=3.3 V for digital I/O pads that interface with the 16-bit calibration DAC.

III. Chip Performance

The SLIDER32 ASIC was fabricated in 2021. Of the 600 available samples, 535 were tested with a dual purpose: on the one hand to verify the performance of the circuit, on the other to select at least 300 good samples to be used for the assembly of the GAPS Si(Li) tracker. To verify the performance of the ASIC, and in particular of the analog readout channel, a reduced set of 10 devices was tested at the temperature of -40 °C expected for the experiment. Since these devices were tested with different bias settings, only the results from subsets of samples that are homogeneous in terms of bias conditions will be shown below. For circuit validation and selection, all the 535 devices have been tested at room temperature. All the tests were performed without detector, by exploiting the injection capacitor integrated in each channel.

A. IP Blocks, ADC and power consumption

In this Section, results related to IP blocks and ADC are provided with the only purpose to prove their functionality.

The reference current, generated with a V-to-I converter starting from the BGR voltage, was evaluated thanks to a current monitor that makes this current available for measurement at the ASIC output. In Fig. **??** the mean value and spread of the reference current is reported as a function of the 3-bit setting (Bias) for 10 samples measured at 27 °C. It is possible to see that, among the 8 bias settings, the ones closest to the 5 μA reference value are 101 and 110. The reference current has also

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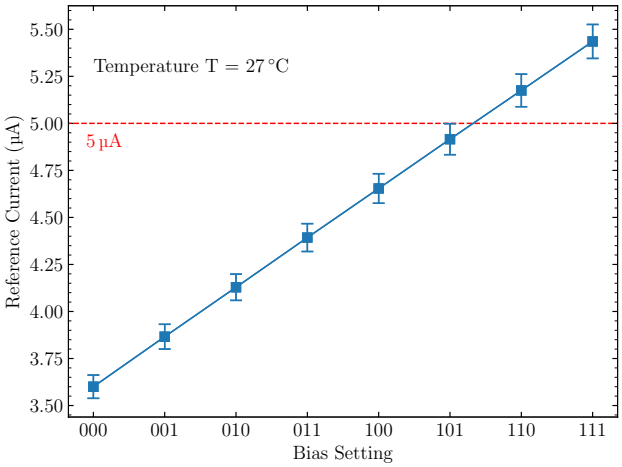

Fig. 4. Mean value and spread (in terms of standard deviation) of the reference current as a function of the 3-bit bias setting from 10 samples measured at 27 °C. The dashed line shows the nominal value of 5 µA expected from design.

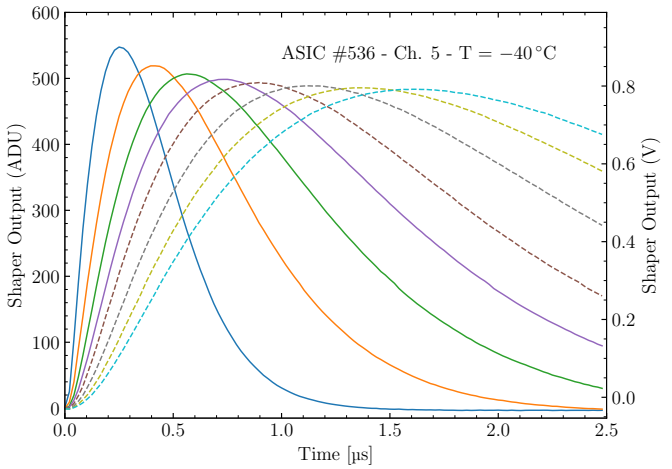

Fig. 5. Digitized waveform reconstructed at the output of the analog channel, after pedestal subtraction and for an input particle energy of 841 keV at the eight selectable peaking times. The ADU (Analog-to-Digital Unit) is the width of the ADC bins: 1 ADU=1.76 mV.

been measured at temperatures varying from -40 °C to 30 °C. A temperature coefficient of -130 ppm/°C was measured over this temperature range and an increase in the reference current of about 50 nA, with respect to the value measured at ambient temperature, is observed when the ASIC is operated at -40 °C.

The 8-bit DAC for global threshold setting provides a differential voltage to the threshold generator with a resolution of 1.6 mV that translates into a threshold resolution in energy of 5.83 keV. The 8-bit DAC has a maximum Differential Non Linearity (DNL) of 0.09 LSB and a maximum Integral Non Linearity (INL) of 0.55 LSB. The 3-bit DAC integrated in each channel allows for further fine-tuning of the threshold in a range of 40 keV with a resolution of 5 keV.

The 11-bit ADC has been fully characterized by using an external 16-bit DAC connected to a dedicated input of the ASIC. Preliminary results obtained using clock frequencies up to 24 MHz (conversion time down to 625 ns) have shown that no missing codes are present and the average resolution is 9.8 effective number of bits (ENOB).

The overall power consumption of the ASIC operated in the idle condition is 264 mW, including both analog and digital sections, resulting in 8.2 mW/channel which meets the experiment requirement. These values were provided directly by the Keysight N6705C Power Analyzer used to supply the ASIC.

B. Channel time response, sensitivity and dynamic range

To evaluate the time response of the analog channel, a digitized waveform was reconstructed at the shaper output by running the ASIC in external-trigger mode and changing the delay between the voltage step that triggers the internal injection circuit and the S&H sampling signal. The result of this digitizing procedure is shown in Fig. **??** for one channel and for the 8 peaking time settings. The plot is expressed in ADU (Analog-to-Digital Unit) as read at the output of the ADC, and also converted in volts (1 ADU=1.76 mV). It can be seen that the filter provides a good unipolar semi-Gaussian CR-(RC)^2 shape, with peaking times (τ_p) from around 0.25 µs to 1.60 µs.

For each peaking time setting, the input-output transcharacteristic of the full analog readout channel, shown in Fig. **??**, is obtained by measuring the peak value of the differential signal digitized at the output of the S&H as a function of the energy released in the detector. As expected, the characteristic exhibits an almost bilinear shape, as it is also evident from the plots of the sensitivity and the relevant resolution shown in Fig. **??**. In the X-ray detection region (energy lower than 100 keV), the channel provides a sensitivity of around 1 ADU/keV (1.76 mV/keV) which makes it possible to satisfy the requirement to have a resolution of 1 keV. In the heavy particle detection region (higher than 10 MeV) the sensitivity decreases and tends to a value of 0.01 ADU/keV (10 µV/keV) with a resolution of 100 keV. As shown in [**?**], this change in channel sensitivity is due to the dynamic compression implemented in the CSA, whose equivalent feedback capacitance C_f adapts from 175 fF, in the X-ray detection region, to 14.7 pF in the heavy particle detection region. The zero in the CSA transfer function introduced by the charge restoration stage affects the gain, that slightly decreases with the peaking time.

The results of the measurement, performed at the temperature of -40°C on 3 samples (96 channels), are reported in Table **??**. The mean value and the standard deviation of the peaking time and the channel sensitivity for both X-ray and particle detection regions are shown. It must be noted that the channel gain is sensitive to the temperature. The tracker is cooled by a passive oscillating heat pipe (OHP) system [**?**] that can control the -40°C temperature required for Si(Li) detector operation. However, both variability of channel sensitivity due to process mismatch and changes due to temperature variations will be compensated for with a specific in-flight calibration procedure that exploits the features of the injection circuit.

As a last remark, it must be noted that, due to a limitation in the calibration circuit, the measurement of the input-output

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TABLE II
MAIN CHANNEL PERFORMANCE AS OBTAINED FROM 3 ASICS (96 CHANNELS).

Peaking Time		Gain		ENC_{FWHM}		$dENC_{FWHM}/dC_D$
Setting	τ_p	X-ray	Particle	C_D=0	C_D=40 pF	C_D=15÷68 pF
#	[µs]	[ADU/keV]	[ADU/MeV]	[keV]		[eV/pF]
0	0.26 ± 0.01	1.49 ± 0.12	12.49 ± 0.10	2.74 ± 0.41	4.40 ± 0.62	129.31 ± 43.10
1	0.41 ± 0.01	1.29 ± 0.09	11.91 ± 0.15	2.81 ± 0.35	4.06 ± 0.46	76.98 ± 4.57
2	0.57 ± 0.01	1.19 ± 0.07	11.65 ± 0.10	2.88 ± 0.36	4.00 ± 0.42	58.20 ± 3.24
3	0.73 ± 0.01	1.14 ± 0.06	11.53 ± 0.10	2.98 ± 0.40	4.02 ± 0.42	47.51 ± 2.32
4	0.89 ± 0.02	1.11 ± 0.06	11.47 ± 0.10	3.04 ± 0.42	4.05 ± 0.41	43.74 ± 1.97
5	1.14 ± 0.02	1.07 ± 0.05	11.42 ± 0.10	3.18 ± 0.46	4.12 ± 0.43	40.47 ± 2.79
6	1.38 ± 0.03	1.05 ± 0.05	11.38 ± 0.10	3.28 ± 0.50	4.13 ± 0.43	33.55 ± 3.55
7	1.63 ± 0.03	1.03 ± 0.05	11.368 ± 0.10	3.40 ± 0.55	4.20 ± 0.44	29.97 ± 3.93

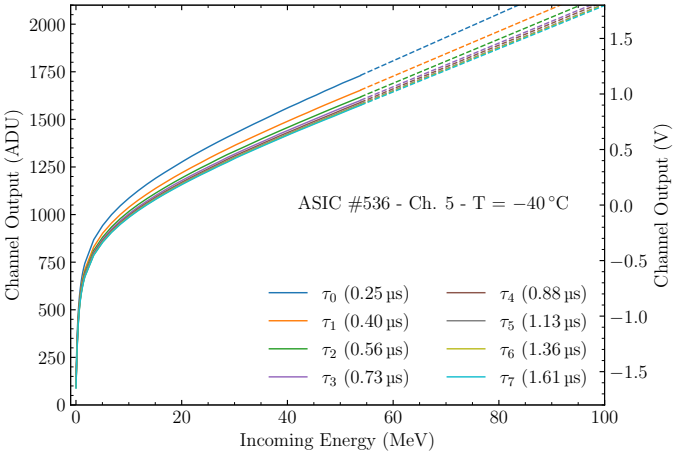

Fig. 6. Amplitude of the differential signal at the output of the sample-and-hold measured (continuous lines) as a function of the energy released in the Si(Li) strip detector. Dashed lines provide the extrapolation to the input dynamic range limits.

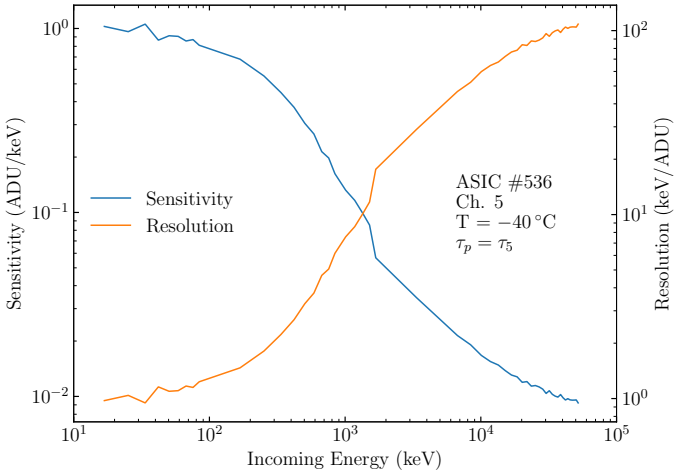

Fig. 7. Sensitivity and resolution of the analog read-out channel with dynamic compression.

trans-characteristic of the readout channel was limited to a maximum value of 55 MeV. Nonetheless, from the extrapolation provided in Fig. **??** (dashed lines), it can be seen that, thanks to the compression implemented at CSA level, the channel can fit an input dynamic range that extends up to 100 MeV into the -1.8 to +1.8 V rail-to-rail input dynamic range of the ADC.

C. Threshold Dispersion

The calibration strategy of the ASIC relies on one or more X-ray sources that will be applied to the sensor to properly anchor the characteristic of each channel to the energy scale. During this test, the ASIC is operated in self-trigger mode and the discriminator threshold is chosen with the aim of optimizing the detection efficiency of the system, that is, to maximize the rate of detected true events without having the system flooded with false, noise-induced hits. Due to mismatch in the CMOS process, in a multichannel system we can have channels with a low threshold that are susceptible to noise hits and channels with a high threshold, that may miss some true hits. Since threshold dispersion requirements cannot be guaranteed by design, a 3-bit DAC for fine threshold tuning is included in each channel. This number of bits and the relevant resolution were chosen by considering results provided by Monte Carlo simulations, according to which a threshold dispersion with a standard deviation of about 10 keV was expected, following the criteria discussed in [**?**].

Per-channel threshold adjustment is performed in two steps, using both the 8-bit DAC for global threshold setting and the 3-bit DAC for fine threshold trimming. First, a threshold scan procedure is repeated iteratively for each channel by varying both the global and the fine threshold. Then, the threshold of each channel is compared to the mean of the thresholds of all channels and its fine trimming DAC is adjusted in order to minimize the width of the threshold distribution.

Fig. **??** shows the distribution of the threshold for the 310 Class A chips selected for tracker assembly, as it appears before (green distribution) and after (blue distribution) fine trimming correction. The measurement was performed at room temperature. However, since the threshold dispersion is mainly ascribed to the threshold mismatch in a pair of transistors in

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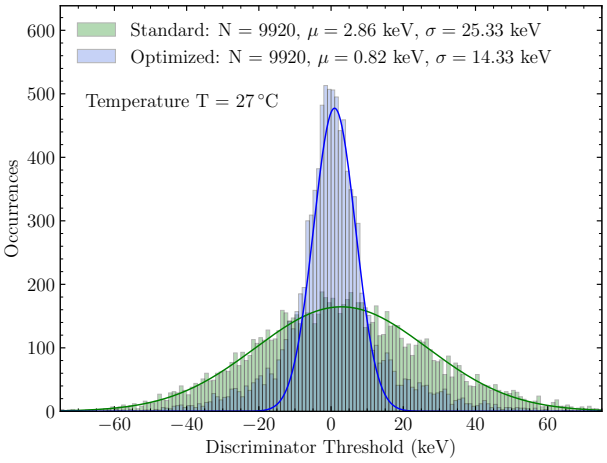

Fig. 8. Threshold dispersion of the 310 Class A chips selected for tracker assembly, before (green distribution) and after (blue distribution) fine trimming correction.

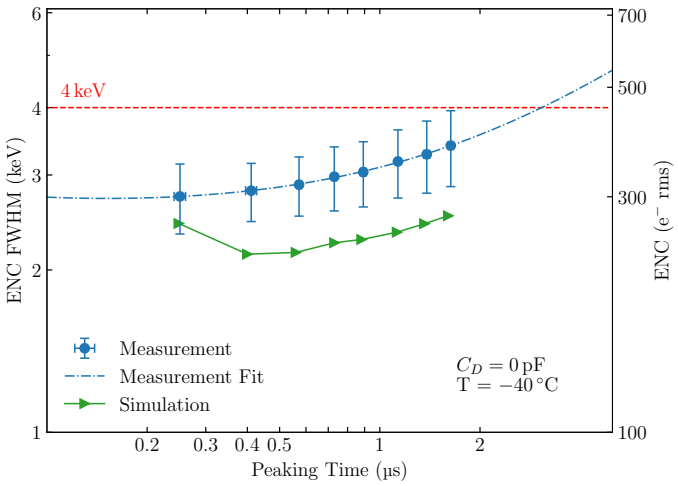

Fig. 9. Measured and simulated FWHM energy resolution (and equivalent noise charge) as a function of the peaking time. The measurement is performed at a temperature of -40 °C and without the external input capacitance.

the shaping stage, results are not expected to change when the ASICs are cooled down to -40°C, as shown in [**?**]. From Fig. **??**, it can be seen that before fine trimming, the threshold of the 9920 channels is distributed according to a Gaussian probability density function (PDF) with a standard deviation of 25.33 keV, more than 2 times worse than the value expected from Monte Carlo simulations. After fine trimming, the PDF is no longer Gaussian but is given instead by the sum of three components. Around the mean value, the distribution is still Gaussian with an improved standard deviation reduced to 14.33 keV. This result shows the effectiveness of the fine trimming DAC. In addition to this, two tails, given by the value of thresholds that are out of the correction range of the fine trimming DAC, are visible. Nevertheless, depending on the energy of the X-ray source, it is possible that the calibration procedure may be repeated for 2 or more values of the global threshold to allow for proper characterization of all channels. For future designs, better results could be obtained either with an increased number of DAC bits, or with a bit width larger than 5 keV.

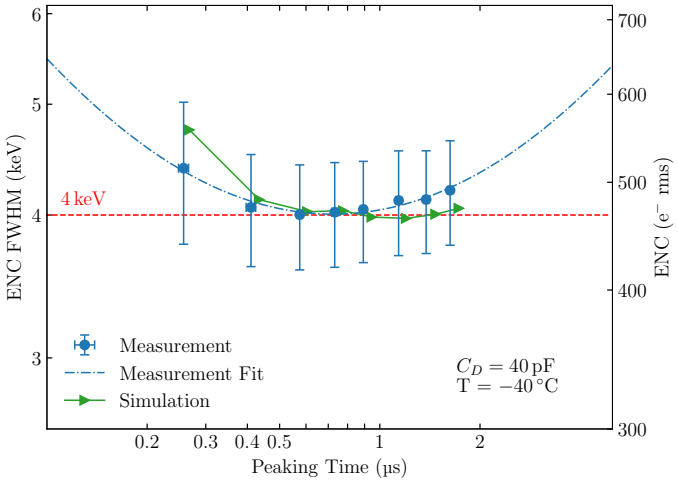

Fig. 10. Measured and simulated FWHM energy resolution (and equivalent noise charge) as a function of the peaking time. The measurement is performed at a temperature of -40 °C and with an external input capacitance of C_D=40 pF.

D. Noise and Energy Resolution

The Si(Li) detector readout channel must provide an energy resolution of at least 4 keV (FWHM) in the 20–100 keV range in order to discriminate between the characteristic X-rays from the de-excitation of antiprotonic and antideuteronic exotic atoms. Energy resolution is limited by electronic noise that can be defined as the root mean square value (r.m.s.) of the voltage fluctuation at the end of the analog processing chain. This fluctuation has been measured by sampling the channel pedestal 1000 times. The Equivalent Noise Charge (ENC), expressed in electrons r.m.s., is extracted from the variance of the distribution of sampled values divided by the channel gain. The energy resolution, in keV (FWHM), is obtained with the following equation:

$$FWHM = 2.35 \cdot \varepsilon \cdot ENC \qquad (1)$$

where 2.35 is the conversion factor from r.m.s. to FWHM and ε is a coefficient that accounts for the average ionization energy of silicon (3.6 eV per electron-hole pair) with 1 keV/(3.6 eV/e$^-$) = 278 e$^-$.

The ENC can be described as follows [**?**]:

$$\mathrm{ENC}^2 = (C_D^*)^2 \left(A_1 \frac{S_w}{\tau_p} + A_2 2\pi A_f \right) + A_3 S_p \tau_p \qquad (2)$$

In Eq. (**??**), $C_D^* = C_D + C_{in} + C_f + C_{par}$ is the total capacitance shunting the input node of the CSA and is given by the sum of the detector capacitance C_D, the input capacitance of the preamplifier input device C_{in}, the feedback capacitance C_f and strays C_{par}. For stray capacitance, a value of 15 pF was extracted likely to be ascribed to contributions from test board input tracks, package pins, wire bonding pads and input metal lines on the ASIC. S_w accounts for the frequency independent contribution to the power spectral density of the input referred

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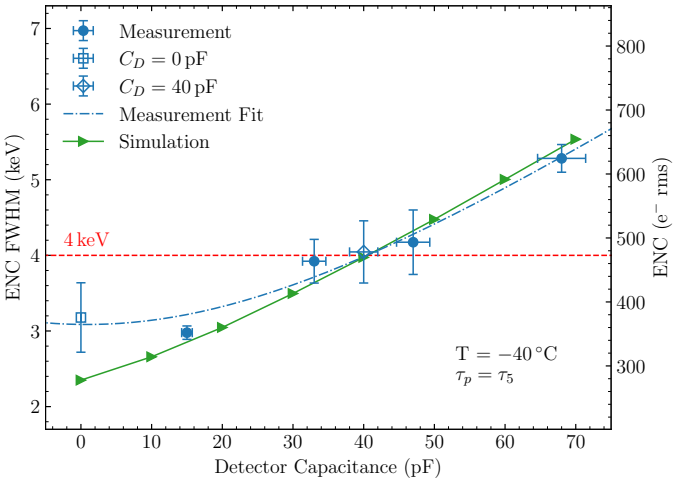

Fig. 11. Measured and simulated FWHM energy resolution (and equivalent noise charge) as a function of the detector capacitance C_D. Results were obtained from a single sample (filled round-shaped markers) and from 3 samples without the detector capacitance (empty squared-shaped marker) and with $C_D = 40$ pF (empty diamond-shaped marker).

series noise source, A_f is a coefficient for $1/f$ noise of the same series noise source. S_p is the frequency independent power spectral density of the input referred parallel noise source. A_1, A_2 and A_3 are shaping coefficients that depend only on the normalized weighting function of the system. For the semi-Gaussian second order shaper used in SLIDER32 A_1=0.85, A_2=0.54 and A_3=0.64 [**?**].

For each of the 8 selectable peaking times, measurements of the ENC have been performed at a temperature of -40 °C. Devices were tested with and without an external input capacitance C_D=40 pF that was added with the purpose of emulating the one expected with the detector connected. In this test, the detector leakage current is not taken into account. However, since this current is in the order of 2 nA per strip, as shown in [**?**], its parallel noise contribution is not expected to affect the resolution even at the highest peaking times.

The average ENC values obtained from measurements performed on 3 chips (96 channels) are reported in Table **??**. It can be seen that with C_D=40 pF, for peaking times around 1 µs the average ENC (FWHM) is close to the 4 keV (480 e$^-$rms) targeted by the experimental application, thus proving the effectiveness of the readout channel. Fig. **??** and **??** show the measured values of the ENC as a function of the peaking time without and with the detector capacitance respectively. Measurement results are provided in units both of keV (FWHM) and of electrons r.m.s. and are compared with values predicted by simulations. In both plots, measurement results are fitted according to Eq. (**??**) to better evaluate the contribution of each noise source to the ENC. With detector emulating capacitor, the measured values are very close to those simulated with the exception of the shortest peaking time for which the measured value is slightly lower than that obtained from the simulations. This discrepancy likely to be ascribed to a reduction in the white noise of the preamplifier input device. For longer peaking times, however, the measured values seem to show a larger contribution coming from the

TABLE III
CONTRIBUTION, IN %, OF CHANNEL NOISE SOURCES TO THE TOTAL INTEGRATED OUTPUT NOISE.

τ_p [µs]	T_0	CSA (total)	G_f	Bias network	Other blocks
0.25	64	78	3	6	13
0.40	60	74	6	9	11
0.57	56	69	9	12	10
0.73	52	65	11	14	10
0.88	48	62	13	16	9
1.13	44	57	16	19	8
1.37	40	53	18	21	8
1.60	38	50	20	23	7

parallel noise source. Therefore, it could be related with a non-optimal bias of the Krummenacher feedback restoration network of the CSA. Furthermore, measurements performed without the detector capacitance present an excess noise. To better understand this aspect and also to evaluate the effect of detector capacitance fluctuations on the noise performance of the readout channel, the ENC was measured on a single sample for different values of C_D. Results are shown in Fig. **??** for the peaking time τ_p=1.13 µs. In the same plot, results coming from measurements performed with and without the detector capacitance are added and all points were fitted according to (**??**). From the resulting interpolation function it can be seen that the slope in the region where a linear dependence is observed, that is for C_D greater than 10 pF, seems close to values predicted from simulation. The variations of the noise as a function of the detector capacitance obtained in this region are shown in Table **??**. The excess noise observed without the detector capacitance appears to be related to a parallel-type source in agreement with what observed in Fig. **??**. However, since the output noise is not only affected by the CSA, as discussed below, we have concluded that it is not possible to identify a single source that uniquely contributes to this excess noise. Other sources related to the test setup are likely to influence the measurement results with a non-negligible contribution.

From a design point of view, it is of some interest to evaluate in detail the contribution of the main noise sources affecting the analog channel resolution to the total integrated output noise. More in detail, the contributions from the following noise sources have been extrapolated from simulation using the worst case noise model: the input device of the charge preamplifier (T_0) and the complete CSA itself, the restoration Krummenacher network (G_f), and the biasing network. Since the overall noise is the quadratic sum of all contributions, from the results reported in Table **??** it can be seen that the input transistor (T_0) contributes about 80% to the CSA total noise. Moreover, the sum of CSA and Krummenacher sources contribute 70-80%, depending on the peaking time, to the total channel noise. Although these results are sufficient to provide the required energy resolution, it must be noted that a margin to improve channel performance exists. In particular by reducing the contribution from the the bias network, an

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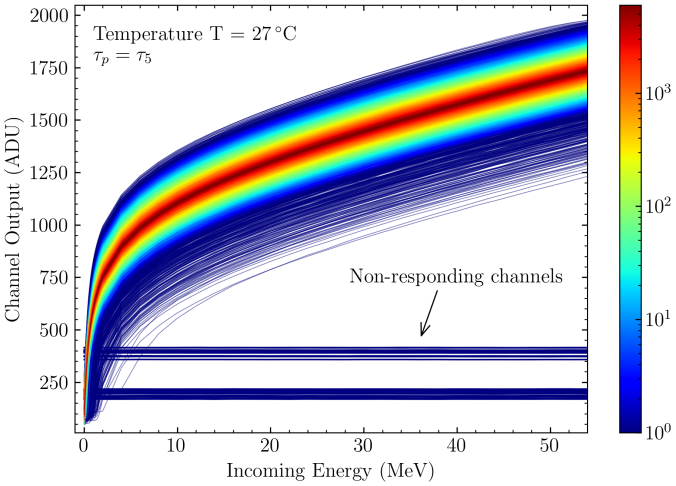

Fig. 12. Input-output trans-characteristic of 17056 channels (533 ASICs) measured at ambient temperature for ASIC classification. The 469 non-responding channels are highlighted.

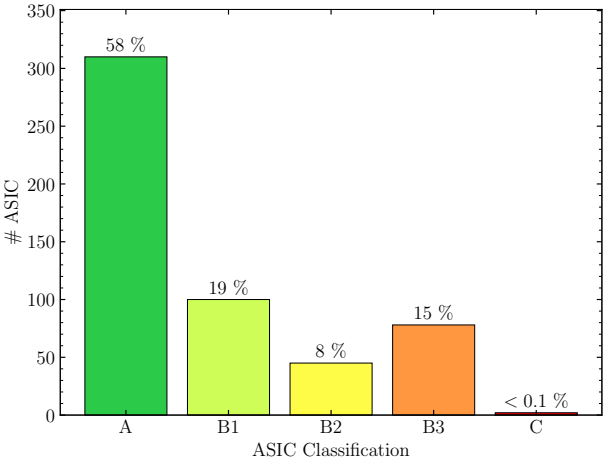

Fig. 13. Classification of the 535 tested ASICs as resulting from tests performed at ambient temperature.

improvement of around 0.4 keV can be obtained for the peaking times around 1 µs. A reduction in the contribution from other blocks in the channel is less straightforward. Since these noise contributions are mainly from blocks following the CSA, a reduction in the equivalent noise at the channel's input can be obtained either by increasing the CSA low-energy gain, which is not possible due to limitation in dynamic range, or at the cost of injecting more current in these blocks, thus increasing the ASIC power consumption.

E. ASIC validation and yield

The validation and selection activity was carried out in two steps. First we checked the capability to communicate with the ASIC. We found that only 2 devices where unable to communicate. So, from this type of test, we got a yield of almost 100%. As a next step, we verified the functionality of the analog readout channels. To this purpose, the input-output characteristic of each channel of the 533 devices that passes the digital test was measured. The result of this measurement

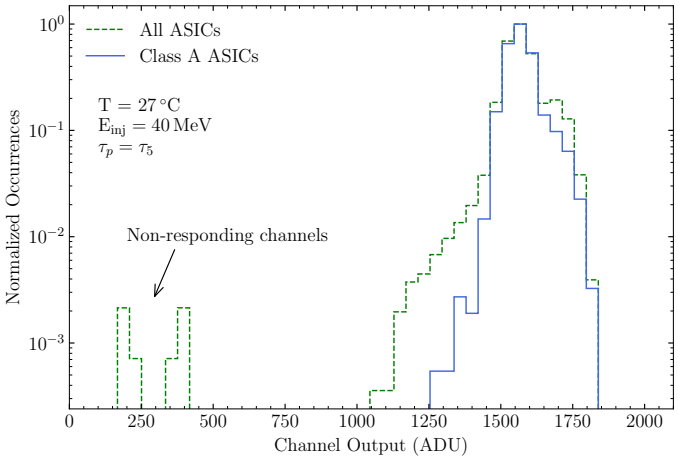

Fig. 14. Normalized distribution of the ADC output obtained for a fixed input of 40 MeV for all the 17056 tested channels and for the 9920 belonging to Class A devices only.

is reported in Fig. **??**. From the plot, it can be seen that a certain number of channels do not respond to the injected input signal. More in detail, 469 channels, out of 17056, were not responding, thus providing a yield, in terms of channels, of about 97%. Based on these results, ASICs were classified according to the following criteria:

- **class A:** all channels respond properly;
- **class B1:** 1 channel does not respond properly;
- **class B2:** 2 channels do not respond properly;
- **class B3:** >2 channels do not respond properly;
- **class C:** the ASIC does not communicate.

Classification results are reported in Fig. **??**. It can be seen that 310 Class A devices (58 %) were deemed suitable for tracker assembly. It is worth noting that, since the analog readout channel has been optimized for operation at -40 °C and its behavior is sensitive to temperature variations, channels that do not respond properly at ambient temperature were observed to recover when cooled. Nonetheless, these channels showed poor performance, in particular in terms of sensitivity in the low-energy range.

To better evaluate the effect of this validation and selection activity, the normalized distribution of the ADC output obtained for a fixed input of 40 MeV is shown in Fig. **??** for all the 17056 tested channels and for the 9920 belonging to Class A devices only. It can be seen that after selection also the spread in channel output is improved.

IV. Conclusions

In this paper, we described the architecture and presented the experimental results from the characterization of the SLIDER32 ASIC for the readout of the Si(Li) tracker of the GAPS experiment. After fabrication, all the functionalities have been successfully verified at the operating temperature of -40 °C. The chip performance was found to meet the experiment requirements. Fully functional chips were selected for the assembly of the detector and of the flight instrument, which is now under construction in view of the first GAPS balloon

flight scheduled for the Antarctic summer of 2024–2025 from the McMurdo National Science Foundation (NSF) Station in Antarctica.

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